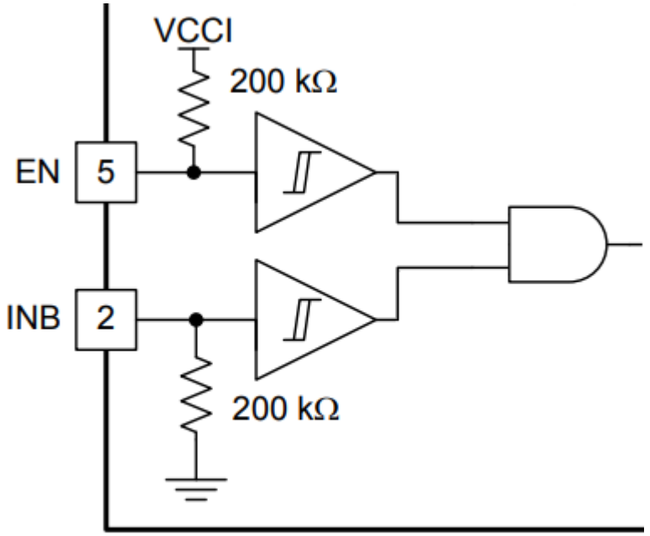
Isolated gate driver challenges and solutions

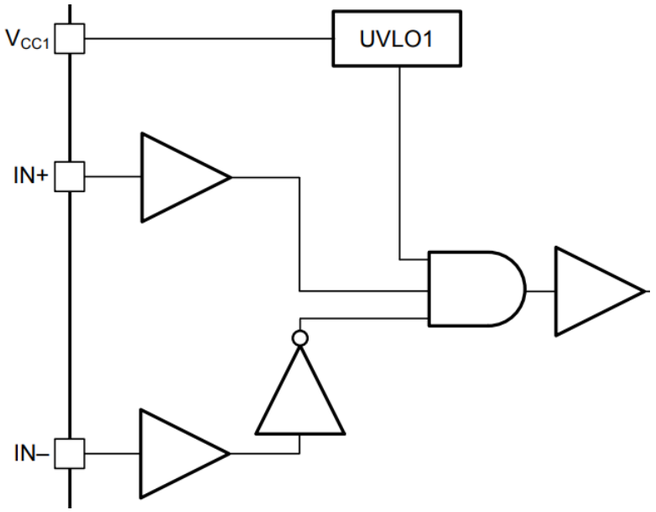
TIPL 504
TI Precision Labs – Isolated Gate Drivers

Presented and Prepared by Derek Payne

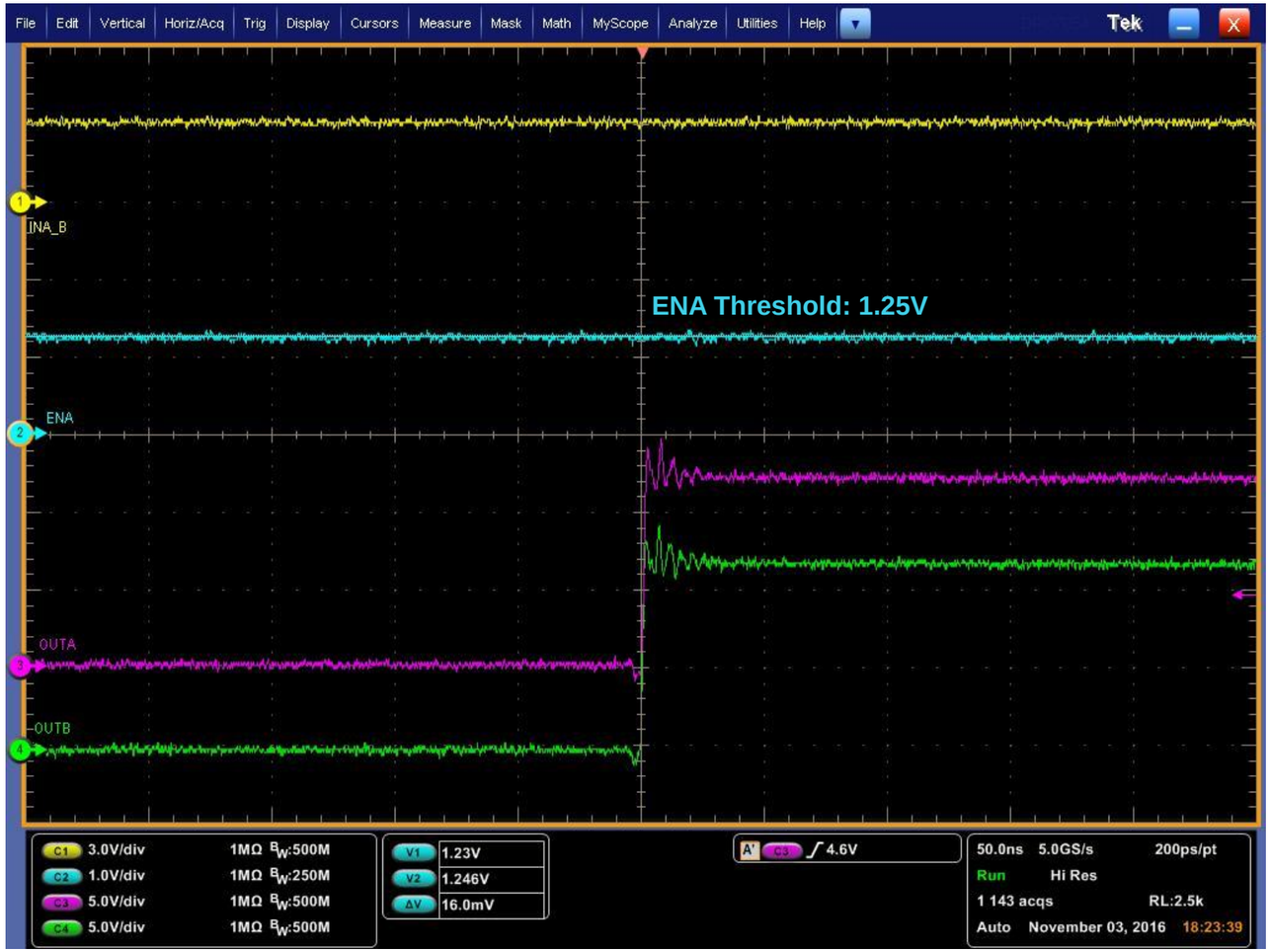
General Challenges – Enable/Disable



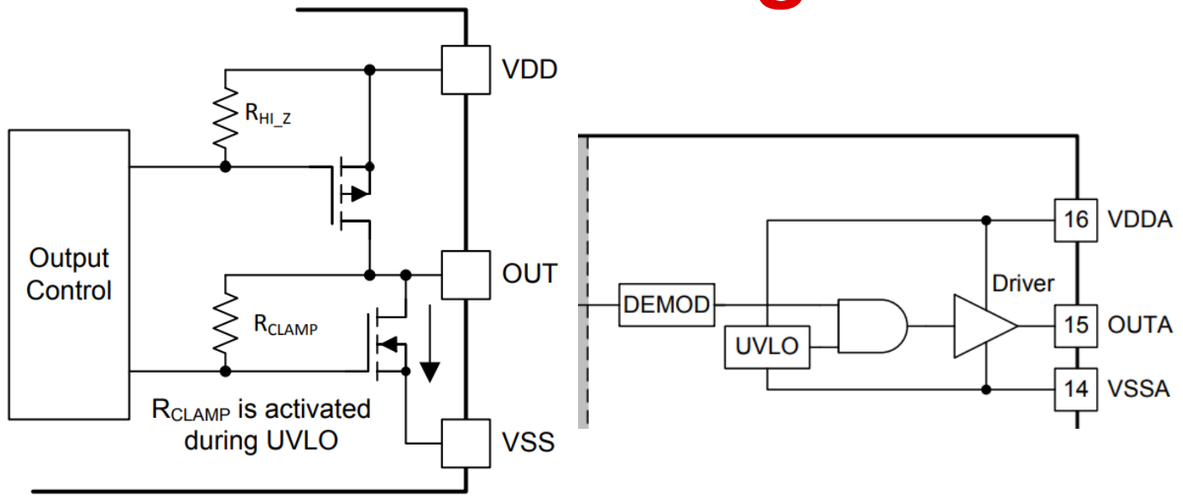
Enable Function

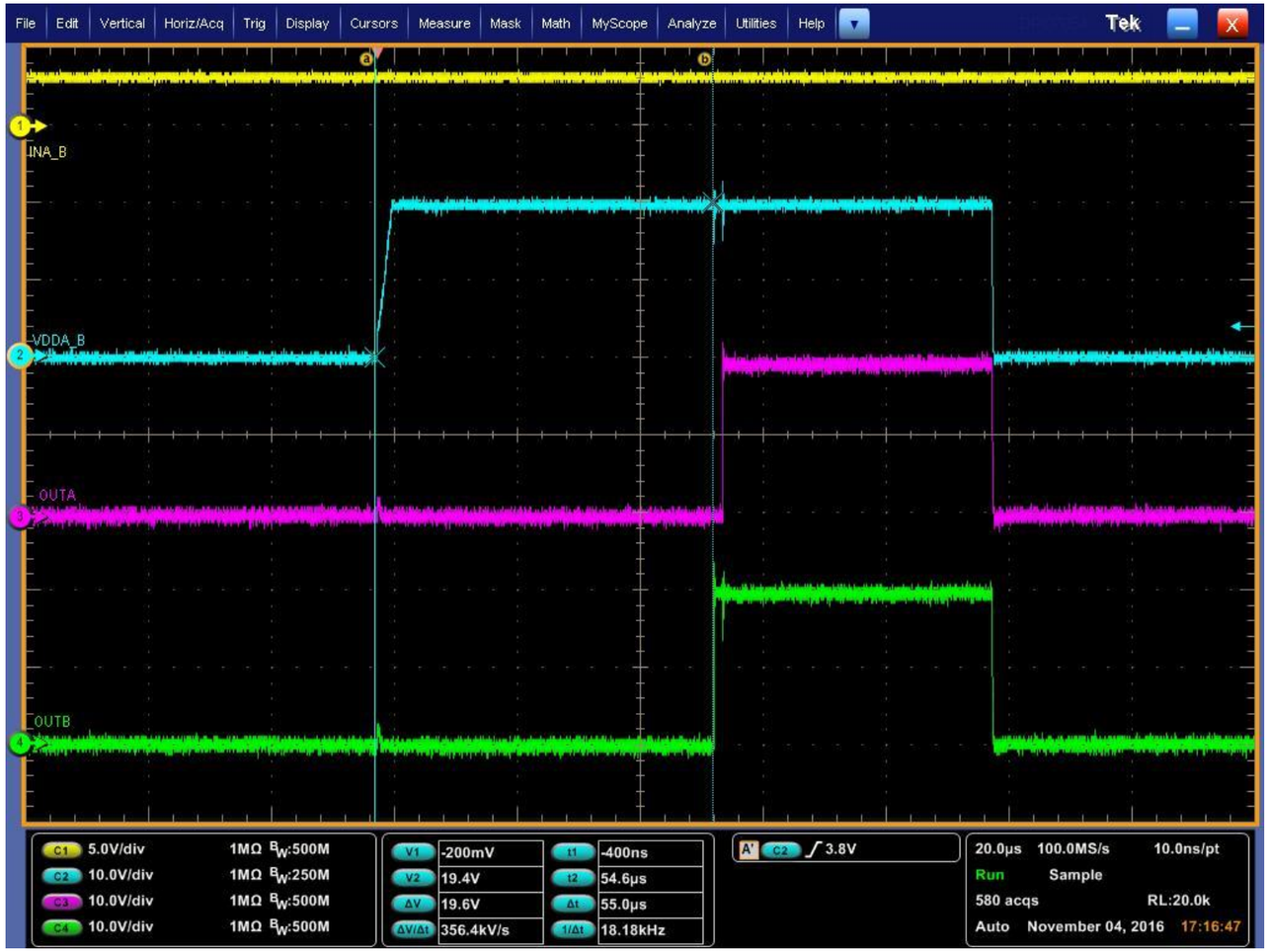


Disable Function



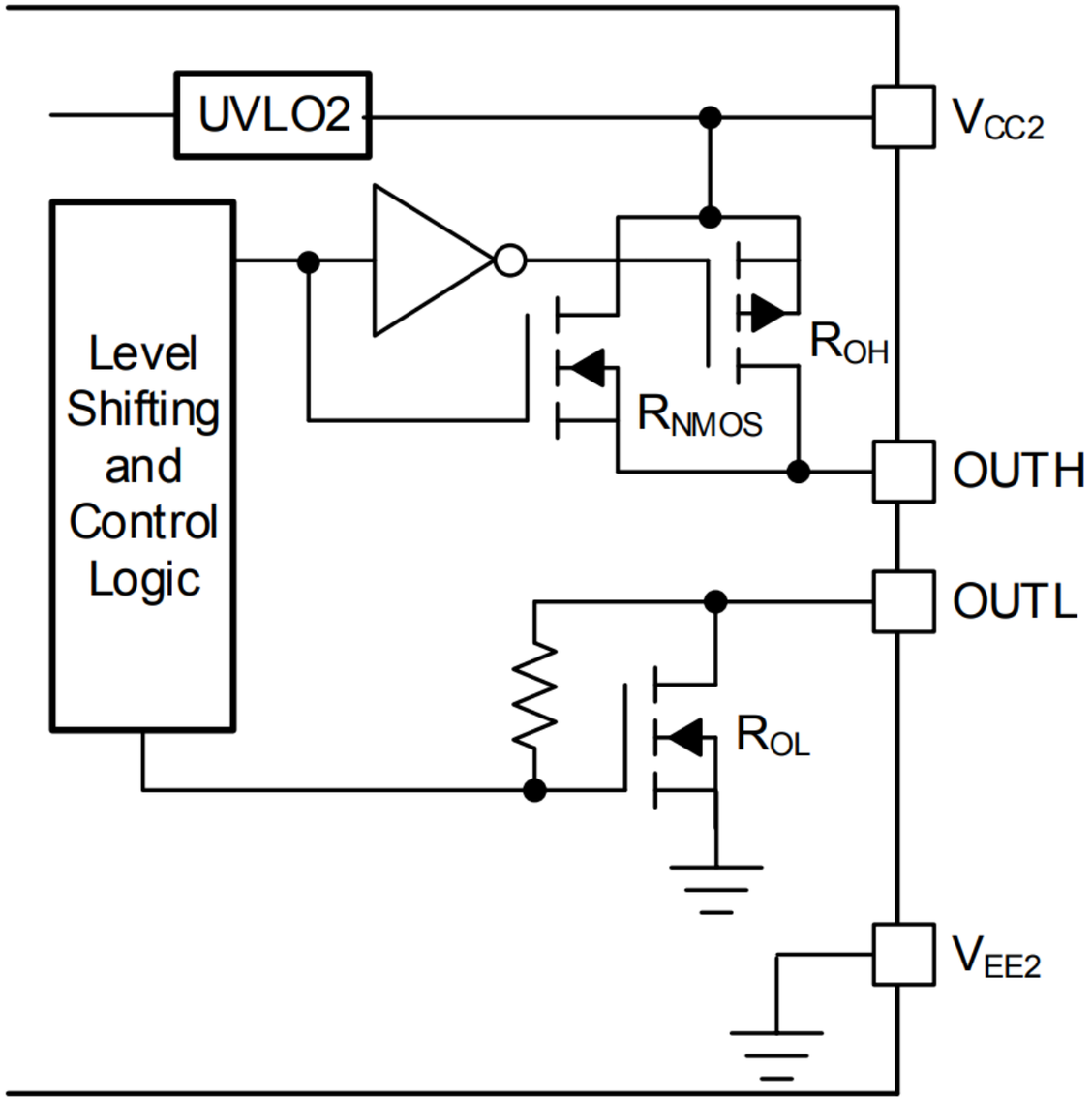
General Challenges – Undervoltage Lockout

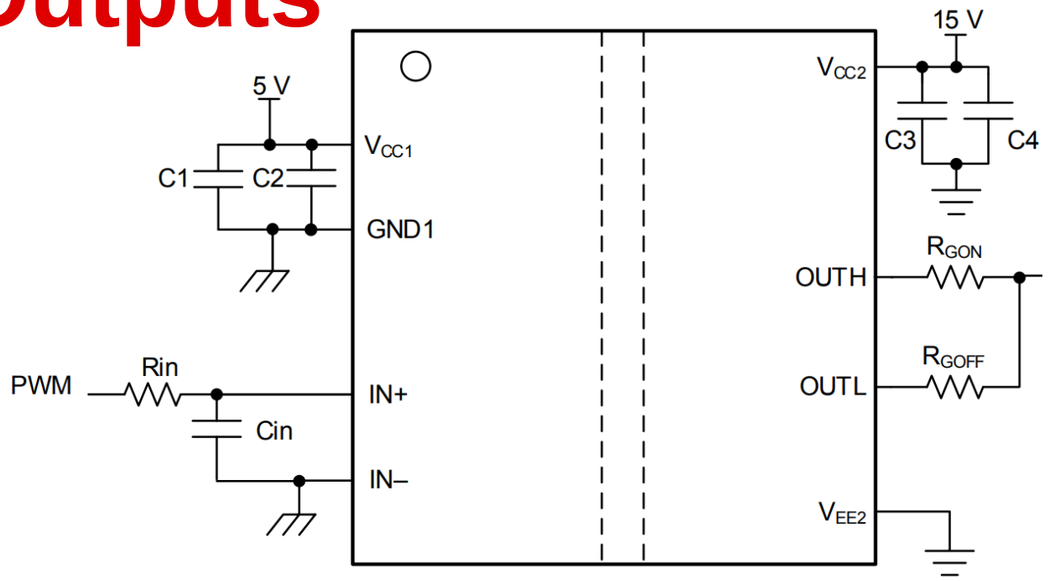


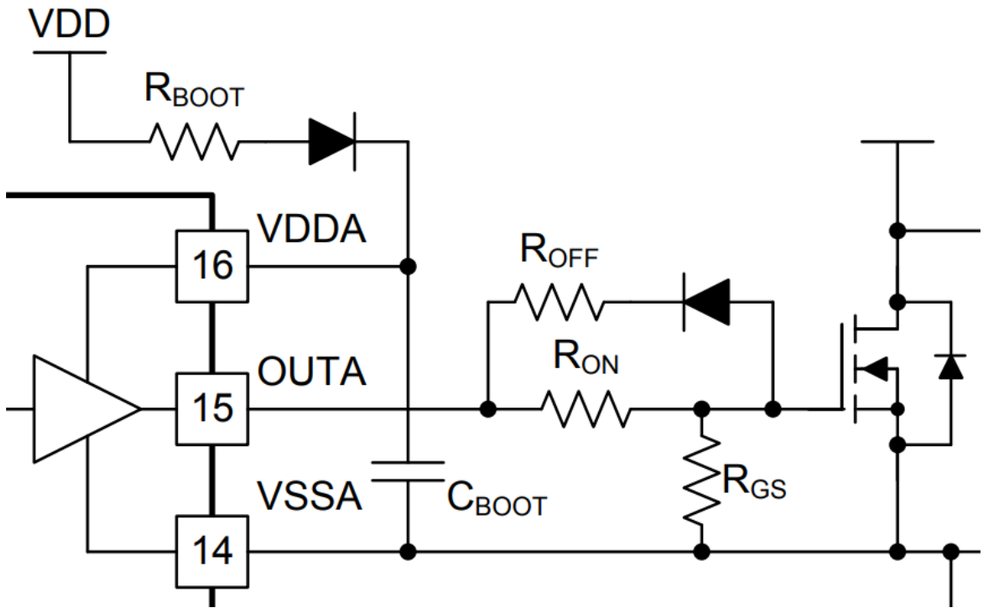


VCCI UVLO THRESHOLDS						
V_{VCCI_ON}	Rising threshold		2.55	2.7	2.85	V
V_{VCCI_OFF}	Falling threshold VCCI_OFF		2.35	2.5	2.65	V
V_{VCCI_HYS}	Threshold hysteresis			0.2		V
UCC21521ADW UVLO THRESHOLDS (5-V UVLO VERSION)						
V_{VDDA_ON}, V_{VDDB_ON}	Rising threshold VDDA_ON, VDDB_ON		5.2	5.8	6.3	V
V_{VDDA_OFF}, V_{VDDB_OFF}	Falling threshold VDDA_OFF, VDDB_OFF		4.9	5.5	6	V
V_{VDDA_HYS}, V_{VDDB_HYS}	Threshold hysteresis			0.3		V
UCC21521DW UVLO THRESHOLDS (8-V UVLO VERSION)						
V_{VDDA_ON}, V_{VDDB_ON}	Rising threshold VDDA_ON, VDDB_ON		8	8.5	9	V
V_{VDDA_OFF}, V_{VDDB_OFF}	Falling threshold VDDA_OFF, VDDB_OFF		7.5	8	8.5	V
V_{VDDA_HYS}, V_{VDDB_HYS}	Threshold hysteresis			0.5		V
UCC21521CDW UVLO THRESHOLDS (12-V UVLO VERSION)						
V_{VDDA_ON}, V_{VDDB_ON}	Rising threshold VDDA_ON, VDDB_ON		12.5	13.5	14.5	V
V_{VDDA_OFF}, V_{VDDB_OFF}	Falling threshold VDDA_OFF, VDDB_OFF		11.5	12.5	13.5	V
V_{VDDA_HYS}, V_{VDDB_HYS}	Threshold hysteresis			1.0		V

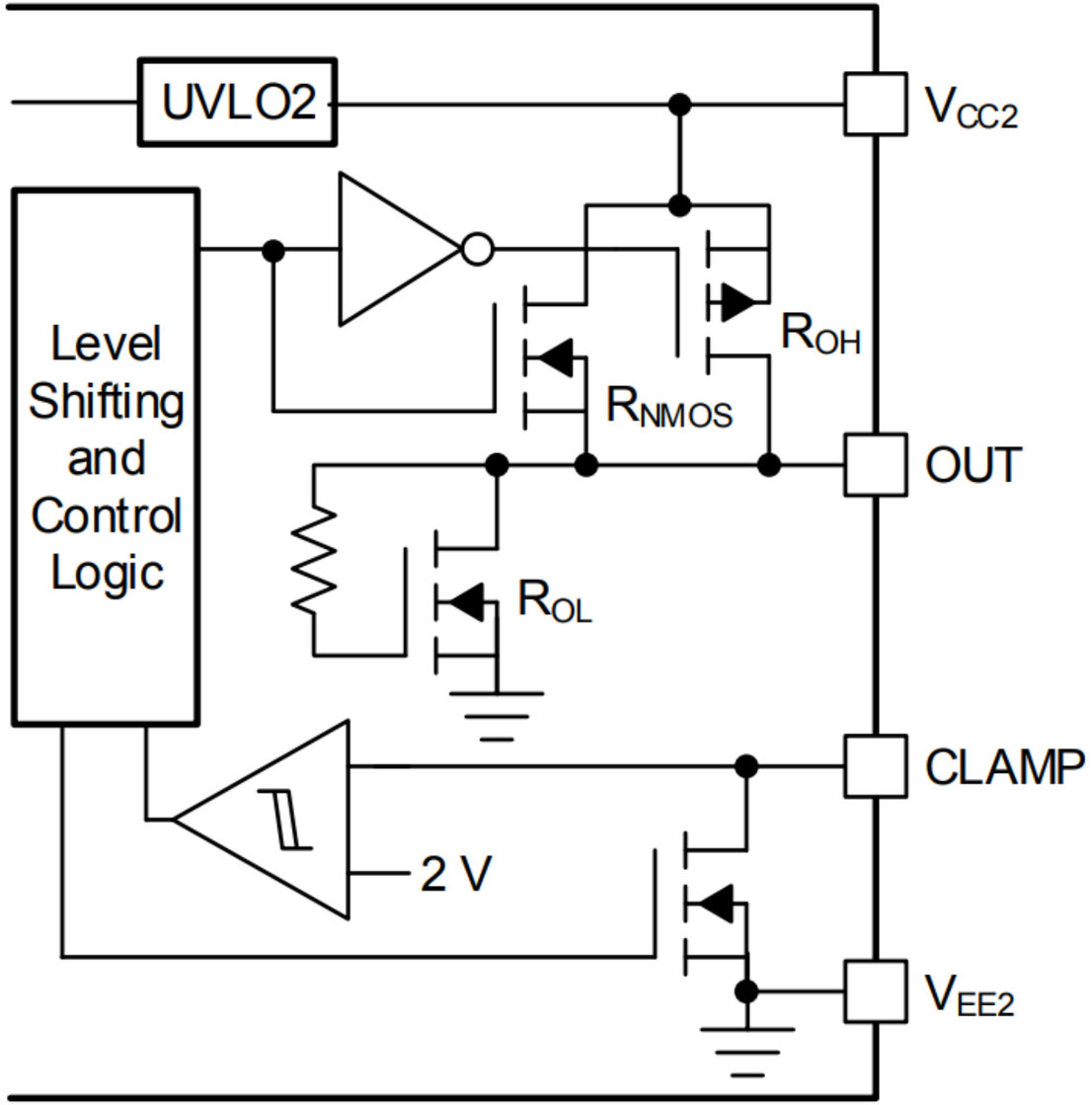
Output Challenges – Split Outputs



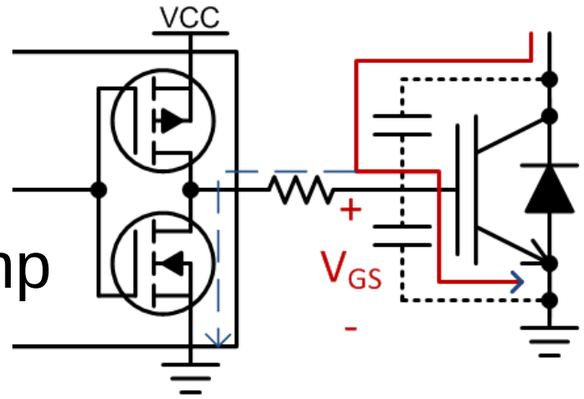


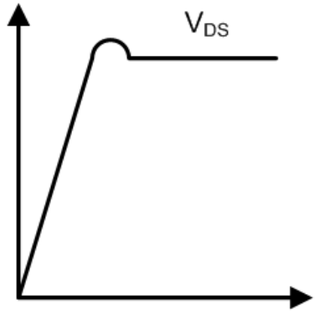


Output Challenges – Miller Clamp

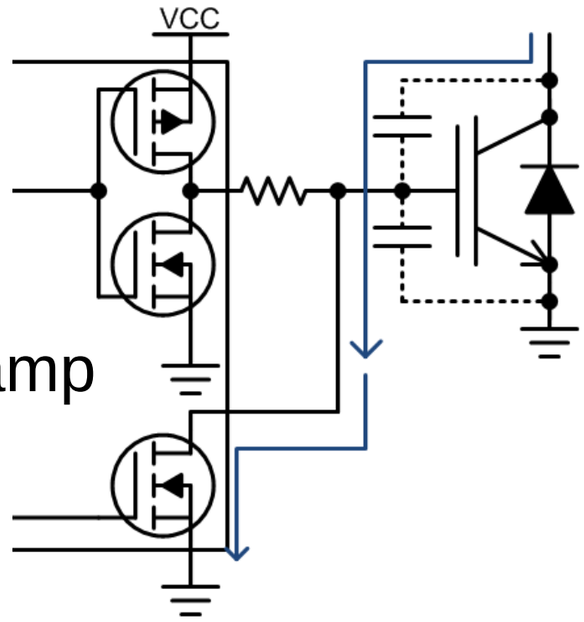


No Clamp

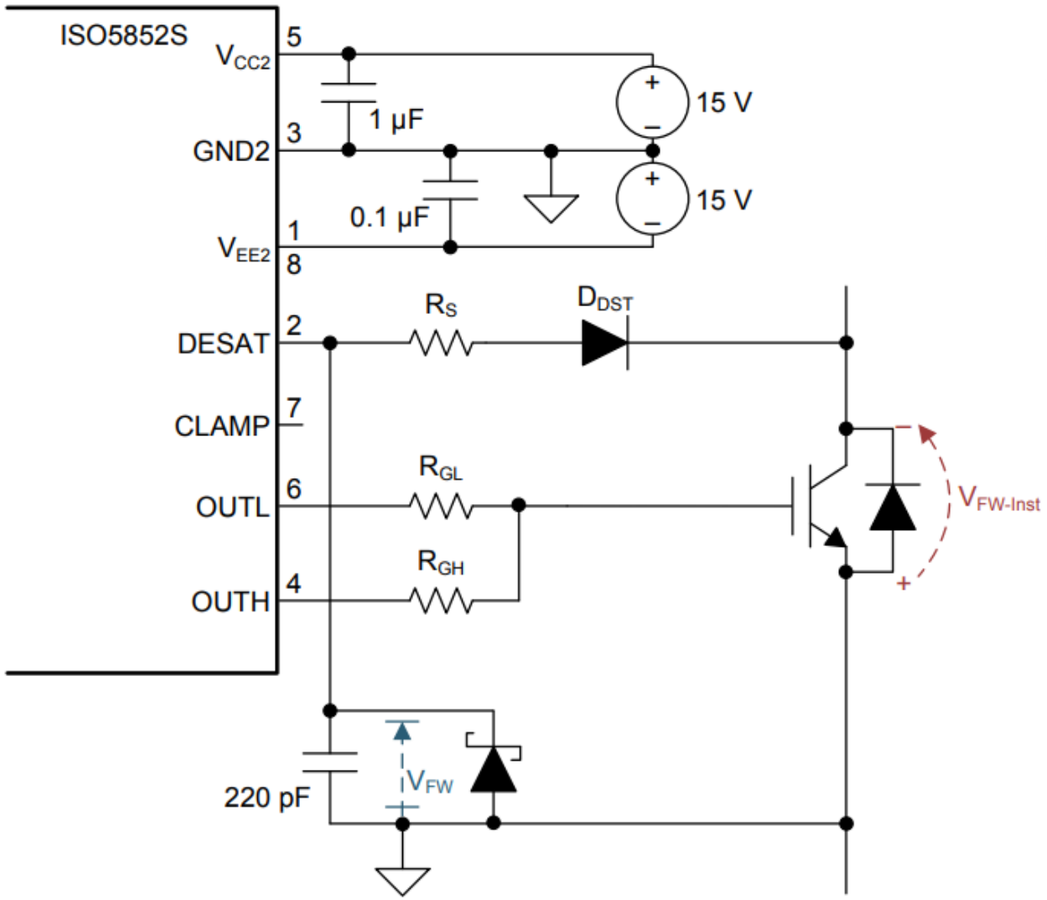




With Clamp

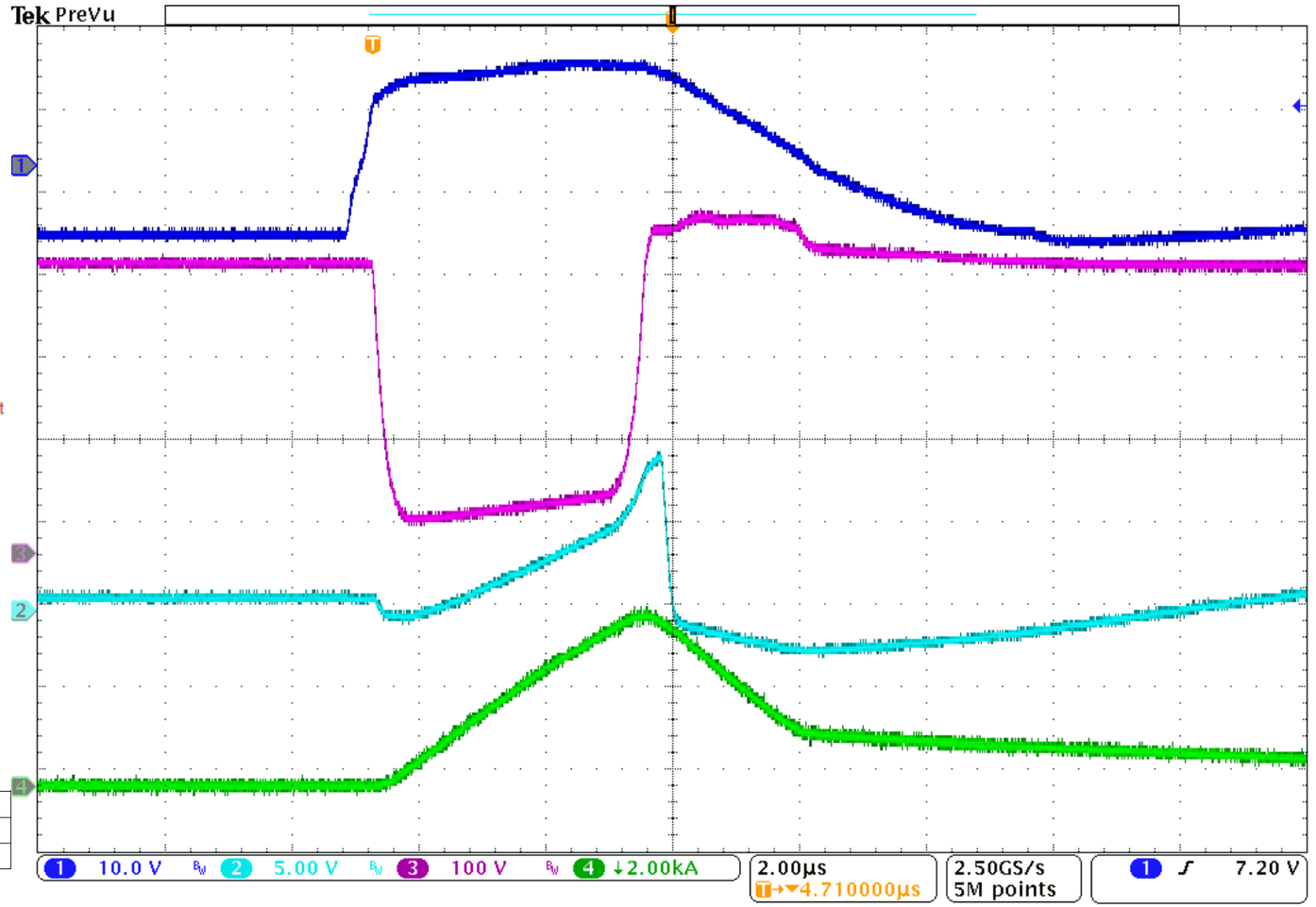


Protection Challenges – Desaturation Detection and Soft Turn Off

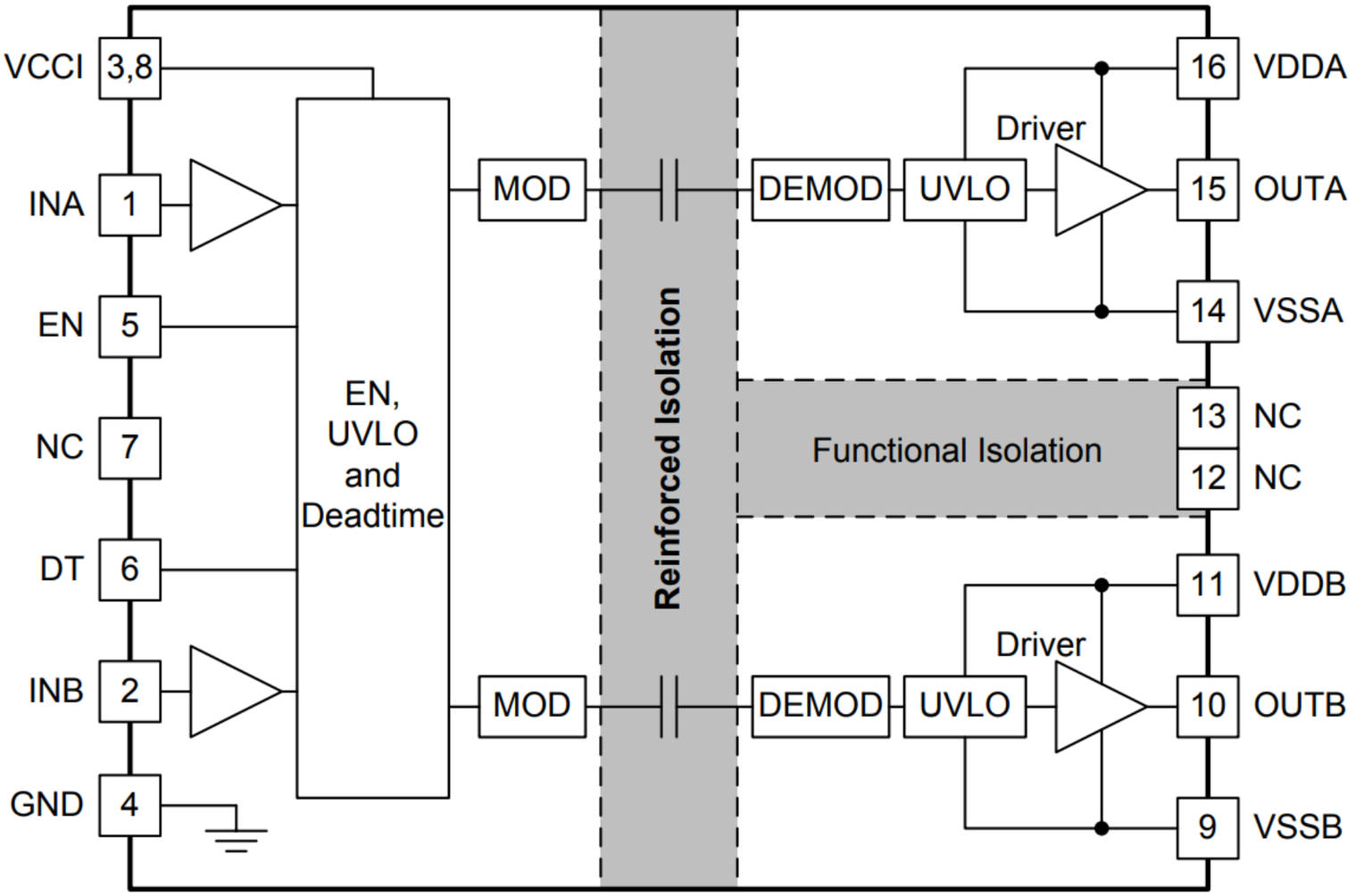


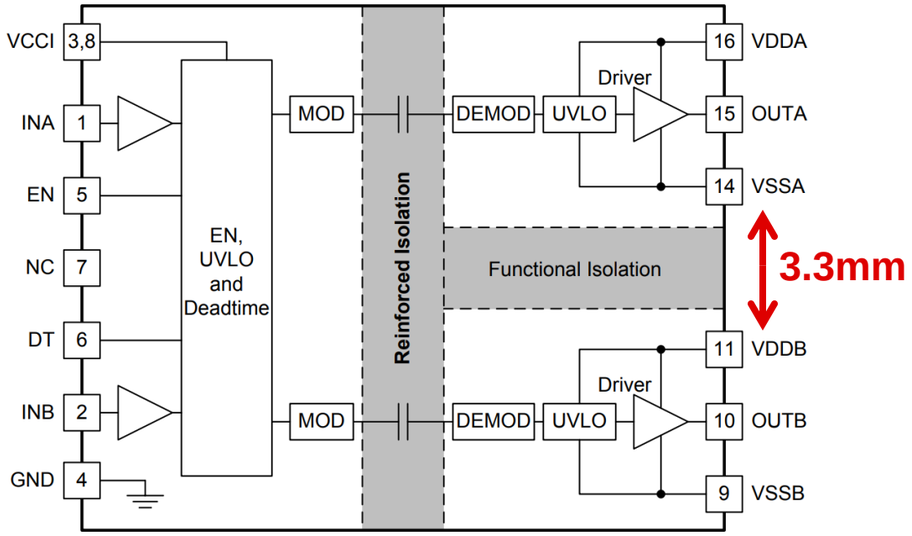
$t_{DS\ (90\%)}$	DESAT sense to 90% $V_{OUTH/L}$ delay	C_{LOAD} = 10 nF	553	760	ns
$t_{DS\ (10\%)}$	DESAT sense to 10% $V_{OUTH/L}$ delay	C_{LOAD} = 10 nF	2	3.5	µs
$t_{DS\ (GF)}$	DESAT-glitch filter delay	C_{LOAD} = 1 nF	330		ns

VCE(100V/div), IC(2kA/div),
VGE(10V/div), VDESAT(5V/div)



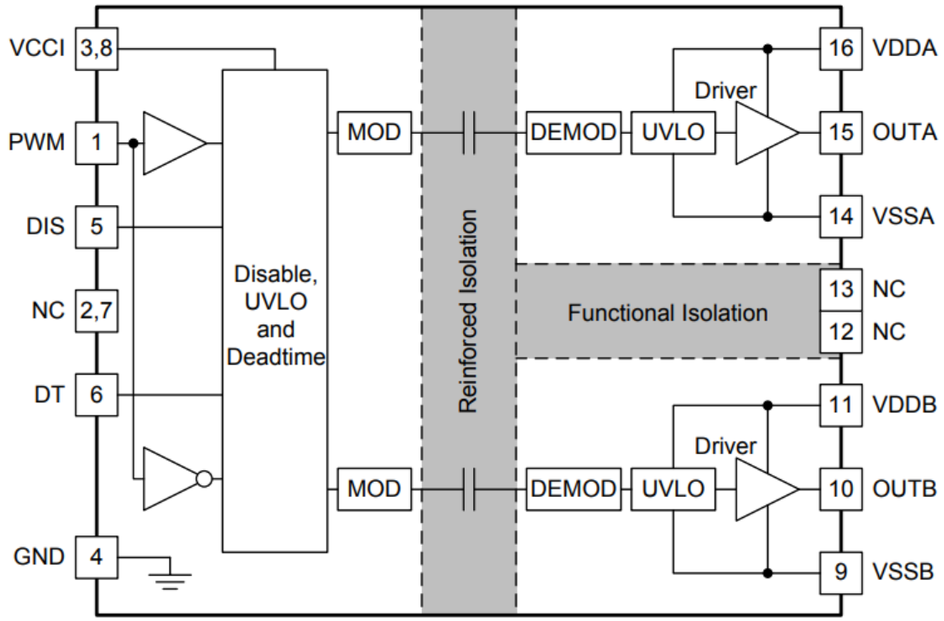
Protection Challenges – Channel-to-Channel Isolation Rating

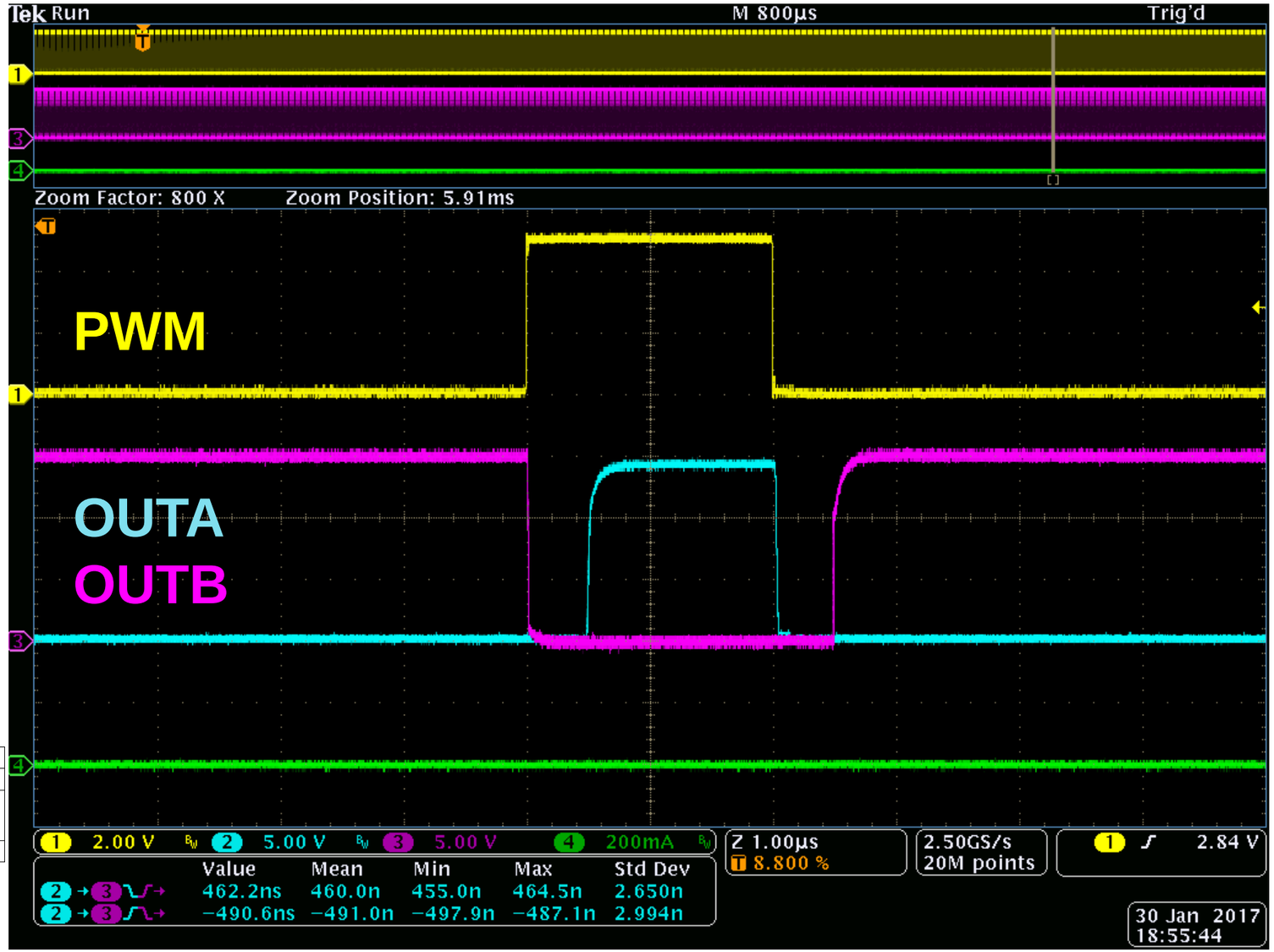




Standard	Spacing (mm)	Voltage rating (Vrms)
IEC60950	3.3	630
IPC9592	4	800
IPC2221	2.4	800

Protection Challenges – Programmable Dead Time





DEADTIME AND OVERLAP PROGRAMMING					
Dead time	Pull DT pin to VCCI		0		ns
	DT pin is left open, min spec characterized only, tested for outliers		8	15	ns
	R_{DT} = 20 kΩ	160	200	240	ns

Thanks for your time!
Please try the quiz.

Isolated Gate Driver Challenges and Solutions

Multiple Choice Quiz

TI Precision Labs – Isolation

Quiz: Isolated Gate Driver Challenges and Solutions

1. **Drivers with differential inputs can emulate an enable function with no additional circuitry by _____**
   a. Sensing a special pattern on the input
   b. Dropping the internal supply voltage below the UVLO threshold
   c. Using one input as the PWM input, and the other input as an enable/disable pin
   d. This isn't possible, an external logic gate must be used

2. **Different undervoltage lockout levels are used for _____**
   a. Logic-level MOSFETs, power MOSFETs, and IGBTs/SiC MOSFETs
   b. Bipolar junction transistors and MOSFETs
   c. Power MOSFETs in parallel
   d. Different undervoltage lockout levels are not used by gate drivers

3. **Which of these is NOT a feature designed to help drive IGBTs and SiC MOSFETs?**
   a. Miller clamp
   b. Split outputs
   c. Desaturation/overcurrent detection
   d. 8V undervoltage lockout options

Quiz: Isolated Gate Driver Challenges and Solutions

4. **The channel-to-channel isolation rating is _____**
   a. Only applicable for half-bridge structures
   b. Unipolar (one channel must be at a higher DC voltage than the other at all times)
   c. Always the same as the control-to-output isolation rating
   d. Determined largely by package geometry and pin/leadframe spacing

5. **Integrated dead time control circuits _____**
   a. Disable the gate driver when both inputs go high, and raise a fault on the control side
   b. Hold the outputs low whenever both inputs are high, and for a fixed time after one input goes low
   c. Measure the duration and order of a sequence of pulses, and repeat those pulses with added dead time inserted
   d. Power down the gate driver during power converter sleep mode, preventing unnecessary energy expenditure

Isolated Gate Driver Challenges and Solutions

Multiple Choice Quiz – Solutions

TI Precision Labs – Isolation

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