

Voltage Reference Introduction

TIPL 4501

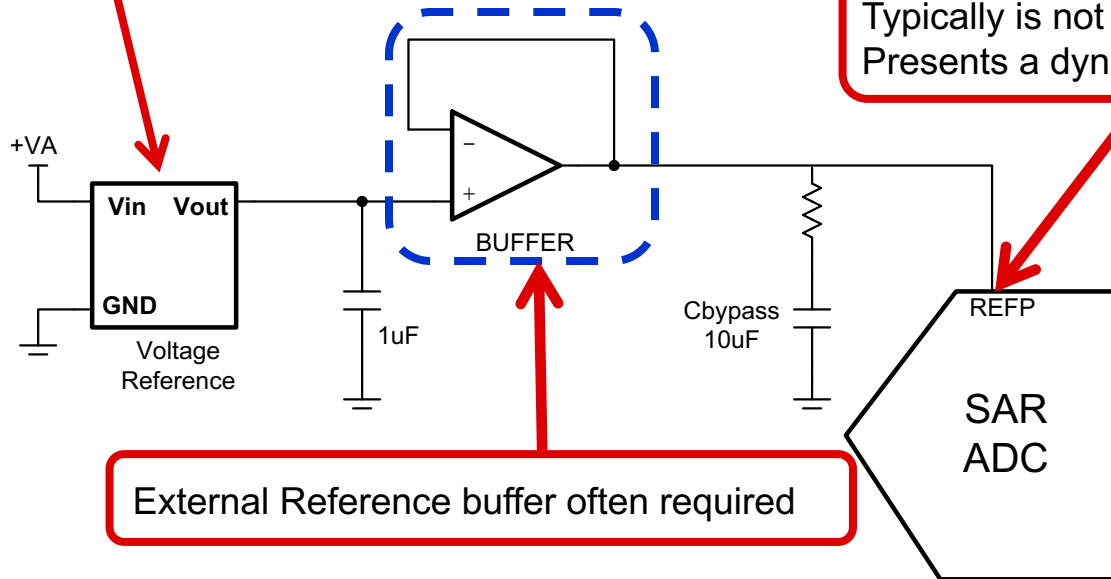
TI Precision Labs – ADCs

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SAR Reference Drive circuit

ADC performance is a function of Reference
Initial accuracy, drift, stability and noise

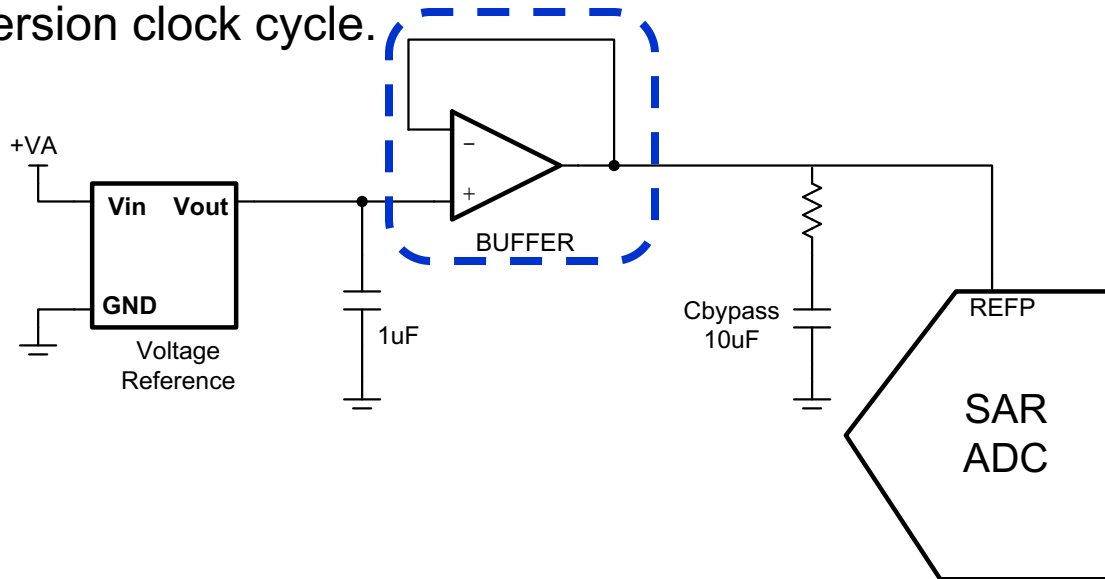


SAR Reference input:
Typically is not high impedance
Presents a dynamic load.

External Reference buffer often required

Overall Objective

- Design low drift, accurate and stable SAR reference drive circuit.
- Reference source must support the dynamic charge/current at the SAR Ref input without affecting noise and stability performance.
- Reference voltage must remain settled within the ADC resolution during each conversion clock cycle.



Agenda for the voltage reference series

Reference Performance Specifications:

Initial Accuracy, Drift, Long Term Drift, and Noise

SAR REF Drive Circuit Topologies:

- Standalone Reference vs. Buffered Reference

- SAR ADCs with Internal Reference Buffer

SAR REF Input Overview: The Capacitive DAC (CDAC)

Build TINA REF Input Model for a SAR:

- Discrete Charge Model

- TI Device Specific Model

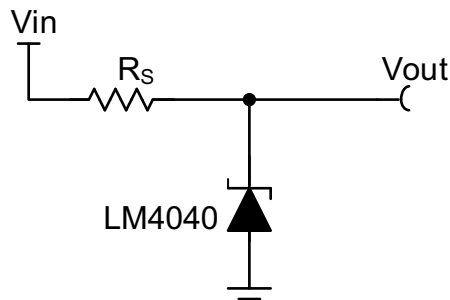
SAR REF Drive Circuit Design:

- Reference Bypass Capacitor

- Reference Buffer Stability and Compensation

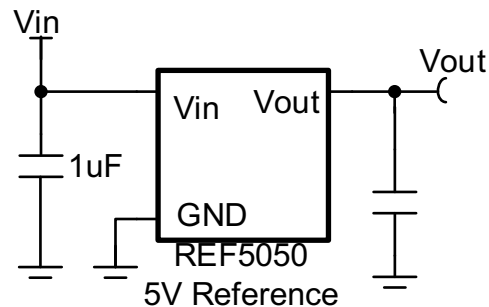
Series or Shunt Reference

Shunt



- Cannot sink current
- Limited ability to respond to load transients
- Used for wide V_{in} and V_{in} transients
- Can be used as floating reference.

Series



- Used in ADC reference input drive
- Output amplifier can source and sink current
- Low dropout
- No external resistor required.

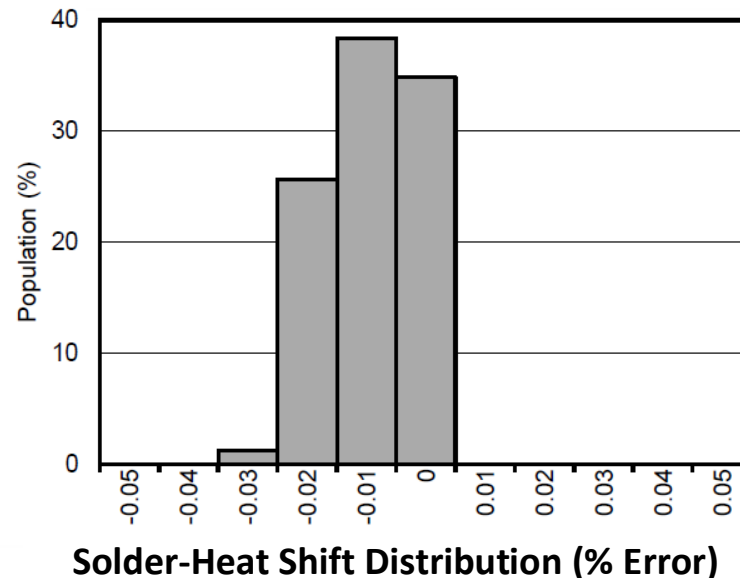
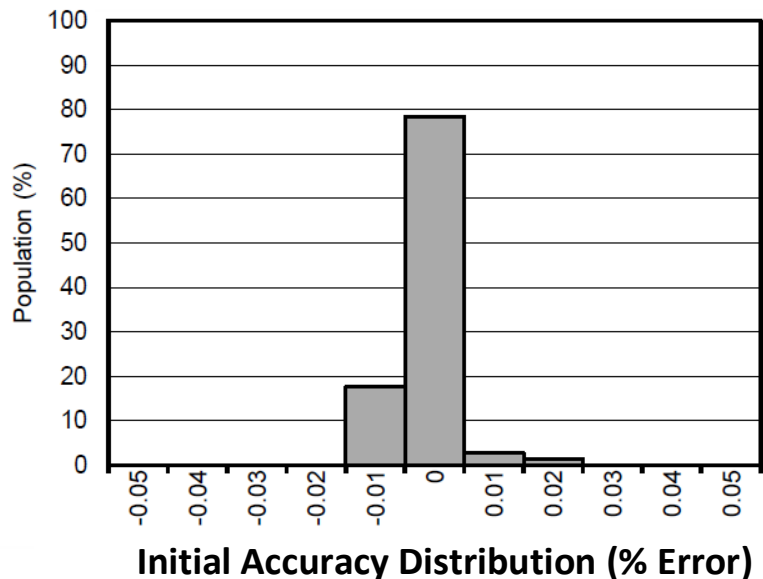
Initial Accuracy

At $T_A = 25^\circ\text{C}$, $I_{\text{LOAD}} = 0$, $C_L = 1\mu\text{F}$, and $V_{\text{IN}} = (V_{\text{OUT}} + 0.2\text{V})$ TO 18V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MIN	UNIT
V_{OUT}	Output Voltage	REF5020		2.048		V
		REF5025		2.500		
		REF5030		3.000		
		REF5040		4.096		
		REF5050		5.000		
		REF5010		10.00		
	Initial Accuracy: High Grade		-0.05		0.05	%
	Initial Accuracy: Standard Grade		-0.1		0.1	%

- Valid at the test conditions: see top of table.
- Does not include effects from temperature drift, soldering, long term shift, or thermal hysteresis.

Initial Accuracy and Solder Shift



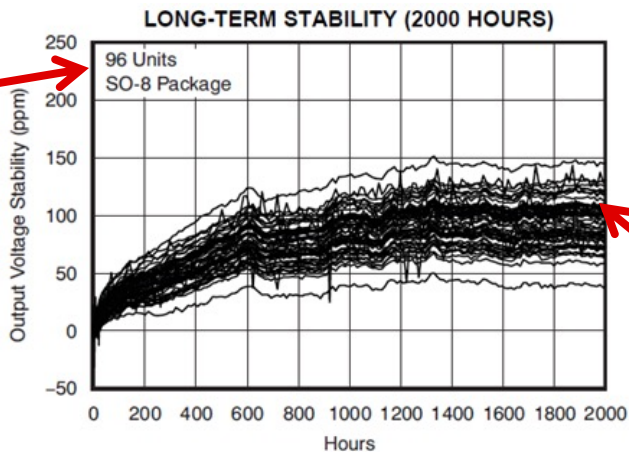
- The solder shift is for a specific test condition:
 - Example: PCB thickness, area, and soldering profile.
 - Other conditions (e.g. multiple reflows) could have larger shifts.

Long Term Shift (stability)

At $T_A = 25^\circ\text{C}$, $I_{\text{LOAD}} = 0$, $C_L = 1\mu\text{F}$, and $V_{\text{IN}} = (V_{\text{OUT}} + 0.2\text{V})$ TO 18V, unless otherwise noted.

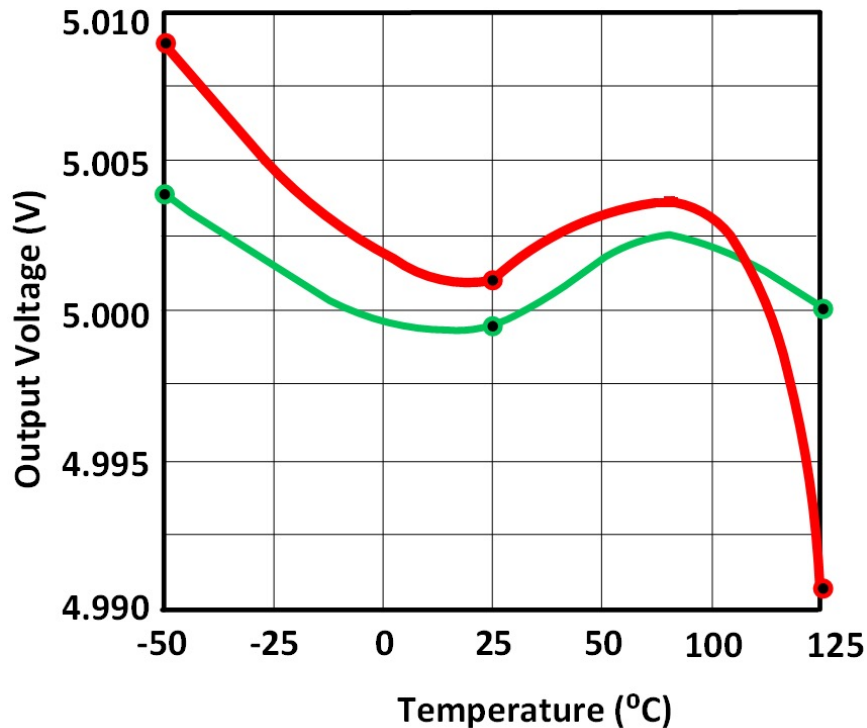
PARAMETER	TEST CONDITIONS	MIN	TYP	MIN	UNIT
LONG-TERM STABILITY: VSSOP-8	0 to 1000 hours at 25°C		125		ppm
LONG-TERM STABILITY: VSSOP-8	1000 to 2000 hours at 25°C		45		ppm
LONG-TERM STABILITY: MSOP-8	0 to 1000 hours at 25°C		100		ppm
LONG-TERM STABILITY: MSOP-8	1000 to 2000 hours at 25°C		50		ppm

96 units
tested.



Caused by curing of the molding compounds, metal migration, and diffusion.
The initial shift (first few months) makes up the majority of change.
Due to Self curing of molding compound.

Temperature Drift (Box Method)

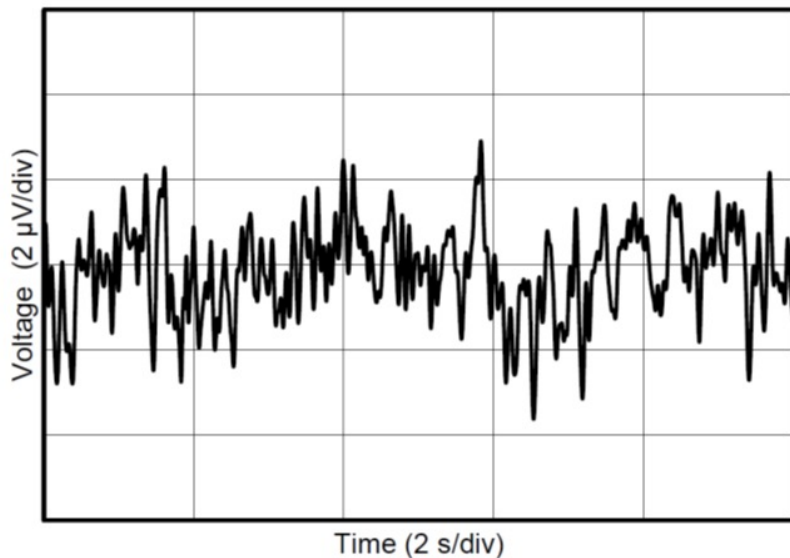


Box Method	$Drift = \left \frac{V_{REF(MAX)} - V_{REF(MIN)}}{V_{REF} \cdot \Delta T} \right \cdot 10^6$
Green	$Drift = \left \frac{5.004 - 4.999}{5.0 \cdot (125^{\circ}C - (-50^{\circ}C))} \right \cdot 10^6 = 5.7ppm/^{\circ}C$
Red	$Drift = \left \frac{5.009 - 4.991}{5.0 \cdot (125^{\circ}C - (-50^{\circ}C))} \right \cdot 10^6 = 20.5ppm/^{\circ}C$

- Change in output voltage vs temp.
- Box method: drift over the entire range.
- Instantaneous drift can be higher or lower.
- If example limit is 20ppm/°C, red fails and green passes.

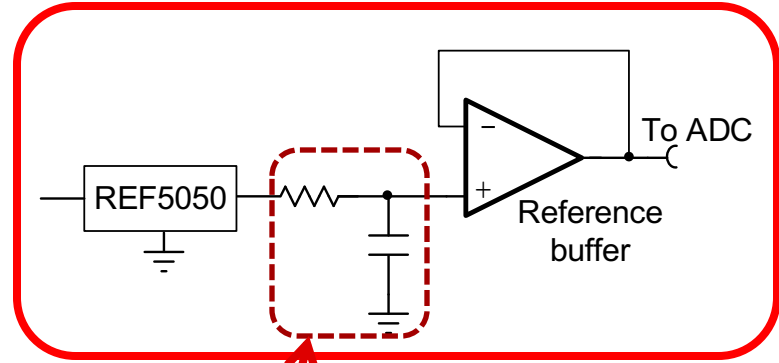
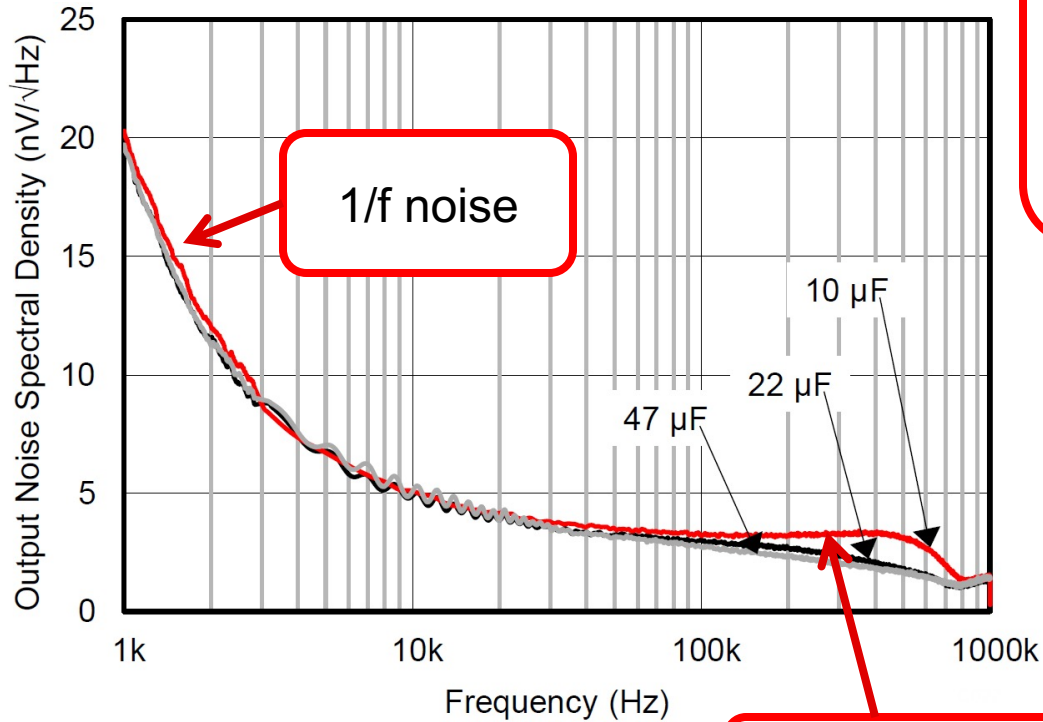
0.1Hz to 10Hz Noise: 1/f noise (flicker noise)

0.1 to 10Hz Noise vs. Time



- Measured using a special band pass filter and oscilloscope.
- Not practical to filter 1/f.
- Looks like temperature drift.
- Good relative comparison of 1/f noise for different references.

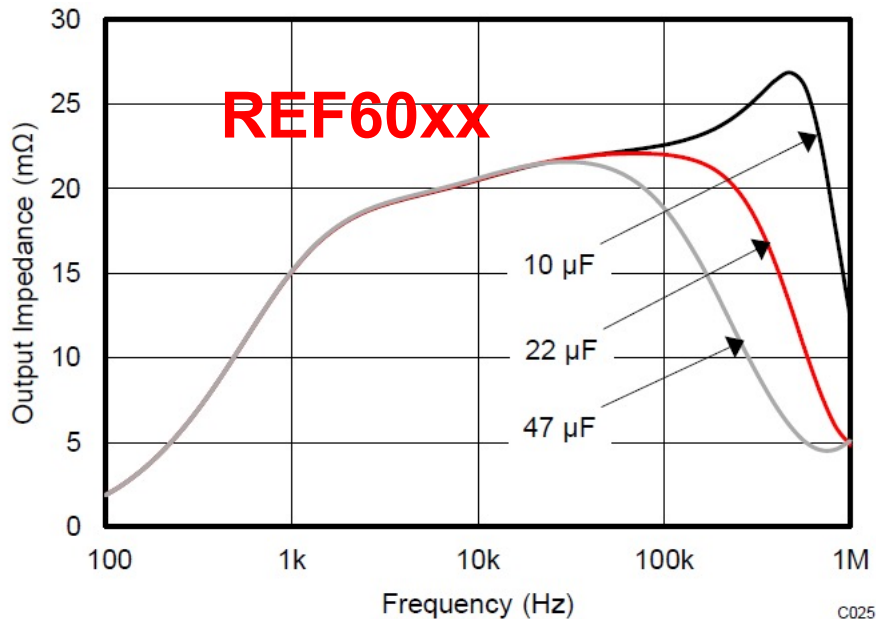
Broadband Noise



Broadband noise minimized with filtering

Broadband noise

Output Impedance



Graph obtained by design simulation

Figure 16. Output Impedance vs Frequency

Important reference specification

Reference Specification	Mitigation
Initial Error	Can be calibrated out.
Solder shift	Can be calibrated out. Can be minimized by careful PCB design and assembly.
Temperature Drift	Very difficult to calibrate.
Long Term Shift	Periodic calibrations can minimize this error. Also, accelerated aging (i.e. baking the system) can be used to eliminate the largest shifts.
Broadband Noise	Increasing the filtering can minimize broadband noise.
1/f Noise	Not practical to eliminate. Choose the lowest 0.1Hz to 10Hz device
Output impedance	Choose references with low output impedance across frequency for driving dynamic loads like SAR reference inputs.

**Thanks for your time!
Please try the quiz.**



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