Deep dive on SiC-based 10kW grid tie inverter design challenges

Bart Basile

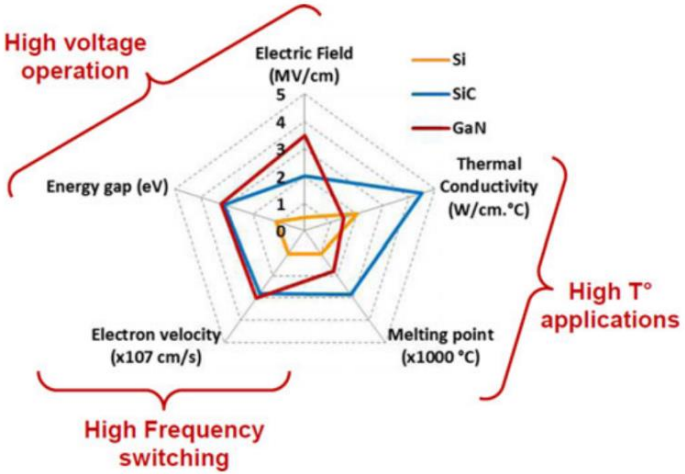
SEM – Grid Infrastructure – Renewable Energy

Asia FAE Summit - 2018

Why SiC?

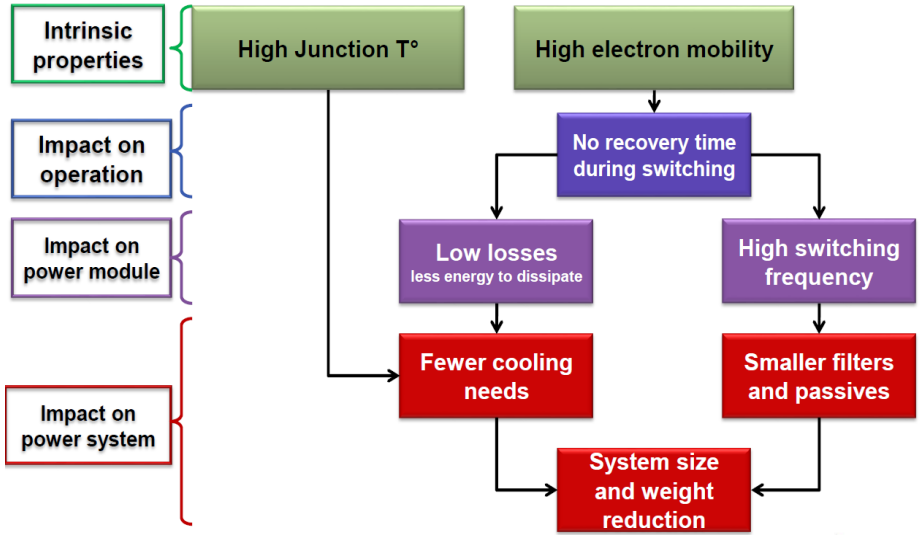
Why SiC?

Intrinsic Material Properties



[Source: "A survey of wide bandgap power semiconductor devices," in *IEEE Transactions on Power Electronics*, 2014, vol. 5]

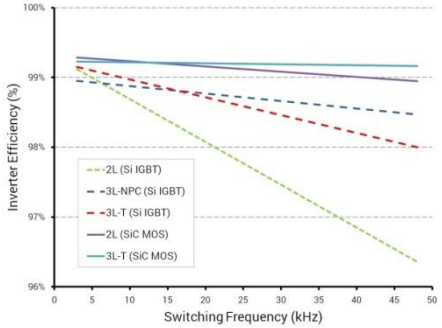
Properties leading to System Benefits

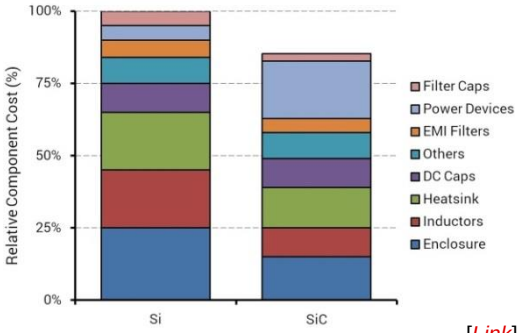


[Source: PSMA Yole Power Market Roadmap 2014]

SiC: system benefit examples

SiC Solution:
- 60% Smaller
- 20% Lower Cost





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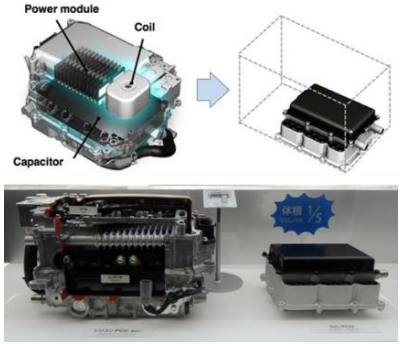
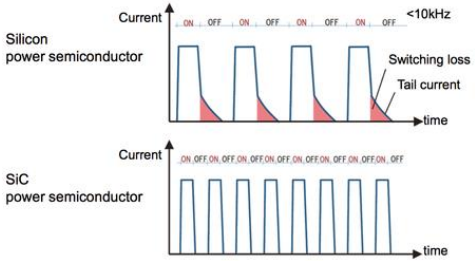
SiC Solution:
- 5X Smaller





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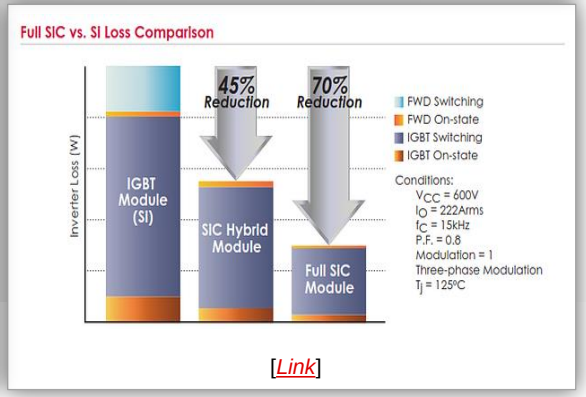

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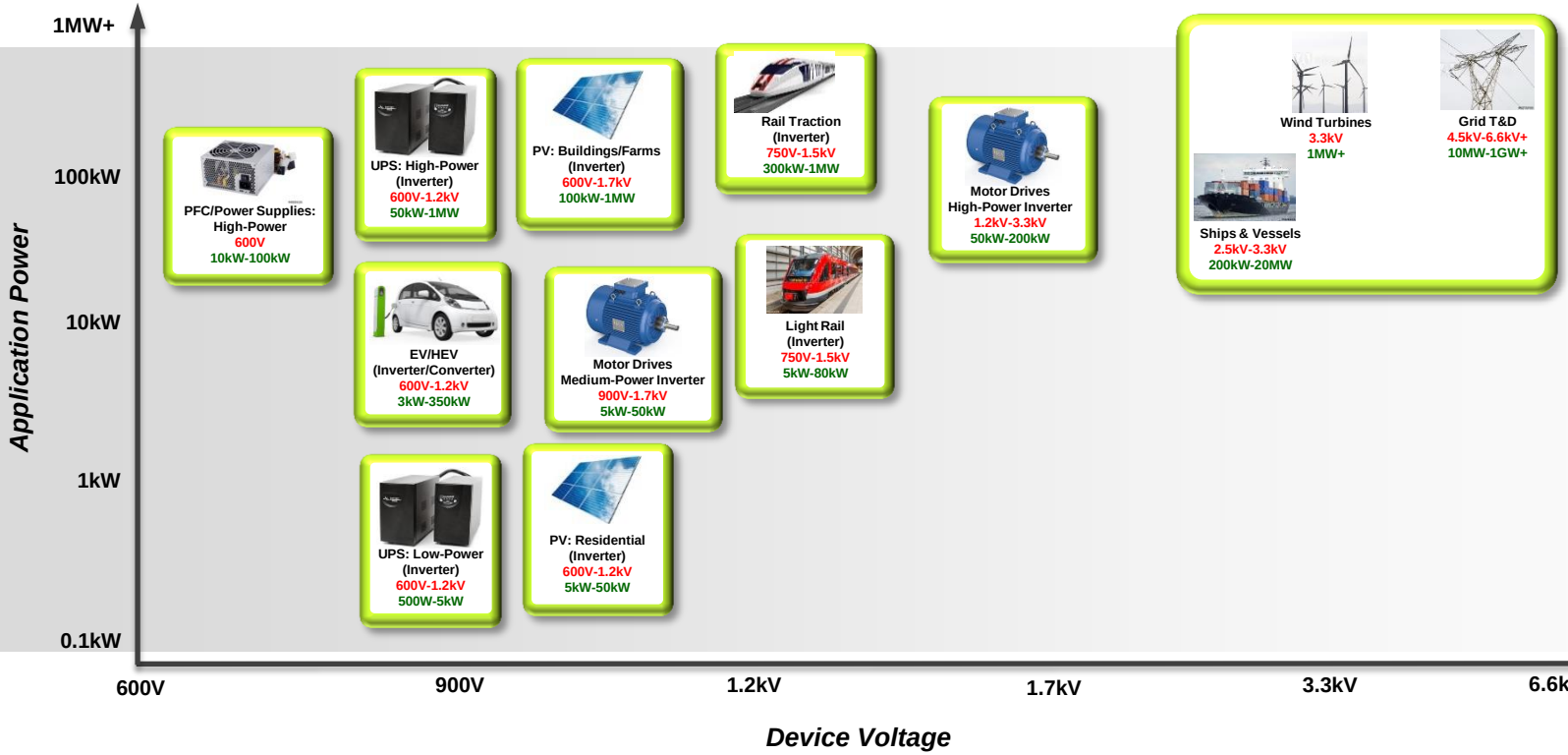
SiC: application landscape



[Sources: PSMA Yole Reports, PCIM'2016]

Texas Instruments

SiC: MOSFET adoption has started …

Rail Traction

Shinkansen Bullet Train

All-SiC Rail Traction Inverter

[Link]

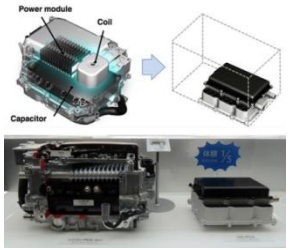
PV: Multi-MW Inverters

[Link]

[Link]

EV/HEV Powertrain Inverter & DC-DC

SiC Solution:
⇒ 5X Smaller than IGBT



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SiC Solution:
⇒ 2X Smaller than IGBT

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EV/HEV On-board & Off-board Chargers

EV On-Board Charger

[Link]

EV/HEV Off-Board Charger

[Link]

SiC: future challenges for mass adoption

System Cost, Size, Weight Reduction

- EV/HEV need **4X-10X smaller size & 40%-80% weight reduction**
- SiC systems need to operate at 4X-10X higher switching frequencies compared to IGBTs
  - ⇒ *Challenge: How to reduce switching losses at considerably higher frequencies?*

Fast Switch Protection

- SiC MOSFETs have **significantly reduced SC capability** (<3µs) compared to IGBTs (10µs)
  - ⇒ *Challenge: How to protect SiC MOSFETs in <2µs in a SC/OC event?*
- SiC systems need to transition at **higher slew rates (*dV/dt*)** as compared to IGBTs
  - ⇒ *Challenge: Need higher isolation & CMTI rated components at lower system cost*

EMI Reduction

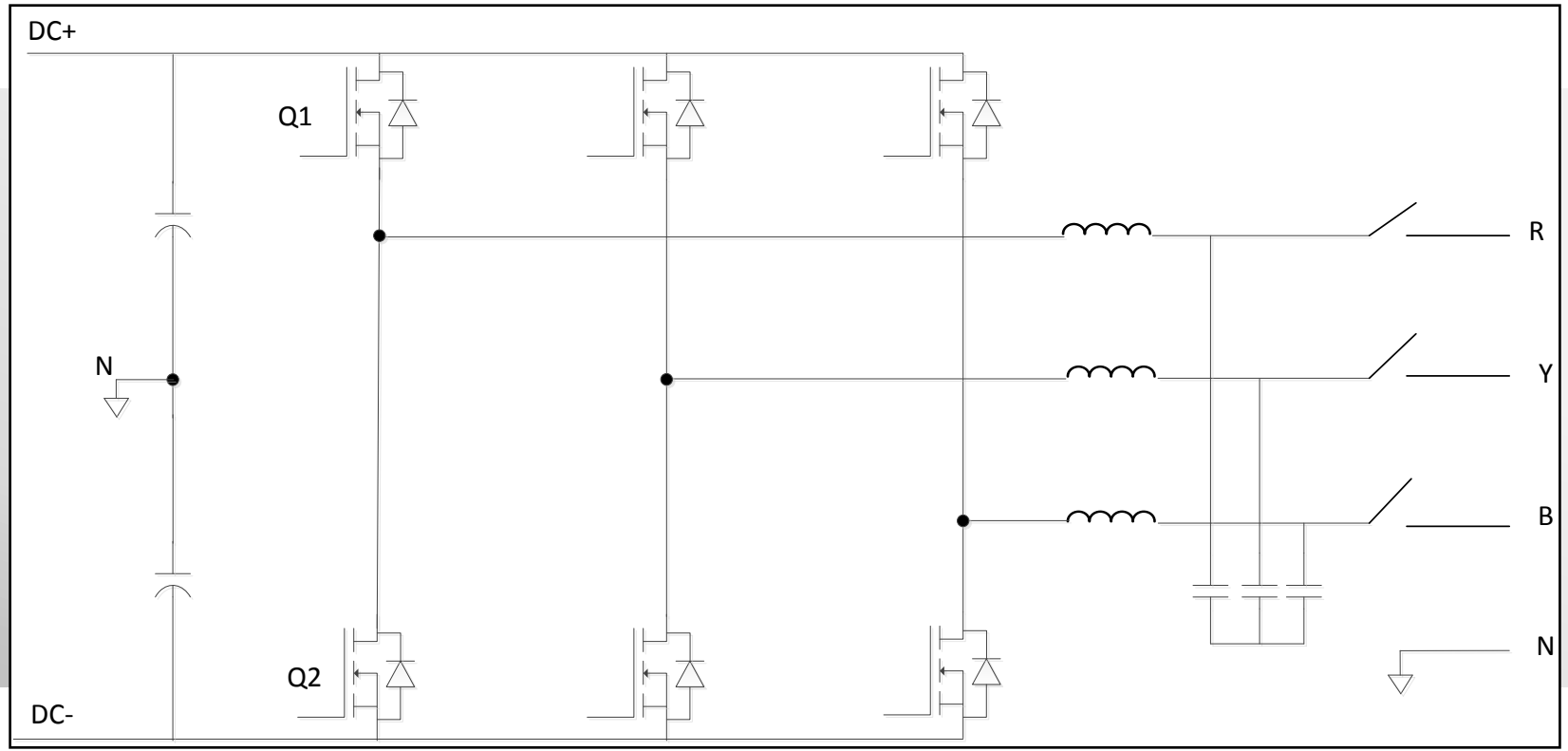
- Higher switching frequencies & slew rates (*dV/dt*) would create **higher Ringing & EMI**
  - ⇒ *Challenge: How to reduce Ringing & EMI without increasing system cost/size/weight?*

System Robustness over Lifetime

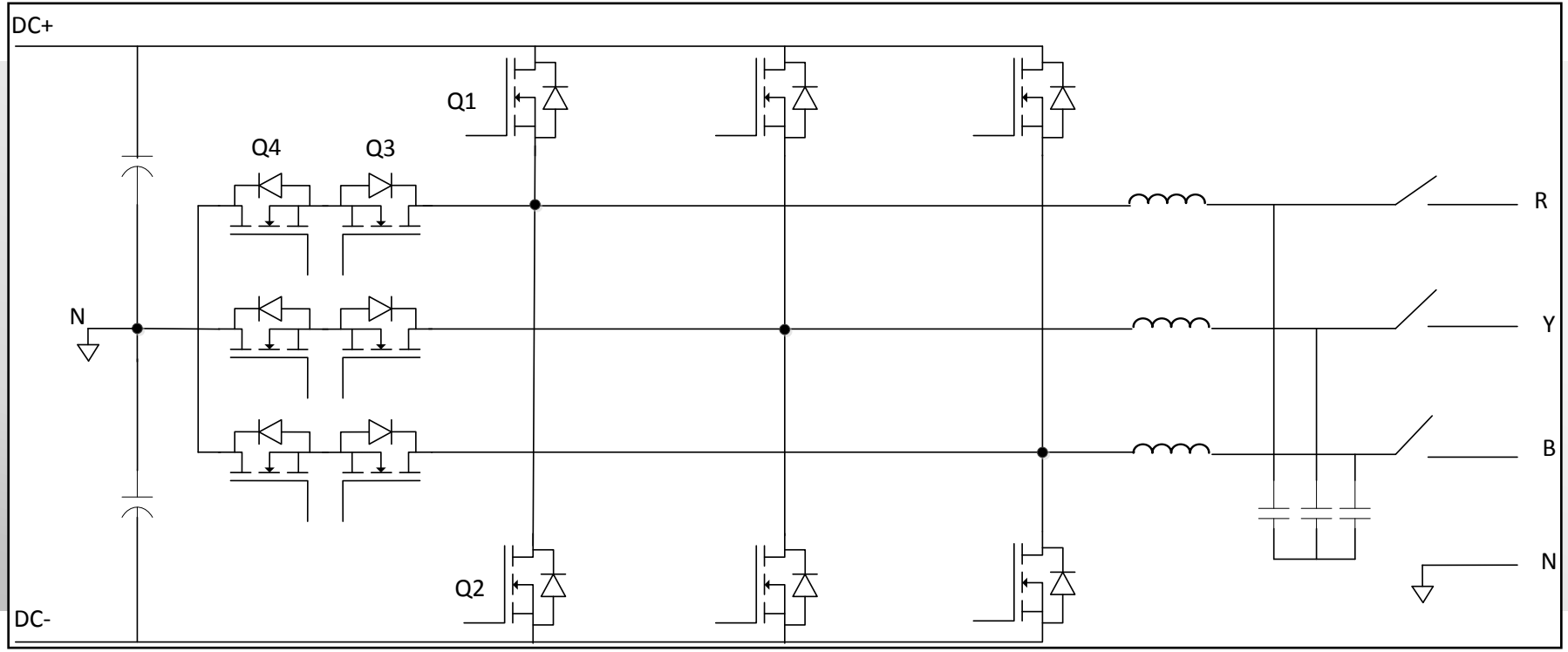
- Higher slew rates (*dV/dt*) would need **higher component derating: Higher system cost**
  - ⇒ *Challenge: How to handle higher dV/dt while reducing system cost?*
- Higher slew rates (*dV/dt*) would **reduce MOSFET lifetime** due to higher voltage excursions
  - ⇒ *Challenge: How to reduce Ringing to guarantee increased lifetime of MOSFETs?*

Topology and FET comparison

Traditional H-bridge inverter



The T-type inverter



T-type advantages

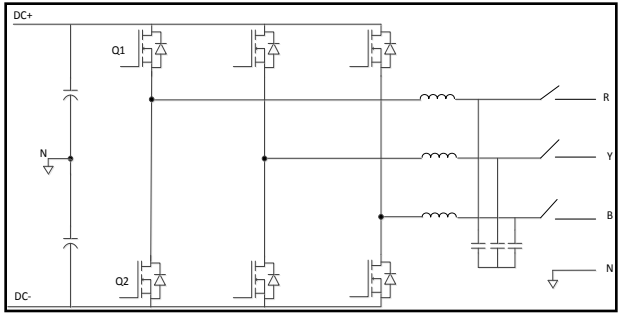
Carried From H-Bridge

- Maintains Low Conduction Losses
- Small Part Count
- Simple Switching Operation

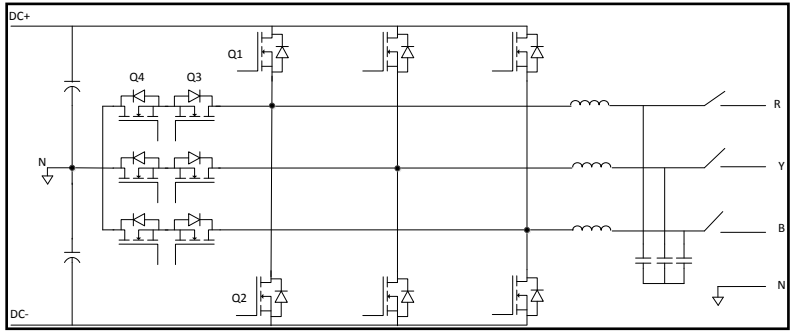
Upgrades to H-Bridge

- Lower Switching Losses
- Lower Output Harmonics
- Reduced Filter Size

Efficiency comparison for grid tie inverter



2-Level Full Bridge



3-Level T-type Inverter

Specifications

AC Output:

3Ph 400V, 50Hz, UPF

10KW output power

DC Input:

800V

Inverter:

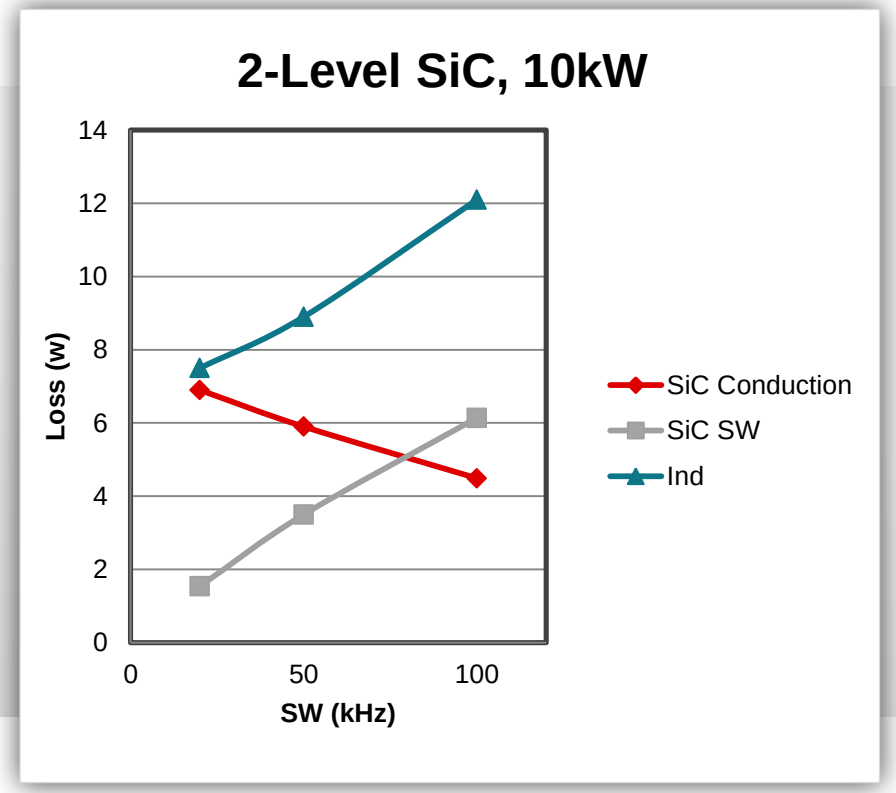
50KHz switching frequency

20% current ripple

2-Level Full Bridge (6 x SiC Mosfet - SIC1MO120E0080)		**3-Level (T-type) Full Bridge** (6 x SiC Mosfet - SIC1MO120E0080) (6 x IGBT – FGH60N60SMD)		**3-Level (T-type) Full Bridge** (6 x SiC Mosfet - SIC1MO120E0080) (6 x Mosfet – IPW65R045C7)	
SiC Mosfet Loss	9.4	SiC Mosfet Loss	5.2	SiC Mosfet Loss	5.2
		IGBT Loss	7.887	Si Mosfet Loss	2.78
3 X Inductors – 833uH		3 X Inductors – 555uH		3 X Inductors – 555uH	
Inductor Loss	8.9	Inductor Loss	6.4	Inductor Loss	6.4
Efficiency		Efficiency		Efficiency	
Total Loss	83.1	Total Loss	100.242	Total Loss	69.6
Efficiency	99.16%	Efficiency	98.99%	Efficiency	99.3%

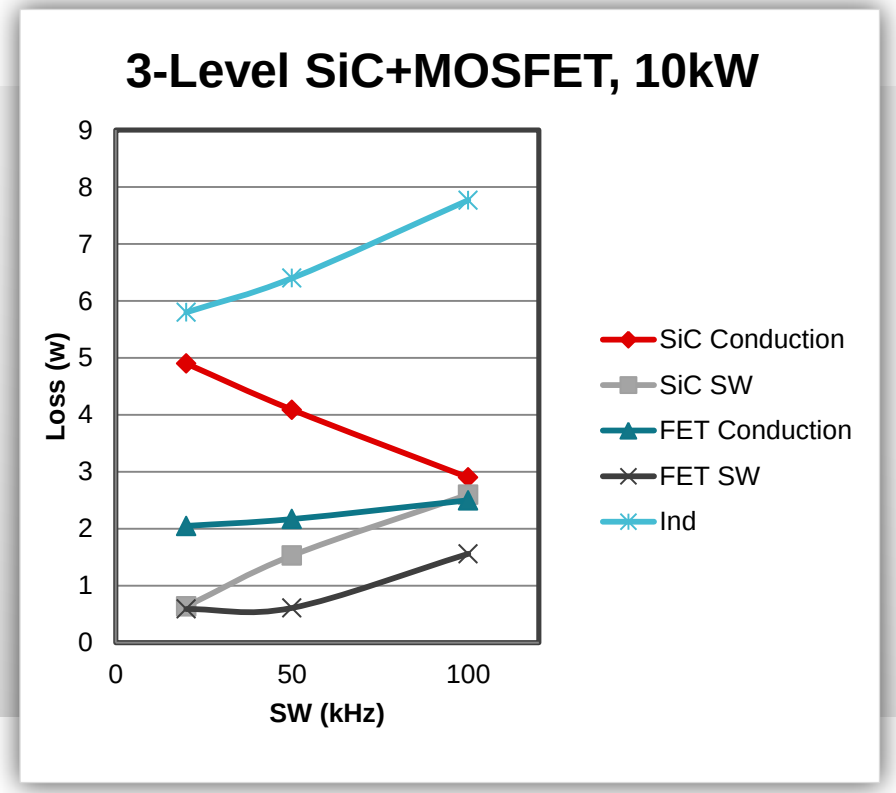
Loss details 2-level SiC

2-Level SiC, 10kW			
SW Speed (kHz)	20	50	100
IND Val	2083uH	833uH	416uH
SiC Conduction	6.9	5.9	4.49
SiC SW	1.54	3.5	6.14
Ind	7.5	8.9	12.1
System Total	73.14	83.1	100.08



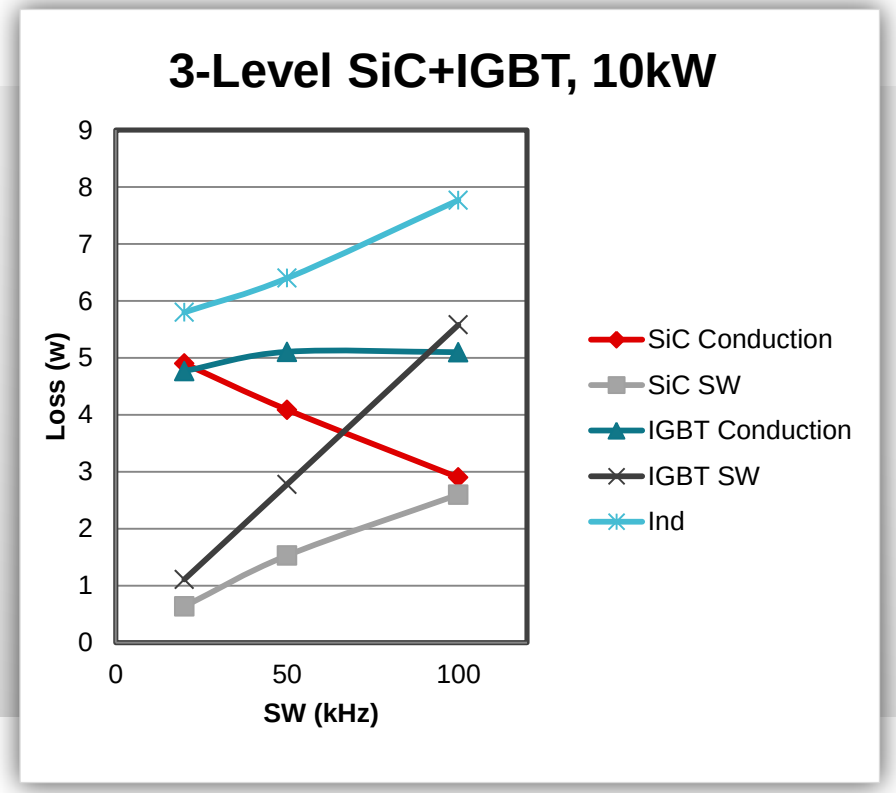
Loss details 3-level SiC+MOSFET

3-Level SiC+SIFET, 10kW			
SW Speed (kHz)	20	50	100
IND Val	1389uH	555uH	277uH
SiC Conduction	4.9	4.09	2.9
SiC SW	0.637	1.53	2.6
FET Conduction	2.05	2.17	2.5
FET SW	0.59	0.61	1.56
Ind	5.8	6.4	7.77
System Total	66.462	69.6	80.67



Loss details 3-level Sic+IGBT

3-Level SiC+IGBT, 10kW			
SW Speed (kHz)	20	**50**	100
IND Val	1389uH	**555uH**	277uH
SiC Conduction	4.9	**4.09**	2.9
SiC SW	0.637	**1.53**	2.6
IGBT Conduction	4.77	**5.107**	5.1
IGBT SW	1.11	**2.78**	5.58
Ind	5.8	**6.4**	7.77
System Total	85.902	**100.242**	120.39



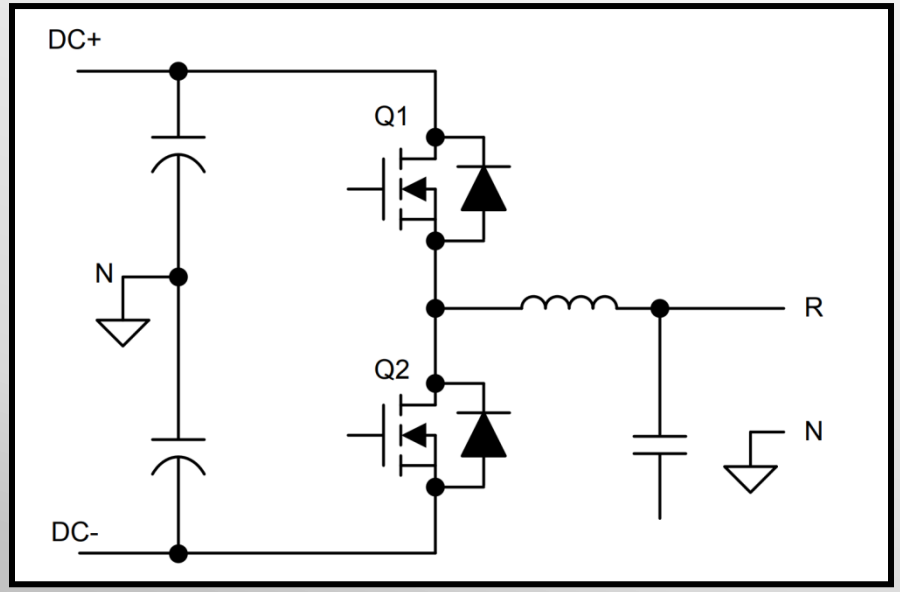
IGBT over SiMOSFET

- Si MOSFET have a resistive feature which helps to reduce conduction loss at light load conditions compared with IGBT, but the high reverse recovery of the body diode will increase voltage and current overshoot. Since SiC MOSFET switches much faster than i devices, the reverse recovery is much more severe.

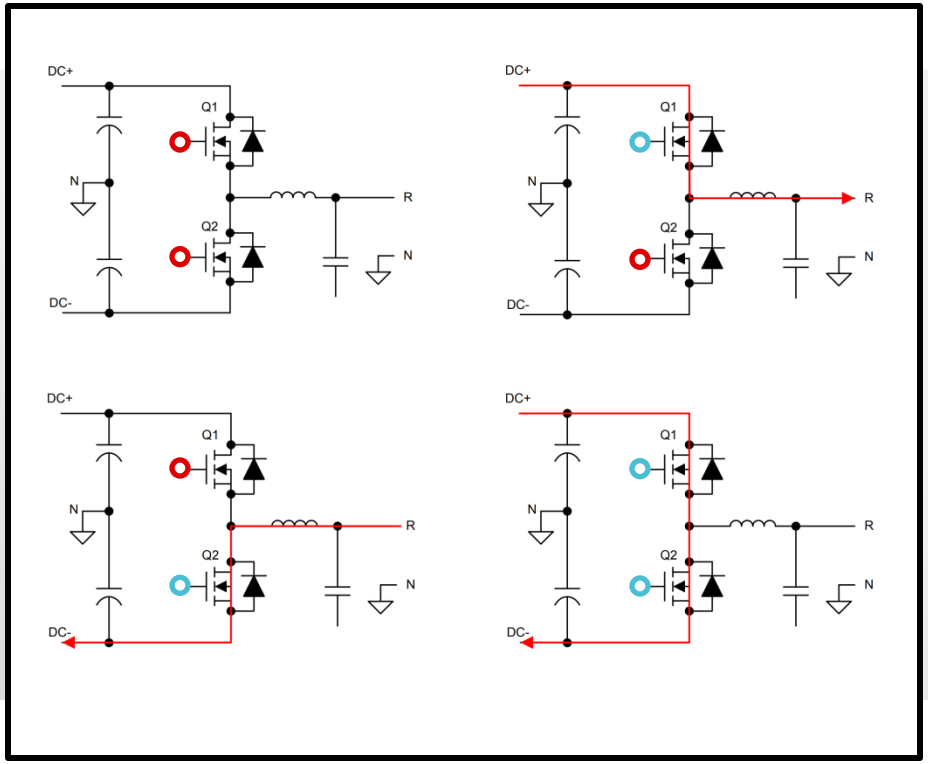
- Si IGBT have higher conduction loss at light load, but the reverse recovery can be lower if a fast recovery diode is used as the antiparallel diode. Moreover, since IGBT is a unidirectional device, the current will always conduct through one anti-parallel diode in T-Type topology, the light load efficiency will be reduced.

T-type conduction

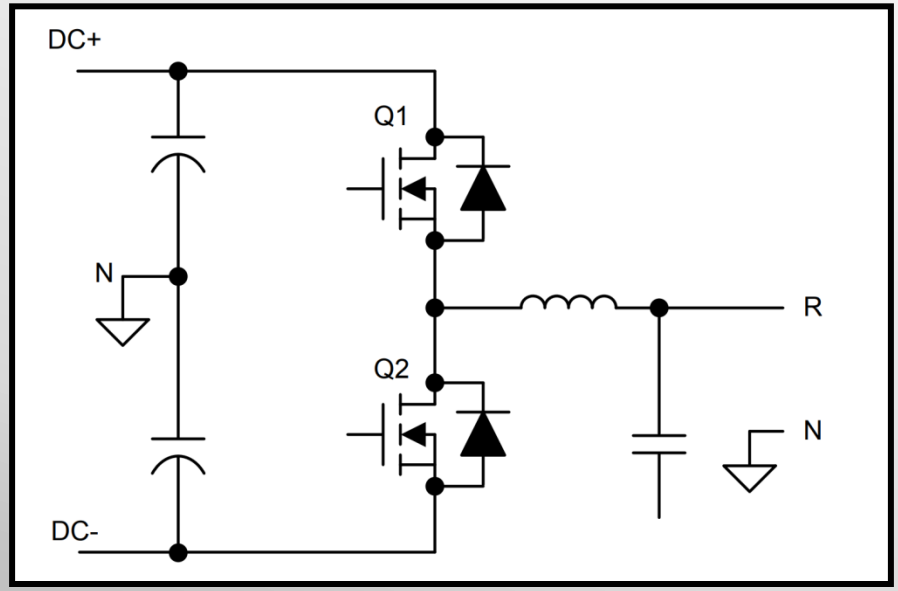
Traditional conduction

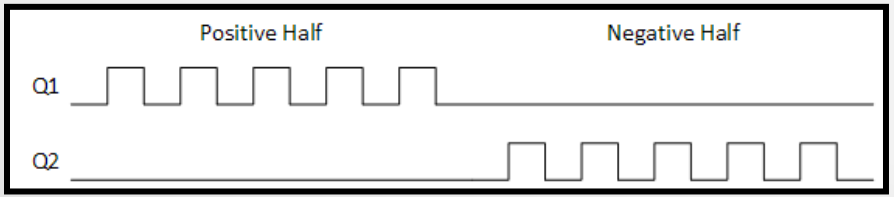


OFF ON



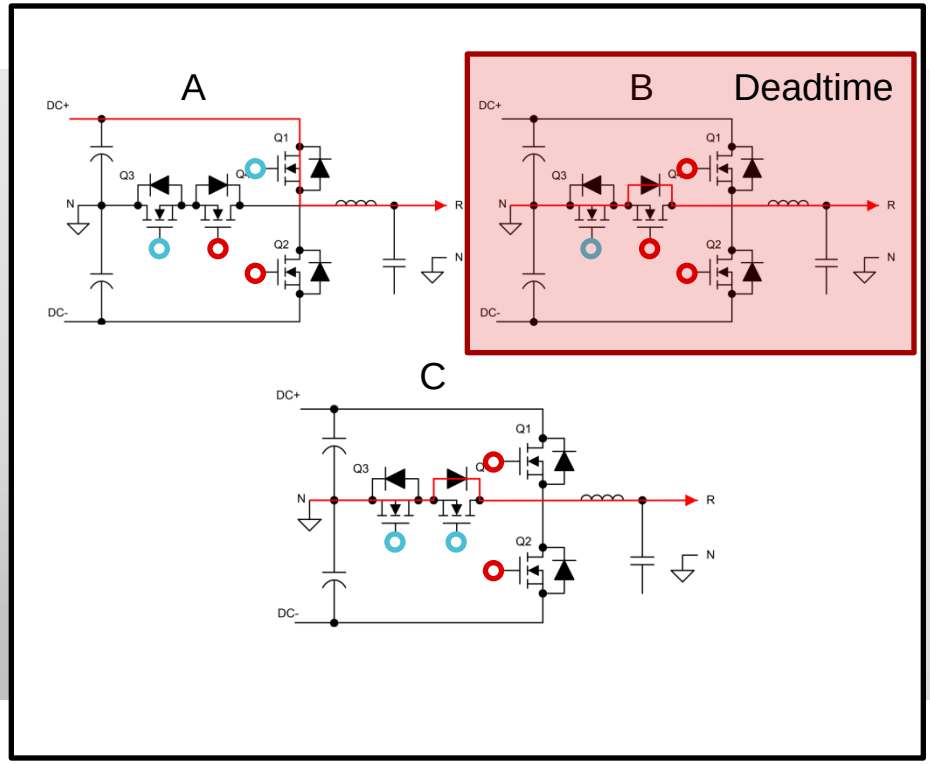
Traditional PWM

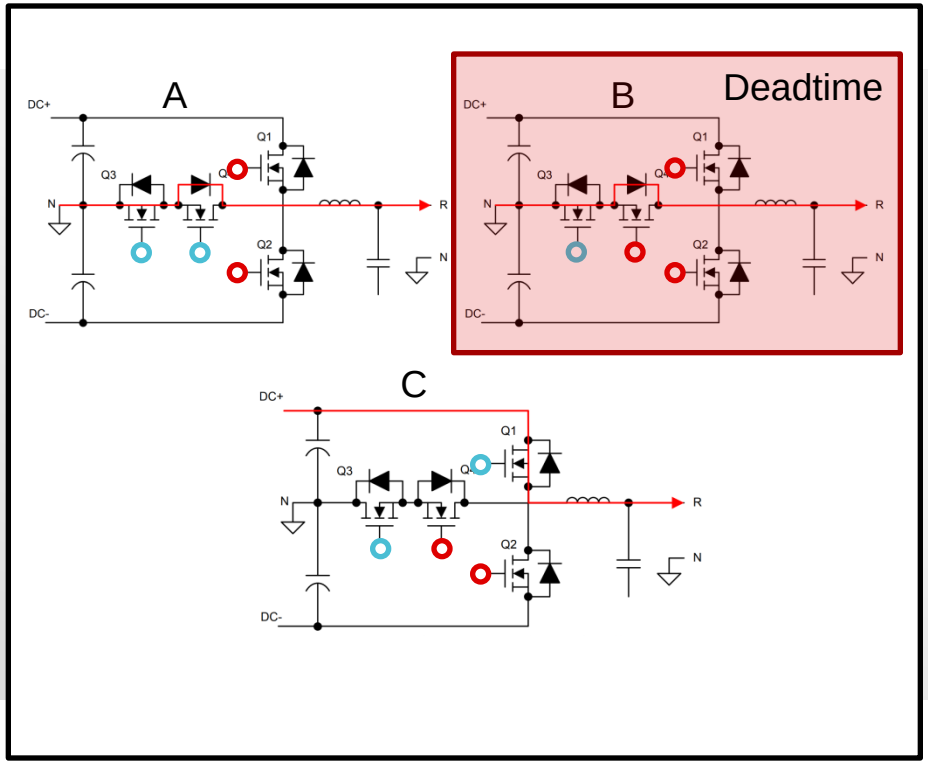




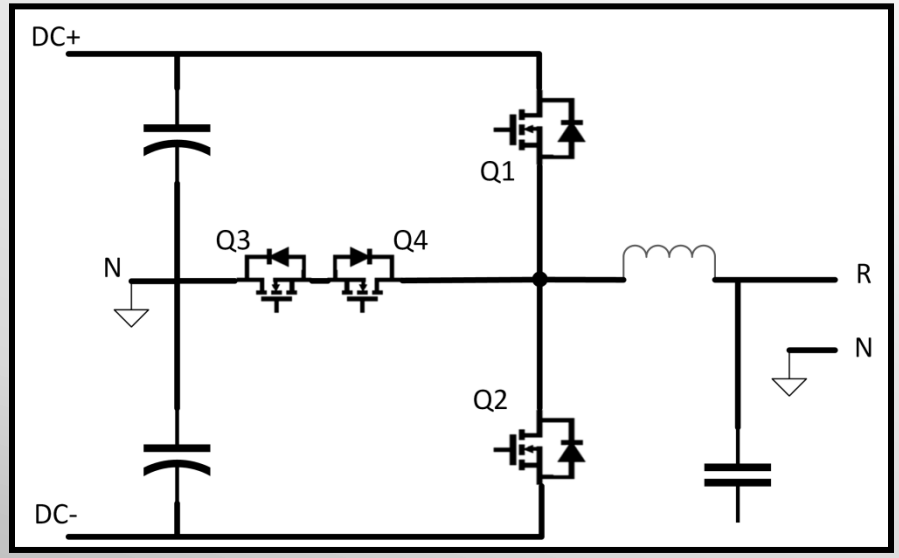
T-Type conduction

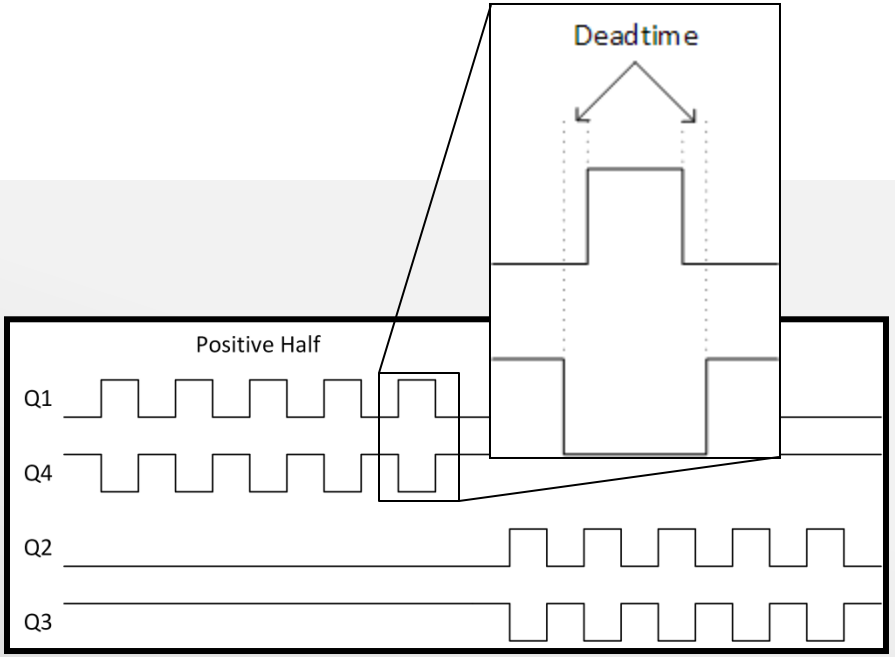
OFF ON





T-Type PWM



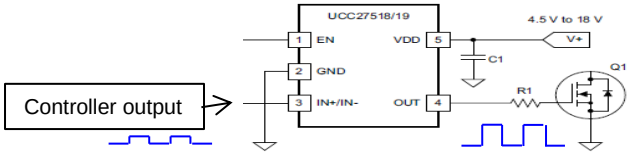


SiC gate drivers

What is a Gate Driver

Definition

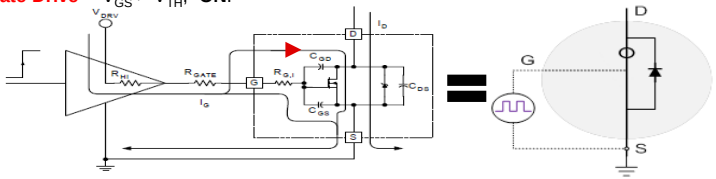
Gate Driver is a power amplifier that turns a low-power signal from a controller IC into the high-current gate drive for a power MOSFET.



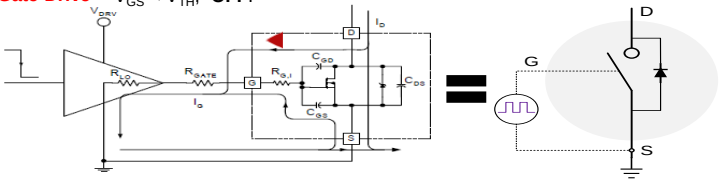
Input Signal: **from controller, can be logic level**

Output signal: **changes state based on input signal**
- **OUT High (ON state) ~ VDD (Souring current)**
- **OUT Low (OFF state) ~ GND (Sinking current)**

Gate Drive $V_{GS} > V_{TH}$, **ON**.



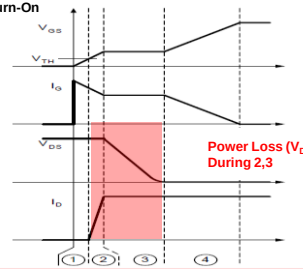
Gate Drive $V_{GS} < V_{TH}$, **OFF**.



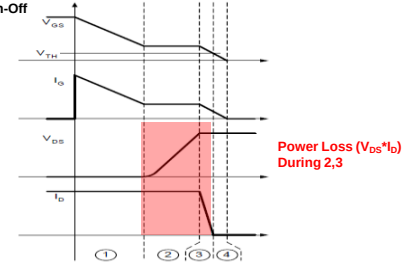
Benefits

Fast charge/discharge of CGS, CGD reduces power loss in time intervals (2) (3)
Therefore reduce Power Dissipation during switching

MOSFET Turn-On

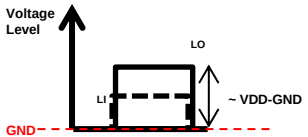


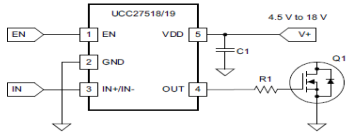
MOSFET Turn-Off



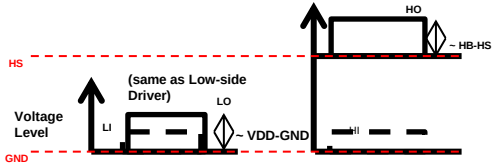
Types

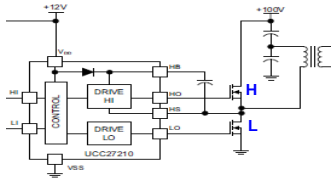
Low side driver





High side-Low side (Half-bridge) driver





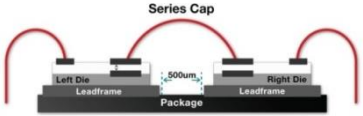
The MOST critical requirements for a SiC driver

- Isolation (Reinforced / Basic)
- High dV_{DS}/dt Immunity (CMTI)
- Fast Over-current / Short-circuit Protection
- Low Propagation Delay & Variation
- High Output Drive Voltage > 25V

SiC driver: new key requirements

Requirement	Reason
High output drive voltage: 25V-35V	Higher Efficiency: Lower conduction loss
▪ Tight voltage control	Gate-oxide protection
▪ Margin to accommodate noise	Gate-oxide protection
▪ Negative supply voltage	Miller turn-ON immunity (Low Vth)
High drive strength	Higher Efficiency: Lower switching loss
High dV_{DS}/dt immunity (CMTI)	Robustness for higher efficiency

TI's Industry-best Capacitive Isolation Technology



- **Industry-leading Integrated Capacitive Isolation**
- **SiO_2 is the most stable dielectric over temperature & moisture**
- **Leverage advantages of TI's customized CMOS process:**
  - High precision
  - Tight part-to-part skew
  - No wear out mechanisms
  - Low defect levels
  - Highest lifetime in the industry: **>1.5 kV_{RMS} for 40 years**
  - Superior transient protection for harsh environments: **>12.8kV peak**

[*Link to* ti.com/isolation]

SiC driver: new key requirements

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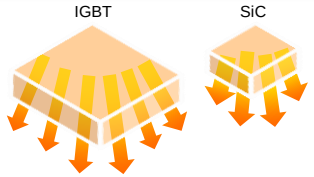
High drive strength	Higher Efficiency: Lower switching loss
High *dV$_{DS}$/dt* immunity (CMTI)	Robustness for higher efficiency
Fast short-circuit protection	Lower short-circuit capability

SiC: Need for Fast Short-Circuit Protection

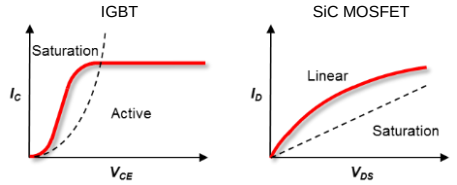
- For same ON resistance, IGBT die is larger than SiC MOSFET die

⇒ SiC MOSFET die has lower thermal dissipation capability than IGBT



- For same rated current & voltage, IGBT reaches active region for significantly lower V_{CE} (high β) as compared to SiC MOSFET

⇒ IGBT self-limits the current increase
⇒ In the case of SiC, I_D continues to increase with increase in V_{DS}, eventually resulting in faster breakdown



[*NOTE*: Drawings not to scale.]

SiC driver: new key requirements

Requirement	Reason
High output drive voltage: 25V-35V	Higher Efficiency: Lower conduction loss
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▪ Negative supply voltage	Miller turn-ON immunity (Low Vth)
High drive strength	Higher Efficiency: Lower switching loss
High dV_{DS}/dt immunity (CMTI)	Robustness for higher efficiency
Fast short-circuit protection	Lower short-circuit capability
Small propagation delay & variation	Higher Efficiency + Faster System Control
Switch Temperature Sensing	Advanced switch protection

Short-circuit protection: hardware validation

Goals

- Evaluate short-circuit protection capability through measurements using IGBT/SiC half-bridge module

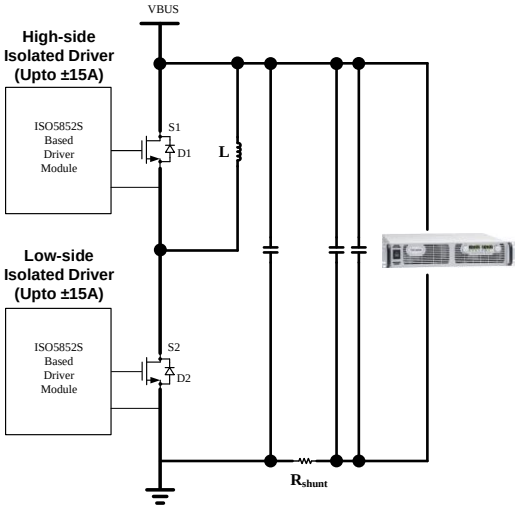
⇒ Test feasibility of reliable short-circuit protection based on ISO5852S driver architecture

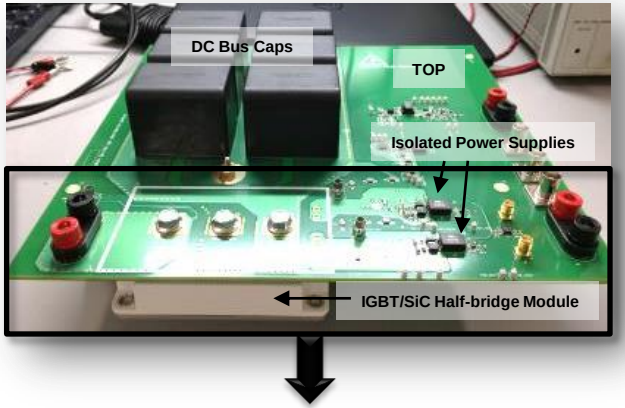
⇒ Test reliable operation of isolated driver in high drive current (up to ±15A) condition

⇒ Confirm reliable short-circuit protection of IGBT/SiC modules

Evaluation Hardware

Schematic for Double-Pulse Test Setup

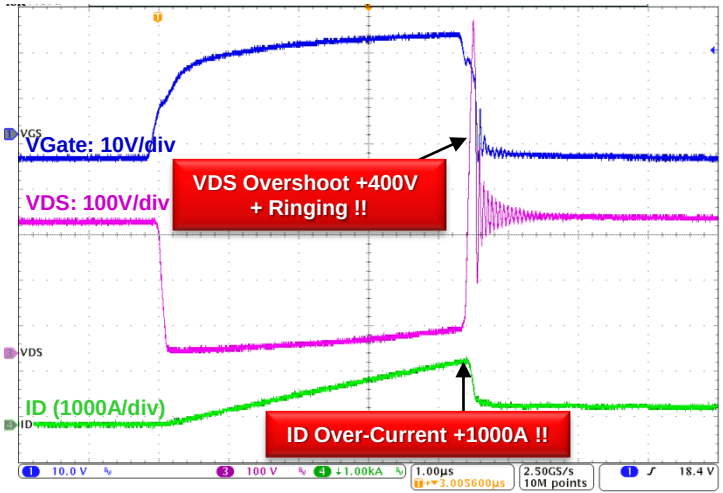




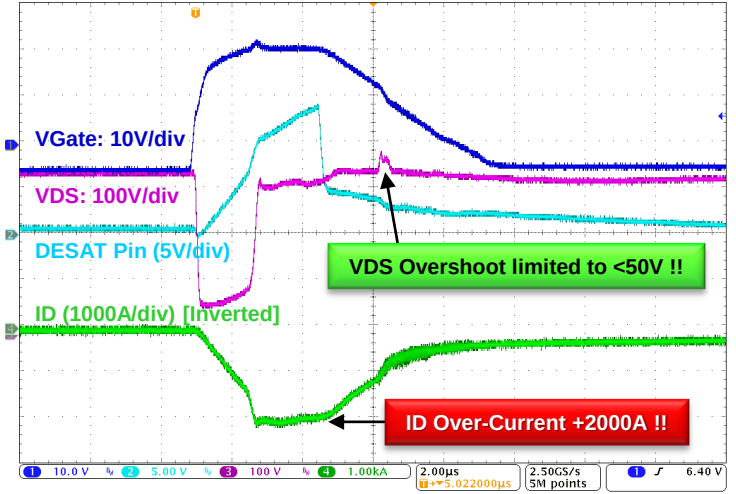
Isolated Half-bridge Drive Stage using ISO5852S-Q1 + 15A Buffer Driver

Short-circuit protection: SiC: delayed load short

Without Soft Turn-OFF



With Soft Turn-OFF

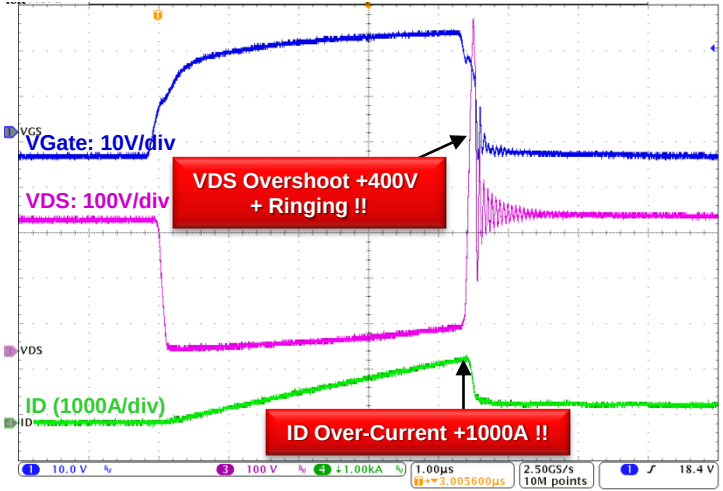


- Reliable short-circuit protection in <1µs
- VDS overshoot significantly improved with Soft Turn-OFF

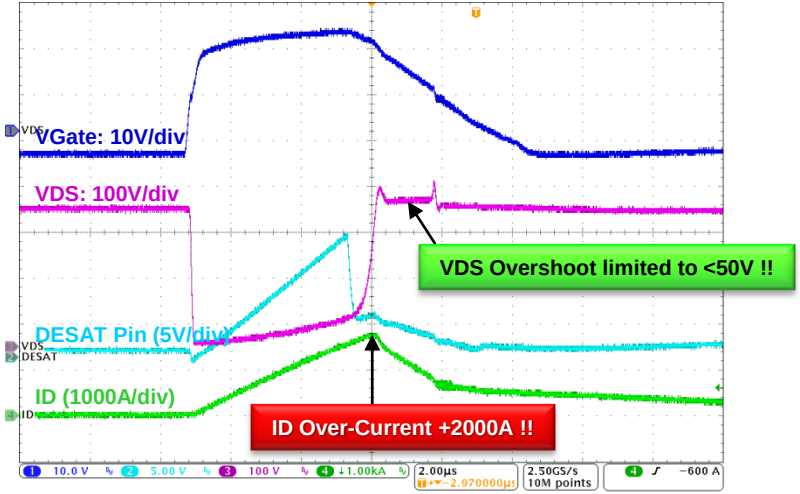
⇒ **ISO5852S: Reliable Soft Turn-OFF for safe shutdown**

Short-circuit protection: SiC: turn ON into short

Without Soft Turn-OFF



With Soft Turn-OFF



- Reliable short-circuit protection in <1µs
- VDS overshoot significantly improved with Soft Turn-OFF

⇒ **ISO5852S: Reliable Soft Turn-OFF for safe shutdown**

Reference Design for Reinforced Isolation 3-Phase Inverter with Current, Voltage and Temp Protection / *TI Design : TIDA-00366*

TIDesigns

Features

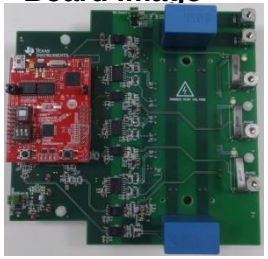
- Reinforced isolated Inverter suited for 200 – 690V AC drives rated up to 10kW
- Simple yet effective gate driver with 4A source, 6A sink output current capability
- 250kHz isolated amplifier for Inverter current, DC link voltage and IGBT module temperature measurement
- Uncalibrated current measurement accuracy of ±0.5% across temperature range from -25˚C to 85˚C
- Protection against DC bus Under-Voltage, Over-Voltage, Over-Current, Ground Fault and Over-Temperature

Target Applications

- Variable Speed AC Drives
- Three-Phase UPS
- Industrial Power Supplies

Tools & Resources

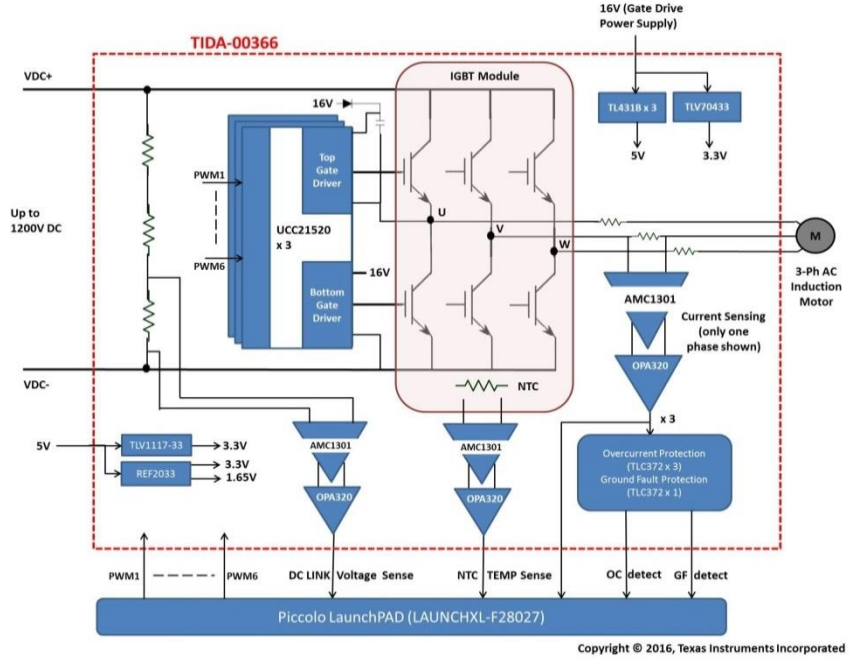
Board Image



- **TIDA-00366 and Tools Folder**
- **Design Guide**
- **Design Files:** Schematics, BOM, Gerbers, and more
- **Device Datasheets:**
  - UCC21520
  - OPA320
  - TLC372
  - REF2033
  - AMC1301
  - TLV1117-33
  - TLV70433
  - TL431B

Benefits

- Using AMC1301 enables use of internal ADC of MCU
- Bootstrap based power supply for high side gate driver reduces overall cost for power supply requirements
- 19ns typical Propagation Delay optimizes dead band distortion



Texas Instruments

ISO5852S

+2.5A/-5A, Isolated, High CMTI, Miller Clamp

Features

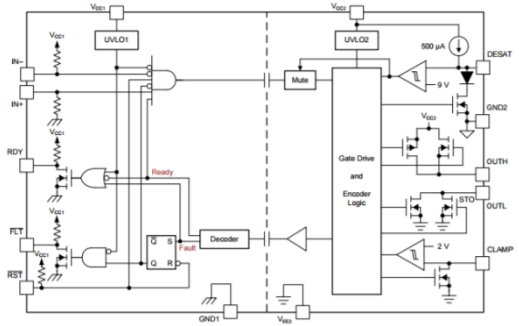
- **Integrated SiO_2 Dielectric Capacitor**
  - CMOS compatible logic input threshold
  - Safety Features: Miller Clamp, Desat Detect, UVLO, Fault feedback, Ready status feedback, auto soft-shutdown on short
  - +2.5/-5A Peak Source/Sink Split Outputs
  - 120 kV/µs CMTI (typ) / 100 kV/µs (min)
  - 30ns Integrated Glitch Filter
  - 110 ns (max) Prop Delay
  - 4kV ESD on all pins
- **Immunity and Certifications**
  - 12.8 kVpk Surge (8 kV V_{IOSM}) per VDE Reinforced Isolation
  - 5.7 kVrms Isolation rating per UL1577
  - 8000 Vpk V_{IOTM} (transient) and 2121 Vpk V_{IORM} (working voltage) per VDE0884-10
  - Enables IEC61800-5-1, IEC60664-1 & IEC62109-1
- **Power and Package**
  - Wide V_{CC2} Range: 15V-30V
  - 16-pin Wide SOIC Package (>8mm Creepage)
  - Extended Temp: -40 to 125 ºC

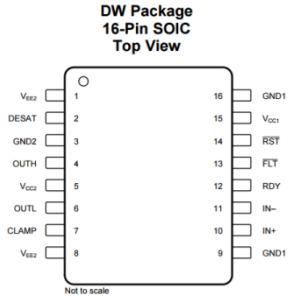
Benefits

: AEC-Q100

- Component-level Reinforced rating
- Improved system performance
- Enabling low power & efficient solutions
- High Immunity for Noisy Environments
- High Reliability in Harsh Environments
- Certified by all 3 World Wide agencies

PART #	Split outputs	Soft Turnoff	UVLO+/ UVLO- (typ)	PKG
ISO5852S	Yes	Yes	11.6/10.3	16DW





UCC5320ECD, UCC5320SCD, UCC5320SCDWV

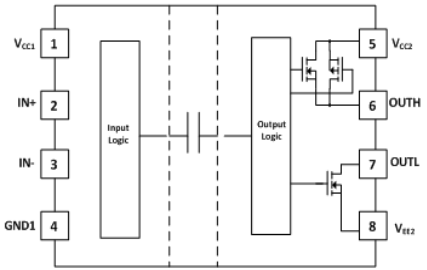
2A/2A Single-Channel Isolated Gate Driver with Split Output (S) or for Bipolar Supply (E)

Features

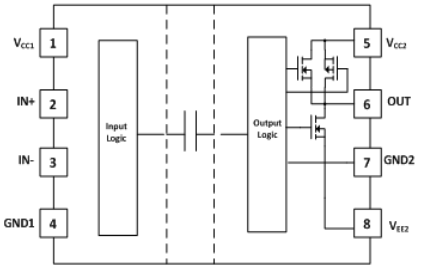
- **Integrated SiO_2 Dielectric Capacitor**
  - 2A/2A Peak Source/Sink Drive
  - >100 kV/us CMTI
  - 100 ns Propagation Delay (max)
  - Negative voltage handling on input pins (-5V)
  - 4kV ESD on all pins
- **Immunity and Certifications**
  - Basic and Reinforced Isolation
  - Safety-related certifications:
    - 7000-VPK Isolation (DWV) and 4242-VPK Isolation (D) per DIN V VDE V 0884-11:2017- 01 (Planned)
    - 5000-V_{RMS} (DWV) and 3000-V_{RMS} (D) Isolation Rating for 1 minute per UL 1577
    - CQC Certification per GB4943.1-2011 (Planned)
- **Power and Package**
  - Wide V_{CC2} Range: 13.2 to 33V
  - 8-pin Narrow Body SOIC (4 mm Creepage) or 8-pin Wide-Body SOIC (8mm Creepage)
  - 3V to 15V input supply range

Benefits

- Family (UCC53x0) with different configuration options available
- UCC53x0SCD allows control of rise and fall time of driver. UCC53x0ECD has UVLO2 referenced to GND2 which facilitates bipolar supplies
- Enabling low power & efficient solutions
- Improved system performance



Split Outputs



UVLO w.r.t GND2

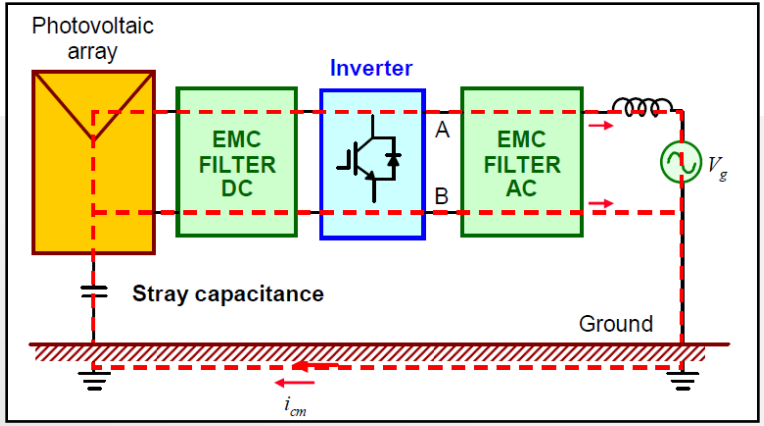
System grounding and isolation

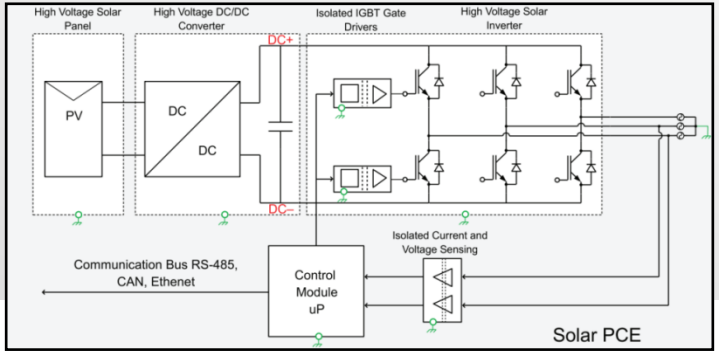
Compliance standard for leakage currents

According to the German standard **VDE 0126-1-1**, there are three different currents that have to be monitored:

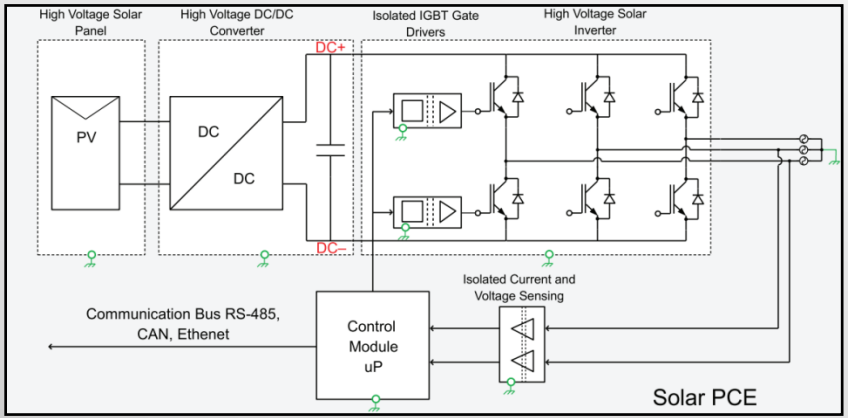
- **Ground Fault current**, which happens in case of insulation failure when the current flows through the ground wire;
- **Fault current**, which represents the sum of the instantaneous values of the main currents, that in normal conditions leads to zero;
- **Leakage Ground currents**, which is the result of potential variations of capacitive coupled parasitic elements

The standard states that disconnection from the grid is necessary within 0.3s in case the leakage current is higher than 300mA





System isolation



Option 1: System ground - Earth

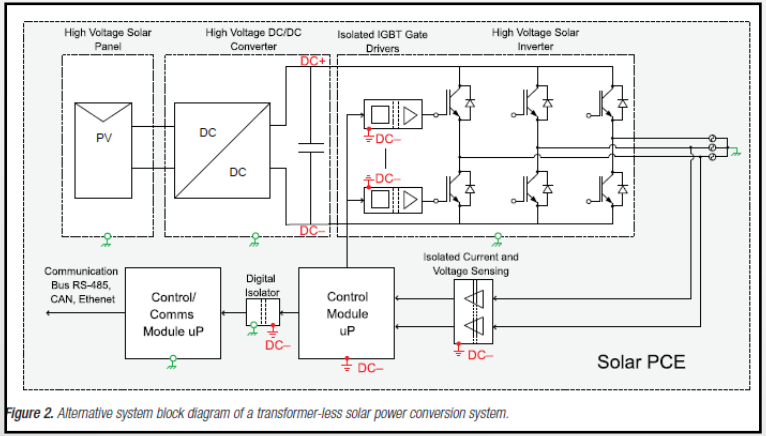
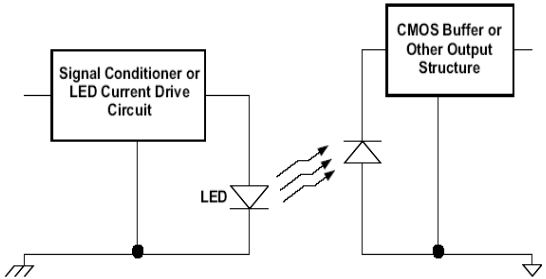


Figure 2. Alternative system block diagram of a transformer-less solar power conversion system.

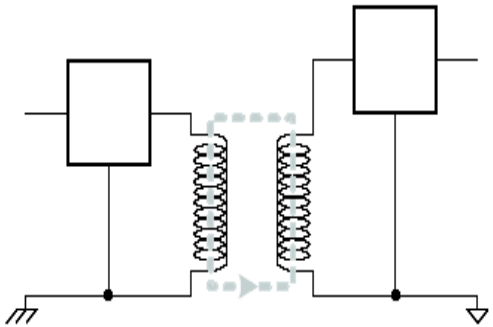
Option 2: System ground – DC-

Isolation technologies

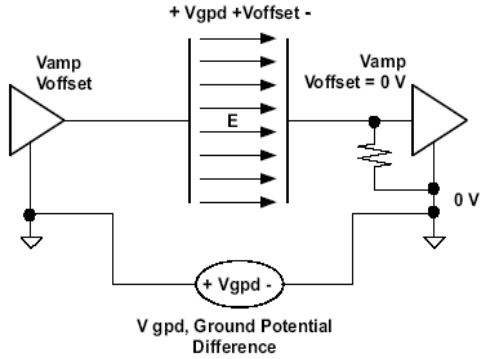
Optical



Magnetic



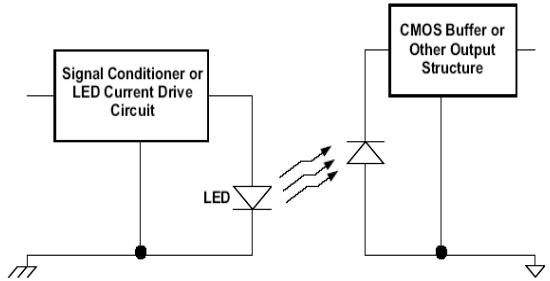
Capacitive



Optical & magnetic isolation: major drawbacks

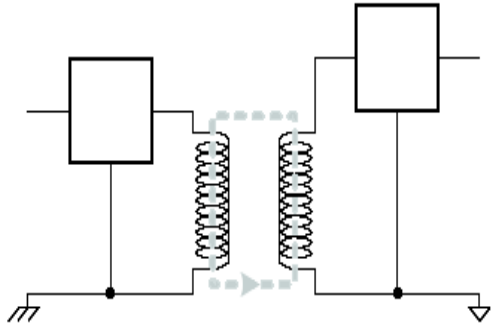
Optical Isolation: Major Drawbacks:

- Low performance
  - Long propagation times
  - Higher quiescent current
- Low robustness and reliability
  - Low noise immunity: Low common mode transient immunity
  - LED Degradation associated with temperature and age



Magnetic Isolation: Major Drawbacks

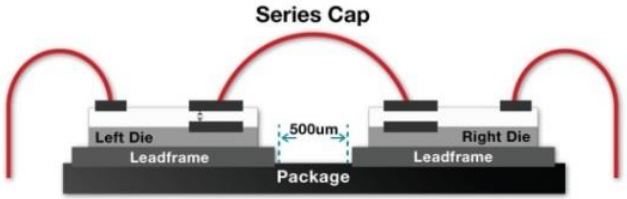
- Low robustness
  - Lower working voltage → Translates to limited applications
  - Low noise immunity: Low common mode transient immunity
  - High EM emissions – noise issues
- Lower reliability
  - Higher quiescent current
  - Insulator degradation over time



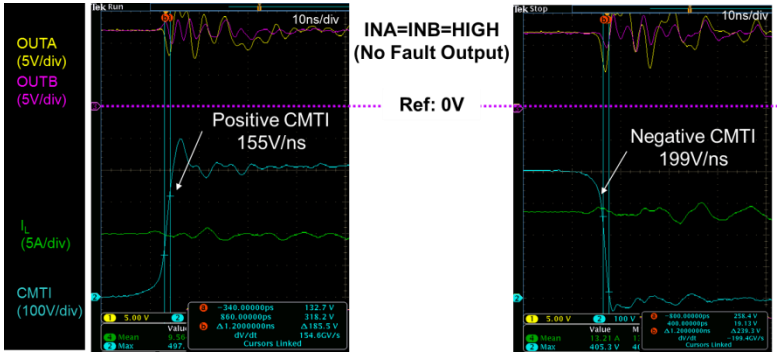
✓ **Capacitive isolation technology does not suffer from the above drawbacks**

TI’s capacitive signal isolation technology

- **Industry-leading Integrated Capacitive Isolation**
- **SiO_2 is the most stable dielectric over temperature & moisture**
- **Leverage advantages of TI’s customized CMOS process:**
  - High precision
  - Tight part-to-part skew
  - No wear out mechanisms
  - Low defect levels
  - Highest lifetime in the industry: **>1.5 kV_{RMS} for 40 years**
  - Superior transient protection for harsh environments: **>12.8kV**



UCC21520 CMTI Results



TIDA-01606 system design

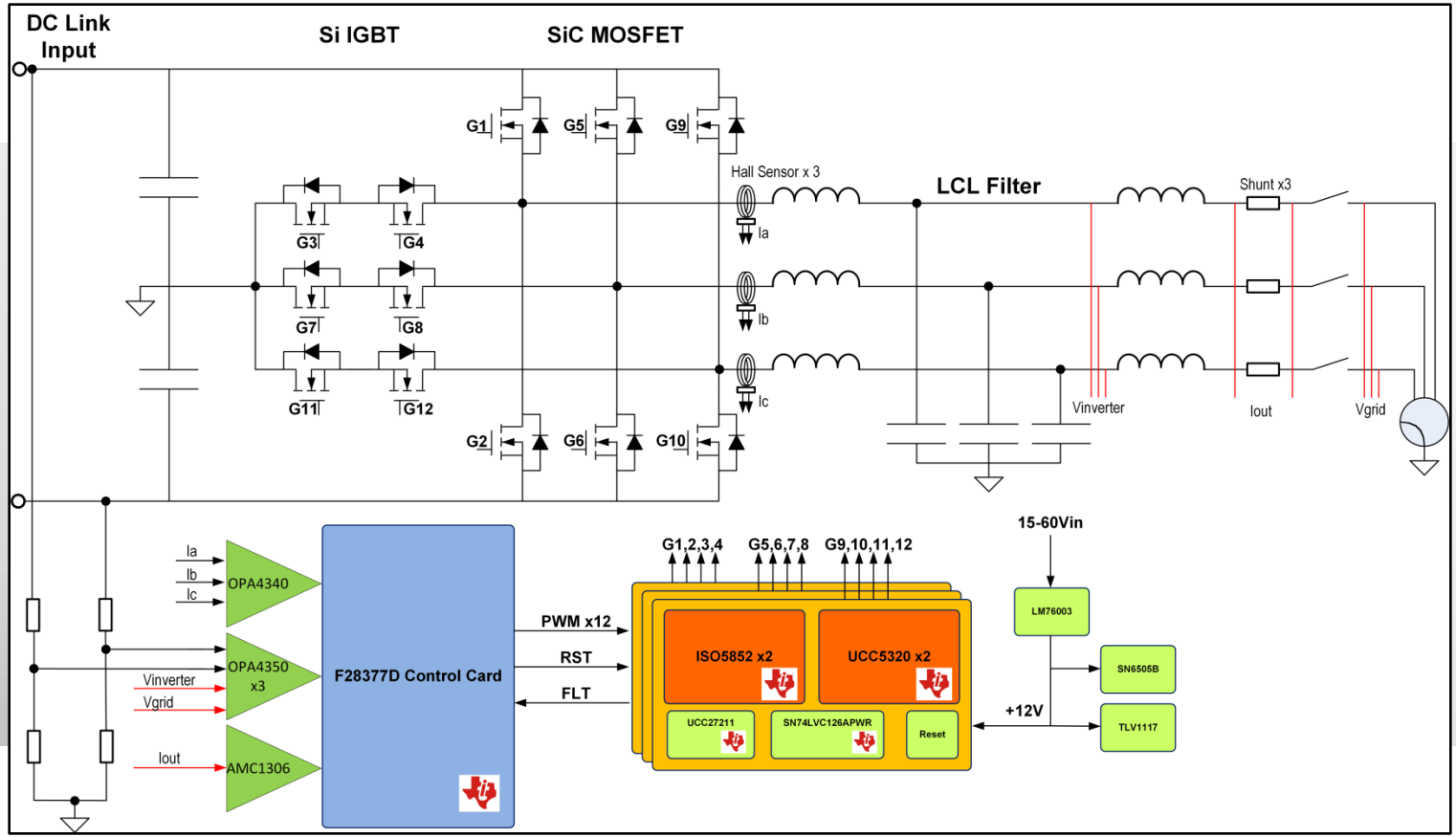
Specifications

AC Output	Power (KW/KVA)	10/10
	PF rated/adjustable	1/0.7lag to 0.7lead
	Grid Voltage (L-L)	400V ± 20%
	No of Phases	3
	Frequency	50/60Hz ± 5Hz
	Current (Max)(A)	18
DC Input	Nominal Voltage (V)	800
	Rated Min/Max Voltage (V)	600/1000
Performance	Efficiency (peak/European)	98.5%
	Output current THD	<2%
Other Specs	Off Grid operation	No
	Operating temperature	-25˚C to +60˚C
	Thermal management	Forced air cooling

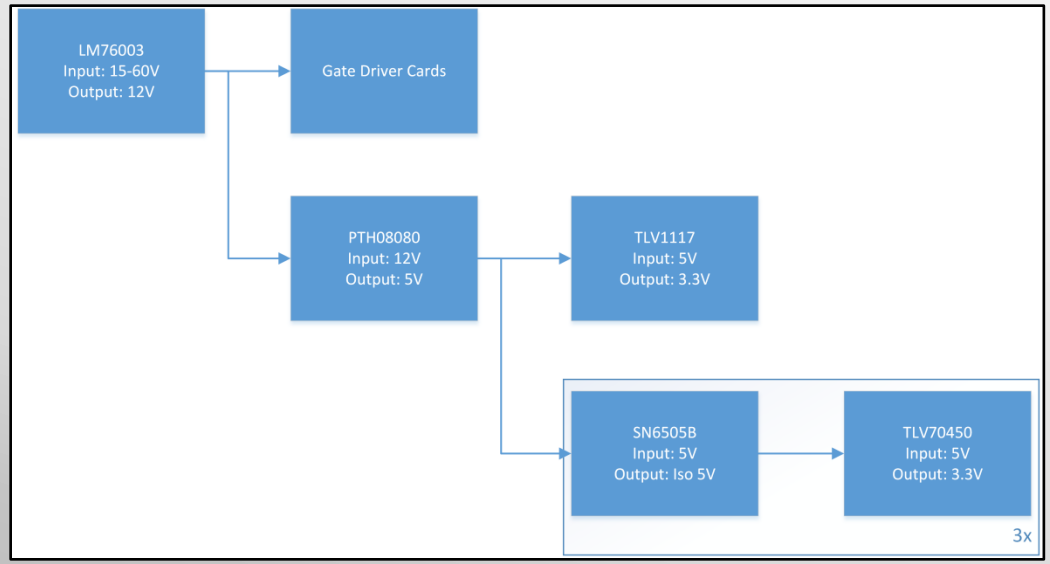
Target End Equipment's

String Inverters – Residential/Commercial

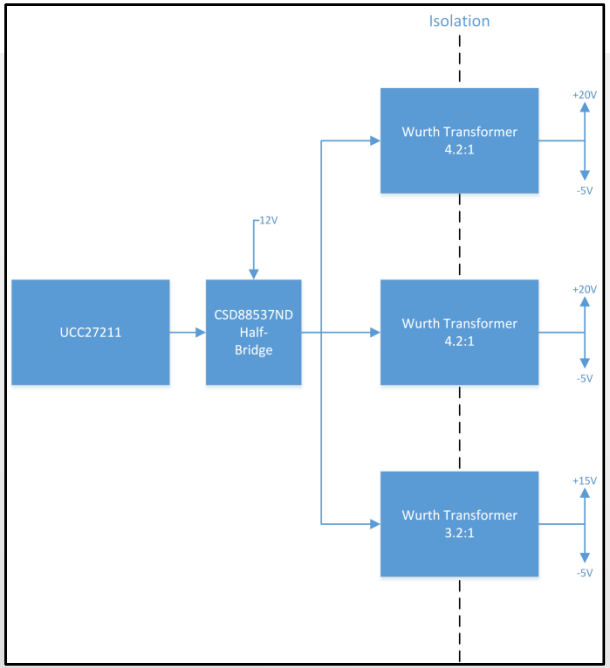
Topology & system architecture



System power topology

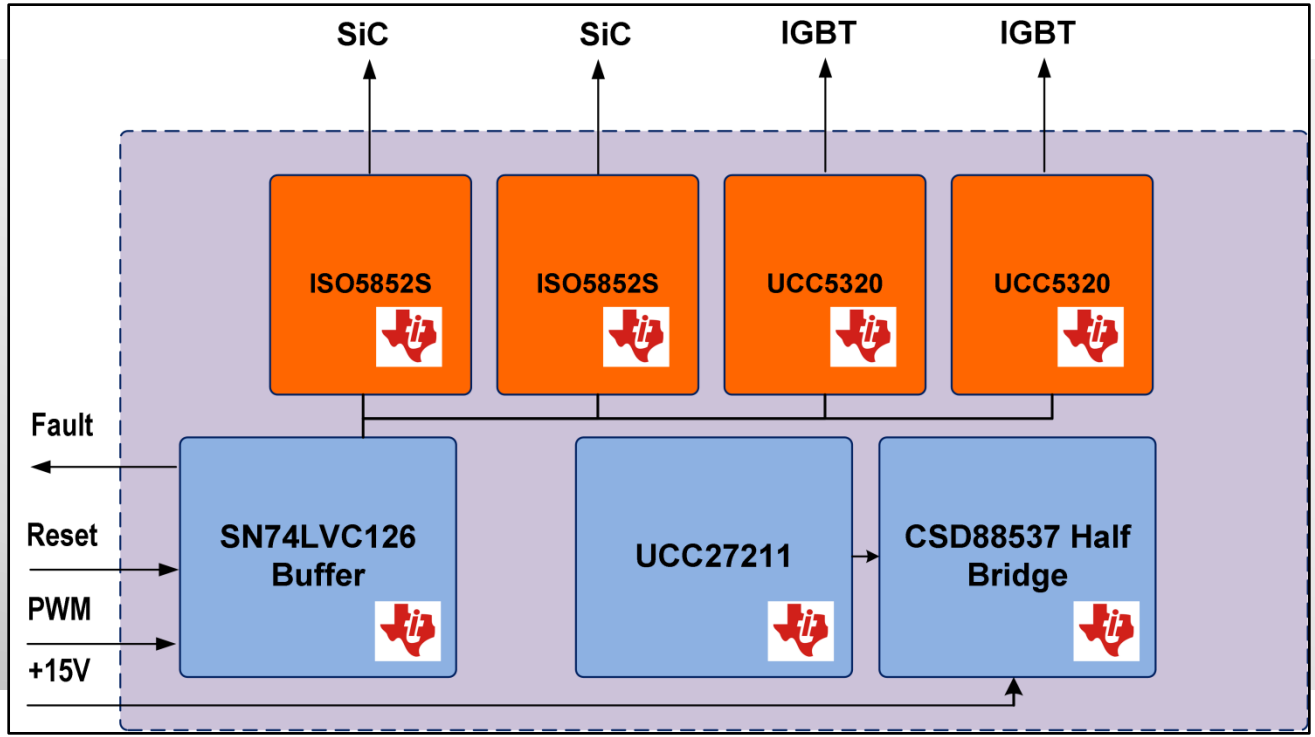


Main System Power Tree

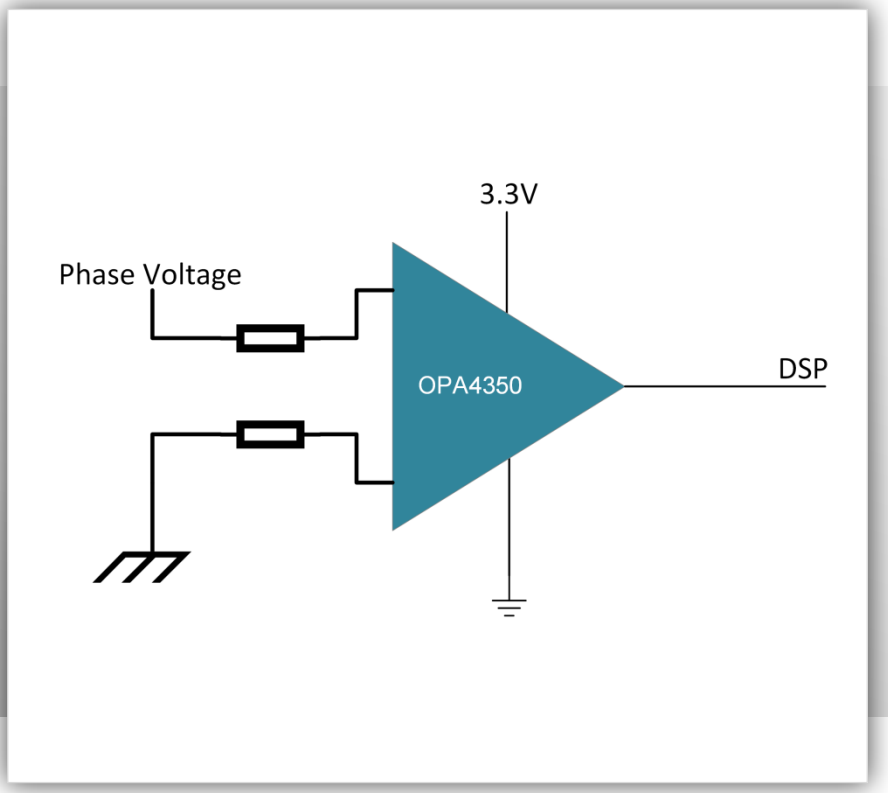


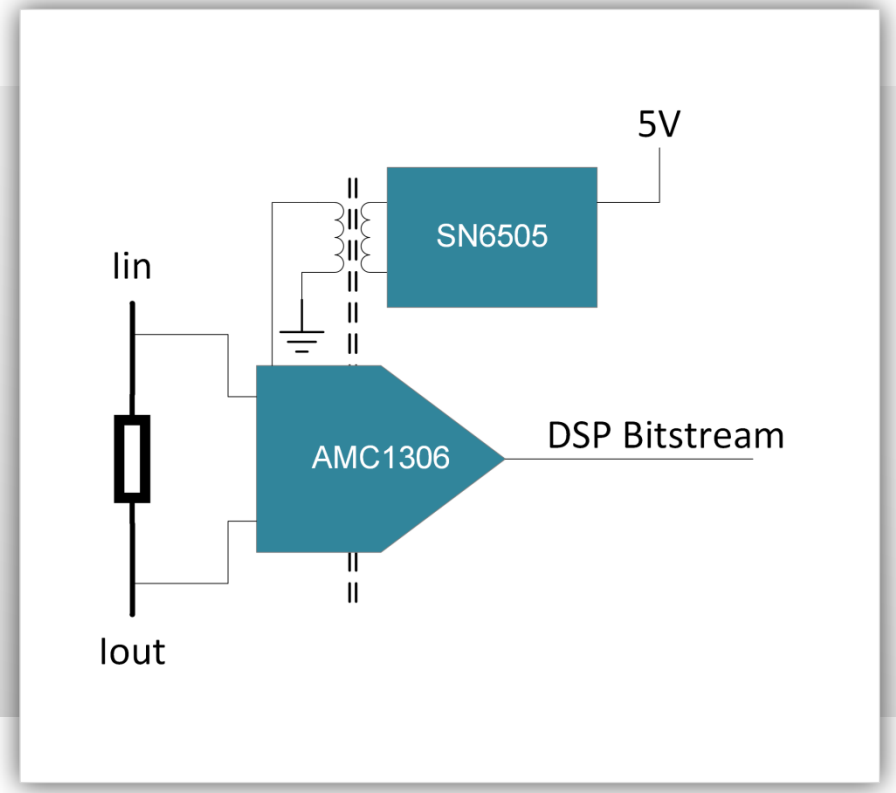
Gate Bias Power Tree

Gate driver detail



Voltage and current sensing





Output filter design

$$L_{inv} = \frac{V_{dc}}{8 \times F_{sw} \times Igrid_{rated} \times \%ripple}$$

$$C_f = \frac{\%x \times Q_{rated}}{2 \times \pi \times F_{grid} \times {V_{grid}}^2}$$

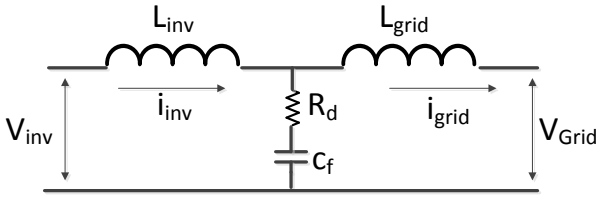
$$\frac{i_{grid}}{i_{inv}} = \frac{1}{\left[r \times \left[1 - L_{inv} \times C_f \times {\omega_{sw}}^2\right]\right] + 1}$$

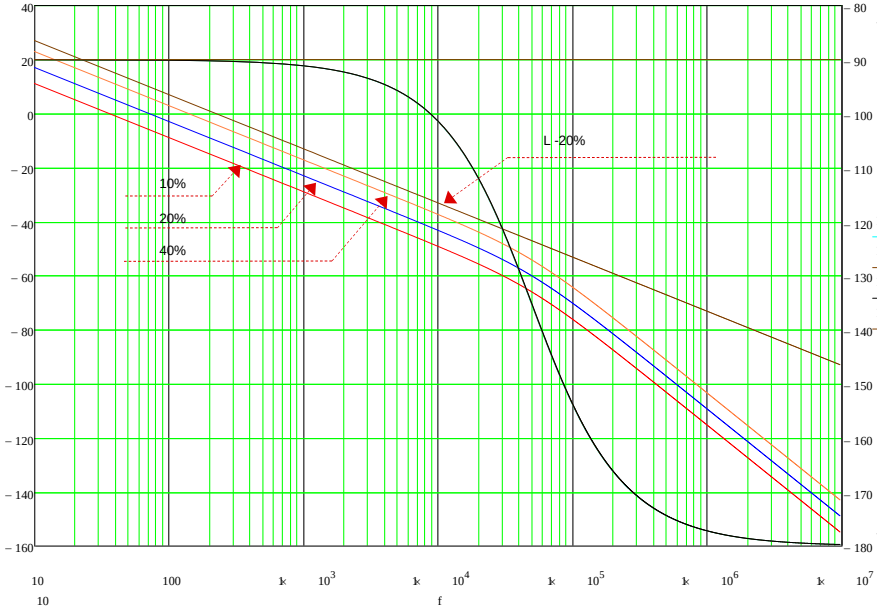
$$L_{grid} = r \times L_{inv}$$

$$R_d = \frac{1}{\left[2 \times \pi \times F_{res} \times C_f\right] \times 3}$$

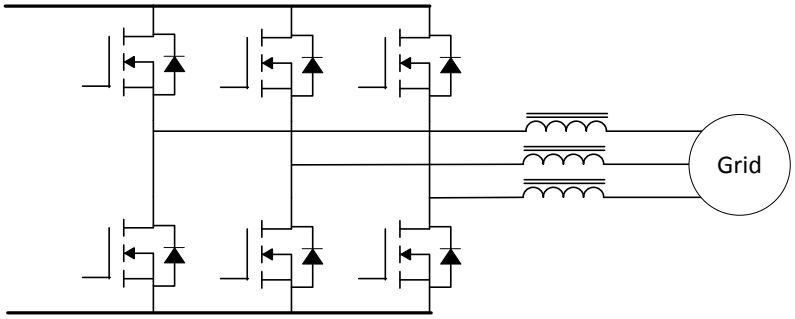
LCL Filter	%ripple		
	10	20	**40**
Linv(µH)	1386	692	**346**
Cf(µF)	9.95	9.95	**9.95**
Lgrid(µH)	9.17	9.18	**9.19**
Filter Gain @ Fsw (dB)	-65.7	-59.8	**-53.9**
Rd	0.319	0.318	**0.316**
Power loss in Rd(W)	0.22	0.387	**1.043**
THD(%)	0.36	0.722	**1.443**

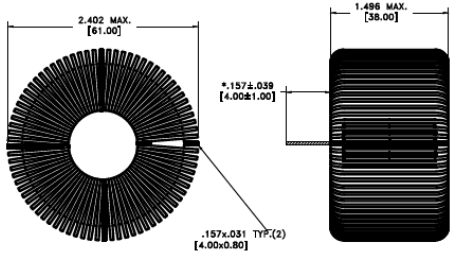
Choose Igrid to Iinv attenuation and calculate ‘r’, chosen 10% for above calculations





50kHz inductor design





- 340uH
- 61mm(d) x 38mm(h)

$$L_{inv} = \frac{V_{DC}}{8 \times f_{sw} \times I_{grid} \times \%_{ripple}}$$

$$L_{inv} = 346uH$$

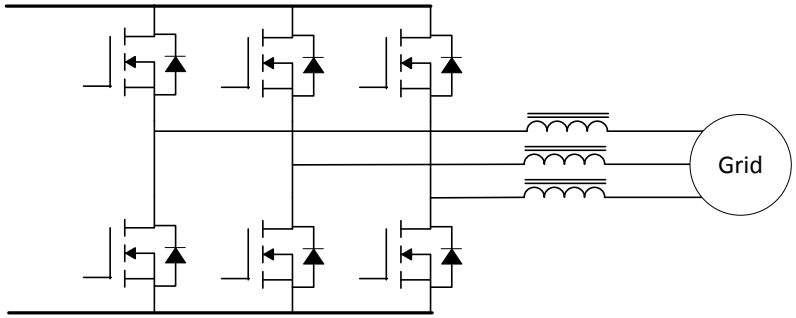
$$R_{AC} = 0.087\Omega$$

$$R_{DC} = 0.024\Omega$$

$$P_{ind\_loss} = 5.64W$$

Rated RMS Current	15A
Peak Current	24A
Core	Kool Mu 26
Windings	84 turns 12AWG Flat

SiC MOSFET loss estimation



More details required

- Eon, Eoff vs Ids at high temperature
- Qrr of diode vs Isd

Specs used for loss estimation

AC Output

$V_{Grid} := 400$

$P_{out} := 10000$

$\%load := 110\%$

$KVA_{out} := 10000 \cdot \%load$

$F_{out} := 50$

$PF_{out} := 1$

$Iout_{max} := 18$

DC Input

$Vin := 600$

$Vin_{min} := 600$

$Vin_{max} := 1000$

Inverter

$F_{sw} := 50000$

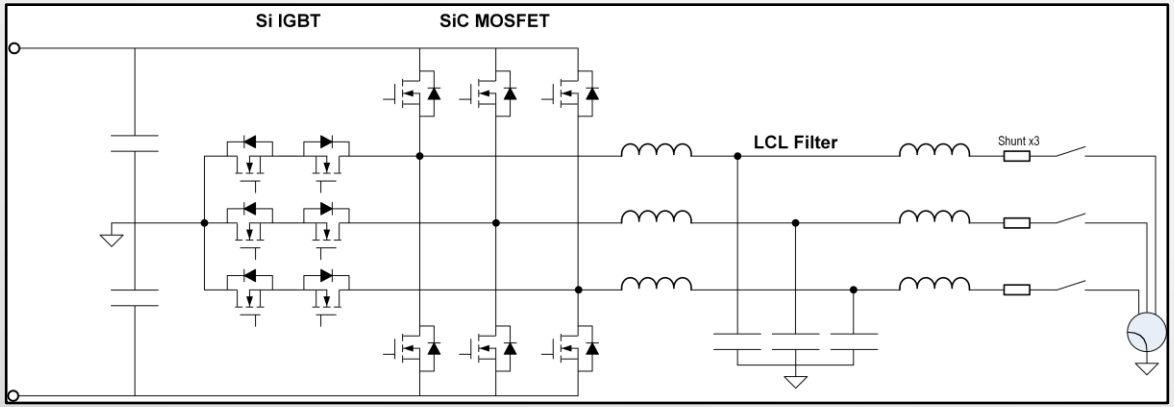
$\%ripple := 10\%$

$Vg_{pos} := 18$

$Vg_{neg} := 5$

Switch	conduction loss	4.095
	Switching Loss	1.536
Diode	Conduction loss	0
	reverse recovery loss	3.21E-03
Total Loss/Switch (W)		5.63W

Total system losses



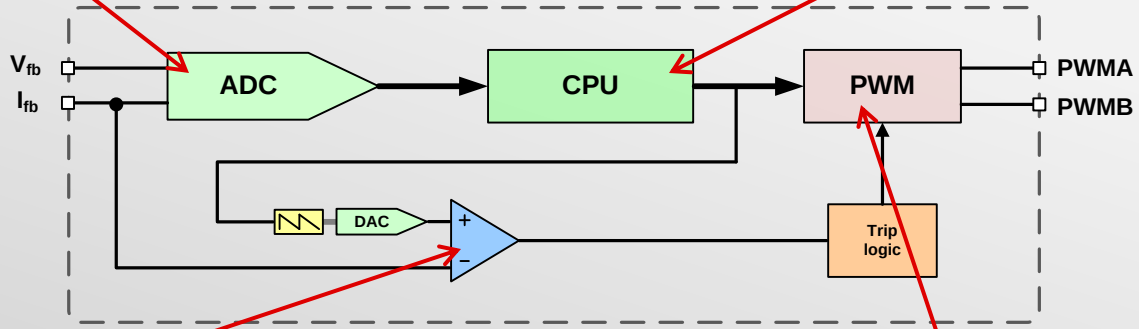
IGBT Loss	SIC Loss	Inductor Loss	Total / Phase	System Total
7.56W	5.63W	5.64W	32.02W	96.06W

Control loop software

Digital power control requirements

1. A high speed ADC which can be synchronized with the switching patterns

2. A high performance CPU for low latency computation of the control law



4. A high speed comparator sub-system to trip PWM outputs on current events

3. A flexible PWM pattern generator

Delfino™ TMS320F2837xD

Features

- **800MIPS** real-time performance of dual C28x core with dual CLA co-processors to run parallel control loops
- 4 differential **16-bit ADC**, 1MSPS each and 3x 12-bit DAC
- **Trigonometric Math Unit (TMU)** - 1 to 3 cycle SIN, COS, ARCTAN instructions
- Direct memory access through dual EMIFs (16bit/32bit)
- **Protection** with 8x Windowed Comparators and X-Bar
- **8 Sigma Delta Decimation Filters** to enable sensing across the isolation boundary

Tools

TMS320F28379D Experimenter's Kit

Part Number: TMDXDOCK28379D

Software

Digital Power SDK & powerSUITE

controlSUITE™ Software

SafeTI

Code Composer Studio (CCS) IDE

TMS320F2837xD

Temperatures	105C	125C	Q100

Sensing

- ADC1: 16-bit, 1.1-MSPS 12-bit, 3.5 MSPS
- ADC2: 16-bit, 1.1-MSPS 12-bit, 3.5 MSPS
- ADC3: 16-bit, 1.1-MSPS 12-bit, 3.5 MSPS
- ADC4: 16-bit, 1.1-MSPS 12-bit, 3.5 MSPS
- 8x Windowed Comparators w/ Integrated 12-bit DAC
- 8x Sigma Delta Interface
- Temperature Sensor
- 3x eQEP
- 6x eCAP

System Modules

- 3x 32-bit CPU Timers
- NMI Watchdog Timer
- 2x 192 Interrupt PIE

Processing

- C28x™ DSP core 200 MHz
- FPU
- TMU
- VCU-II
- CLA DSP core 200 MHz Floating-Point Math
- 6ch DMA

Memory

- Up to 512 KB Flash
- Up to 102 KB SRAM

Processing

- C28x™ DSP core 200 MHz
- FPU
- TMU
- VCU-II
- CLA DSP core 200 MHz Floating-Point Math
- 6ch DMA

Memory

- Up to 512 KB Flash
- Up to 102 KB SRAM

- 2x 128-bit Security Zones
- Boot ROM
- 2x EMIF

Actuation

- 12x ePWM Modules (Type 4) 24x Outputs (16x High-Res)
- Fault Trip Zones
- 3x 12-bit DAC

Connectivity

- 4x UART
- 2x I2C (w/ true PMBus)
- 3x SPI
- 2x McBSP
- 2x CAN 2.0
- USB 2.0 OTG FS MAC & PHY
- uPP

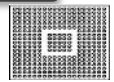
Power & Clocking

- 2x 10 MHz OSC
- Ext OSC Input

Debug

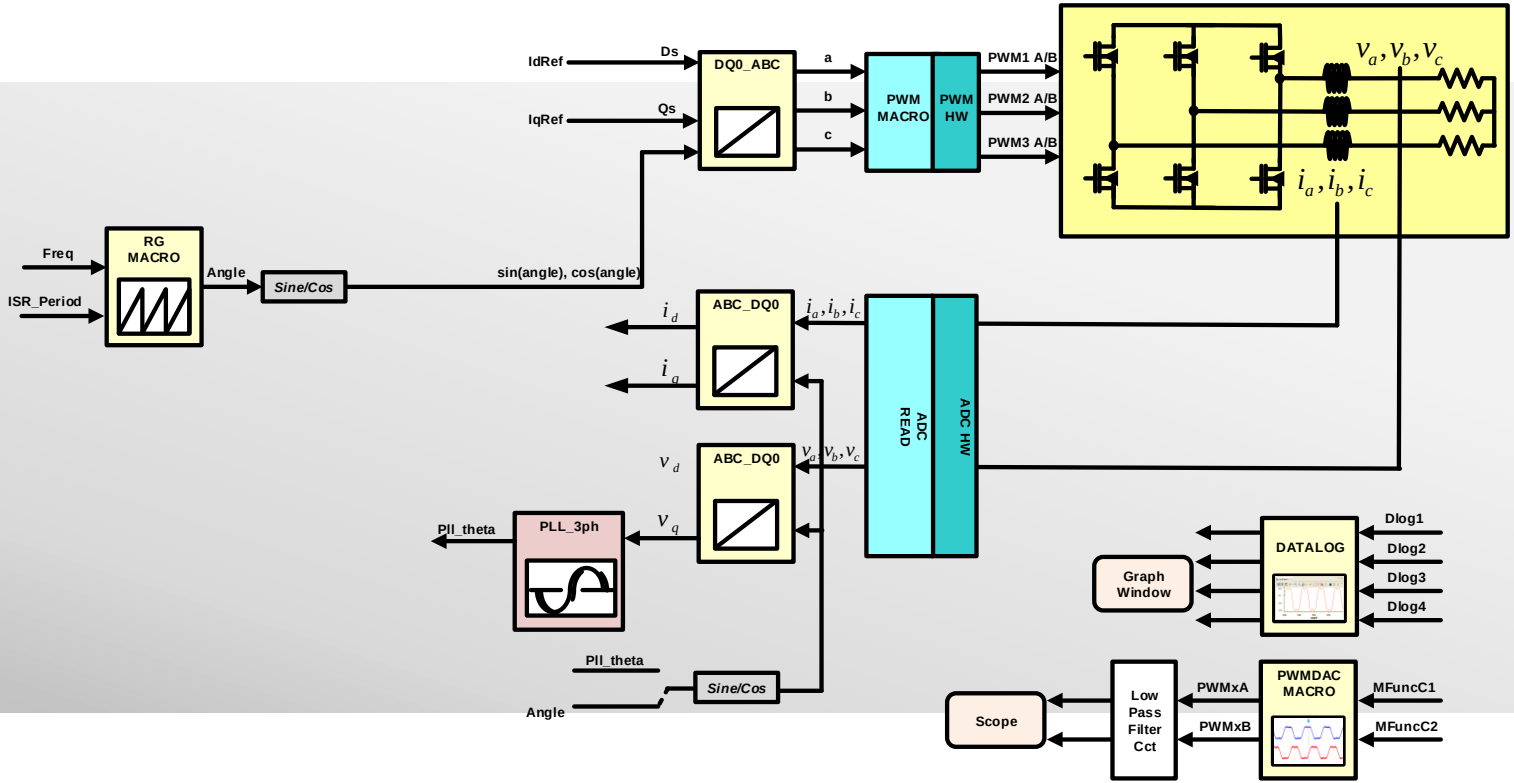
- Real-time JTAG

Packages

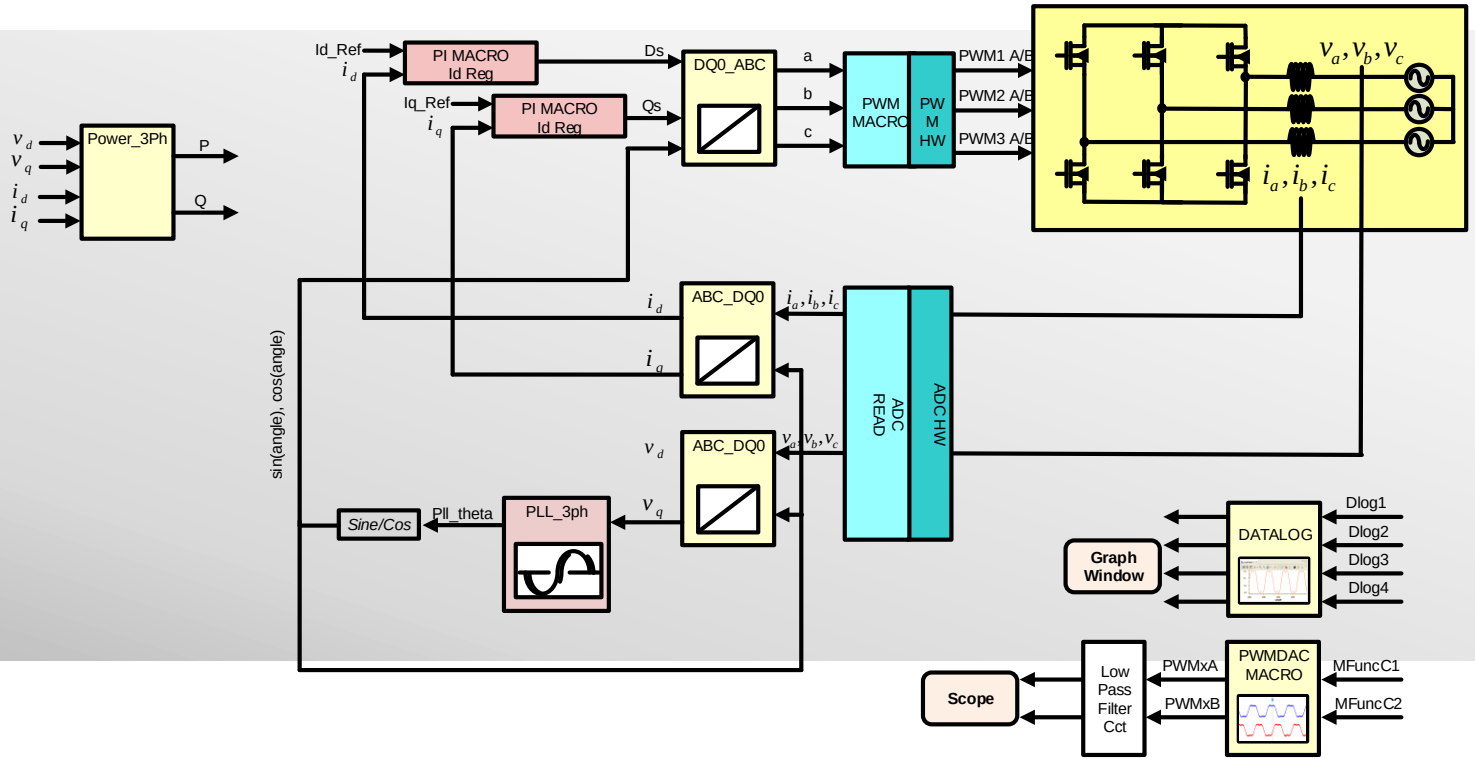


Package	Dimension
176-pin HLQFP	24x24mm²
337-pin NFBGA	16x16mm²

Open loop control software



Grid connected control software



TI control loop features

Includes

- All filter blocks tested
- Feedback sensing validated
- Hardware control validation
- Basic grid connected current feedback control loop

Left to the Customer

- P&Q Control
- DC Bus Regulation
- Unbalanced Load Control
- Anti-Islanding
- Additional Safety Features

TIDA-01606 overview

TIDA-01606

10kW 3-Phase 3-Level Grid Tie inverter reference design for solar string inverter

Design Features

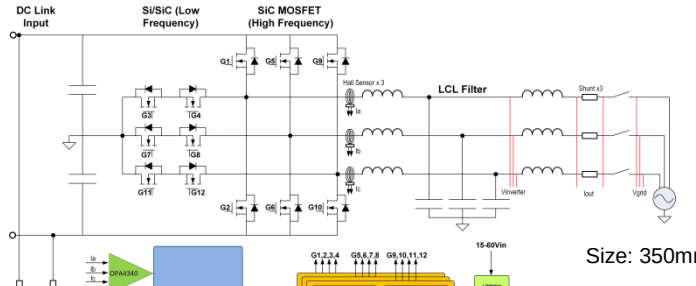
- 10kW 3-Phase 3-Level inverter using SiC MOSFETs
- System Specifications:
  - Input : 800V/1000V
  - Output : 400VAC 50/60 Hz
  - Power : 10KW/10KVA
  - Efficiency : > 99% peak efficiency
  - PWM frequency : 50kHz
- Uses ISO5852, UCC5320 gate driver & C2000 MCU controller
- Uses Littelfuse LSIC1MO120E0080 1200V 80mOhms SiC MOSFETS
- Reduces output filter size by switching inverter at 50KHz
- Isolated current sensing using AMC1306 for load current monitoring
- Differential voltage sensing using OPA4350 for load voltage monitoring
- Targets less than 2% output current THD at full load

Tools & Resources

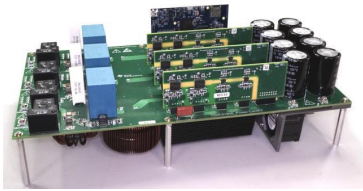
- **TIDA-01606 Tools Folder**
- **Test Data/Design Guide**
- **Design Files:** Schematics, BOM and BOM Analysis, Design Files
- **Key TI Devices:** UCC5320, ISO5852, AMC1306, SN6505, TMS320F28379D, OPA4350, OPA350, LM76003, PTH08080WAZT, UCC27211

Design Benefits

- 3-Level T-type inverter topology for reduced ground current in transformer-less grid-tie inverter applications
- Reduced size at higher efficiency using low Rdson SiC MosFET and higher switching frequency (50kHz) at higher power (10kW)
- Platform for testing both 2-level and 3-level inverter by enabling or disabling middle devices through digital control.



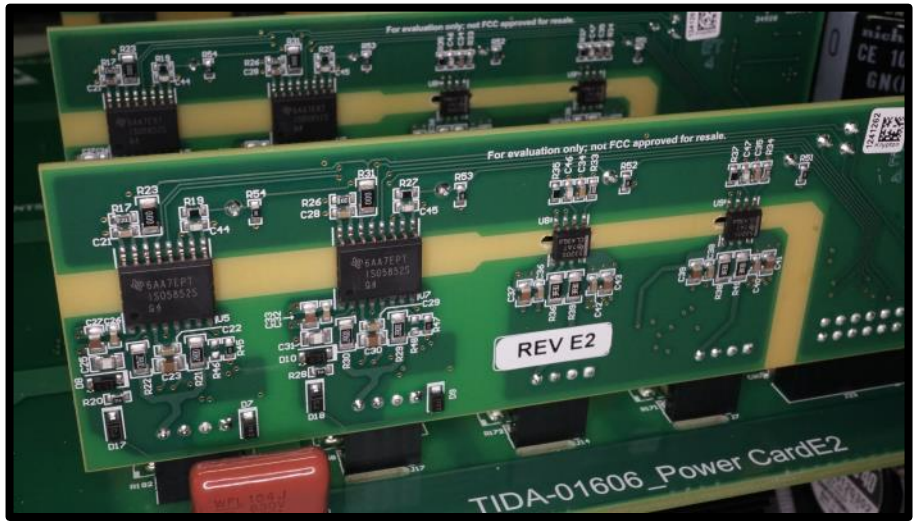
Size: 350mm X 200mm X 100mm



Key TI parts

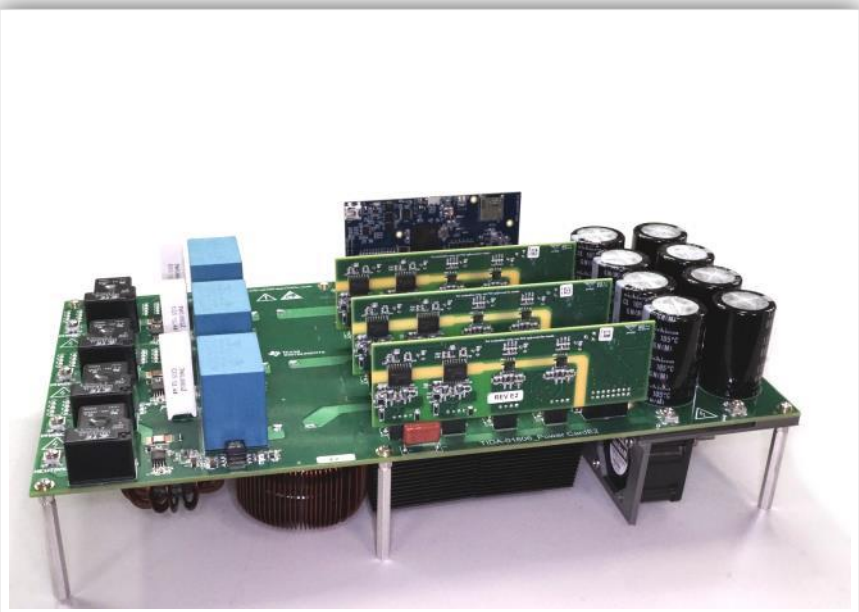
TI Part Number	Device Description	Why did we pick this device?
ISO5852S	5A/5A, 5.7Vrms Isolated Single Channel Gate Driver	High current source/sink with bipolar supply voltage best fit for driving SiC Mosfet.
TMDSCNCD28379D	Dual-Core Delfino Microcontroller	Standard 180pin form factor control card with C2000 controller provides enough bandwidth for complete digital control of 3phase inverter.
AMC1306M05	Precision, ±50mV Input, 3µs Delay, Reinforced Isolated Amplifier	Replaces bulky low frequency CT with shunt for measuring 50/60Hz current.
OPA4350	High-Speed, Single-Supply, Rail-to-Rail Operational Amplifiers	Low noise with high slew rate ideally suited for high frequency input signal conditioning.

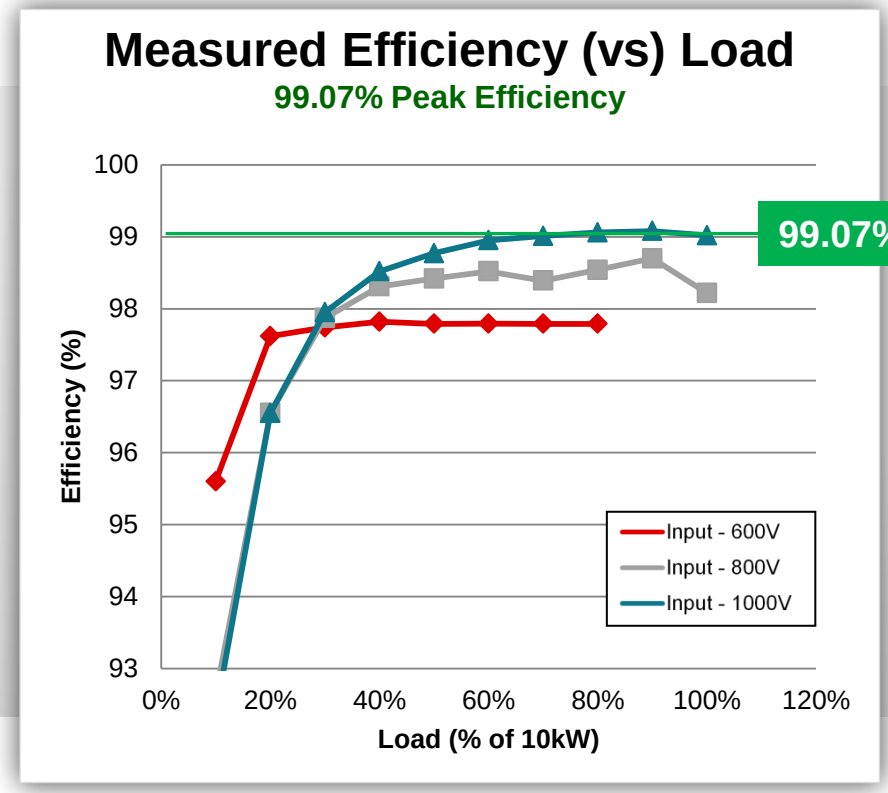
Key hardware



Total Size: **350mmx 200mm x 100mm**

Testing results





Summary

- **99.07%** Peak Efficiency at **8kW**
- **99.02%** Efficiency at **10kW**
- **1.4kW/l**

Measured Results Summary

SYSTEM PARAMETER	VALUE
Input Voltage	600-1000Vdc
Output Voltage	400VAC 50/60Hz
Maximum Power	10kW
PWM Frequency	50kHz
Efficiency (Peak)	**99.07% @ 8kW**
Efficiency (Full Load)	**99.02% @ 10kW**
Size	**350mm x 200mm x 100mm**