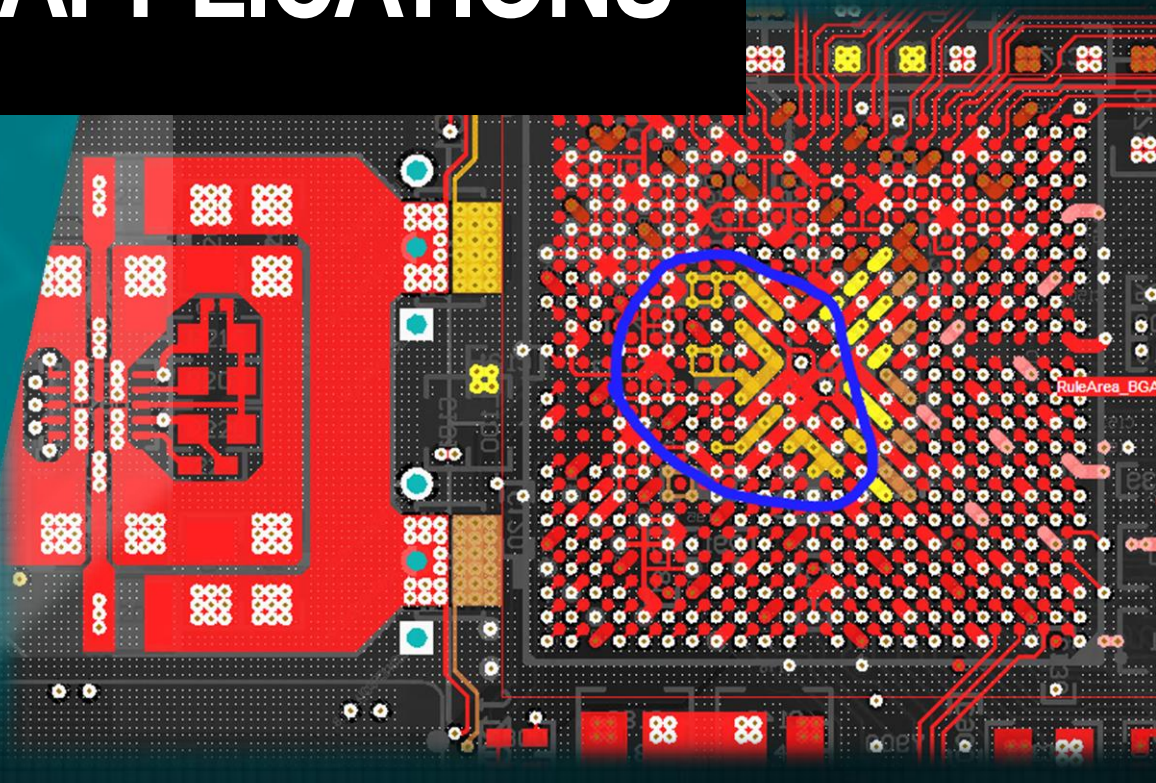
POWER DISTRIBUTION FOR SOC AND FPGA APPLICATIONS

WHAT SPECS TO LOOK FOR

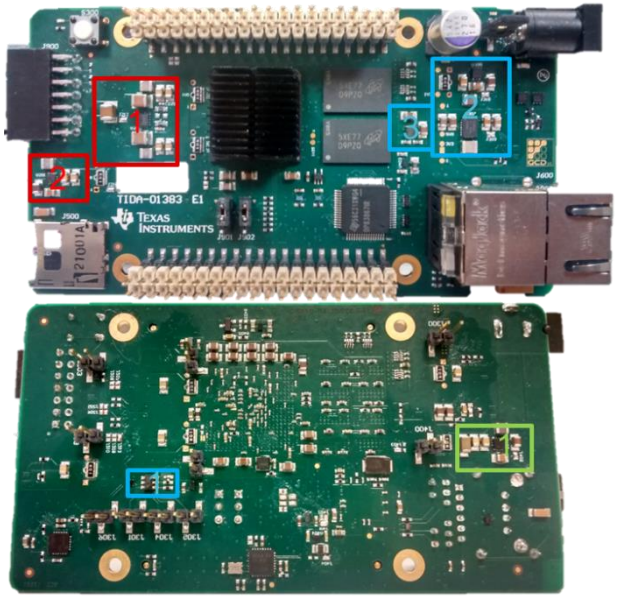


Detailed Agenda

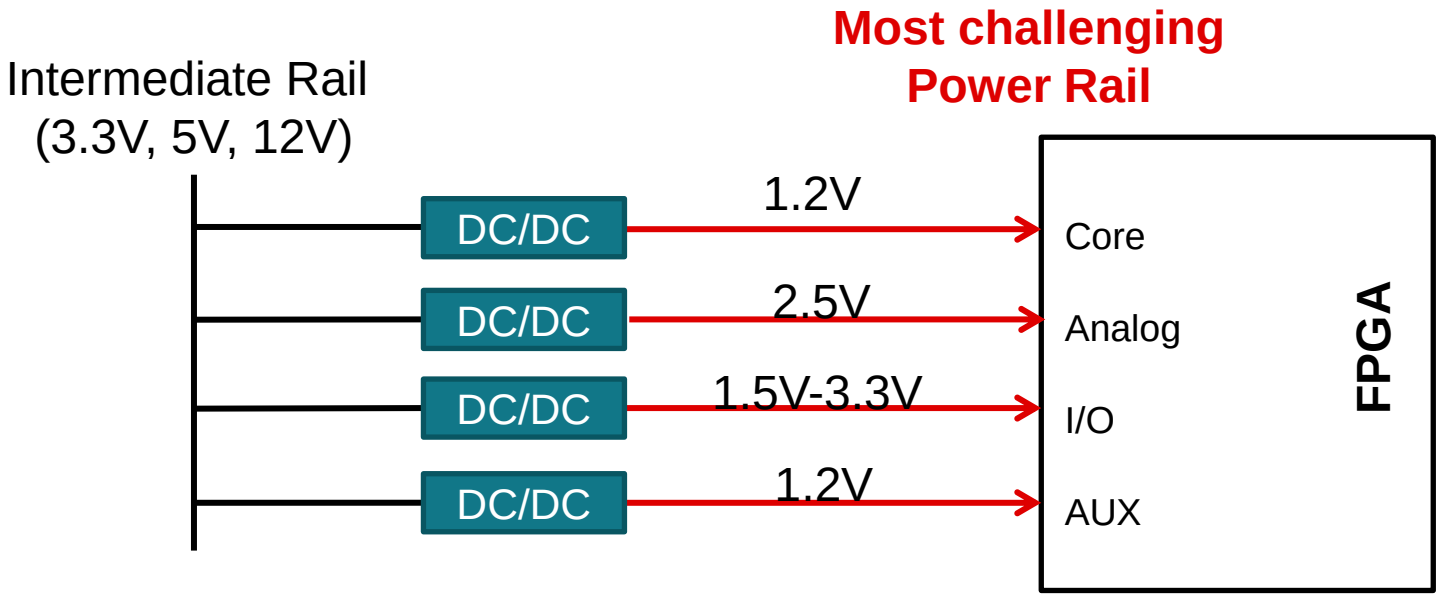
Power Distribution for SoC and FPGA applications:

Microprocessors and Programmable Logic require several voltage supply rails, often with tight regulation accuracy and sequencing requirements. It's of key importance to identify the specs of those rails and their challenges, in order to address them with the right power devices.

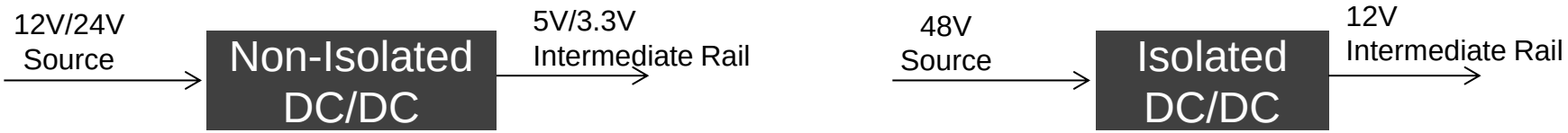
- SoCs power requirements
  - System overview
  - Typical SoC's and FPGA specs
  - Electrical specifications: DC and AC accuracy
  - Devices performances comparison example



Typical SoC Supply Rails



Typical System Architectures



Intermediate Rail	Advantage	Disadvantage
12V	Lower input current	Lower efficiency conversion to POL Possible duty cycle limitation
5V	Higher efficiency conversion to POL	Higher input current compared to 12V
3.3V	Higher efficiency conversion to POL	Highest input current Fewer available parts (min Vin range)

CPU+FPGA SoC Typical Power Specs

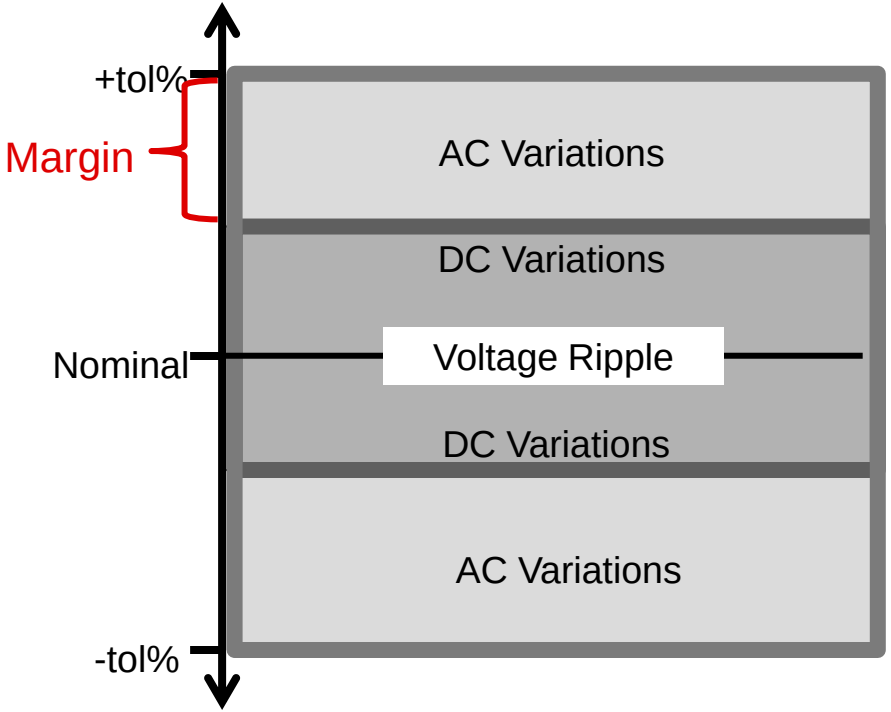
- Example:Xilinx Zynq XC7Z020
  - CPU max frequency 766 MHz
  - Artix-7 FPGA
  - 220 Programmable DSP slices
  - DSP Performance: 276 GMACs
- Current consumption is based on Xilinx Power Estimator (XPE) under these conditions:
  - F=400MHz
  - Logic enabled 100%
  - **Logic toggled 25%**
- Regulation Accuracy is Critical!

PIN	Description	Voltage (V)	Current (A)	Sequencing
VCCINT	PL core	1 ±5%	4.7	1
VCCPINT	APU core	1 ±5%	0.2	
VCCBRAM	PL block RAM/FIFO	1 ±5%	0.05	
VCCAUX, VCCBATT	PL auxiliaries	1.8 ±5%	0.5	2
VCCPLL	APU PLL	1.8 ±5%	0.01	
VCCPAUX	APU auxiliaries	1.8 ±5%	0.010	
VCCO1	PL HR IOs (2+2 banks)	1.8	0.2	3
VCCO2		3.3	0.2	
VCCO_DDR	APU Internal DDR	1.35	0.01	

Output Voltage Accuracy

Power supply performance is considered under two operating conditions:

- **Static:** Fixed/gradual changes (DC)
- **Dynamic:** Quick changes (AC)

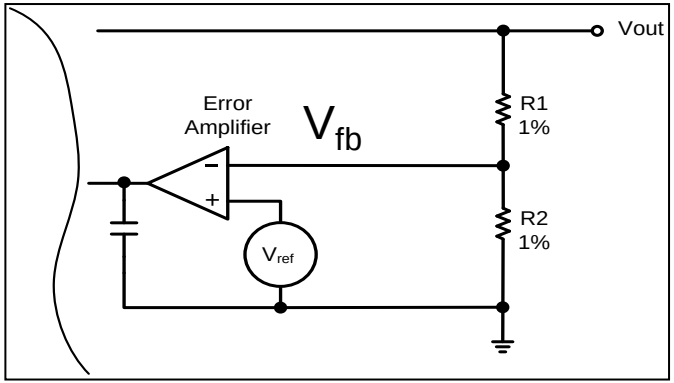


See also: http://www.powerelectronics.com/regulators/optimal-transient-response-processor-based-systems

Static: Output voltage accuracy (DC)

Influencing Parameters:

- Reference voltage Vref accuracy
- Feedback divider resistors tolerances
- Load and line regulation due to Error's Amplifier finite gain.



V_{OUT}	Load regulation	V_{OUT} = 3.3 V PWM mode operation	0.05 %	/ A
V_{OUT}	Line regulation	3V ≤ V_{IN} ≤ 17 V, V_{OUT}= 3.3 V, I_{OUT} = 1000 mA PWM mode operation	0.02 %	/ V

- Non ideal Vout sensing and PCB traces effects (uncompensated DC losses)

Static: Examples for a 1.8V output

Based on: http://www.ti.com/lit/an/slva423/slva423.pdf

$$\Delta V_{out}/V_{out} \cong \pm 2T_R\left(1 - \frac{V_{ref}}{V_{out}}\right) + T_{V_{ref}}$$

T_R = Tolerance of Resistors in %
T_{Vref} = Tolerance of Reference Voltage in %
V_{ref} = Reference Voltage of IC
V_{out} = Set output voltage

	Example 1	Example 2	Example 3	Example 4
T_R	**1%**	0.1%	1%	**0.1%**
T_{Vref}	**2%**	2%	2%	**1%**
V_{ref}	0.8V	0.8V	0.7V	0.8V
V_{out}	1.8V	1.8V	1.2V	1.8V
Error	**3.1%**	2.1%	2.83%	**1.1%**

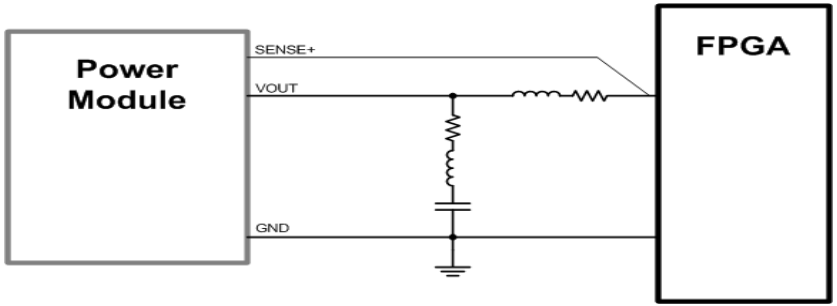
Highest Margin for load regulation and AC tolerance

The line and load regulation need to be added on top!

Static: Minimizing DC Loss

DC loss is the voltage drop due to non ideal sensing. This issue can be reduced by means of:

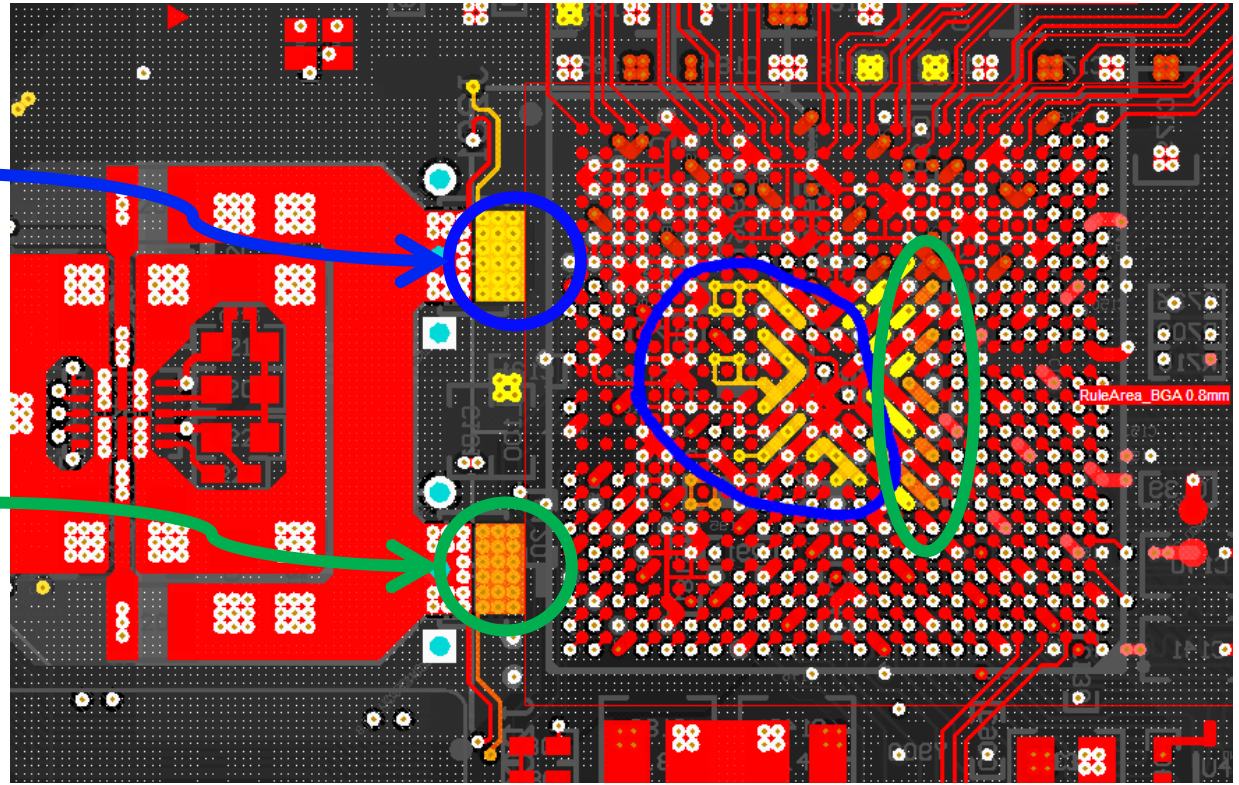
- **Remote Sense**
  - R1 is connected as close as possible to the FPGA core supply pin (note: FPGAs have usually more than one core supply pin and they are often found in BGA packaging formats)



- **Wide/thick copper traces**
  - reduced output resistance
- **Place power supply close to FPGA supply input**
  - shorter traces reduce resistance, as well as inductive loops.

Static: Minimizing DC Loss
Example: TPS62480 layout with Xilinx Zynq XC7Z020

- **More than one pin** for the FPGA supply VCCINT (yellow traces circled in blue)… …**which pin should we sense?**
- Placing the TPS62480 close to FPGA and using wider traces minimizes DC losses.
- Here TPS62480 is used also for the **DualCore CPU supply (VCCPINT)**.



Calculation Example for Core supply : Static

TPS62135 for Altera MAX 10 FPGA

Rail Requirement	
Intermediate rail	**12 V**
Core Voltage	1.2V
Tolerance	5%
Max current	4A

TPS62480 for Xilinx Zynq XC7Z020

Rail Requirement	
Intermediate rail	**5V**
Core Voltage	1V
Tolerance	5%
Max current	6A

Calculation Example for Core supply : Static

TPS62135 Datasheet	Target Vout=1.2V
Vref	0.7V
Tolerance Vref	1%
Tolerance resistors	0.1%
Load regulation	0.05 %/A

TPS62480 Datasheet	Target Vout=1V
Vref	0.6V
Tolerance Vref	1%
Tolerance resistors	0.1%
Load regulation	0.02%/A

$$\Delta V_{out}/V_{out} \cong \pm 2T_R\left(1-\frac{V_{ref}}{V_{out}}\right) + T_{V_{ref}} + Load\ regulation$$

Contributes	
Tolerances	1.08%
Load regulation @4A	0.2%
Total	**1.28%**

3.7% (and plus) AC margin!!!

Contributes	
Tolerances	1.08%
Load regulation @6A	0.12%
Total	**1.20%**

Output Voltage Accuracy

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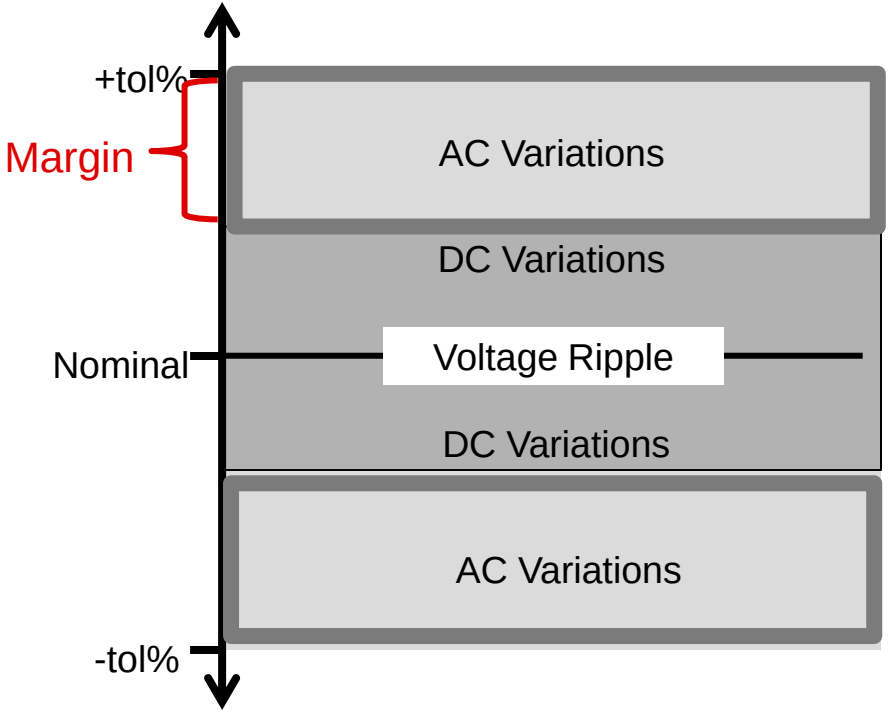
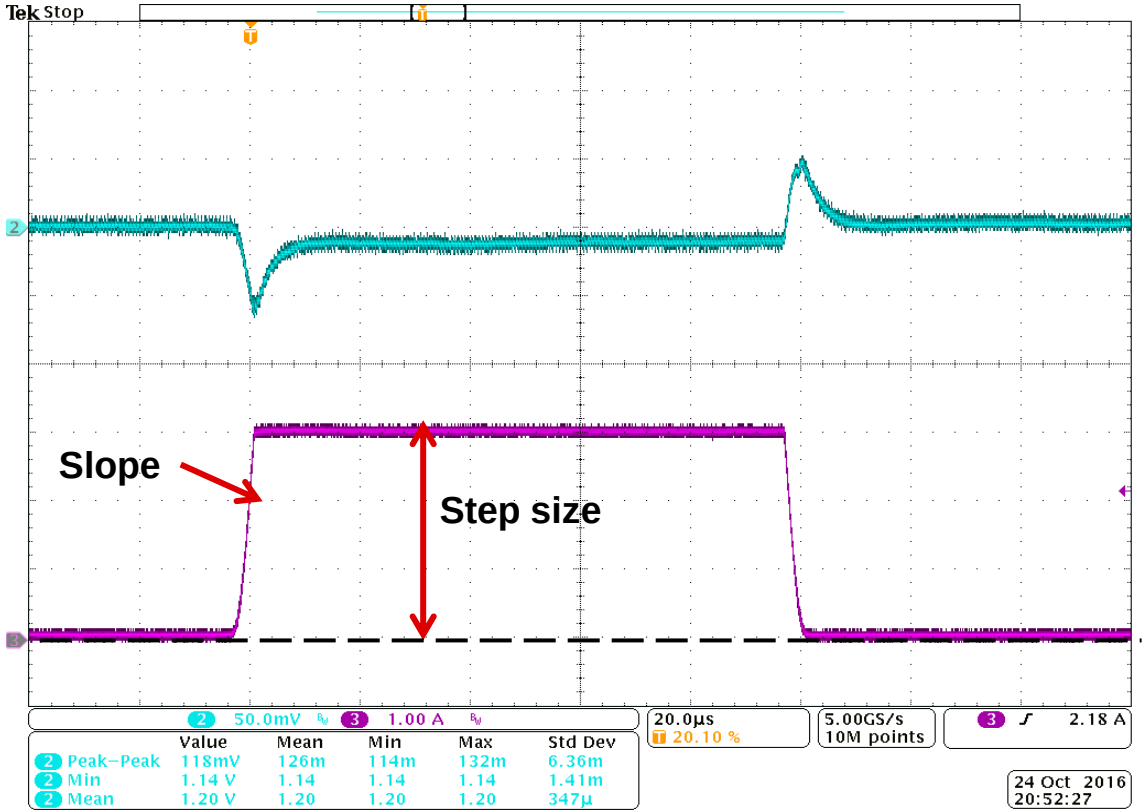


See also: http://www.powerelectronics.com/regulators/optimal-transient-response-processor-based-systems

Dynamic: Output voltage accuracy (AC)

Load Transient response

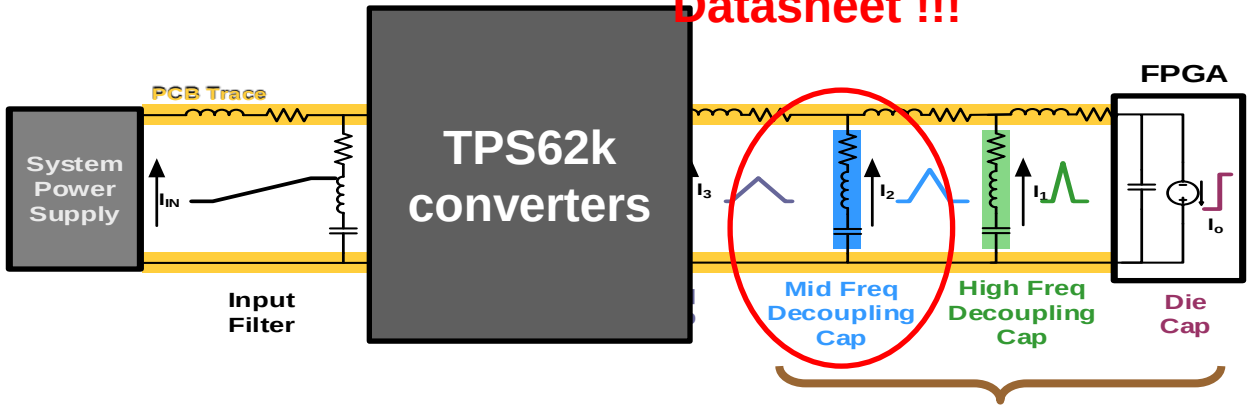
- **Influencing Parameters:**
  - Slope (A/us)
  - Step size (A)
  - Control Topology
    - Voltage Mode
    - Current Mode
    - Hysteretic
    - DCS-Control
  - Output Filter



Dynamic: Output Capacitor Network

- No external compensation needed, enables faster design cycles
- Optimized internal compensation minimizes transient response
- Only input/output capacitors must be selected, according to Datasheet's guidelines

Suggested on Datasheet !!!

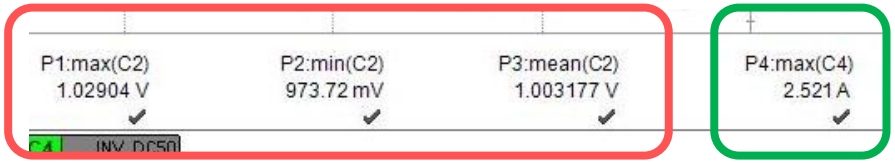


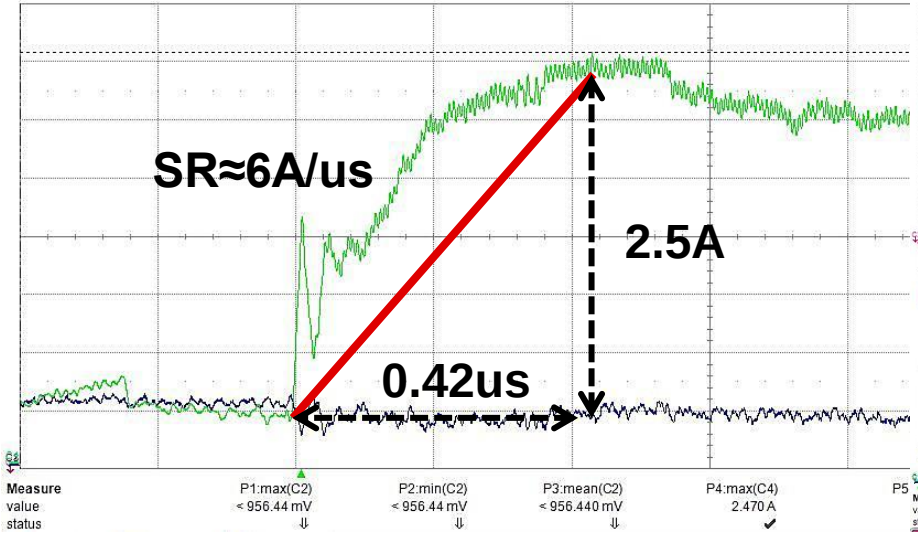
High Bandwidth converter **eliminates the need of low freq. bulk cap**

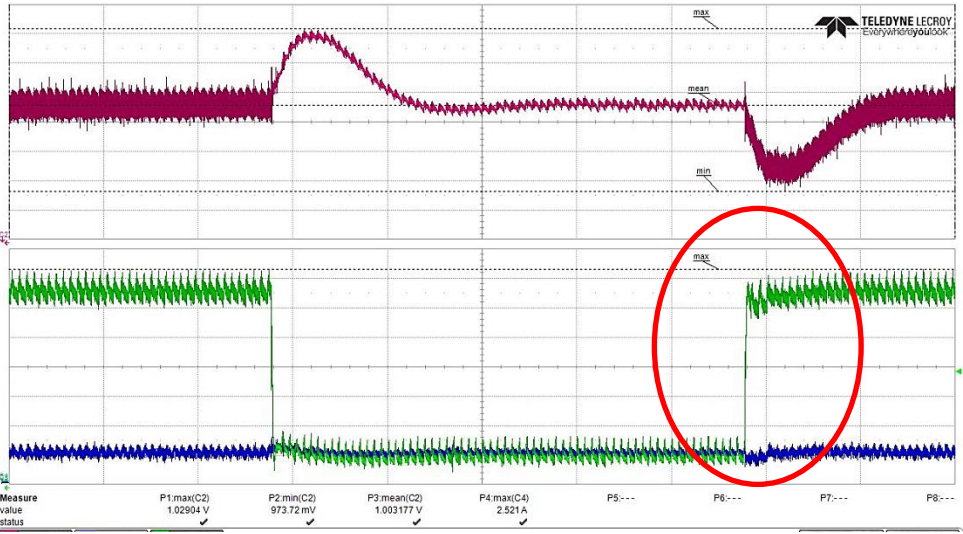
Complete and **effective decoupling network**
Ceramic X5R and X7R dielectrics are great choices

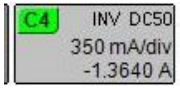
Dynamic: TPS62480 on Xilinx Zynq® 7000

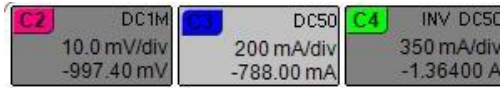
Less than 30 mV over/undershoot on the VCCINT pins!!!

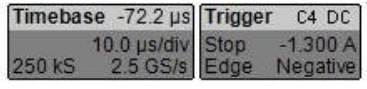






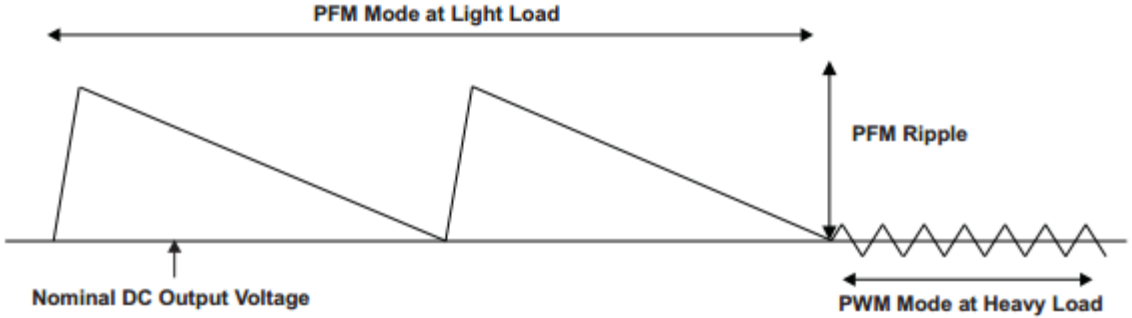






Why is PWM mode operation crucial for FPGAs ?

For ensuring good DC Accuracy at all load conditions, **PWM mode must be forced.**



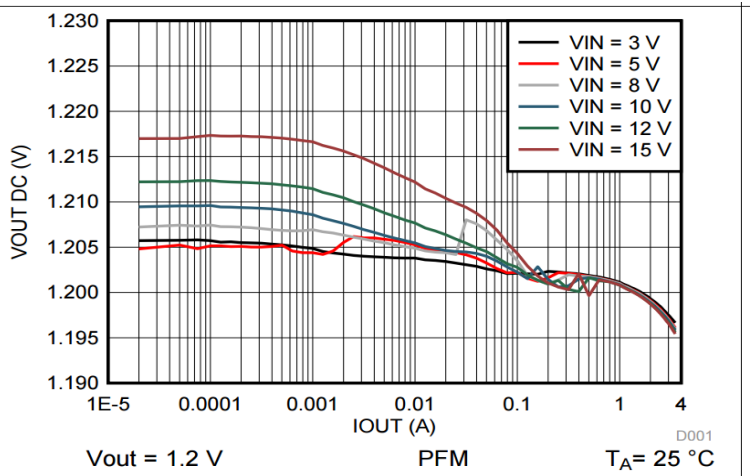


Figure 16. Output Voltage vs Output Current

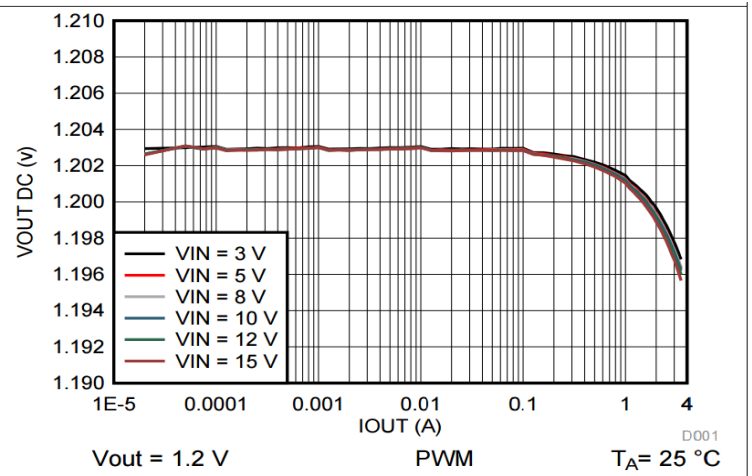
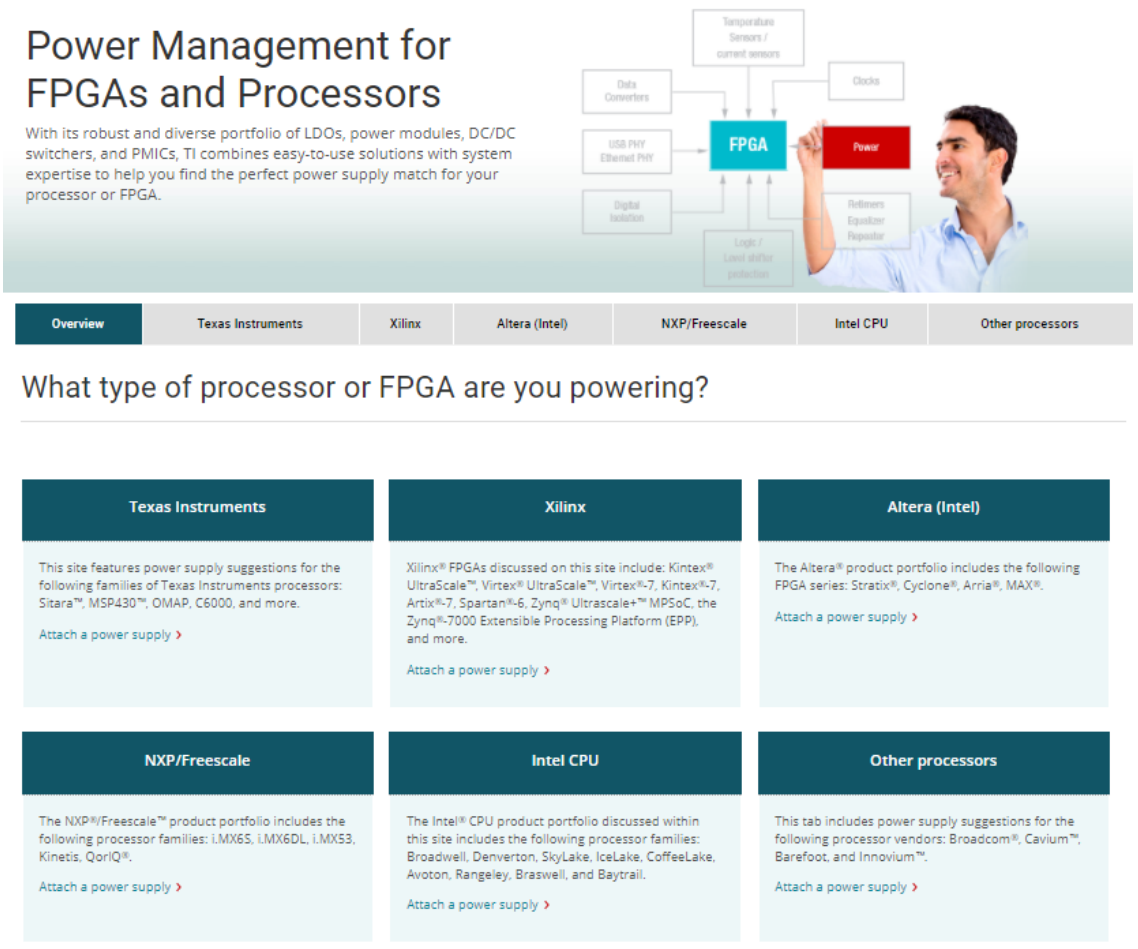


Figure 17. Output Voltage vs Output Current

FPGA support webpage

www.ti.com/powerfpga
(*best use with Chrome*)

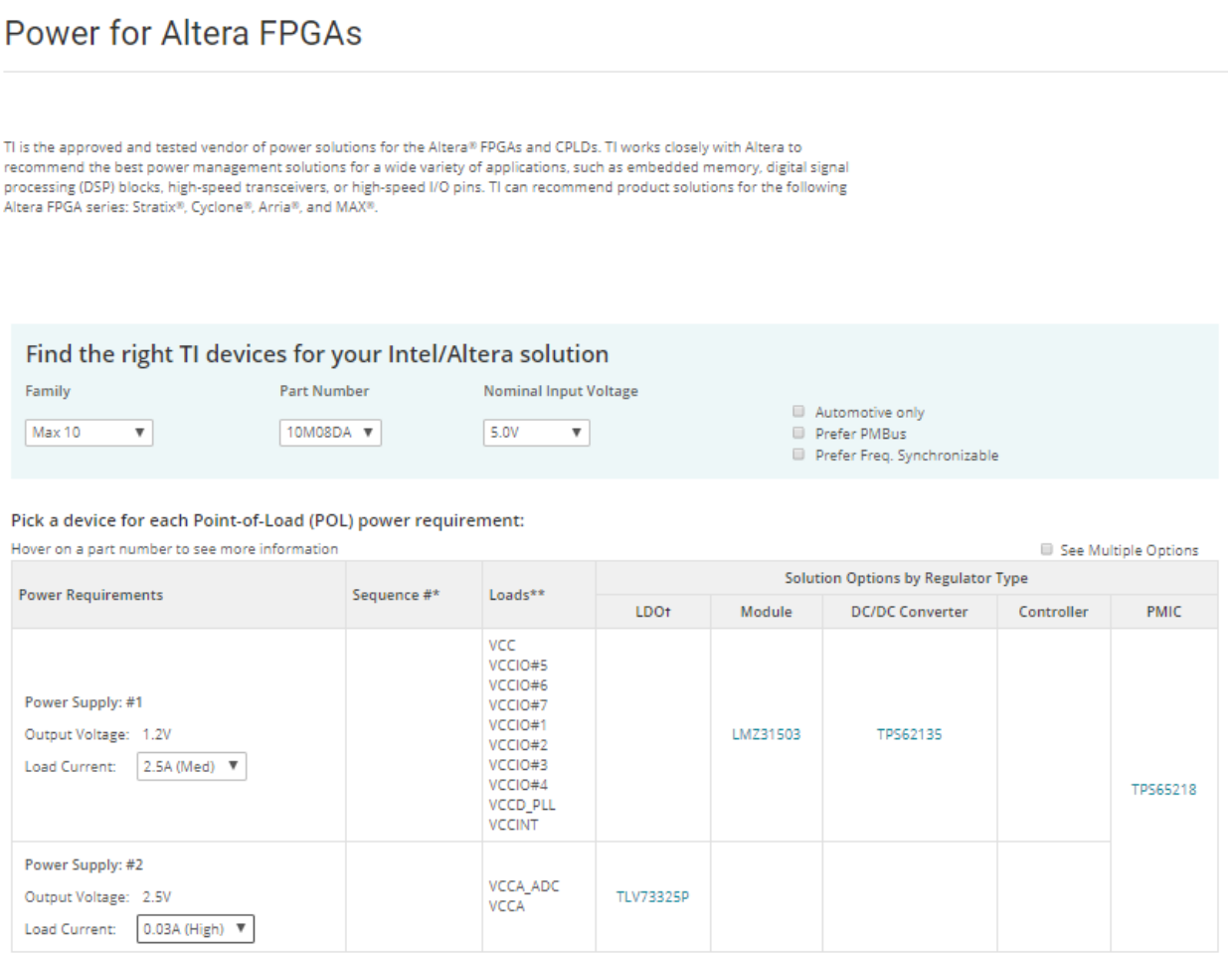
- **Complete solutions** for a large variety of **MicroProcessors and MicroControllers**



FPGA support webpage

www.ti.com/powerfpga
(*best use with Chrome*)

- **PMIC and Discrete** solution for each Power Rail
- **Adaptive** according to different application specs (System's Input Voltage and Rail's Load Current)



Power for Altera FPGAs

TI is the approved and tested vendor of power solutions for the Altera® FPGAs and CPLDs. TI works closely with Altera to recommend the best power management solutions for a wide variety of applications, such as embedded memory, digital signal processing (DSP) blocks, high-speed transceivers, or high-speed I/O pins. TI can recommend product solutions for the following Altera FPGA series: Stratix®, Cyclone®, Arria®, and MAX®.

Find the right TI devices for your Intel/Altera solution

Family: Max 10 | Part Number: 10M08DA | Nominal Input Voltage: 5.0V

- Automotive only
- Prefer PMBus
- Prefer Freq. Synchronizable

Pick a device for each Point-of-Load (POL) power requirement:

Hover on a part number to see more information

See Multiple Options

Power Requirements	Sequence #*	Loads**	Solution Options by Regulator Type				
			LDO†	Module	DC/DC Converter	Controller	PMIC
Power Supply: #1 Output Voltage: 1.2V Load Current: 2.5A (Med)		VCC VCCIO#5 VCCIO#6 VCCIO#7 VCCIO#1 VCCIO#2 VCCIO#3 VCCIO#4 VCCD_PLL VCCINT		LMZ31503	TPS62135		TPS65218
Power Supply: #2 Output Voltage: 2.5V Load Current: 0.03A (High)		VCCA_ADC VCCA	TLV73325P