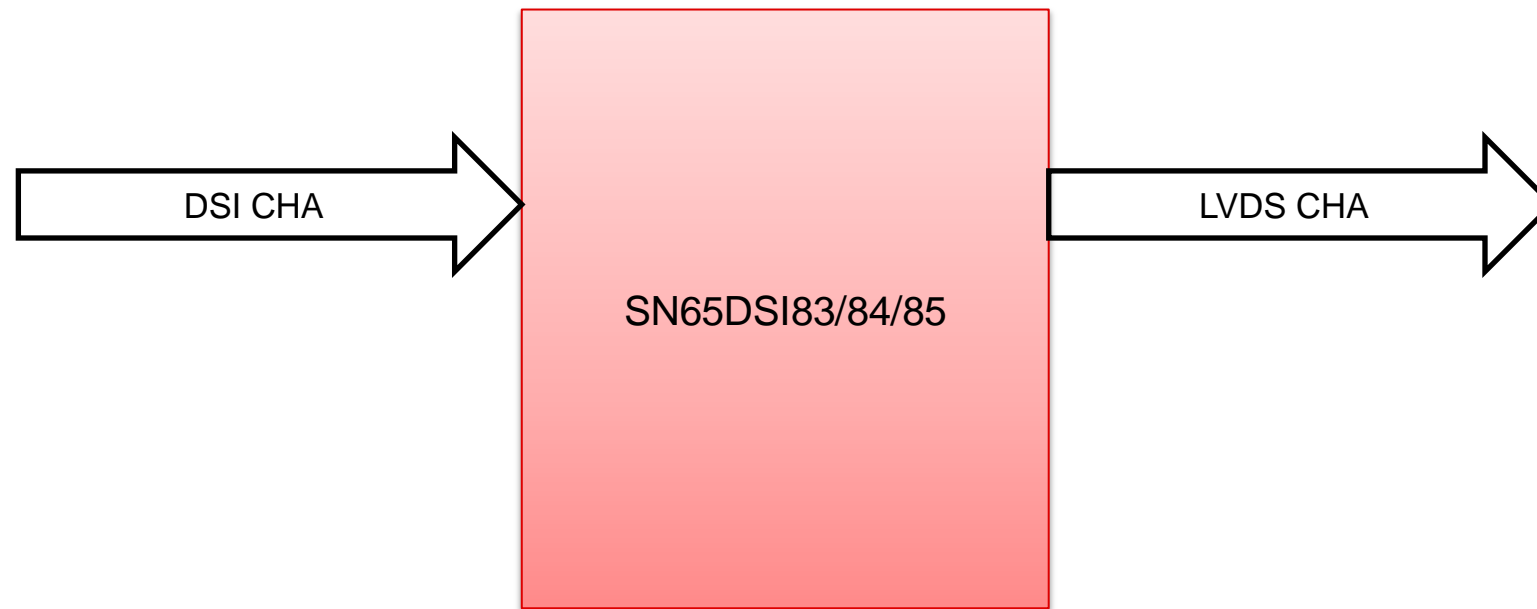


SN65DSI83/84/85- Single DSI Input to Single-Link LVDS

Ikechukwu (I.K.) Anyiam

Single to single

- The SN65DSI83, DSI84, and DSI85 can all be used for single channel DSI to single channel LVDS, but we will use the SN65DSI83 for this demo



Single to single

- From display datasheet, identify:
- Resolution:

<i>Display area</i>	210.432 (H) × 157.824 (V) mm
<i>Diagonal size of display</i>	26cm (10.4 inches)
<i>Drive system</i>	a-Si TFT active matrix
<i>Display color</i>	16,777,216 colors (At 8-bit input, FRC terminal= High) 262,144 colors (At 6-bit input, FRC terminal= Low or Open)
<i>Pixel</i>	1,024 (H) × 768 (V) pixels
<i>Pixel arrangement</i>	RGB (Red dot, Green dot, Blue dot) vertical stripe

- This is a 1024 x 768 panel

Single to single

- Fill out corresponding section in tool:

DSI83/84/85/86 Tuner - SN65DSI83

Panel Inputs DSI_Inputs Outputs

Panel Info

Channel A

Panel Vendor

Panel Model

Resolution 1024 pixels x 768 lines

LVDS Mode Single

Test Pattern

Pixels

	LVDS Channel A	LVDS Channel B
LVDS_HPW	<input type="text"/>	<input type="text"/>
LVDS_HBP	<input type="text"/>	<input type="text"/>
LVDS_HFP	<input type="text"/>	<input type="text"/>
LVDS_HActive	1024	<input type="text"/>
Htotal	1024	0

Lines

	LVDS Channel A
LVDS_VPW	<input type="text"/>
LVDS_VBP	<input type="text"/>
LVDS_VFP	<input type="text"/>
LVDS_VActive	768
Vtotal	768

Additional Panel Info

Channel A

FORMAT Format 1

Data Enable Polarity Positive

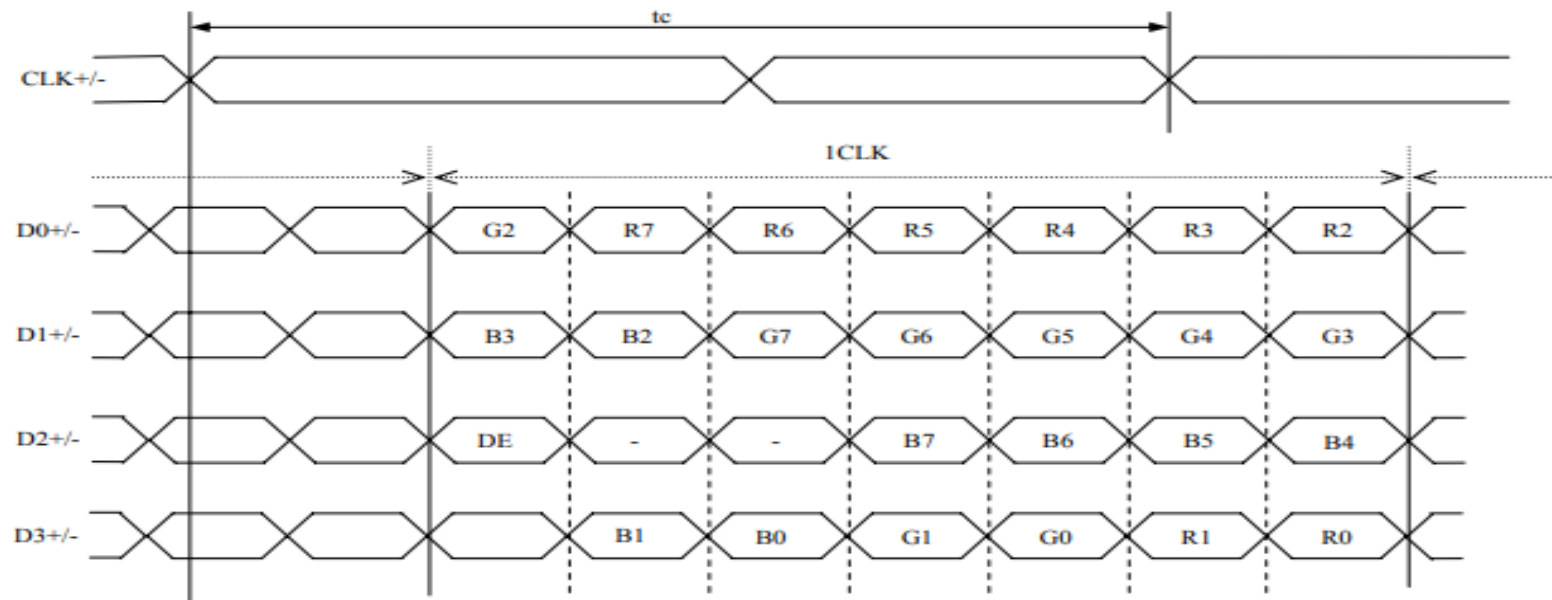
Horizontal Sync Polarity Negative

Vertical Sync Polarity Negative

Bits Per Pixel 18bpp

Single to single

- From display datasheet, identify:
- Mapping format:



- This is Format 1 (JEIDA), 24bpp

Single to single

- Fill out corresponding section in tool:

DSI83/84/85/86 Tuner - SN65DSI83

Panel Inputs DSI_Inputs Outputs

Panel Info

Channel A

Panel Vendor

Panel Model

Resolution 1024 pixels x 768 lines

LVDS Mode Single

Test Pattern

Pixels

	LVDS Channel A	LVDS Channel B
LVDS_HPW	<input type="text"/>	<input type="text"/>
LVDS_HBP	<input type="text"/>	<input type="text"/>
LVDS_HFP	<input type="text"/>	<input type="text"/>
LVDS_HActive	1024	<input type="text"/>
Htotal	1024	0

Lines

	LVDS Channel A
LVDS_VPW	<input type="text"/>
LVDS_VBP	<input type="text"/>
LVDS_VFP	<input type="text"/>
LVDS_VActive	768
Vtotal	768

Additional Panel Info

Channel A

FORMAT Format 1

Data Enable Polarity Positive

Horizontal Sync Polarity Negative

Vertical Sync Polarity Negative

Bits Per Pixel 24bpp

TEXAS INSTRUMENTS

Single to single

- From display datasheet, identify:
- Timing Parameters:

		Parameter	Symbol	min.	typ.	max.	Unit	Remarks
CLK	Frequency		1/tc	60.0	65.0	68.0	MHz	15.385ns (typ.)
	Duty		-				-	-
	Rise time, Fall time		-				ns	-
DATA	CLK-DATA	Setup time	-				ns	-
		Hold time	-				ns	
	Rise time, Fall time		-				ns	
Horizontal Pixels	Horizontal	Cycle	th	19.67	20.676	22.4	µs	48.363kHz (typ.)
		Display period	thd				CLK	
					1,344	-		
Active Horizontal Pixels	Vertical (One frame)	Cycle	tv	13.3	16.666	18.5	ms	60.0Hz (typ.)
		Display period	tvd				H	
					780	806		
Vertical Pixels	CLK-DE	Setup time	-				ns	-
		Hold time	-				ns	
		Rise time, Fall time		-				
					768			

- This particular datasheet states the total display area and the active display area

Single to single

- From display datasheet, identify:
- Timing Parameters:

Parameter		Symbol	min.	typ.	max.	Unit	Remarks
CLK	Frequency	1/tc	60.0	65.0	68.0	MHz	15.385ns (typ.)
	Duty	-				-	-
	Rise time, Fall time	-				ns	-
DATA	CLK-DATA	Setup time				ns	-
		Hold time				ns	
	Rise time, Fall time	-				ns	
DE	Horizontal	Cycle	19.67	20.676	22.4	μs	48.363kHz (typ.)
		Display period	-	1,344	-	CLK	
			1,024			CLK	
	Vertical (One frame)	Cycle	13.3	16.666	18.5	ms	60.0Hz (typ.)
		Display period	780	806	-	H	
			768			H	
CLK-DE	Setup time	-				ns	-
	Hold time	-				ns	
	Rise time, Fall time	-				ns	

- Horizontal Blanking = $1344 - 1024 = 320$
- Vertical Blanking = $806 - 768 = 38$

Single to single

- Fill out corresponding section in tool:

- Horizontal blanking (320) is divided among HPW, HBP, and HFP

- Vertical blanking (38) is divided among VPW, VBP, and VFP

DSI83/84/85/86 Tuner - SN65DSI83

Panel Inputs DSI_Inputs Outputs

Panel Info

Channel A

Panel Vendor

Panel Model

Resolution 1024 pixels x 768 lines

LVDS Mode Single

Test Pattern

Pixels

	LVDS Channel A	LVDS Channel B
LVDS_HPW	107	
LVDS_HBP	107	
LVDS_HFP	106	
LVDS_HActive	1024	
Htotal	1344	0

Additional Panel Info

Channel A

FORMAT Format 1

Data Enable Polarity Positive

Horizontal Sync Polarity Negative

Vertical Sync Polarity Negative

Bits Per Pixel 24bpp

Lines

	LVDS Channel A
LVDS_VPW	13
LVDS_VBP	13
LVDS_VFP	12
LVDS_VActive	768
Vtotal	806

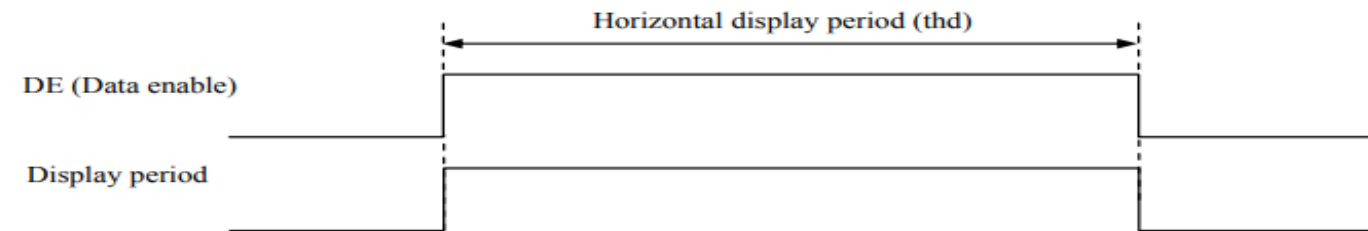
TEXAS INSTRUMENTS

Single to single

- From display datasheet, identify HSYNC, VSYNC, and DE polarity
- This particular display operates in DE mode, so HSYNC/VSYNC Polarity don't matter.
- DE is positive during active display, so DE polarity is positive

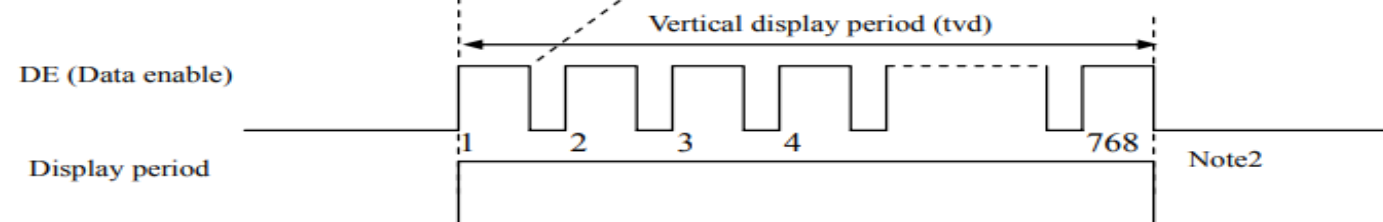
- Horizontal signal

Note1



- Vertical signal

Note1



Single to single

- Fill out corresponding section in tool:

DSI83/84/85/86 Tuner - SN65DSI83

Panel Inputs DSI_Inputs Outputs

Panel Info

Channel A

Panel Vendor

Panel Model

Resolution 1024 pixels x 768 lines

LVDS Mode Single

Test Pattern

Pixels

	LVDS Channel A	LVDS Channel B
LVDS_HPW	107	
LVDS_HBP	107	
LVDS_HFP	106	
LVDS_HActive	1024	
Htotal	1344	0

Lines

	LVDS Channel A
LVDS_VPW	13
LVDS_VBP	13
LVDS_VFP	12
LVDS_VActive	768
Vtotal	806

Additional Panel Info

Channel A

FORMAT Format 1

Data Enable Polarity Positive

Horizontal Sync Polarity Negative

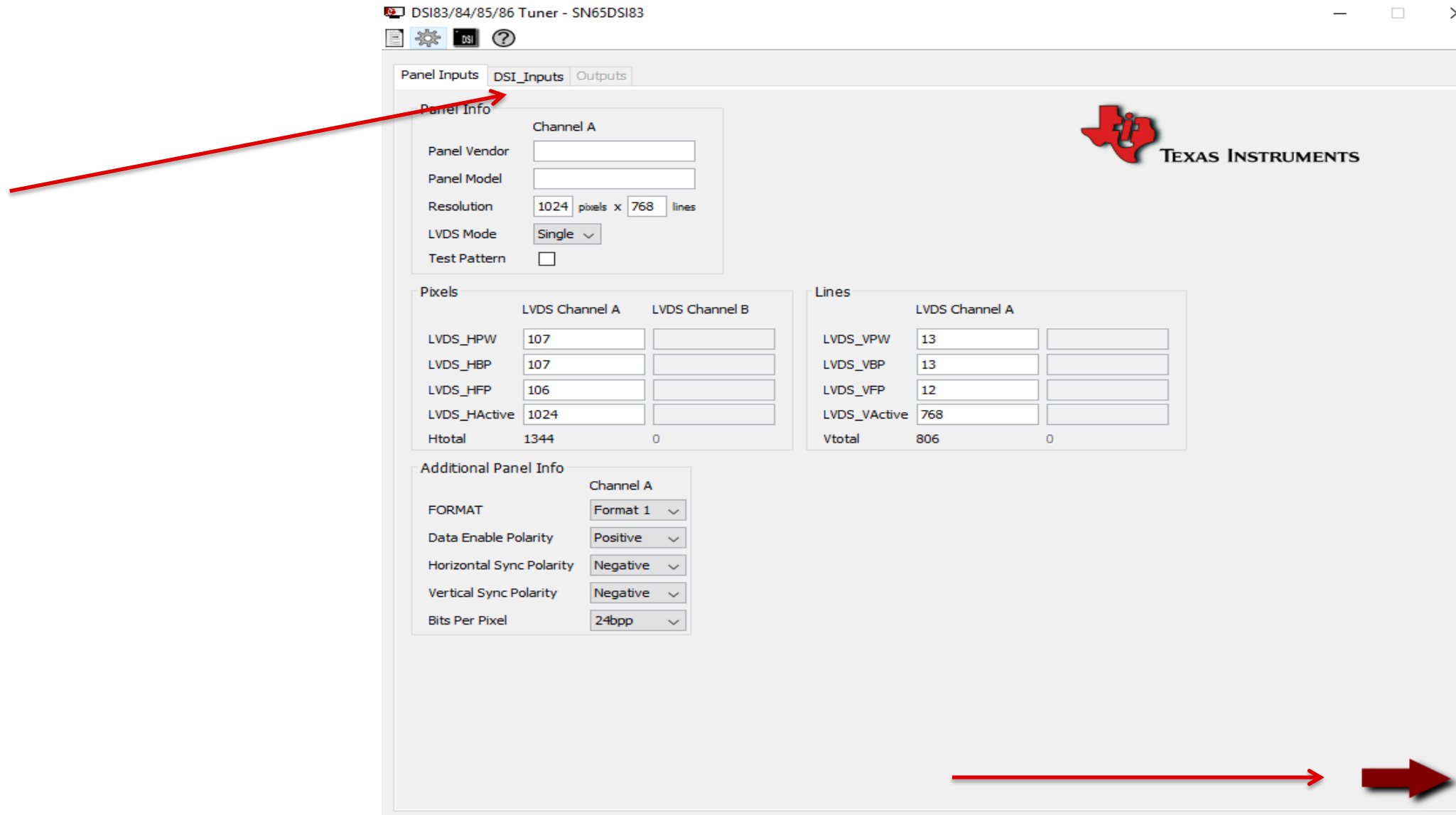
Vertical Sync Polarity Negative

Bits Per Pixel 24bpp

TEXAS INSTRUMENTS

Single to single

- Switch to “DSI_Inputs” window by either clicking the tab or clicking the arrow:



Single to single

- The inputs to this window mainly depend on the DSI source
- The parameters entered **must** match the actual DSI parameters transmitted by the DSI source

DSI83/84/85/86 Tuner - SN65DSI83

Panel Inputs DSI_Inputs Outputs

DSI Info

Panel Resolution: 1024x768
DSI Ch Mode: Single
Left right or even odd LR CROP Enable: No

Informational

LP: All
Burst Mode: Burst
Sync Mode: Event

Pixels

DSI Channel A Inputs: DSI_HPW, DSI_HBP, DSI_HFP, DSI_HActive: 1024, DSI_Htotal: 1024
DSI Channel B Inputs: (empty)

Lines

DSI Channel A Inputs: DSI_VPW, DSI_VBP, DSI_VFP, DSI_VActive: 768, DSI_Vtotal: 768
DSI Channel B Inputs: (empty)

Additional Channel info

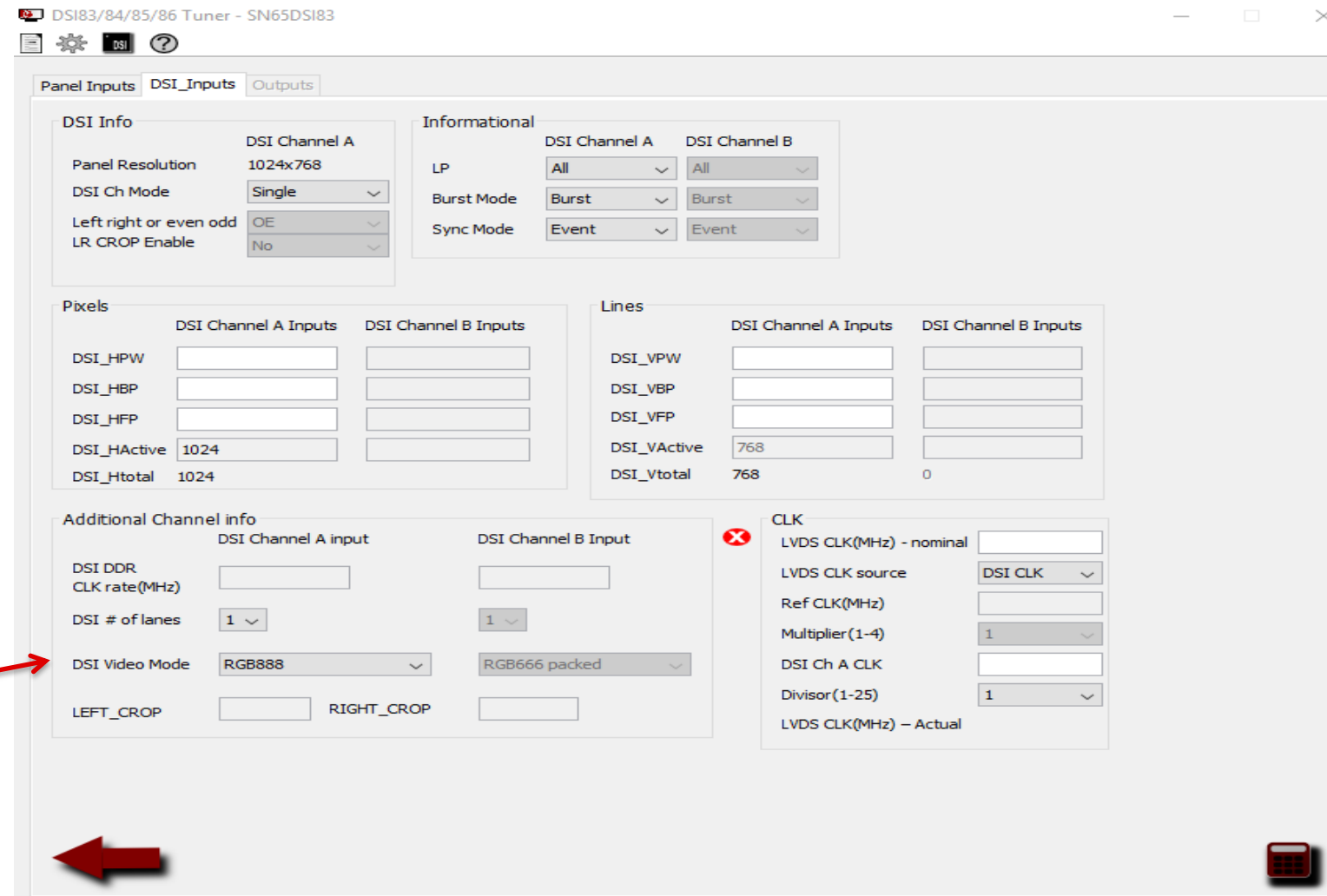
DSI Channel A input: DSI DDR, CLK rate(MHz), DSI # of lanes: 1, DSI Video Mode: RGB888, LEFT_CROP
DSI Channel B Input: DSI DDR, CLK rate(MHz), DSI # of lanes: 1, DSI Video Mode: RGB666 packed, RIGHT_CROP

CLK

LVDS CLK(MHz) - nominal: (empty)
LVDS CLK source: DSI CLK
Ref CLK(MHz): (empty)
Multiplier(1-4): 1
DSI Ch A CLK: (empty)
Divisor(1-25): 1
LVDS CLK(MHz) - Actual: (empty)

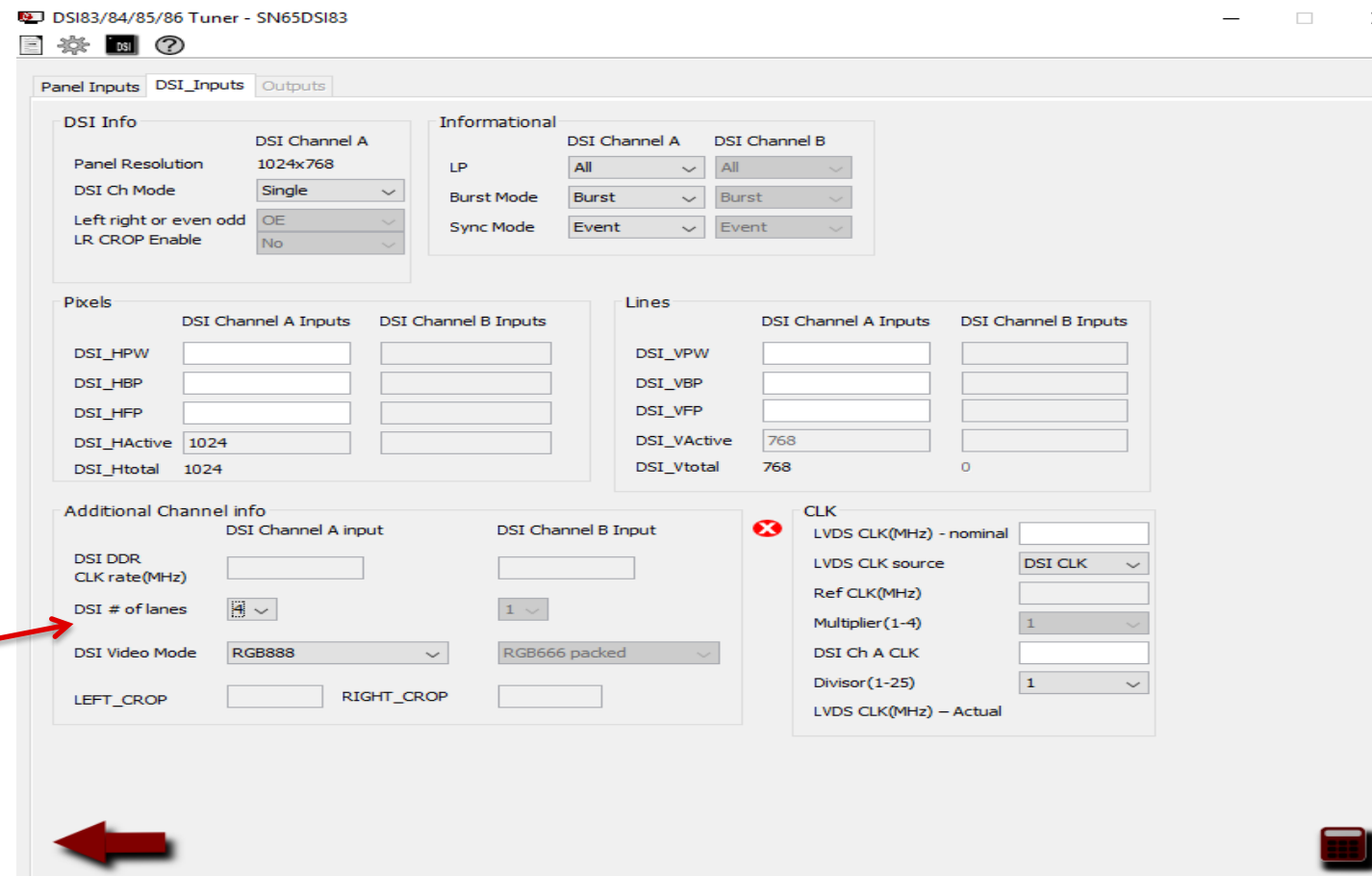
Single to single

- Since the display is 24bpp, select “RGB888” as the DSI Video Mode



Single to single

- The “DSI # of lanes” depends on the required throughput to meet the display resolution
- Each lane can support up to 1 Gbps



Single to single

- Enter the pixel/line information. Typically this will match the display inputs:

DSI83/84/85/86 Tuner - SN65DSI83

Panel Inputs | **DSI_Inputs** | Outputs

DSI Info

DSI Channel A

Panel Resolution: 1024x768

DSI Ch Mode: Single

Left right or even odd: OE

LR CROP Enable: No

Informational

DSI Channel A | DSI Channel B

LP: All | All

Burst Mode: Burst | Burst

Sync Mode: Event | Event

Pixels

	DSI Channel A Inputs	DSI Channel B Inputs
DSI_HPW	107	
DSI_HBP	107	
DSI_HFP	106	
DSI_HActive	1024	
DSI_Htotal	1344	

Lines

	DSI Channel A Inputs	DSI Channel B Inputs
DSI_VPW	13	
DSI_VBP	13	
DSI_VFP	12	
DSI_VActive	768	
DSI_Vtotal	806	

Additional Channel info

	DSI Channel A input	DSI Channel B Input	
DSI DDR CLK rate(MHz)			
DSI # of lanes	4	1	
DSI Video Mode	RGB888	RGB666 packed	
LEFT_CROP		RIGHT_CROP	

CLK

LVDS CLK(MHz) - nominal: []

LVDS CLK source: DSI CLK

Ref CLK(MHz): []

Multiplier(1-4): 1

DSI Ch A CLK: []

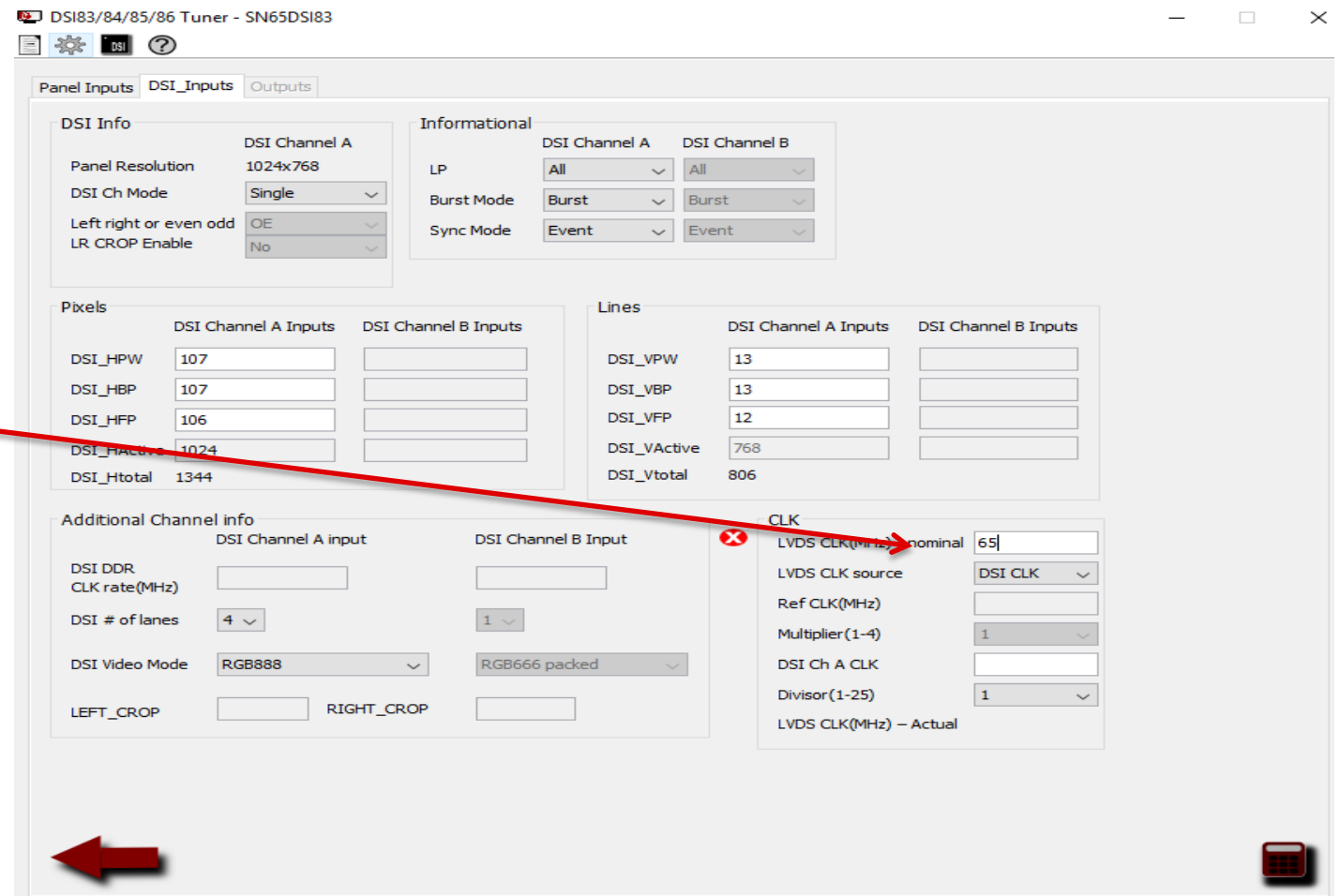
Divisor(1-25): 1

LVDS CLK(MHz) - Actual: []

Single to single

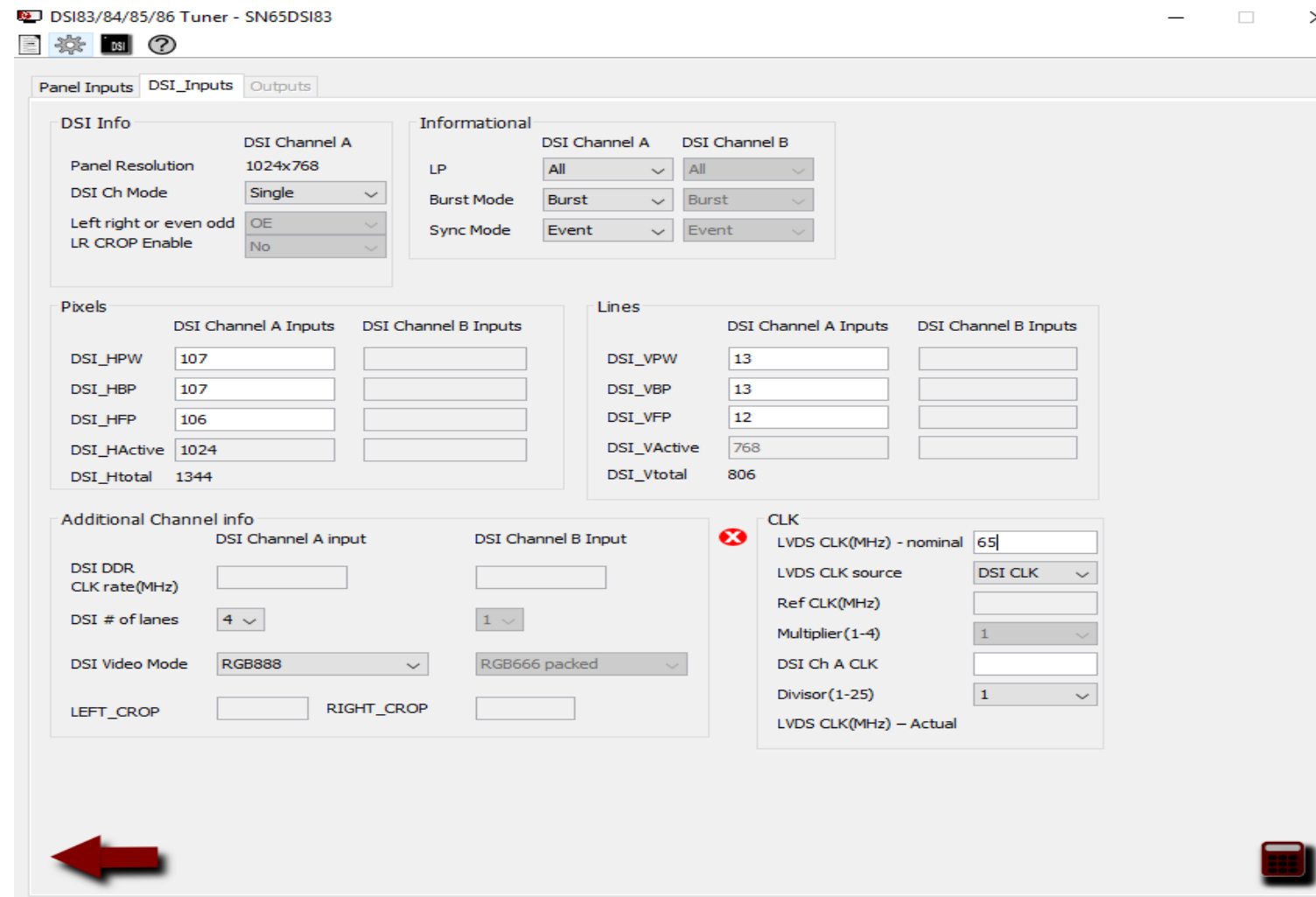
- Enter the “LVDS CLK(MHz) – nominal value from the frequency specified in the display datasheet
- The LVDS CLK range for the SN65DSI83/84/85 is 25 to 154MHz, so make sure you’re within this range

Parameter		Symbol	min.	typ.	max.	Unit	Remarks	
CLK	Frequency	1/tc	60.0	65.0	68.0	MHz	15.385ns (typ.)	
	Duty	-	-	-	-	-	-	
	Rise time, Fall time	-	-	-	-	ns	-	
DATA	CLK-DATA	Setup time	-	-	-	ns	-	
		Hold time	-	-	-	ns	-	
	Rise time, Fall time	-	-	-	-	ns	-	
DE	Horizontal	Cycle	th	19.67	20.676	22.4	μs	48.363kHz (typ.)
		Display period	thd	-	1,344	-	CLK	
	Vertical (One frame)	Cycle	tv	13.3	16.666	18.5	ms	60.0Hz (typ.)
		Display period	tvd	780	806	-	H	
	CLK-DE	Setup time	-	-	-	-	ns	-
		Hold time	-	-	-	-	ns	-
Rise time, Fall time	-	-	-	-	ns	-		



Single to single

- The LVDS CLK source can be derived from either the DSI Ch A CLK (DSI DDR CLK) or an external reference clock



Single to single

- To calculate the minimum required DSI CLK frequency, use the below equation:

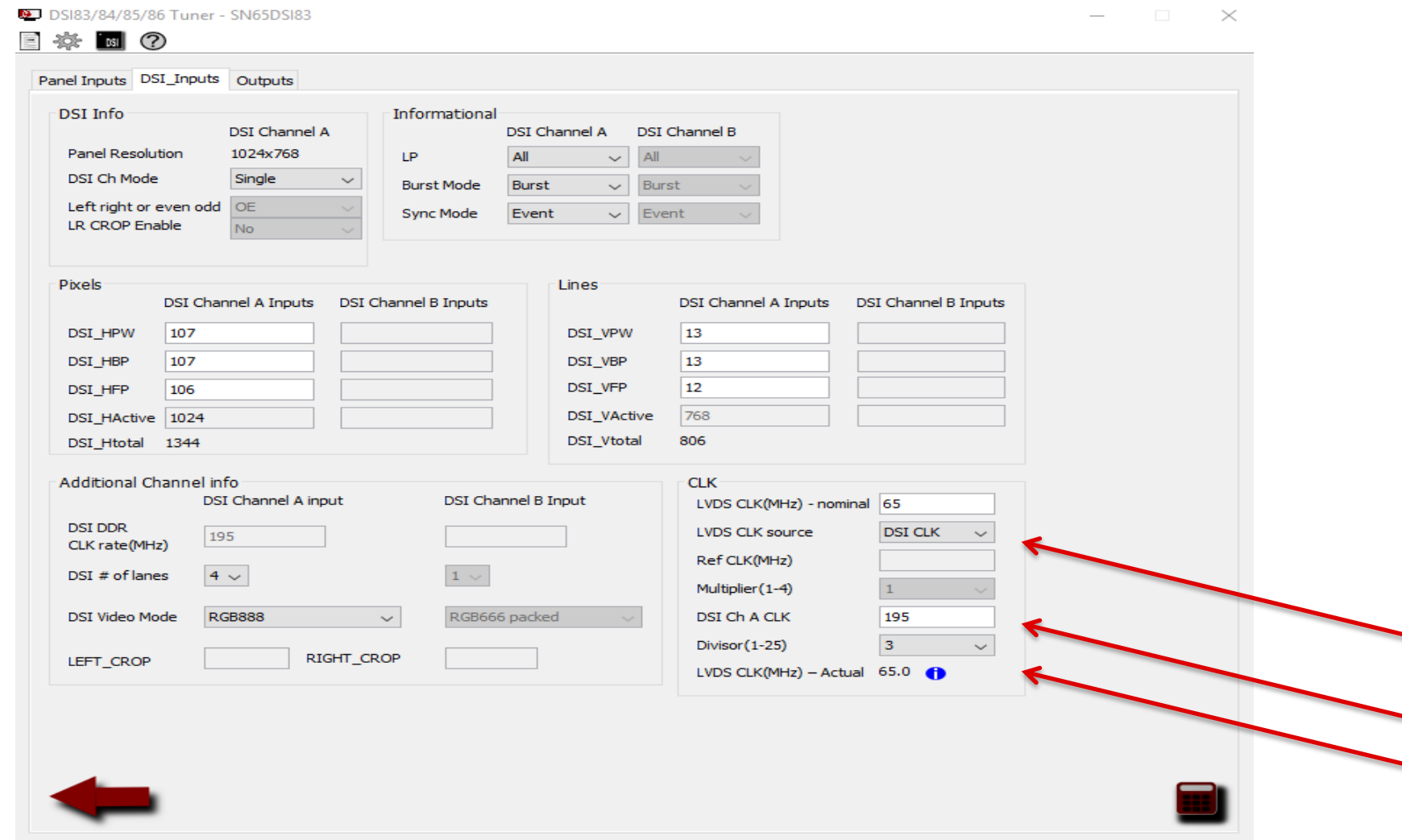
- $$\text{Minimum DSICLK frequency} = \frac{\text{Throughput}}{2 \times \# \text{ of DSI Lanes}} = \frac{\text{LVDS CLK} \times \text{bpp}}{2 \times \# \text{ of DSI Lanes}}$$

- For this example:

- $$\text{Minimum DSICLK frequency} = \frac{65 \text{ MHz} \times 24 \text{ bpp}}{2 \times 4} = \frac{1560 \text{ Mbps}}{2 \times 4} = 195 \text{ MHz}$$

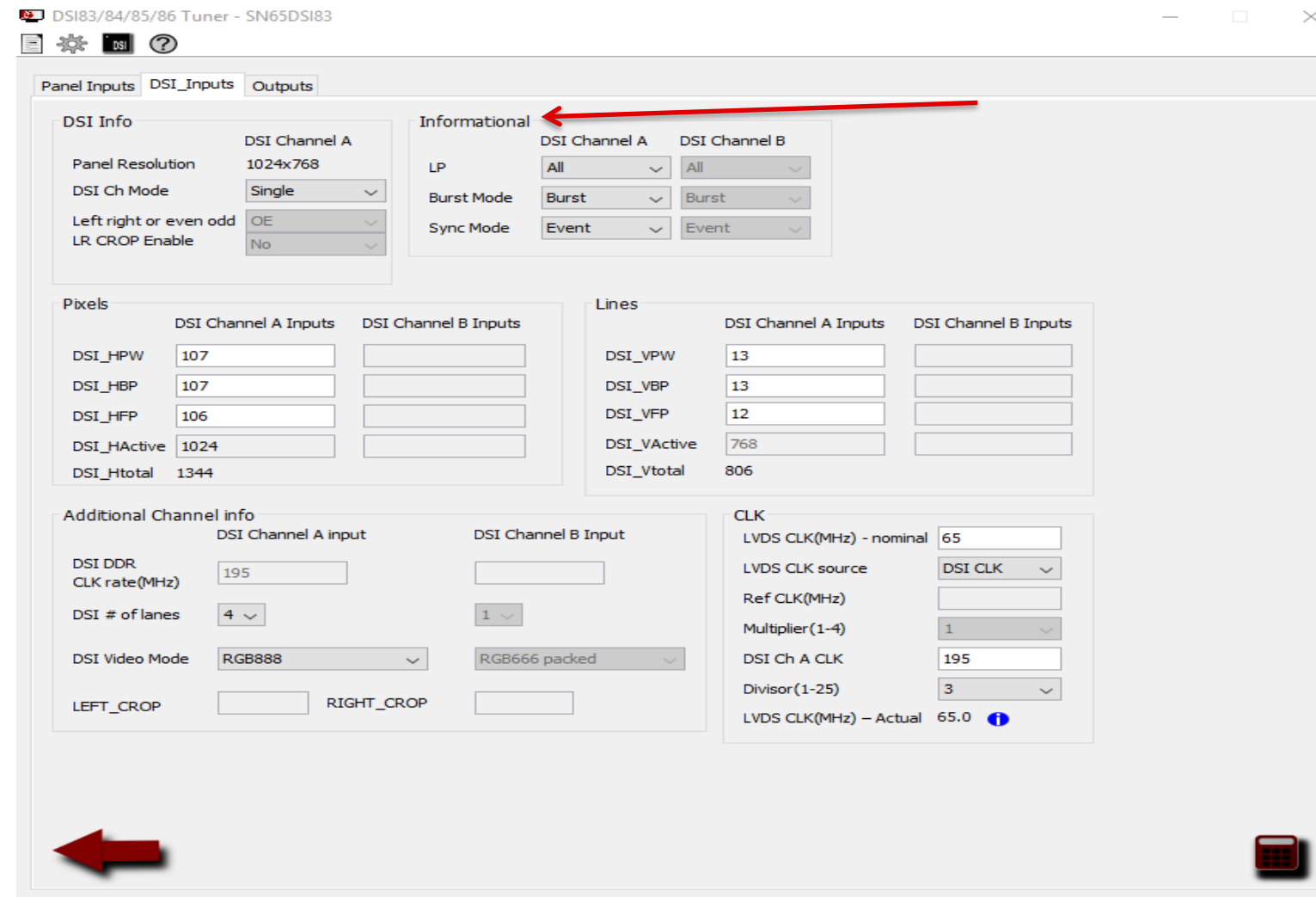
Single to single

- Fill out the corresponding section in the tool and select the correct divisor:



Single to single

- The “Informational” section depends on the DSI source:



Single to single


- Click the calculator icon in the lower right to get to the “Outputs” window
- Make note of the LINE TIME requirement. The line time (horizontal sync to the next horizontal) on the input is preserved when outputting onto the LVDS interface.

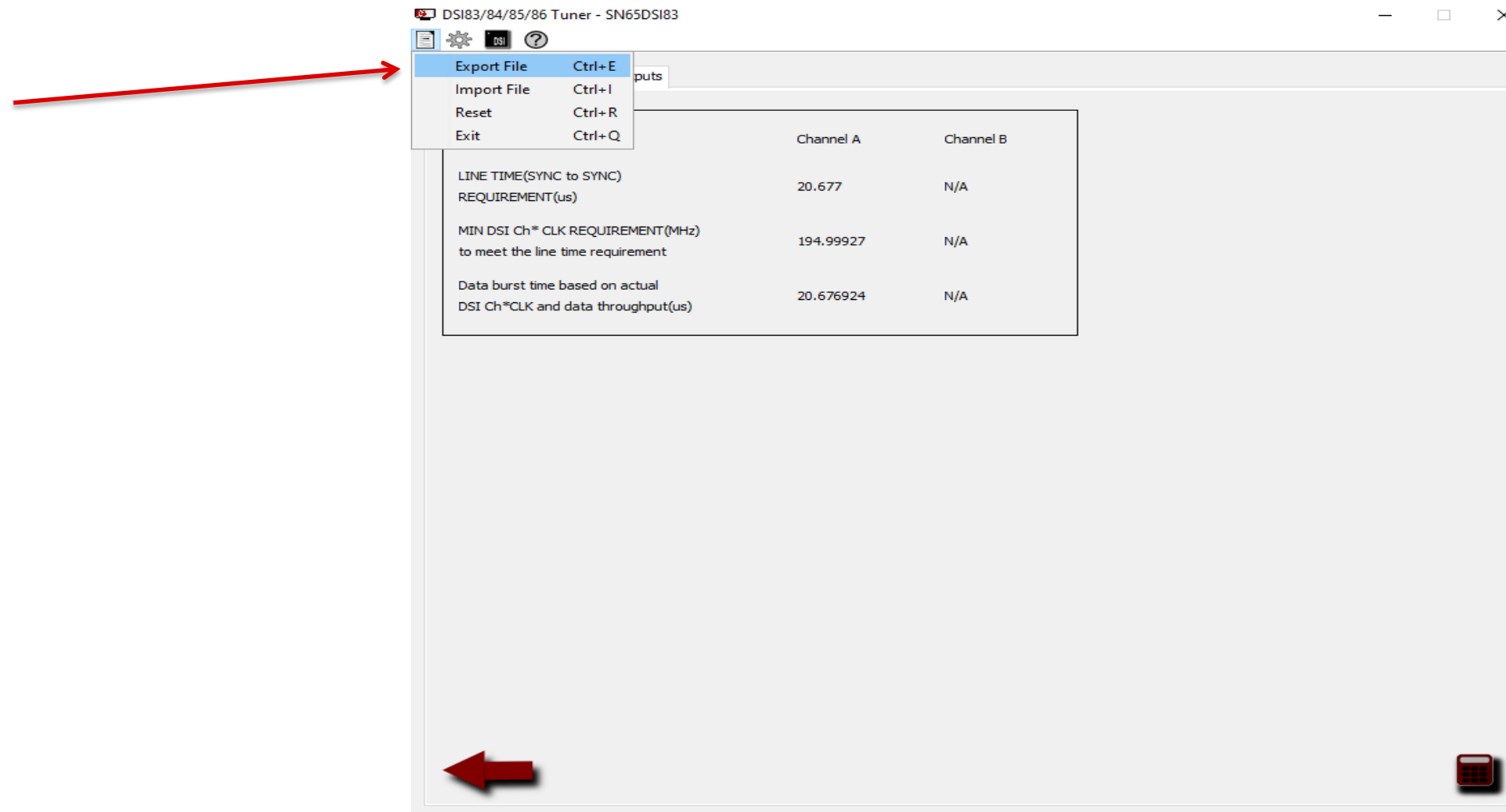
DSI83/84/85/86 Tuner - SN65DSI83

Panel Inputs DSI_Inputs Outputs

	Channel A	Channel B
LINE TIME(SYNC to SYNC) REQUIREMENT(us)	20.677	N/A
MIN DSI Ch* CLK REQUIREMENT(MHz) to meet the line time requirement	194.99927	N/A
Data burst time based on actual DSI Ch*CLK and data throughput(us)	20.676924	N/A

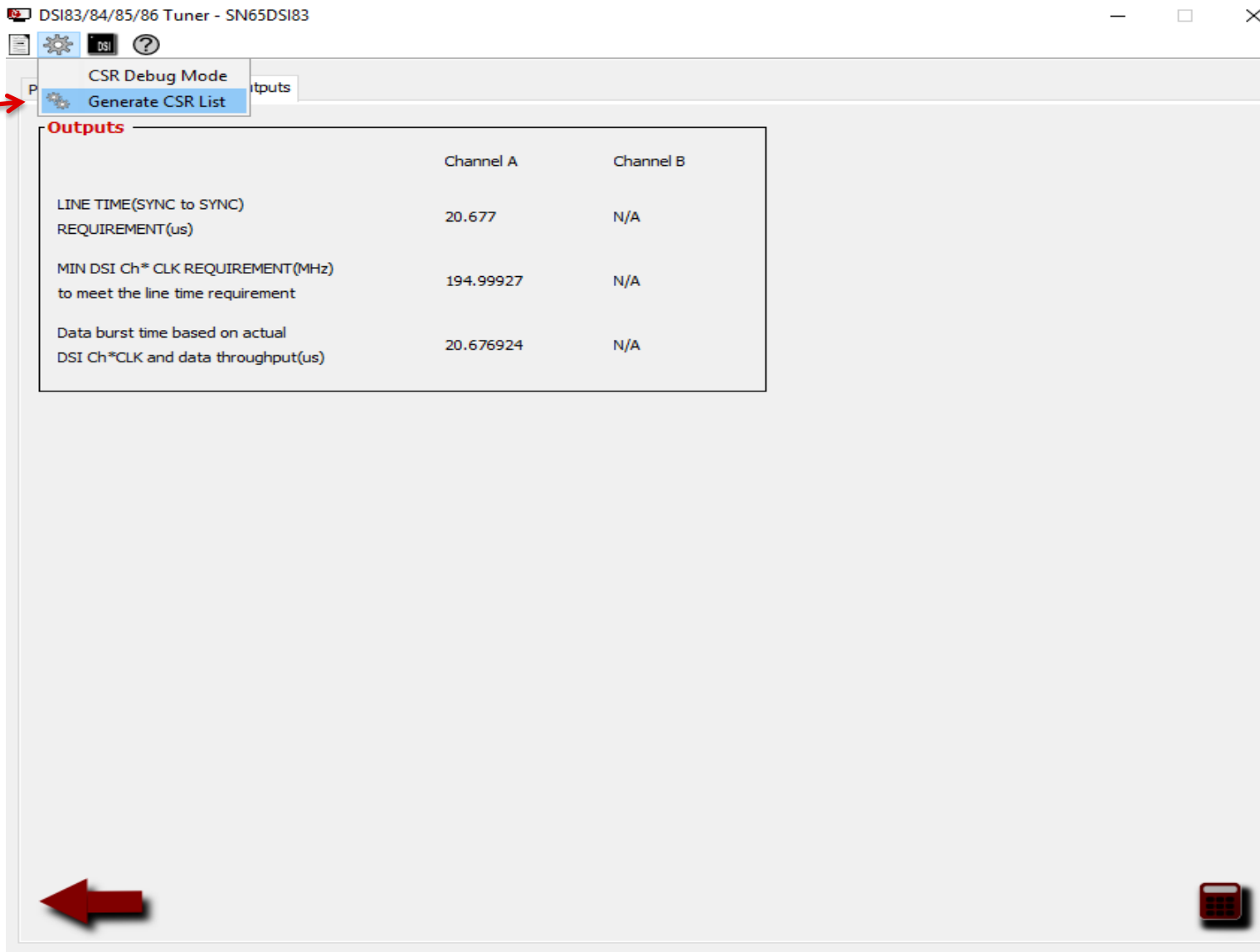
Single to single

- Click the  icon in the upper left to export/save the .dsi file
- You can import it later without having to re-enter all the settings



Single to single

- Click the  icon in the upper left and Generate CSR list



DSI83/84/85/86 Tuner - SN65DSI83

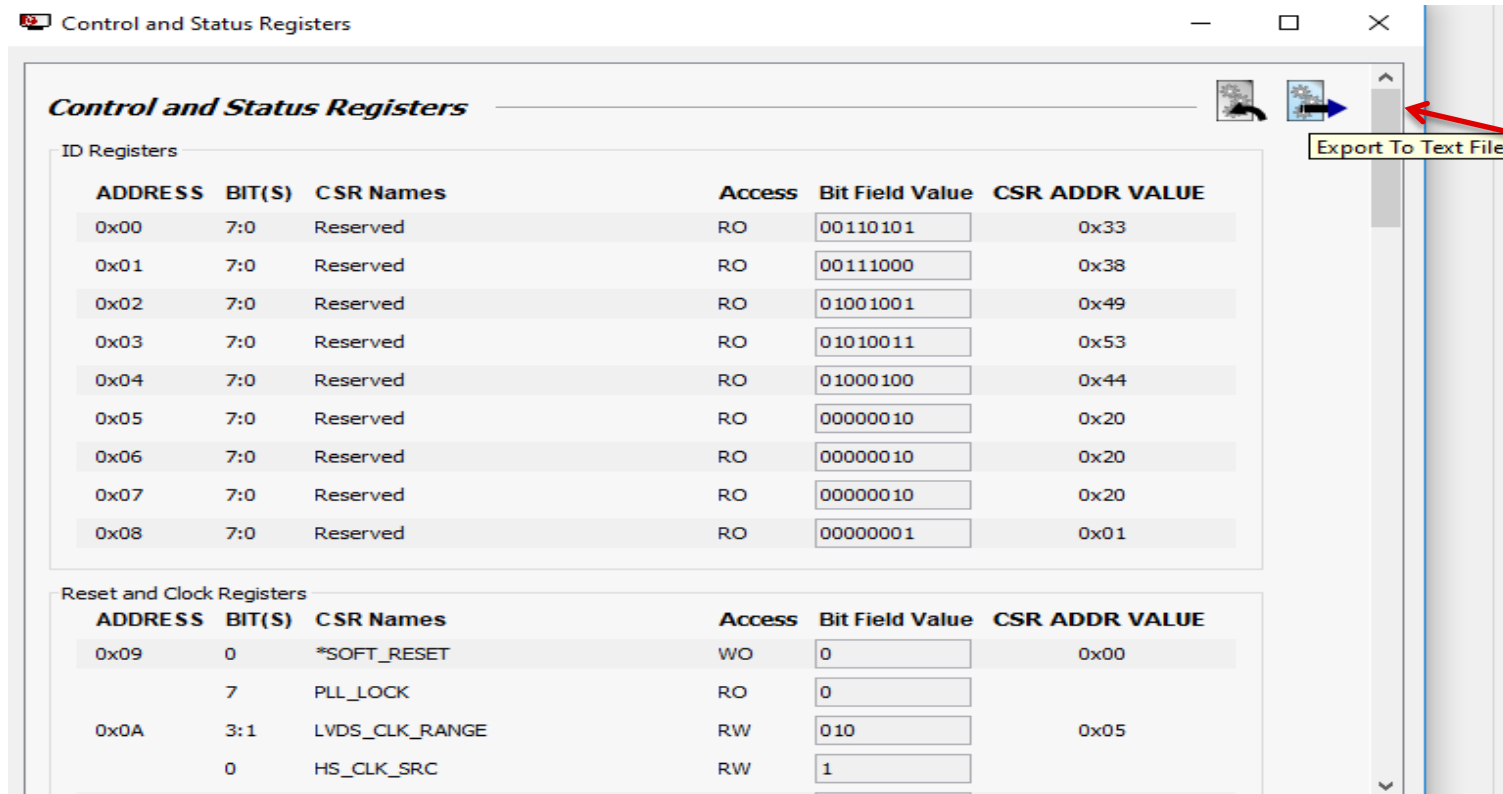
CSR Debug Mode
Generate CSR List

Outputs

	Channel A	Channel B
LINE TIME(SYNC to SYNC) REQUIREMENT(us)	20.677	N/A
MIN DSI Ch* CLK REQUIREMENT(MHz) to meet the line time requirement	194.99927	N/A
Data burst time based on actual DSI Ch*CLK and data throughput(us)	20.676924	N/A

Single to single

- When the “Control and Status Registers” window pops up, click the  icon to export the settings to a .txt file



The screenshot shows a window titled "Control and Status Registers" with a table of registers. The table is divided into two sections: "ID Registers" and "Reset and Clock Registers".

ADDRESS	BIT(S)	CSR Names	Access	Bit Field Value	CSR ADDR VALUE
0x00	7:0	Reserved	RO	00110101	0x33
0x01	7:0	Reserved	RO	00111000	0x38
0x02	7:0	Reserved	RO	01001001	0x49
0x03	7:0	Reserved	RO	01010011	0x53
0x04	7:0	Reserved	RO	01000100	0x44
0x05	7:0	Reserved	RO	00000010	0x20
0x06	7:0	Reserved	RO	00000010	0x20
0x07	7:0	Reserved	RO	00000010	0x20
0x08	7:0	Reserved	RO	00000001	0x01

ADDRESS	BIT(S)	CSR Names	Access	Bit Field Value	CSR ADDR VALUE
0x09	0	*SOFT_RESET	WO	0	0x00
	7	PLL_LOCK	RO	0	
0x0A	3:1	LVDS_CLK_RANGE	RW	010	0x05
	0	HS_CLK_SRC	RW	1	

The "Export To Text File" button is located in the top right corner of the window, indicated by a red arrow.

Single to single

- Open up the .txt file that was just generated. The column on the left contains the I2C register addresses, and the column on the right contains the values that need to be written

```
CSR.txt - Notepad
File Edit Format View Help
-----
// Filename : CSR.txt
//
// (C) Copyright 2013 by Texas Instruments Incorporated.
// All rights reserved.
//
-----
0x09      0x00
0x0A      0x05
0x0B      0x10
0x0D      0x00
0x10      0x26
0x11      0x00
0x12      0x27
0x13      0x00
0x18      0x7a
0x19      0x00
0x1A      0x03
0x1B      0x00
0x20      0x00
0x21      0x04
0x22      0x00
0x23      0x00
0x24      0x00
0x25      0x00
0x26      0x00
0x27      0x00
0x28      0x21
0x29      0x00
0x2A      0x00
0x2B      0x00
0x2C      0x6b
0x2D      0x00
0x2E      0x00
0x2F      0x00
0x30      0x0d
0x31      0x00
0x32      0x00
0x33      0x00
0x34      0x6b
0x35      0x00
0x36      0x00
0x37      0x00
0x38      0x00
0x39      0x00
0x3A      0x00
0x3B      0x00
0x3C      0x00
0x3D      0x00
0x3E      0x00
```

The PLL_EN bit and SOFT_RESET bit are not set as they need to be set per the recommended sequence defined in the datasheet

Thanks for your time!