

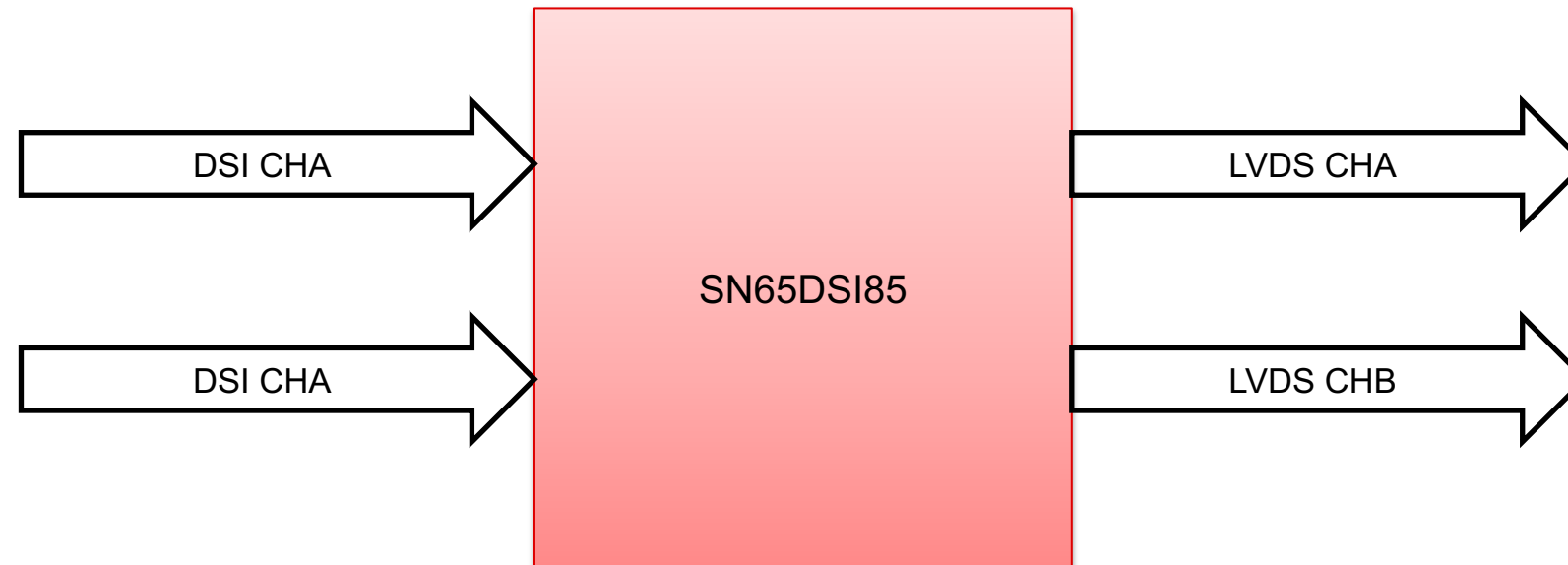
Dual DSI Input to Dual-Link LVDS

TI Precision Labs – SN65DSI83/84/85

Presented and prepared by Ikechukwu Anyiam

Dual to dual

- The SN65DSI85 is the only device that can be used for this application



Dual to dual

- From display datasheet, identify:
- Resolution:

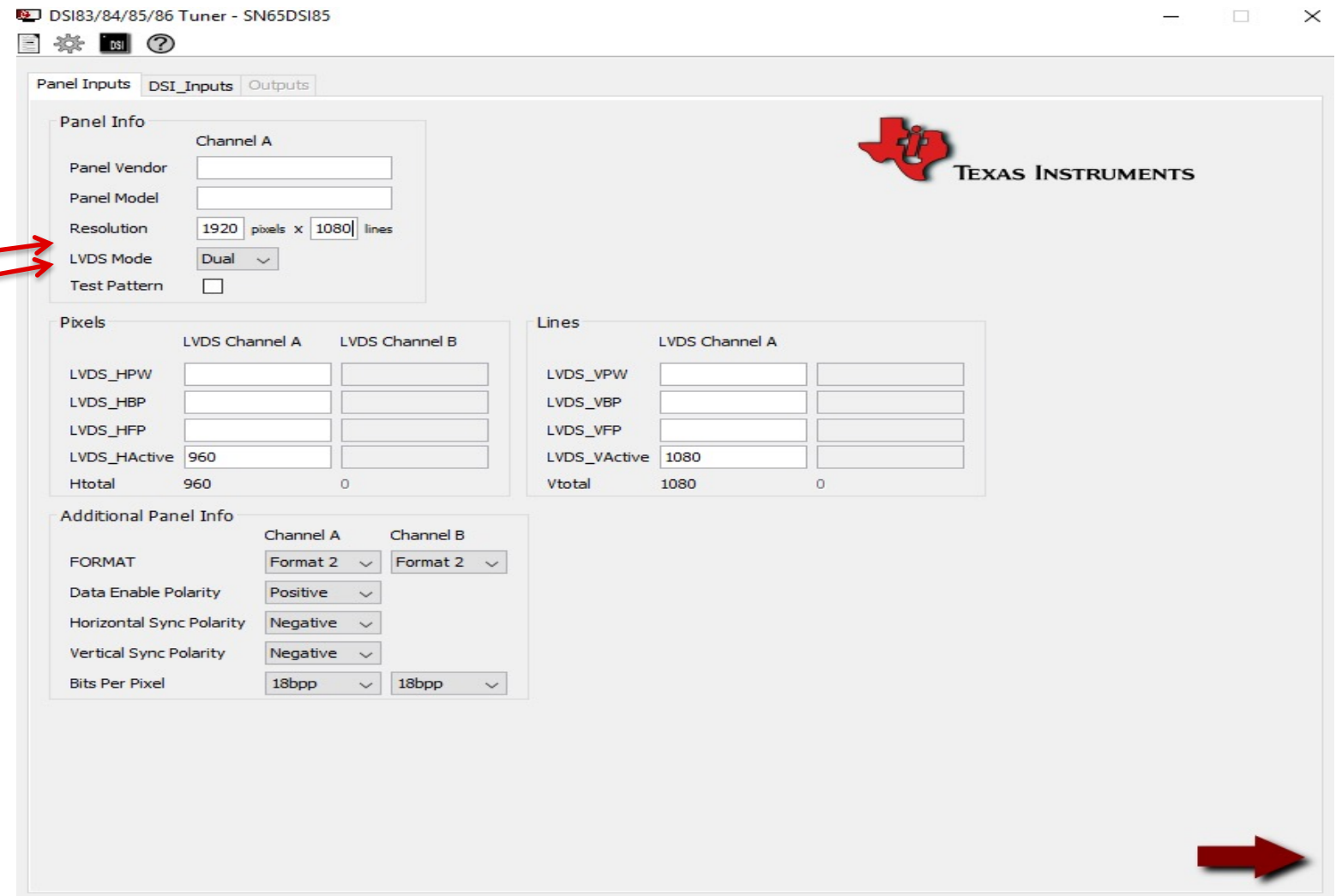
Items	Unit	Specification
Screen Diagonal	[mm]	609.7 (24.0")
Active Area	[mm]	531.36 (H) x 298.89 (V)
Pixels H x V		1920 x 1080
Pixel Pitch	[µm]	276.75 (per one triad) ~276.75

- This is a 1920 x 1080 panel

Dual to dual

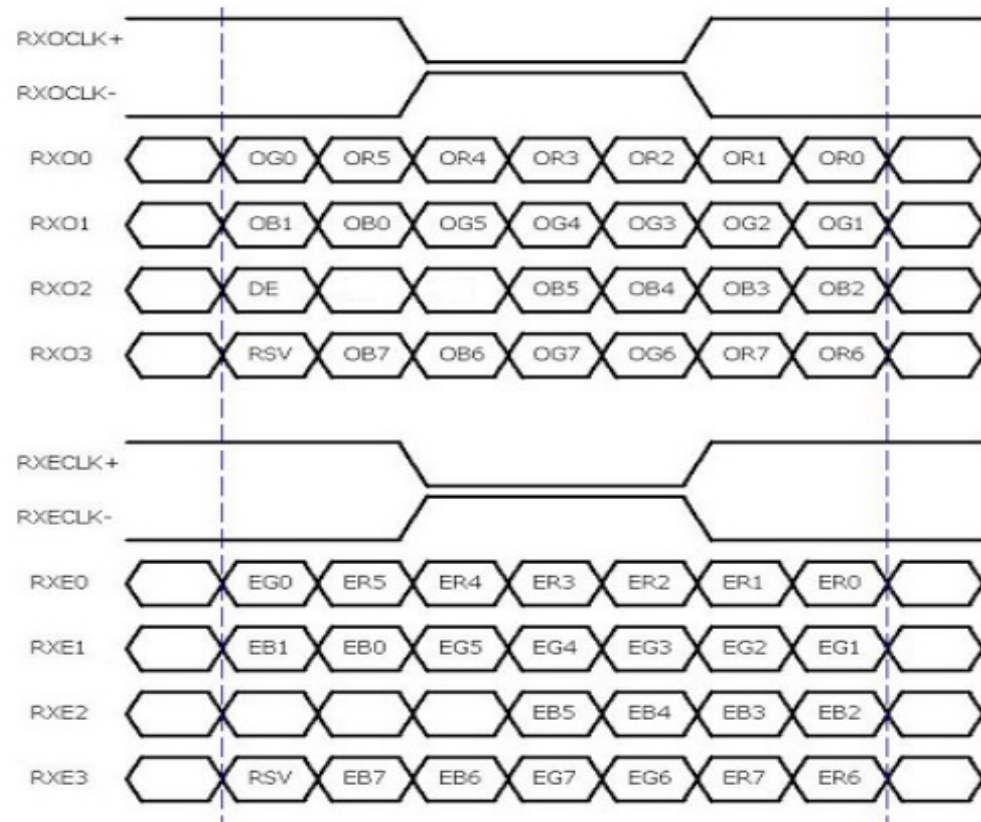
- After changing the “LVDS Mode” to “Dual”, fill in the resolution:

- Notice how the tool automatically divides “LVDS_HActive” by 2.



Dual to dual

- From display datasheet, identify:
- Mapping format:



- This is Format 2 (VESA), 24bpp

Dual to dual

- Fill out corresponding section in tool:

DSI83/84/85/86 Tuner - SN65DSI85

Panel Inputs | DSI_Inputs | Outputs

Panel Info

Channel A

Panel Vendor:

Panel Model:

Resolution: 1920 pixels x 1080 lines

LVDS Mode: Dual

Test Pattern:

Pixels

	LVDS Channel A	LVDS Channel B
LVDS_HPW	<input type="text"/>	<input type="text"/>
LVDS_HBP	<input type="text"/>	<input type="text"/>
LVDS_HFP	<input type="text"/>	<input type="text"/>
LVDS_HActive	960	<input type="text"/>
Htotal	960	0

Lines

	LVDS Channel A	LVDS Channel B
LVDS_VPW	<input type="text"/>	<input type="text"/>
LVDS_VBP	<input type="text"/>	<input type="text"/>
LVDS_VFP	<input type="text"/>	<input type="text"/>
LVDS_VActive	1080	<input type="text"/>
Vtotal	1080	0

Additional Panel Info

	Channel A	Channel B
FORMAT	Format 2	Format 2
Data Enable Polarity	Positive	<input type="text"/>
Horizontal Sync Polarity	Negative	<input type="text"/>
Vertical Sync Polarity	Negative	<input type="text"/>
Bits Per Pixel	24bpp	24bpp

Dual to dual

- From display datasheet, identify:
- Timing Parameters:

Signal	Item	Symbol	Min	Typ	Max	Unit
Vertical Section	Period	Tv	1092	1130	1818	Th
	Active	Tdisp(v)	1080	1080	1080	Th
	Blanking	Tblk(v)	12	50	738	Th
Horizontal Section	Period	Th	1034	1050	1100	Tclk
	Active	Tdisp(h)	960	960	960	Tclk
	Blanking	Tblk(h)	74	90	140	Tclk
Clock	Period	Tclk	10.6	14.0	17.7	Ns
	Frequency	Freq	56.5	71.2	94	MHz
Frame rate	Frame rate	VFreq	50	60	76	Hz
Hsync Frequency	Hsync Frequency	HFreq	55	68	91	KHz

- From this, we can see that the total vertical blanking is 50, and the total horizontal blanking is 90
 - $VPW+VBP+VFP=50$
 - $HPW+HBP+HFP=90$

Dual to dual

- Fill out corresponding section in tool:
- Horizontal blanking (90) is divided among HPW, HBP, and HFP

- Vertical blanking (50) is divided Among VPW, VBP, and VFP

DSI83/84/85/86 Tuner - SN65DSI85

Panel Inputs | DSI_Inputs | Outputs

Panel Info

Channel A

Panel Vendor:

Panel Model:

Resolution: 1920 pixels x 1080 lines

LVDS Mode: Dual

Test Pattern:

Pixels

	LVDS Channel A	LVDS Channel B
LVDS_HPW	30	30
LVDS_HBP	30	30
LVDS_HFP	30	30
LVDS_HActive	960	960
Htotal	1050	1050

Lines

	LVDS Channel A
LVDS_VPW	17
LVDS_VBP	17
LVDS_VFP	16
LVDS_VActive	1080
Vtotal	1130

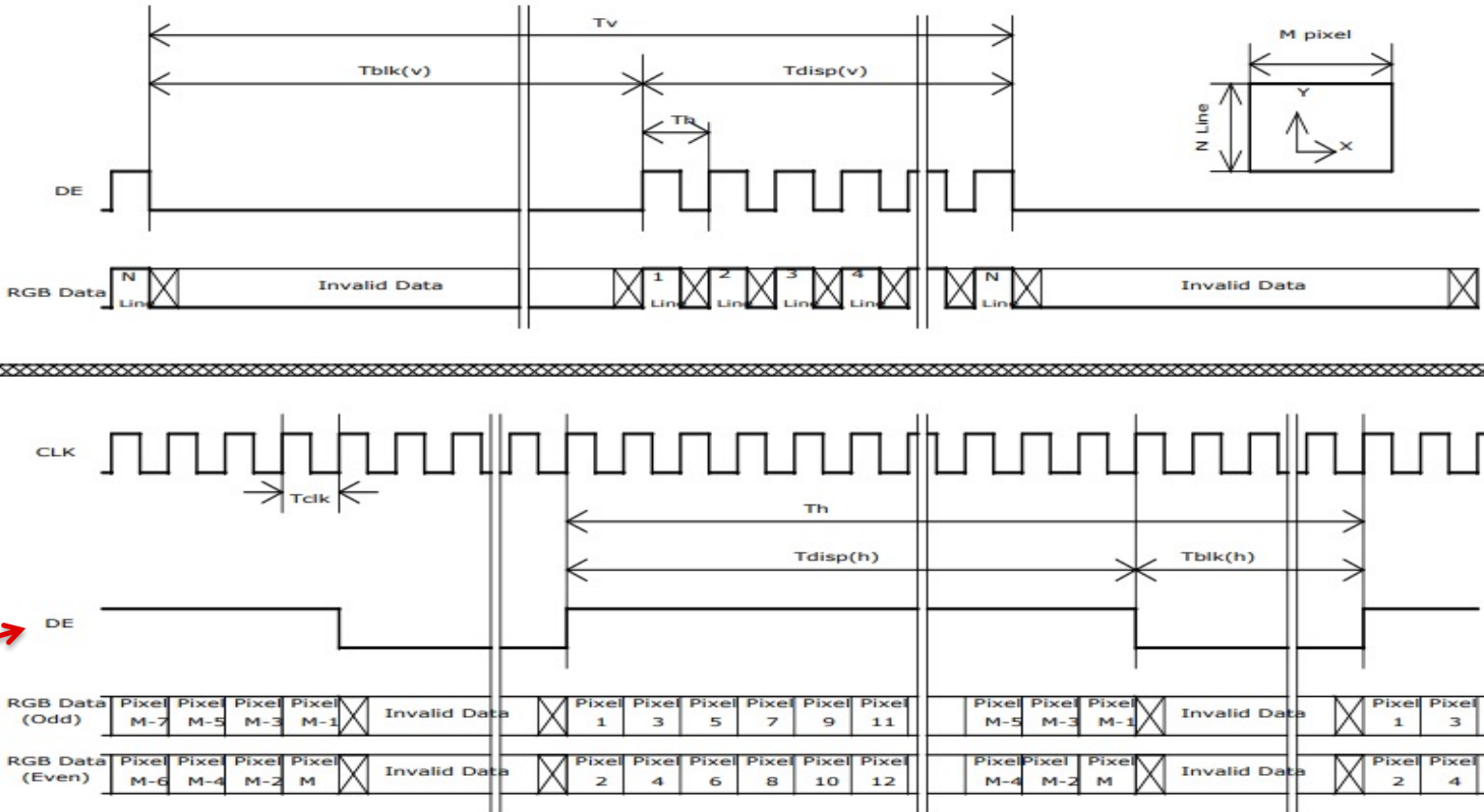
Additional Panel Info

	Channel A	Channel B
FORMAT	Format 2	Format 2
Data Enable Polarity	Positive	
Horizontal Sync Polarity	Negative	
Vertical Sync Polarity	Negative	
Bits Per Pixel	24bpp	24bpp

TEXAS INSTRUMENTS

Dual to dual

- From display datasheet, identify:
- HSYNC, VSYNC, and DE polarity:
- This particular display operates in DE mode, so HSYNC/VSYNC polarity don't matter.
- DE is positive during active display → so DE polarity is positive



Dual to dual

- Fill out corresponding section in tool:

DSI83/84/85/86 Tuner - SN65DSI85

Panel Inputs | DSI_Inputs | Outputs

Panel Info

Channel A

Panel Vendor:

Panel Model:

Resolution: 1920 pixels x 1080 lines

LVDS Mode: Dual

Test Pattern:

Pixels

	LVDS Channel A	LVDS Channel B
LVDS_HPW	30	30
LVDS_HBP	30	30
LVDS_HFP	30	30
LVDS_HActive	960	960
Htotal	1050	1050

Lines

	LVDS Channel A
LVDS_VPW	17
LVDS_VBP	17
LVDS_VFP	16
LVDS_VActive	1080
Vtotal	1130

Additional Panel Info

	Channel A	Channel B
FORMAT	Format 2	Format 2
Data Enable Polarity	Positive	
Horizontal Sync Polarity	Negative	
Vertical Sync Polarity	Negative	
Bits Per Pixel	24bpp	24bpp

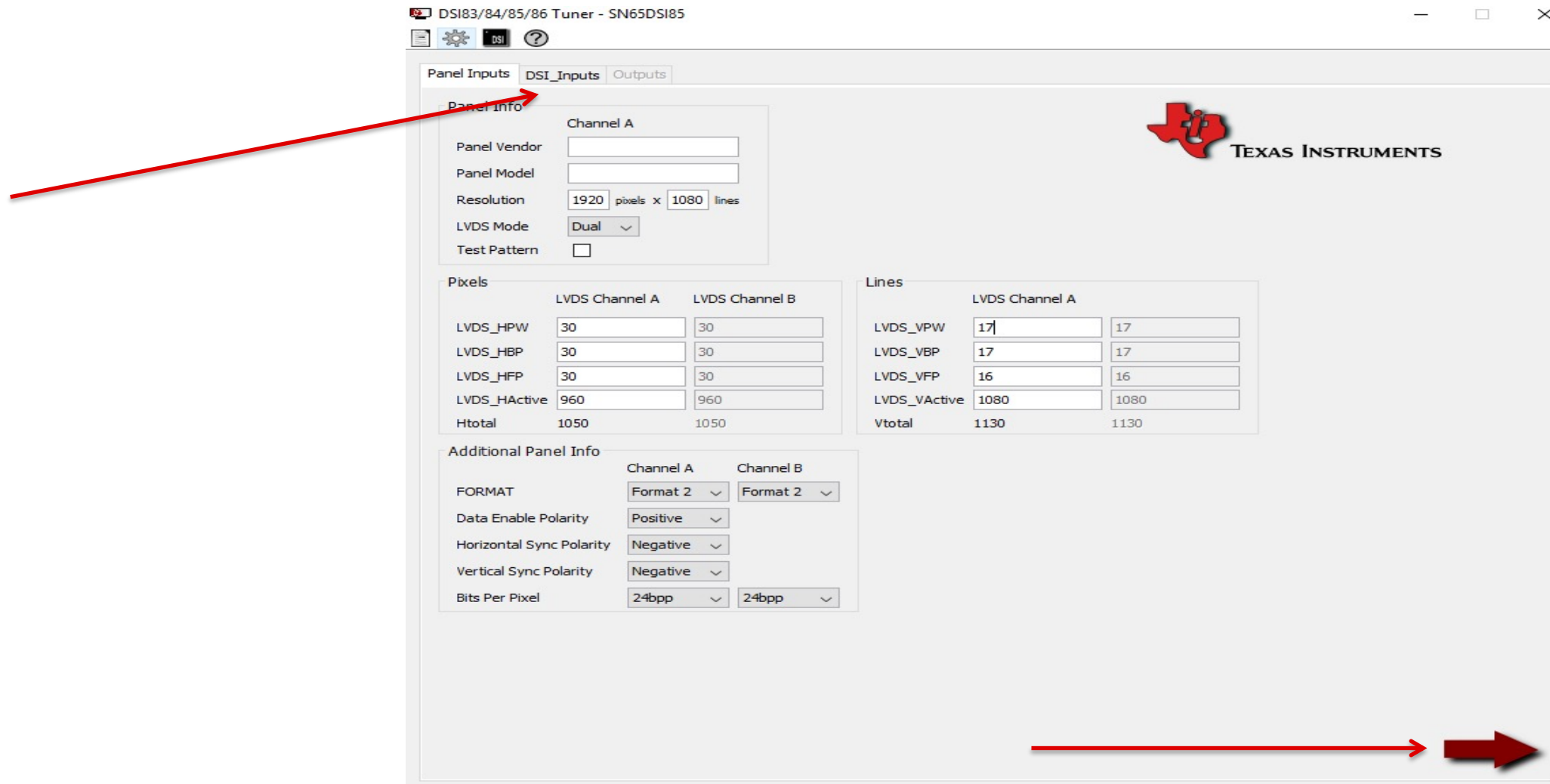
TEXAS INSTRUMENTS

Red arrow pointing to the 'Additional Panel Info' section.

Red arrow pointing to the bottom right corner of the tool window.

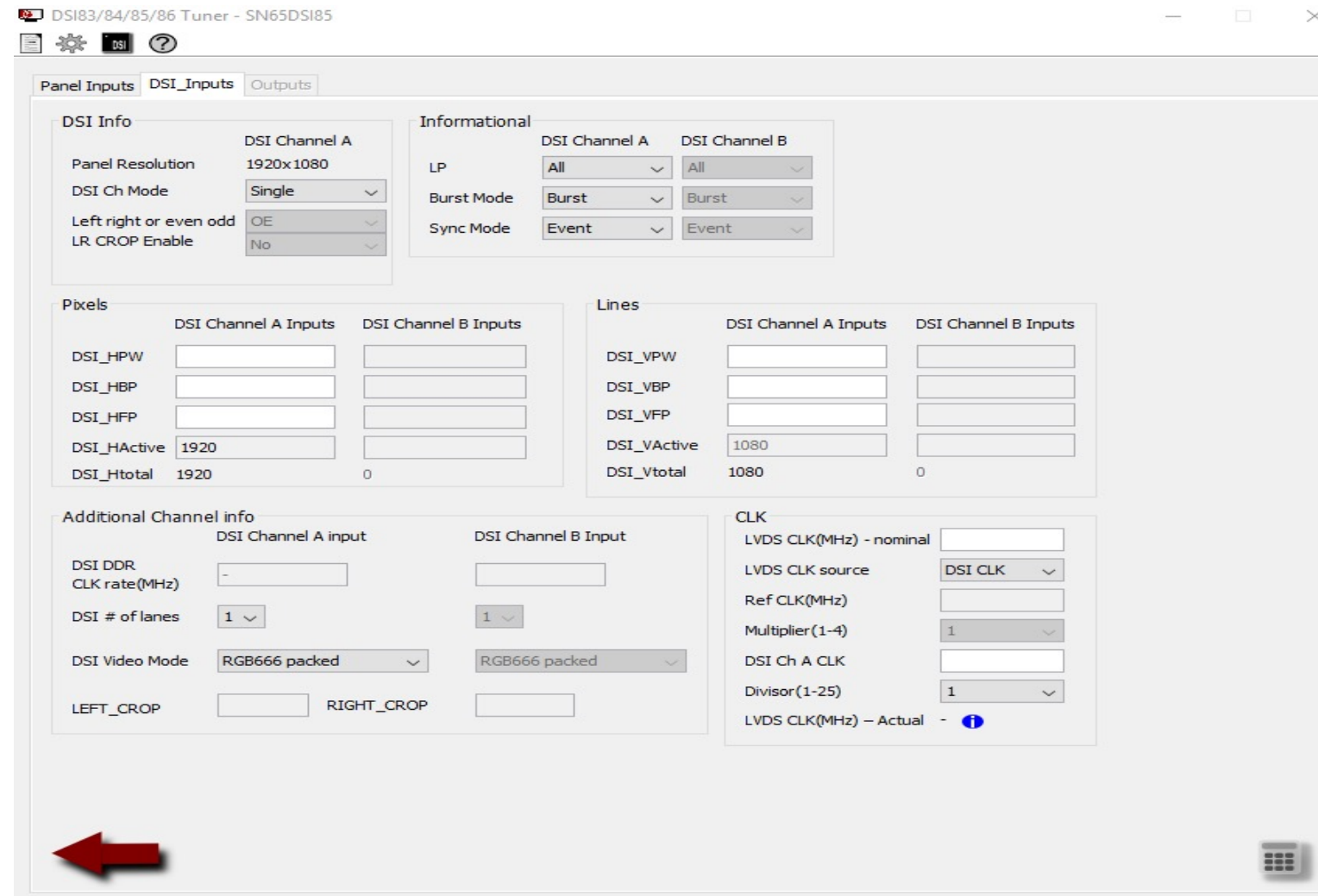
Dual to dual

- Switch to “DSI_Inputs” window by either clicking the tab or clicking the arrow:



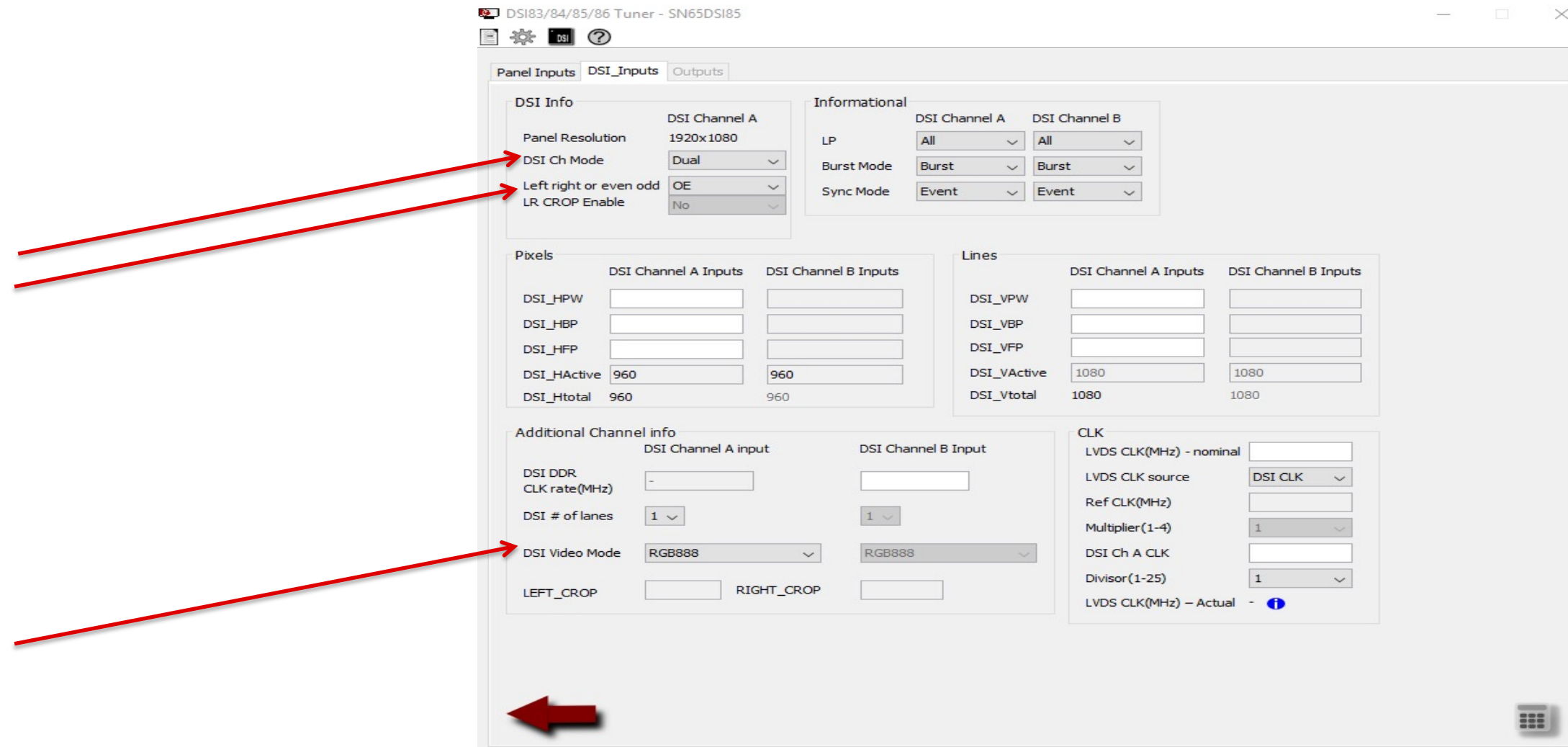
Dual to dual

- The inputs to this window mainly depend on the DSI source
- The parameters entered **must** match the actual DSI parameters transmitted by the DSI source



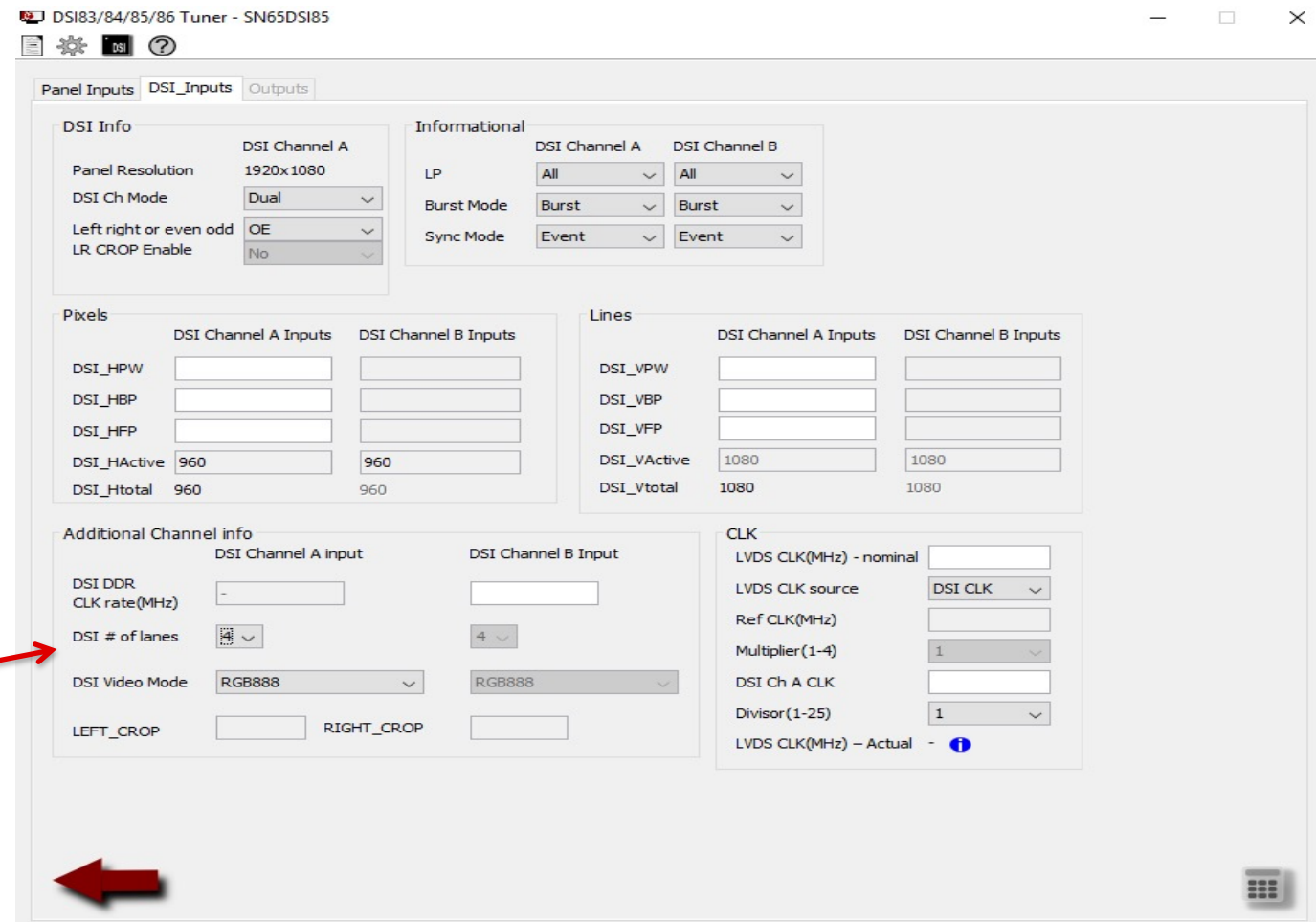
Dual to dual

- Select “Dual” as the “DSI Ch Mode”
- Since the panel is 24bpp, select “RGB888” as the DSI Video Mode



Dual to dual

- The “DSI # of lanes” depends on the required throughput to meet the panel resolution
- Each lane can support up to 1 Gbps



Dual to dual

- Enter the pixel/line information. Typically this will match the panel inputs:

The screenshot shows the configuration interface for a DSI83/84/85/86 Tuner. The window title is "DSI83/84/85/86 Tuner - SN65DSI85". The interface is divided into several sections:

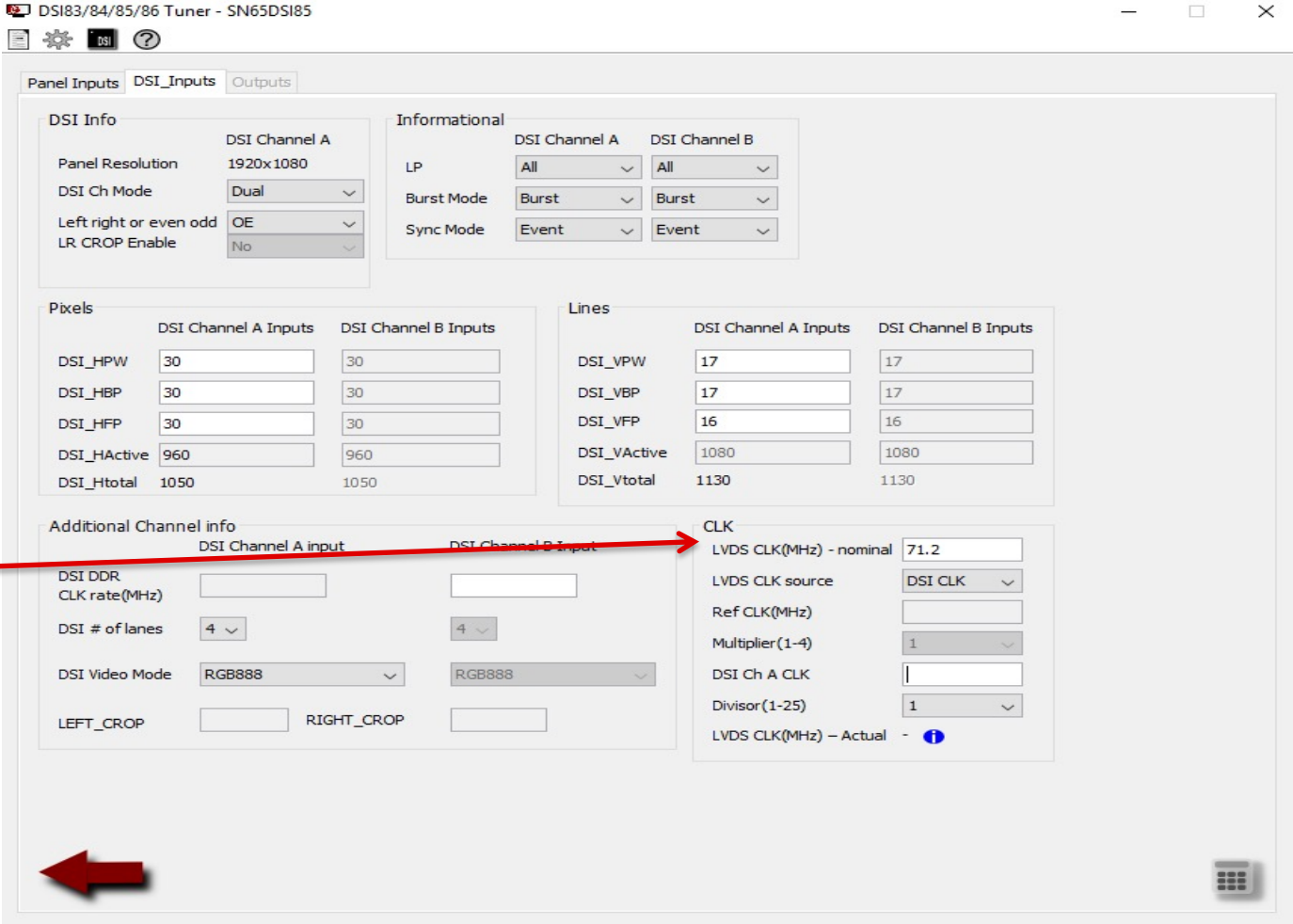
- Panel Inputs:** Includes tabs for "Panel Inputs", "DSI_Inputs", and "Outputs".
- DSI Info:** Shows "DSI Channel A" settings: Panel Resolution (1920x1080), DSI Ch Mode (Dual), Left right or even odd (OE), and LR CROP Enable (No).
- Informational:** Shows settings for both DSI Channel A and B: LP (All), Burst Mode (Burst), and Sync Mode (Event).
- Pixels:** A table with columns for "DSI Channel A Inputs" and "DSI Channel B Inputs". Values include DSI_HPW (30), DSI_HBP (30), DSI_HFP (30), DSI_HActive (960), and DSI_Htotal (1050).
- Lines:** A table with columns for "DSI Channel A Inputs" and "DSI Channel B Inputs". Values include DSI_VPW (17), DSI_VBP (17), DSI_VFP (16), DSI_VActive (1080), and DSI_Vtotal (1130).
- Additional Channel info:** Shows settings for "DSI Channel A input" and "DSI Channel B Input": DSI DDR CLK rate (MHz), DSI # of lanes (4), DSI Video Mode (RGB888), and LEFT_CROP / RIGHT_CROP.
- CLK:** Shows clock settings: LVDS CLK(MHz) - nominal, LVDS CLK source (DSI CLK), Ref CLK(MHz), Multiplier (1-4) (1), DSI Ch A CLK, Divisor (1-25) (1), and LVDS CLK(MHz) - Actual.

Red arrows point to the DSI_HPW field in the Pixels section, the DSI_VBP field in the Lines section, and the bottom-left corner of the window.

Dual to dual

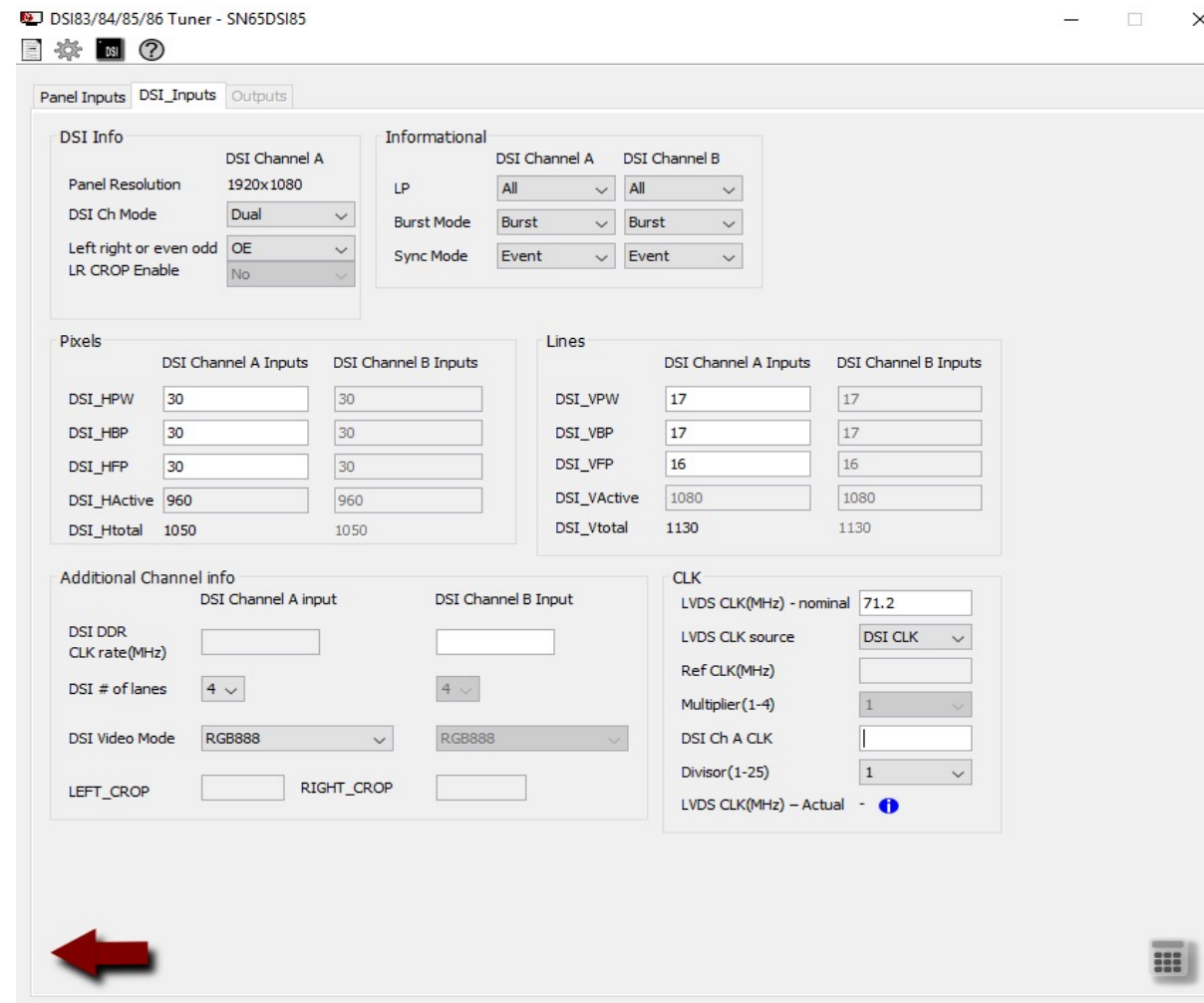
- Enter the “LVDS CLK(MHz)” – nominal value from the frequency specified in the panel datasheet
- The LVDS CLK range for the SN65DSI83/84/85 is 25 to 154MHz, so make sure you’re within this range

Signal	Item	Symbol	Min	Typ	Max	Unit
Vertical Section	Period	Tv	1092	1130	1818	Th
	Active	Tdisp(v)	1080	1080	1080	Th
	Blanking	Tblk(v)	12	50	738	Th
Horizontal Section	Period	Th	1034	1050	1100	Tclk
	Active	Tdisp(h)	960	960	960	Tclk
	Blanking	Tblk(h)	74	90	140	Tclk
Clock	Period	Tclk	10.6	14.0	17.7	Ns
	Frequency	Freq	56.5	71.2	94	MHz
Frame rate	Frame rate	VFreq	50	60	76	Hz
Hsync Frequency	Hsync Frequency	HFreq	55	68	91	KHz



Dual to dual

- The LVDS CLK source can be derived from either the DSI CLK or an external reference clock



Dual to dual

- Assume the DSI CLK will be used as the LVDS CLK source. To calculate the minimum required DSI CLK frequency, use the below equation:

- $$\text{Minimum DSICLK frequency} = \frac{\text{Throughput}}{2 \times \# \text{ of DSI Lanes}} = \frac{\text{LVDS CLK} \times \text{bpp}}{2 \times \# \text{ of DSI Lanes}}$$

- For this example:

- $$\text{Minimum DSICLK frequency} = \frac{71.2 \text{ MHz} \times 24 \text{ bpp}}{2 \times 4} = \frac{1708.8 \text{ Mbps}}{2 \times 4} = 214 \text{ MHz}$$

Dual to dual

- Fill out corresponding sections in tool and select the correct divisor:

DSI83/84/85/86 Tuner - SN65DSI85

Panel Inputs | DSI_Inputs | Outputs

DSI Info

DSI Channel A

Panel Resolution: 1920x1080

DSI Ch Mode: Dual

Left right or even odd: OE

LR CROP Enable: No

Informational

	DSI Channel A	DSI Channel B
LP	All	All
Burst Mode	Burst	Burst
Sync Mode	Event	Event

Pixels

	DSI Channel A Inputs	DSI Channel B Inputs
DSI_HPW	30	30
DSI_HBP	30	30
DSI_HFP	30	30
DSI_HActive	960	960
DSI_Htotal	1050	1050

Lines

	DSI Channel A Inputs	DSI Channel B Inputs
DSI_VPW	17	17
DSI_VBP	17	17
DSI_VFP	16	16
DSI_VActive	1080	1080
DSI_Vtotal	1130	1130

Additional Channel info

	DSI Channel A input	DSI Channel B Input	
DSI DDR	214	214	
DSI # of lanes	4	4	
DSI Video Mode	RGB888	RGB888	
LEFT_CROP		RIGHT_CROP	

CLK

LVDS CLK(MHz) - nominal: 71.2

LVDS CLK source: DSI CLK

Ref CLK(MHz):

Multiplier (1-4): 1

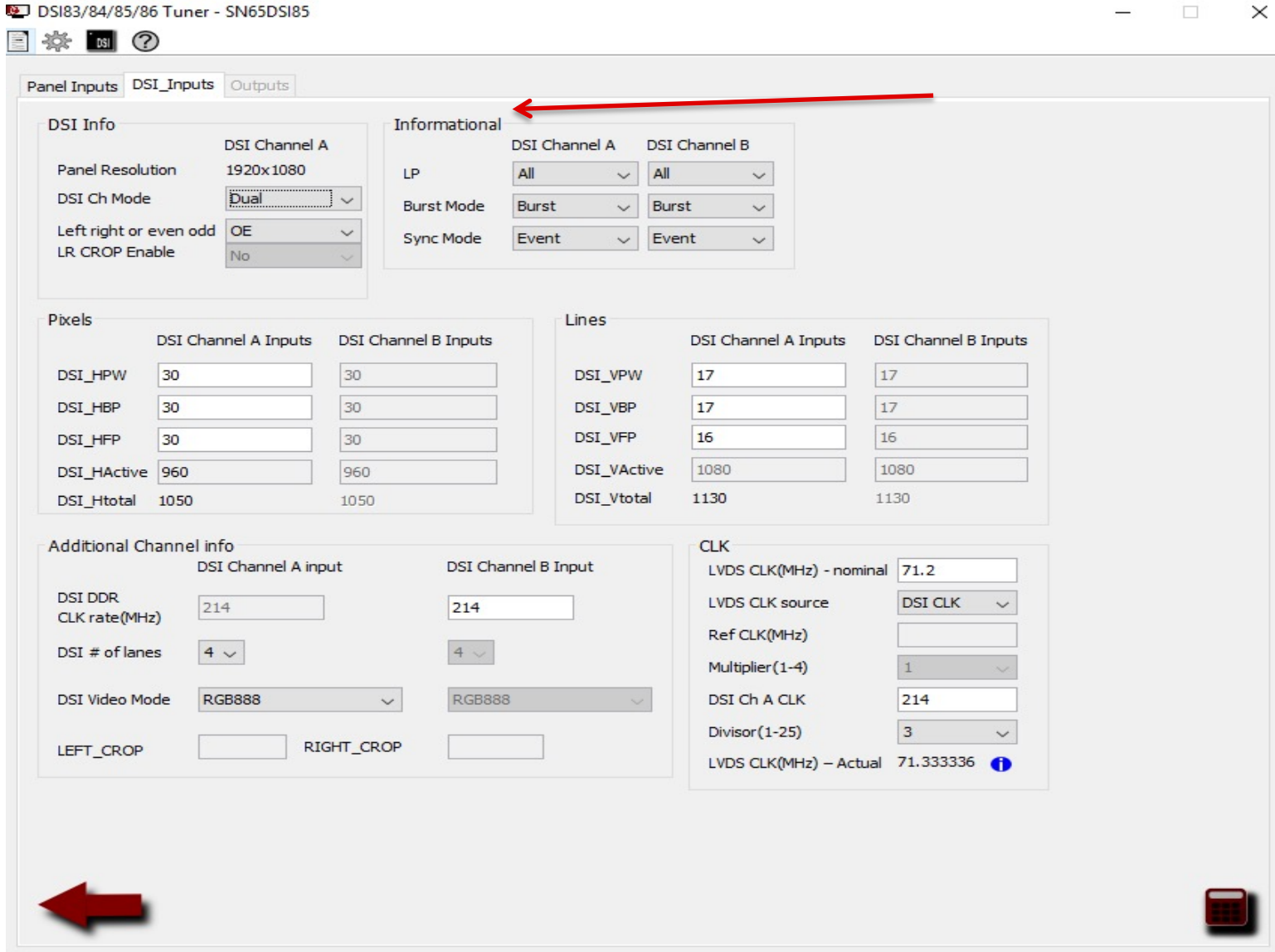
DSI Ch A CLK: 214

Divisor (1-25): 3

LVDS CLK(MHz) - Actual: 71.333336

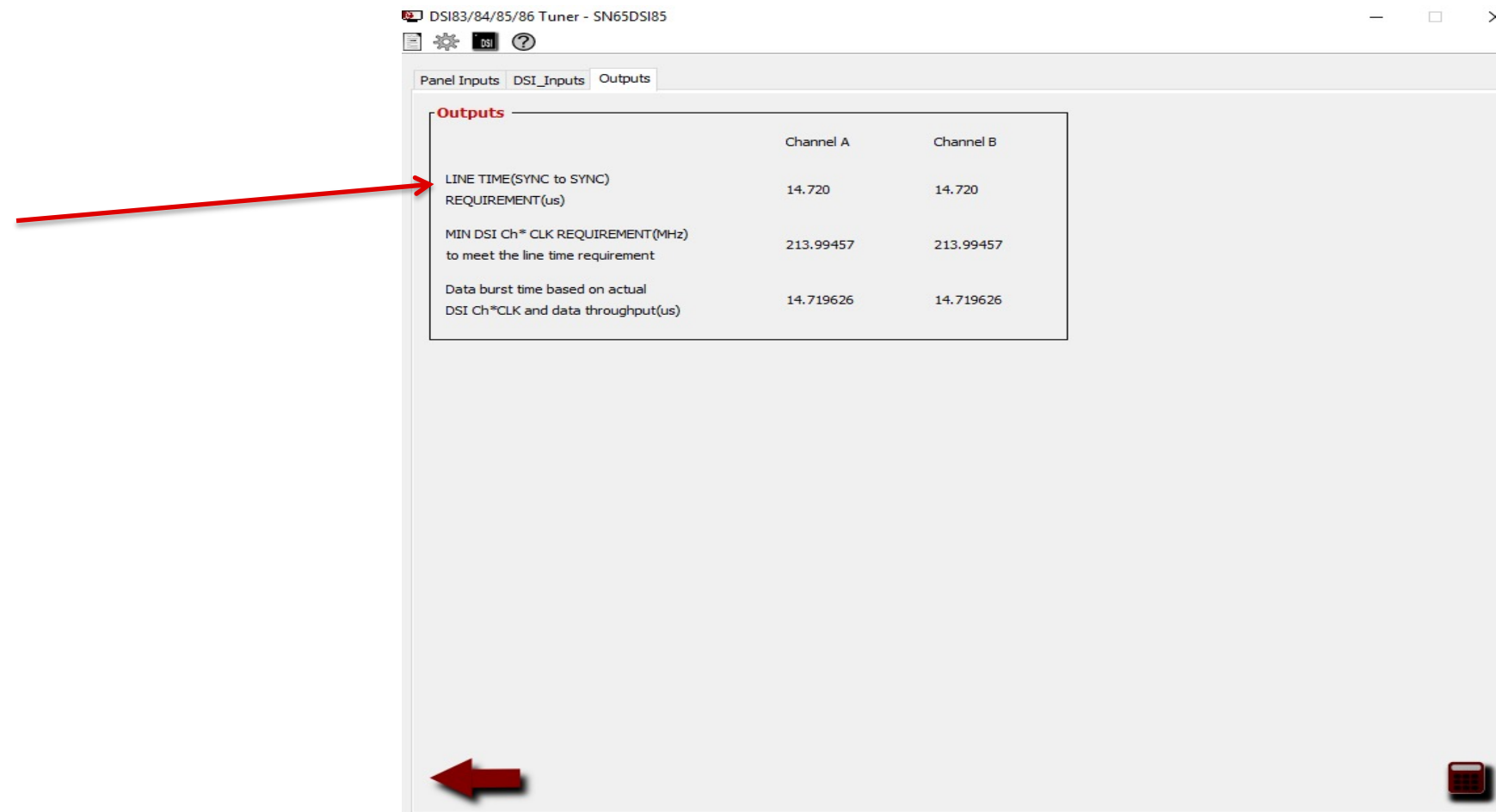
Dual to dual

- The “Informational” section depends on the DSI source




Dual to dual

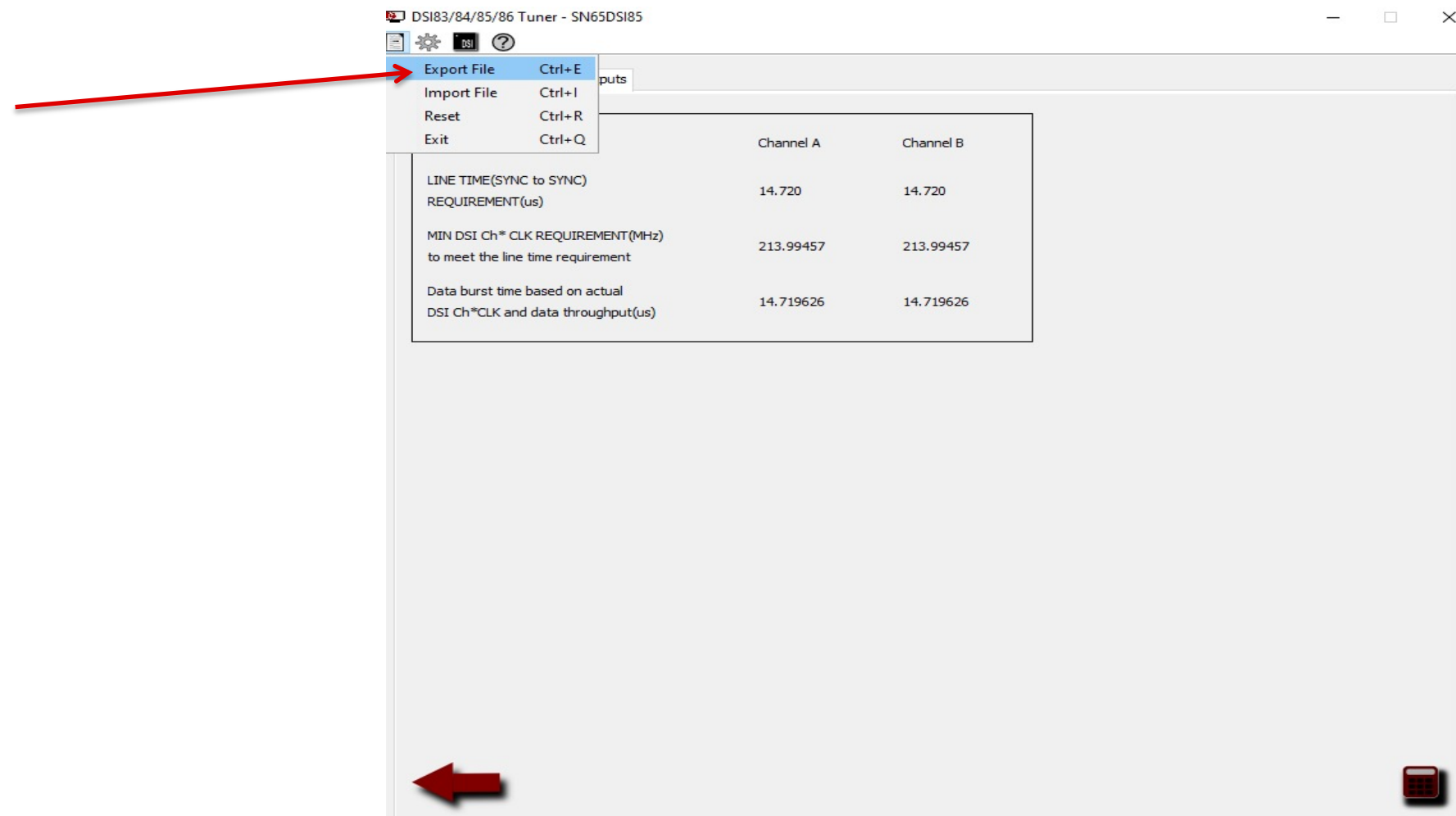
- Click the calculator icon in the lower right to get to the “Outputs” window
- Make note of the LINE TIME requirement. The line time (horizontal sync to the next horizontal) on the input is preserved when outputting onto the LVDS interface.



	Channel A	Channel B
LINE TIME(SYNC to SYNC) REQUIREMENT(us)	14.720	14.720
MIN DSI Ch* CLK REQUIREMENT(MHz) to meet the line time requirement	213.99457	213.99457
Data burst time based on actual DSI Ch*CLK and data throughput(us)	14.719626	14.719626

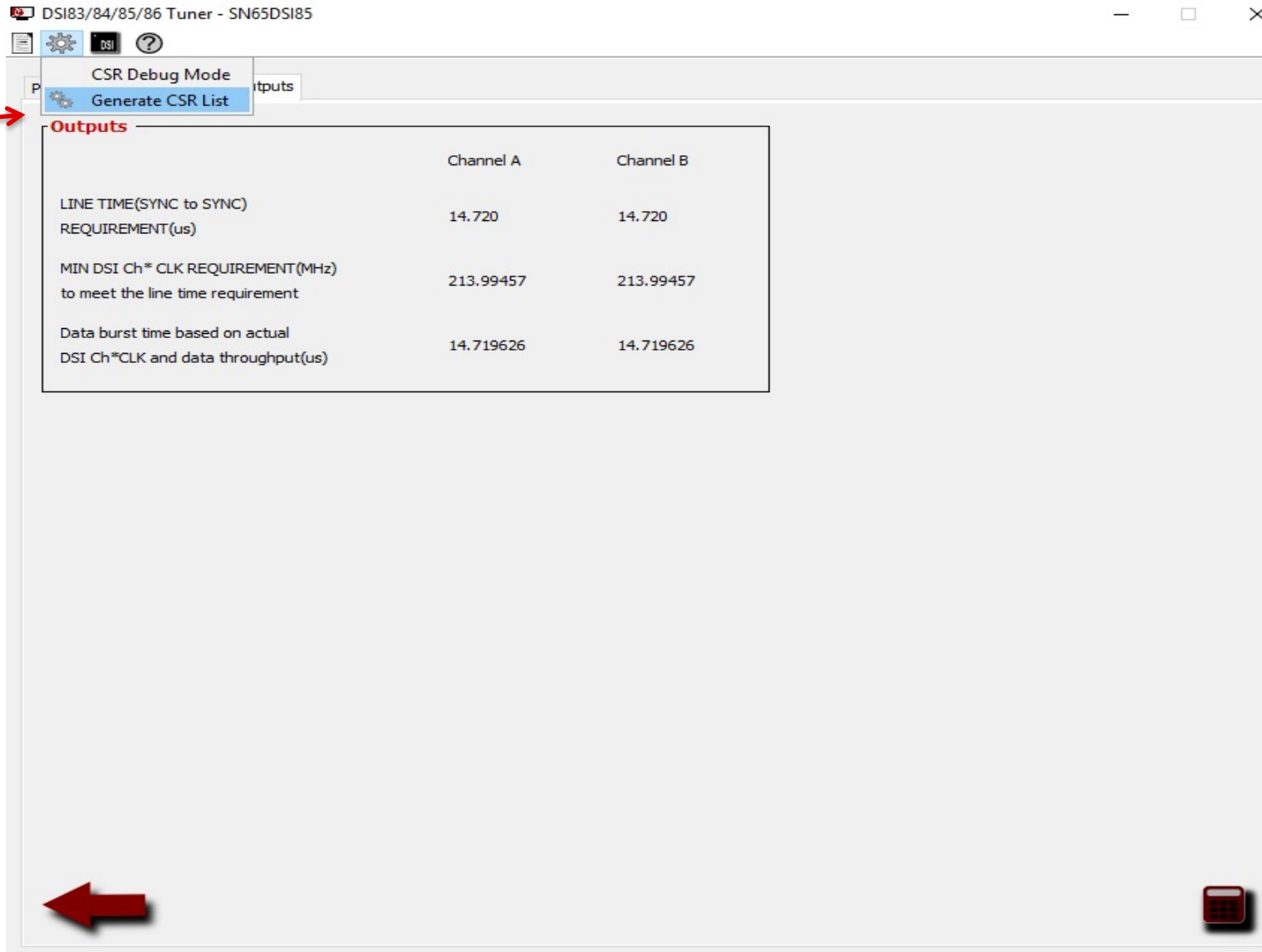
Dual to dual

- Click the  icon in the upper left to export/save the .dsi file
- You can import it later without having to re-enter all the settings



Dual to dual

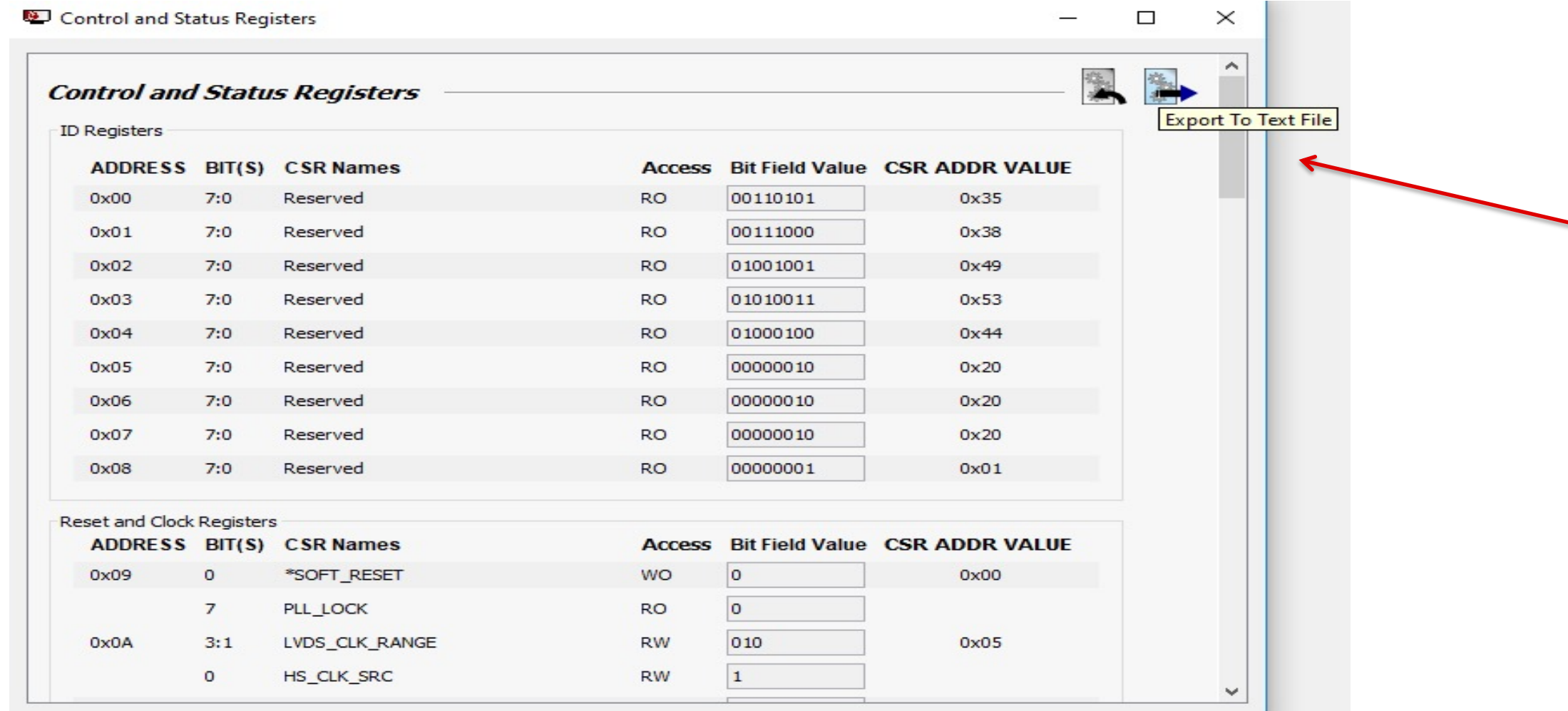
- Click the  icon in the upper left and Generate CSR list



	Channel A	Channel B
LINE TIME(SYNC to SYNC) REQUIREMENT(us)	14.720	14.720
MIN DSI Ch* CLK REQUIREMENT(MHz) to meet the line time requirement	213.99457	213.99457
Data burst time based on actual DSI Ch*CLK and data throughput(us)	14.719626	14.719626

Dual to dual

- When the “Control and Status Registers” window pops up, click the  icon to export the settings to a .txt file



The screenshot shows a software window titled "Control and Status Registers". It contains two tables of registers. The first table, "ID Registers", lists registers from 0x00 to 0x08, all with bit ranges 7:0 and access type RO. The second table, "Reset and Clock Registers", lists registers 0x09, 0x0A, and 0x0B with various bit ranges and access types. In the top right corner of the window, there is an "Export To Text File" button with a right-pointing arrow icon. A red arrow points to this button.


ADDRESS	BIT(S)	CSR Names	Access	Bit Field Value	CSR ADDR VALUE
0x00	7:0	Reserved	RO	00110101	0x35
0x01	7:0	Reserved	RO	00111000	0x38
0x02	7:0	Reserved	RO	01001001	0x49
0x03	7:0	Reserved	RO	01010011	0x53
0x04	7:0	Reserved	RO	01000100	0x44
0x05	7:0	Reserved	RO	00000010	0x20
0x06	7:0	Reserved	RO	00000010	0x20
0x07	7:0	Reserved	RO	00000010	0x20
0x08	7:0	Reserved	RO	00000001	0x01

ADDRESS	BIT(S)	CSR Names	Access	Bit Field Value	CSR ADDR VALUE
0x09	0	*SOFT_RESET	WO	0	0x00
	7	PLL_LOCK	RO	0	
0x0A	3:1	LVDS_CLK_RANGE	RW	010	0x05
	0	HS_CLK_SRC	RW	1	

Dual to dual

- Open up the .txt file that was just generated. The column on the left contains the I2C register addresses, and the column on the right contains the values that need to be written

```
CSR2.txt - Notepad
File Edit Format View Help
-----
// Filename : CSR2.txt
//
// (C) Copyright 2013 by Texas Instruments Incorporated.
// All rights reserved.
//
//-----
0x09          0x00
0x0A          0x05
0x0B          0x10
0x0D          0x00
0x10          0x00
0x11          0x00
0x12          0x2a
0x13          0x2a
0x18          0x6c
0x19          0x00
0x1A          0x03
0x1B          0x00
0x20          0xc0
0x21          0x03
0x22          0xc0
0x23          0x03
0x24          0x00
0x25          0x00
0x26          0x00
0x27          0x00
0x28          0x21
0x29          0x00
0x2A          0x00
0x2B          0x00
0x2C          0x1e
0x2D          0x00
0x2E          0x00
0x2F          0x00
0x30          0x11
0x31          0x00
0x32          0x00
0x33          0x00
0x34          0x1e
0x35          0x00
0x36          0x00
0x37          0x00
0x38          0x00
0x39          0x00
0x3A          0x00
0x3B          0x00
0x3C          0x00
0x3D          0x00
0x3E          0x00
```

 The PLL_EN bit and SOFT_RESET bit are not set as they need to be set per the recommended sequence defined in the datasheet

Thanks for your time!