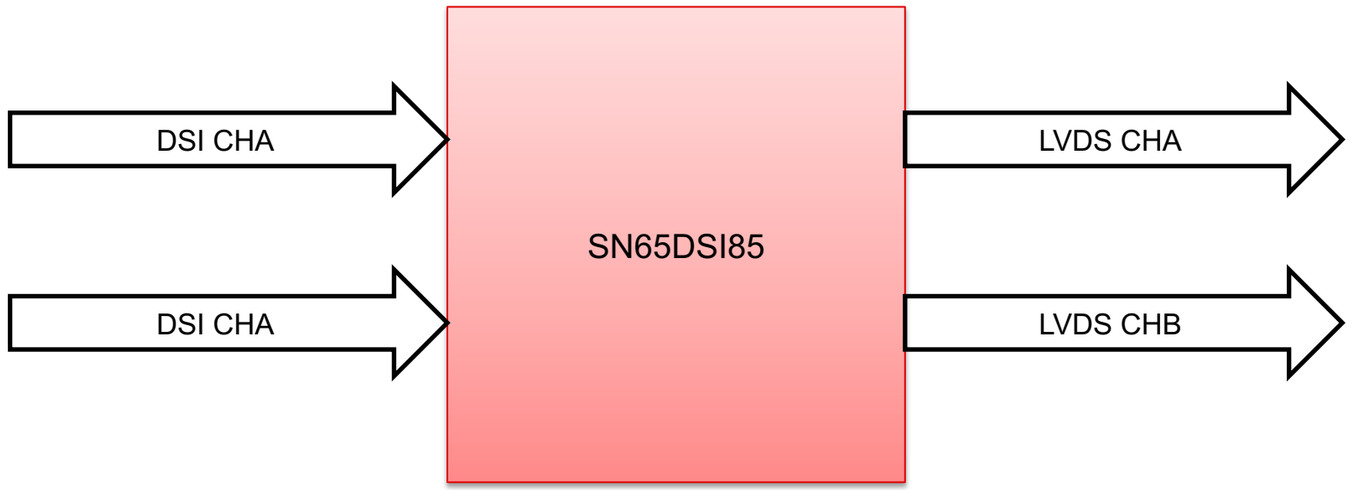
Dual DSI Input to Dual-Link LVDS

TI Precision Labs – SN65DSI83/84/85

Presented and prepared by Ikechukwu Anyiam

Dual to dual

- The SN65DSI85 is the only device that can be used for this application



Dual to dual

- From display datasheet, identify:
- Resolution:

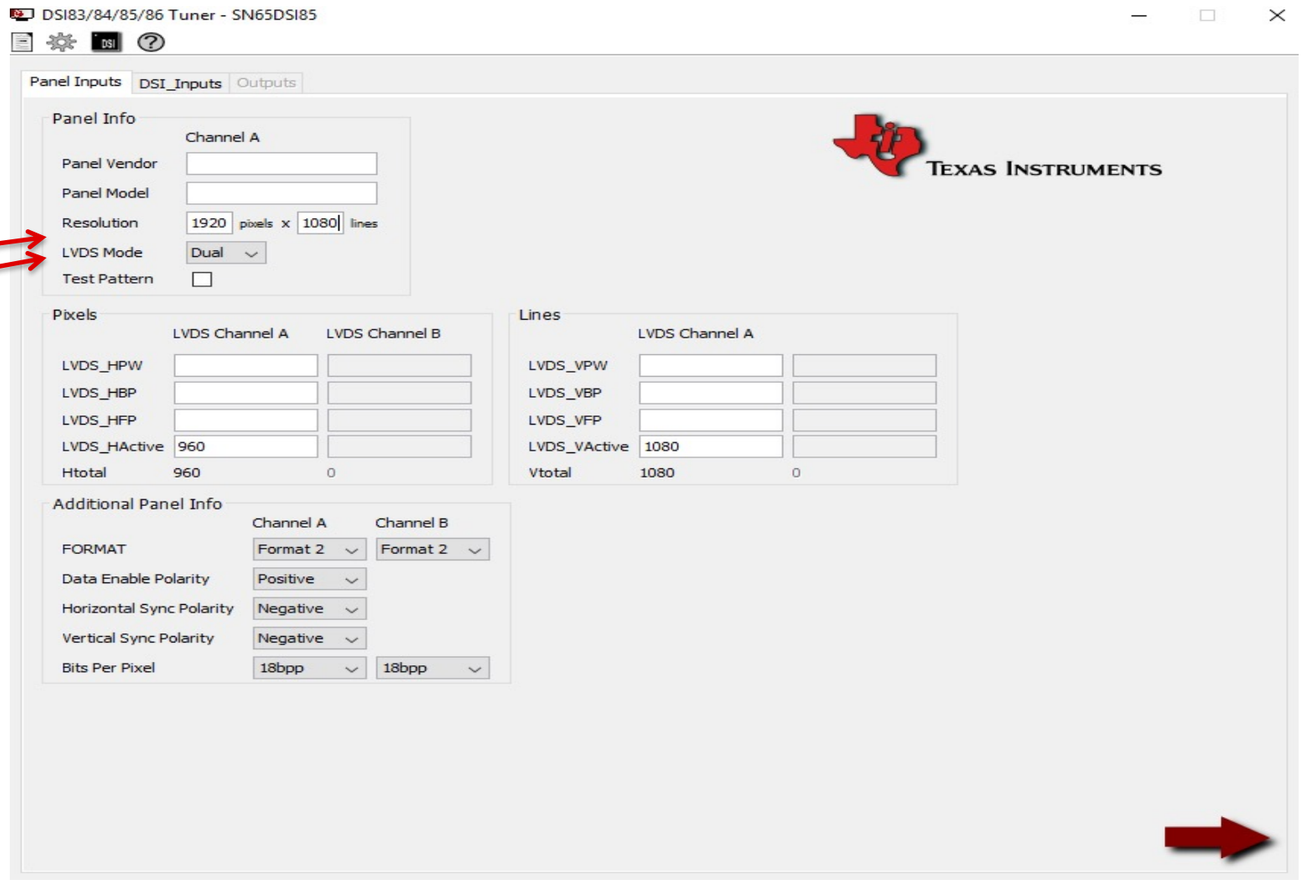
Items	Unit	Specification
Screen Diagonal	[mm]	609.7 (24.0”)
Active Area	[mm]	531.36 (H) x 298.89 (V)
Pixels H x V		1920 x 1080
Pixel Pitch	[um]	276.75 (per one triad) x276.75

- This is a 1920 x 1080 panel

Dual to dual

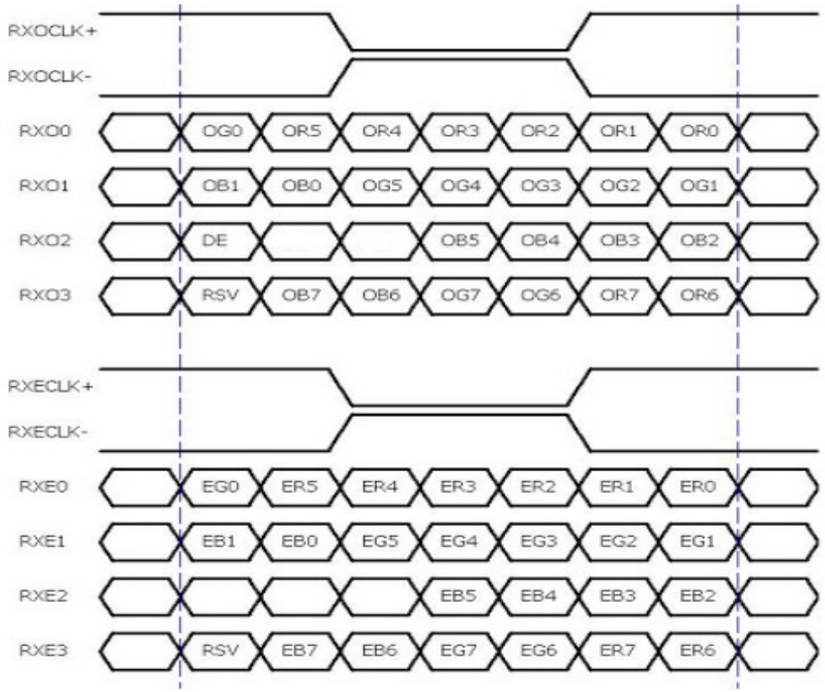
- After changing the “LVDS Mode” to “Dual”, fill in the resolution:

- Notice how the tool automatically divides “LVDS_HActive” by 2.



Dual to dual

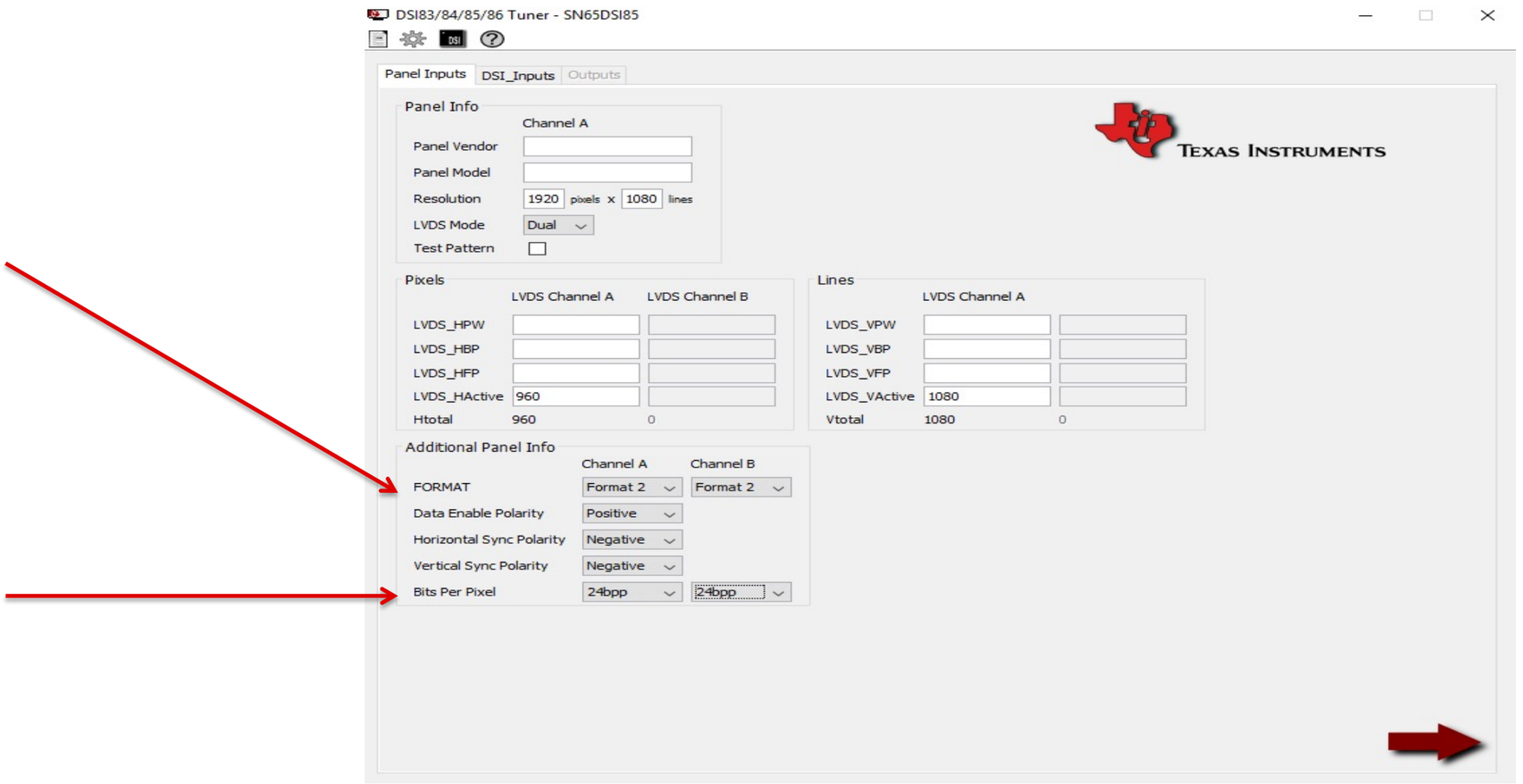
- From display datasheet, identify:
- Mapping format:



- This is Format 2 (VESA), 24bpp

Dual to dual

- Fill out corresponding section in tool:



Dual to dual

- From display datasheet, identify:
- Timing Parameters:

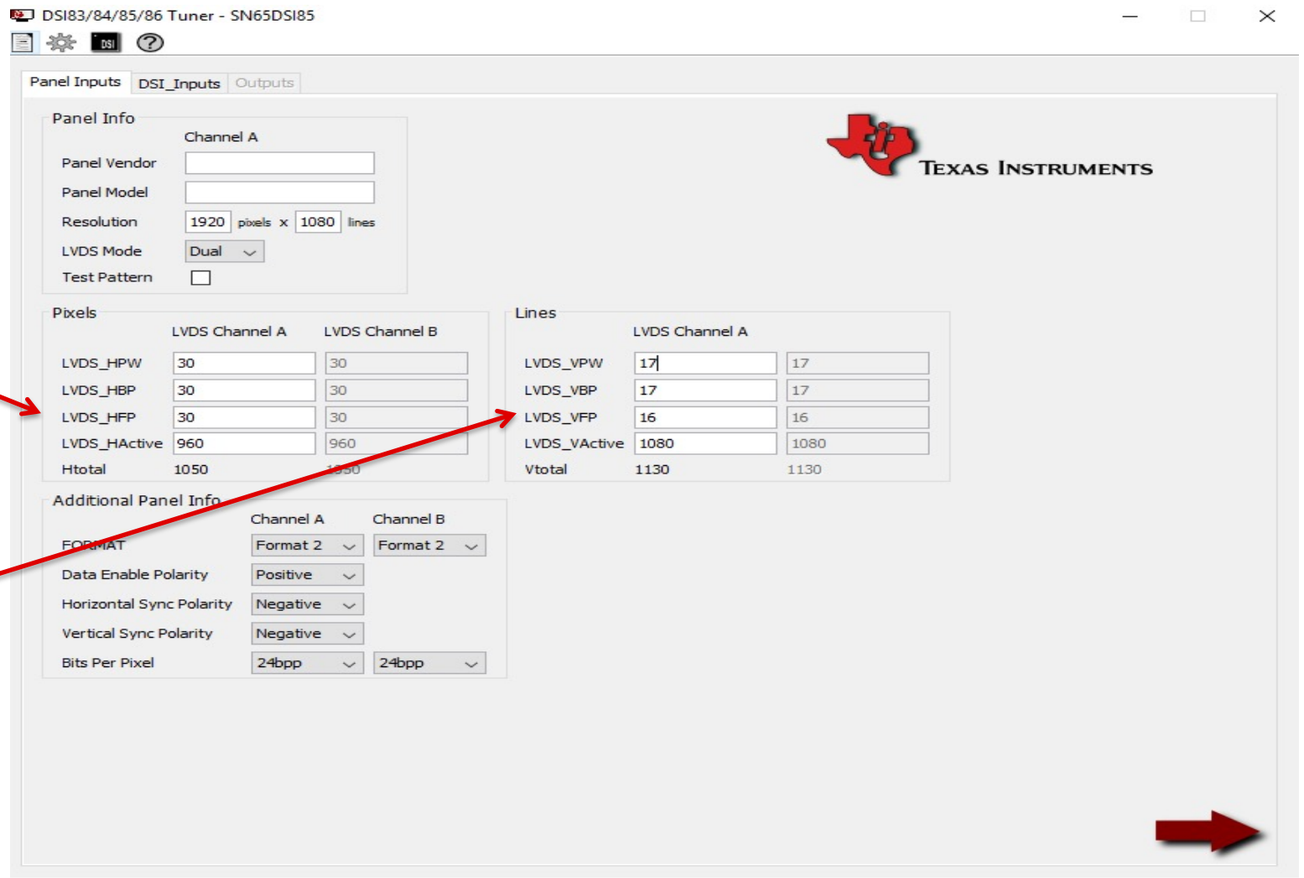
Signal	Item	Symbol	Min	Typ	Max	Unit
Vertical Section	Period	Tv	1092	1130	1818	Th
	Active	Tdisp(v)	1080	1080	1080	Th
	Blanking	Tblk(v)	12	50	738	Th
Horizontal Section	Period	Th	1034	1050	1100	Tclk
	Active	Tdisp(h)	960	960	960	Tclk
	Blanking	Tblk(h)	74	90	140	Tclk
Clock	Period	Tclk	10.6	14.0	17.7	Ns
	Frequency	Freq	56.5	71.2	94	MHz
Frame rate	Frame rate	VFreq	50	60	76	Hz
Hsync Frequency	Hsync Frequency	HFreq	55	68	91	KHz

- From this, we can see that the total vertical blanking is 50, and the total horizontal blanking is 90
  - VPW+VBP+VFP=50
  - HPW+HBP+HFP=90

Dual to dual

- Fill out corresponding section in tool:
- Horizontal blanking (90) is divided among HPW, HBP, and HFP

- Vertical blanking (50) is divided Among VPW, VBP, and VFP

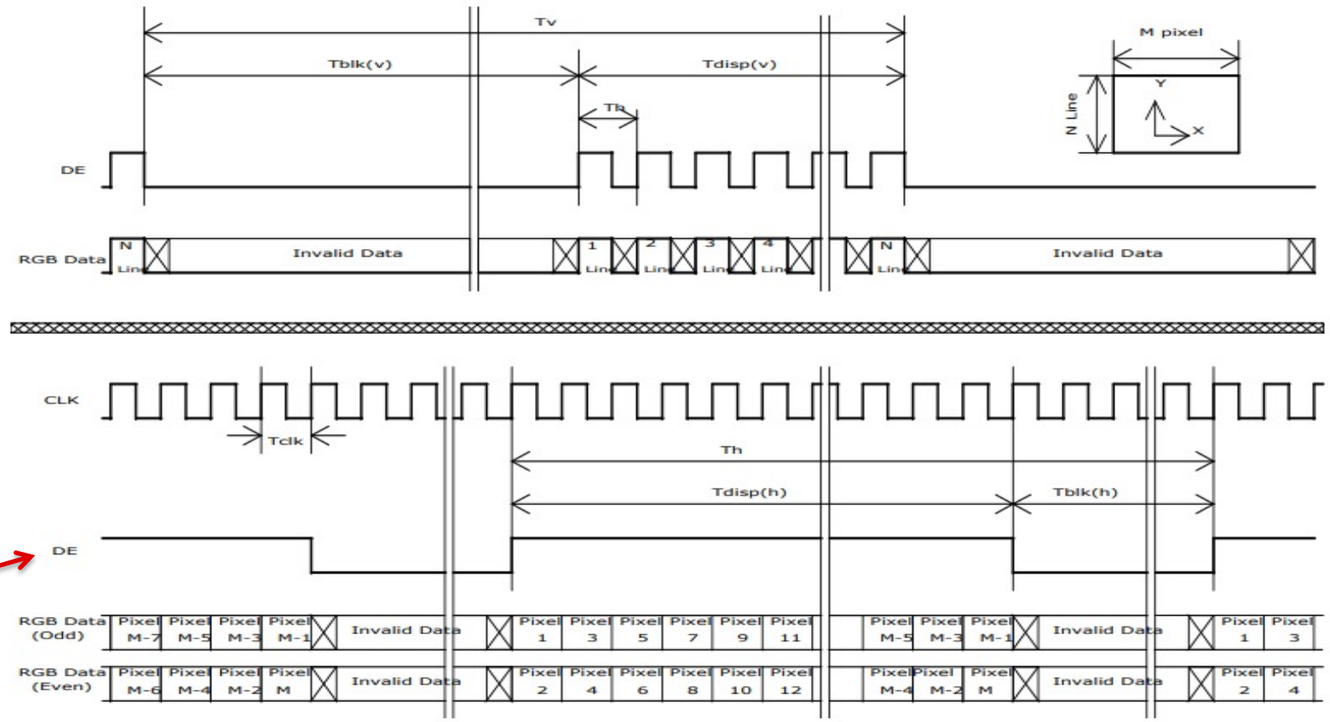


Dual to dual

- From display datasheet, identify:
- HSYNC, VSYNC, and DE polarity:

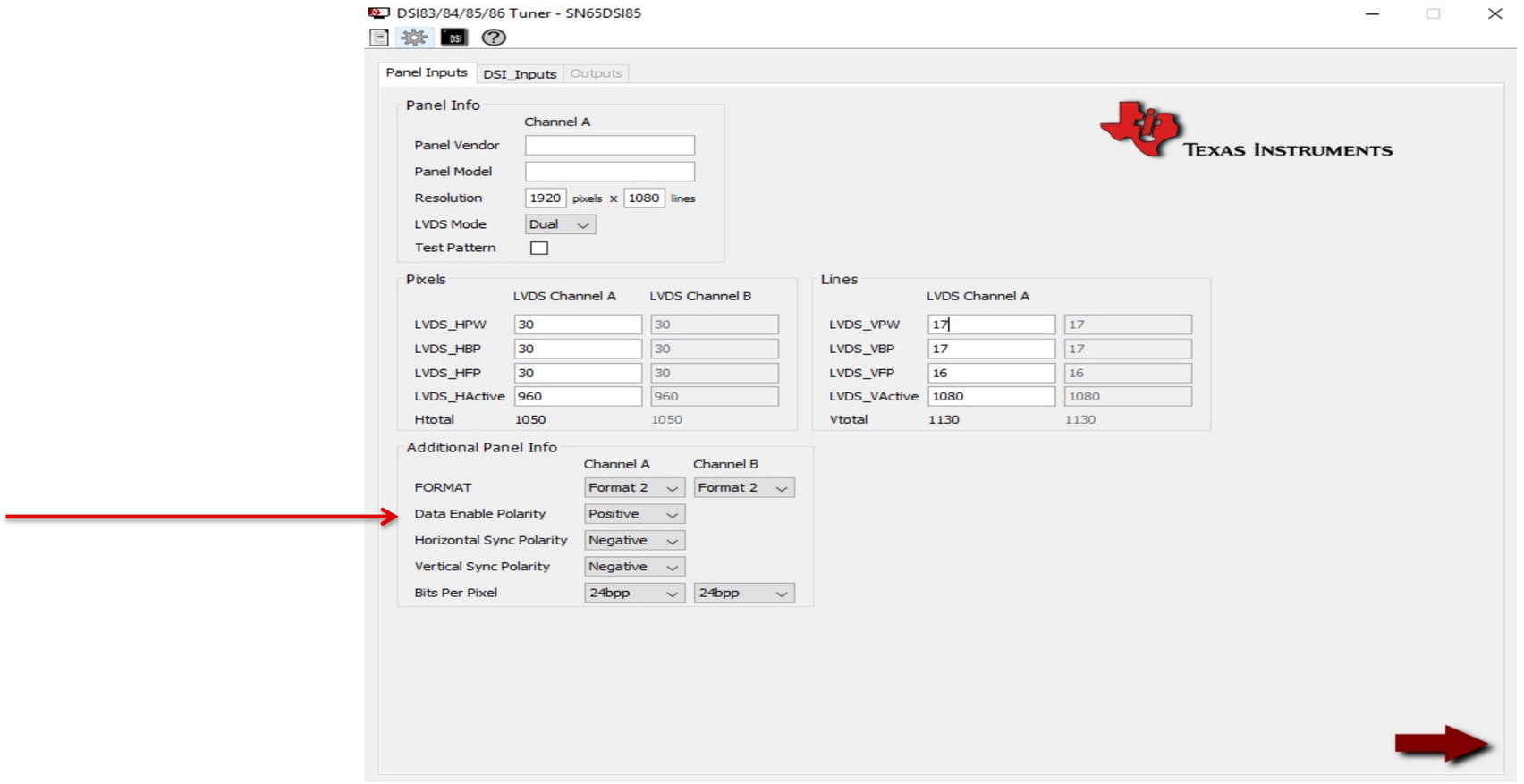
- This particular display operates in DE mode, so HSYNC/VSYNC polarity don’t matter.

- DE is positive during active display so DE polarity is positive



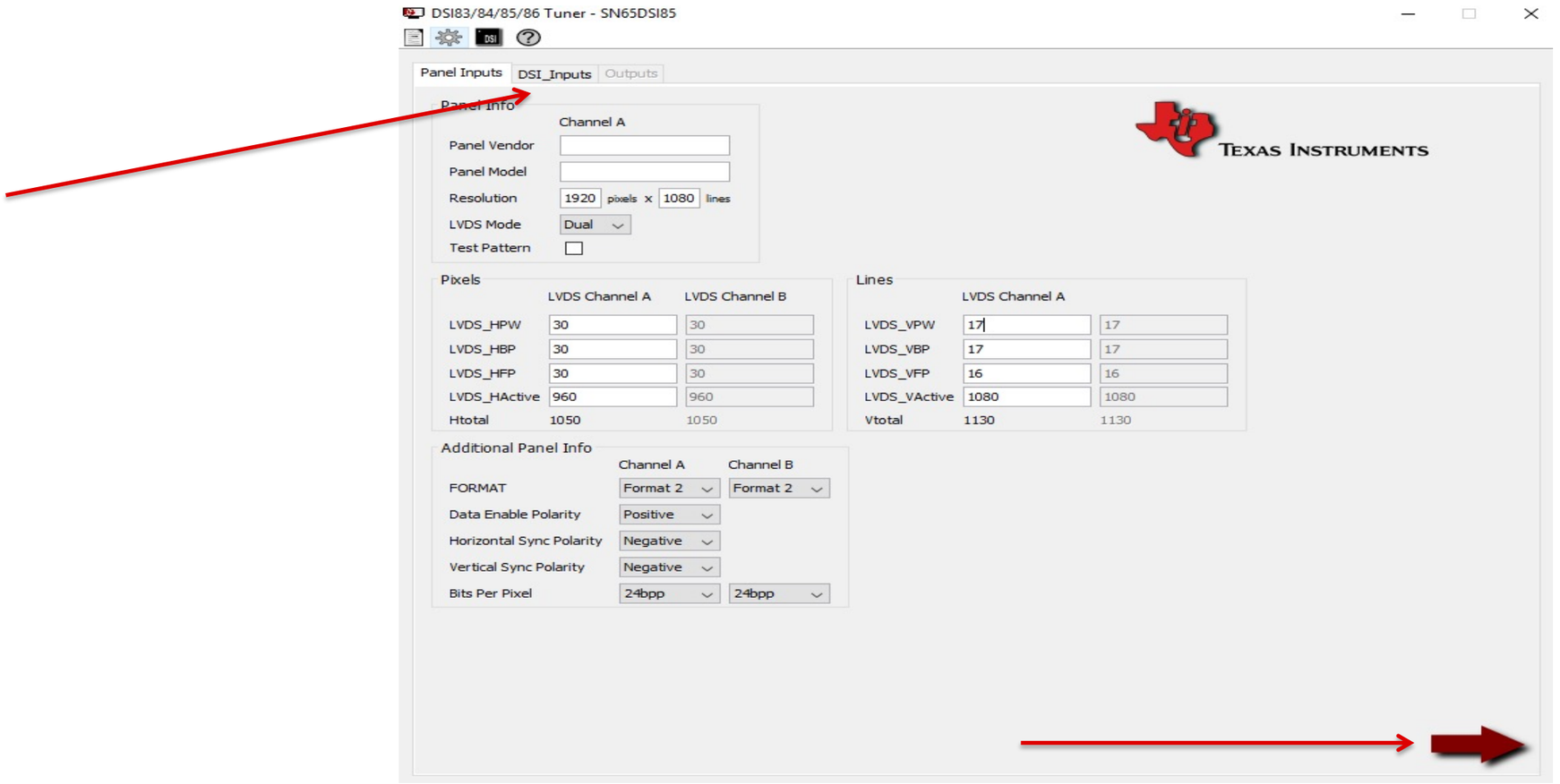
Dual to dual

- Fill out corresponding section in tool:



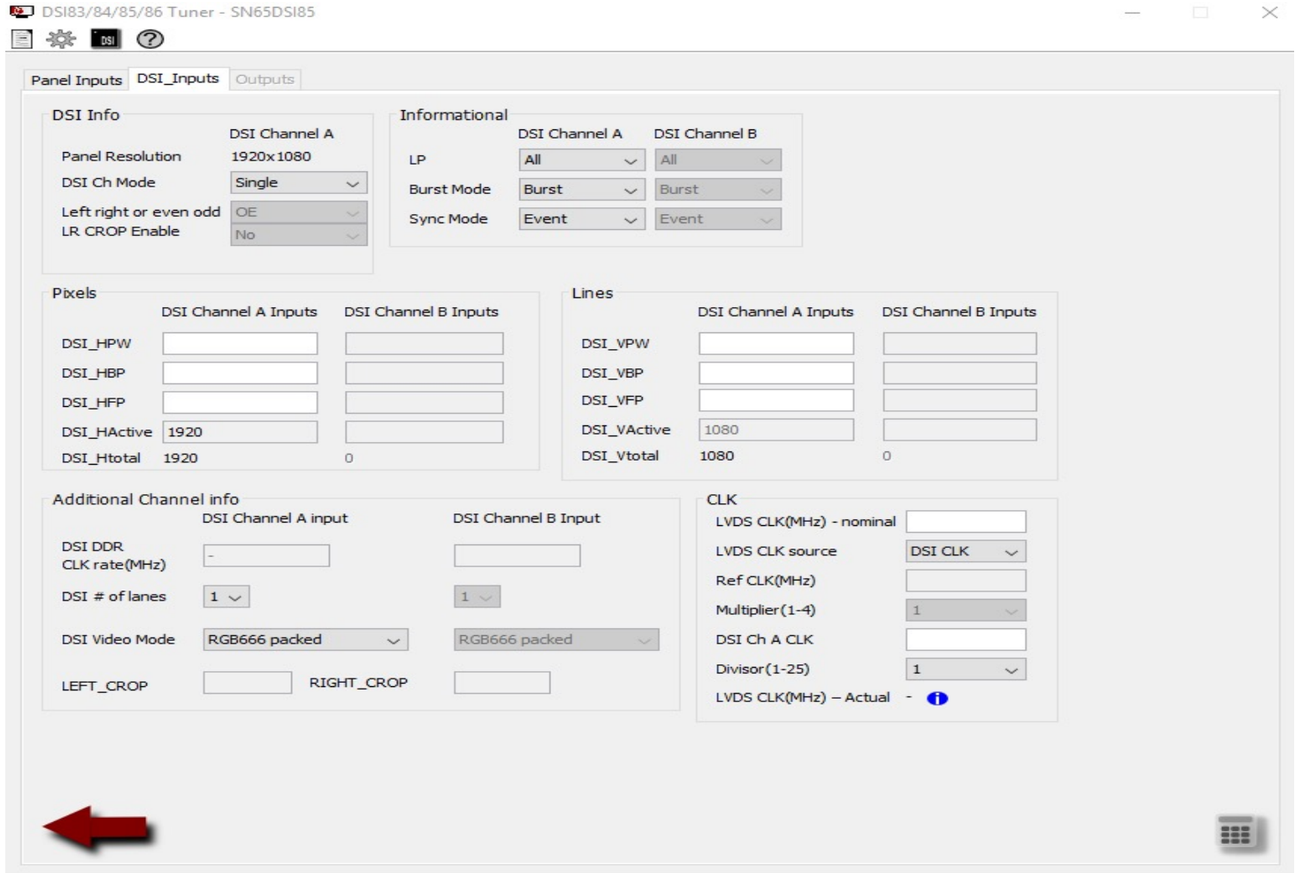
Dual to dual

- Switch to “DSI_Inputs” window by either clicking the tab or clicking the arrow:



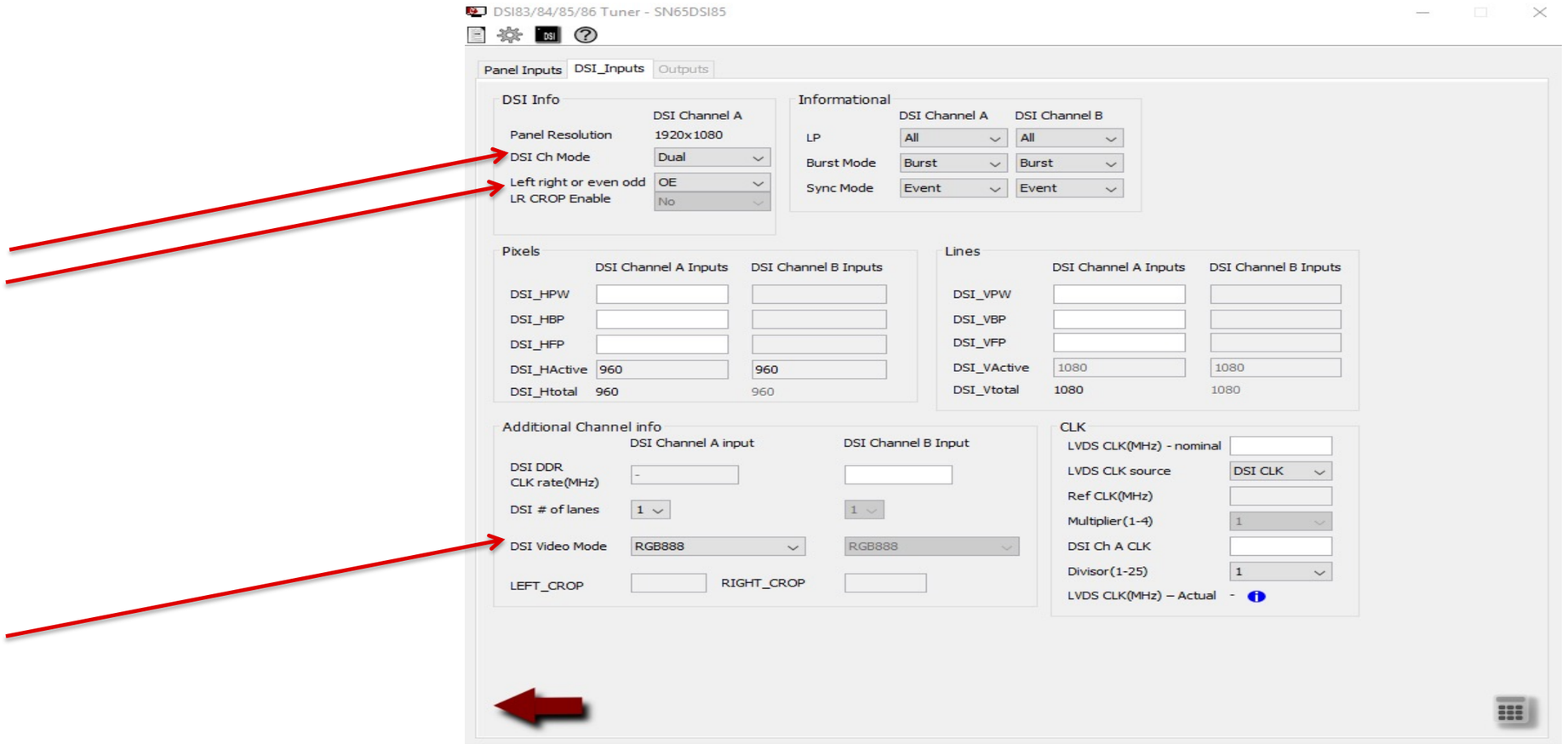
Dual to dual

- The inputs to this window mainly depend on the DSI source
- The parameters entered **must** match the actual DSI parameters transmitted by the DSI source



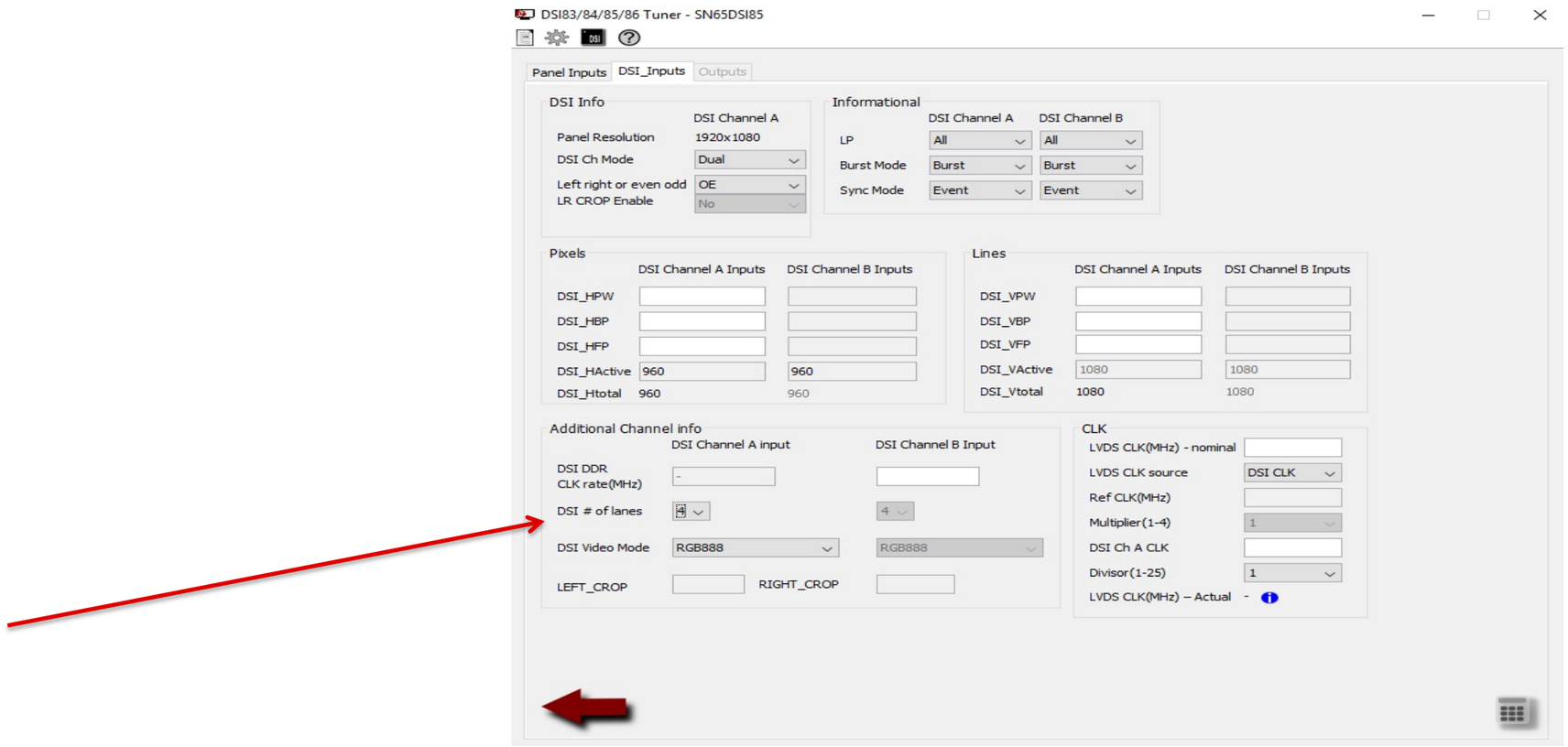
Dual to dual

- Select “Dual” as the “DSI Ch Mode”
- Since the panel is 24bpp, select “RGB888” as the DSI Video Mode



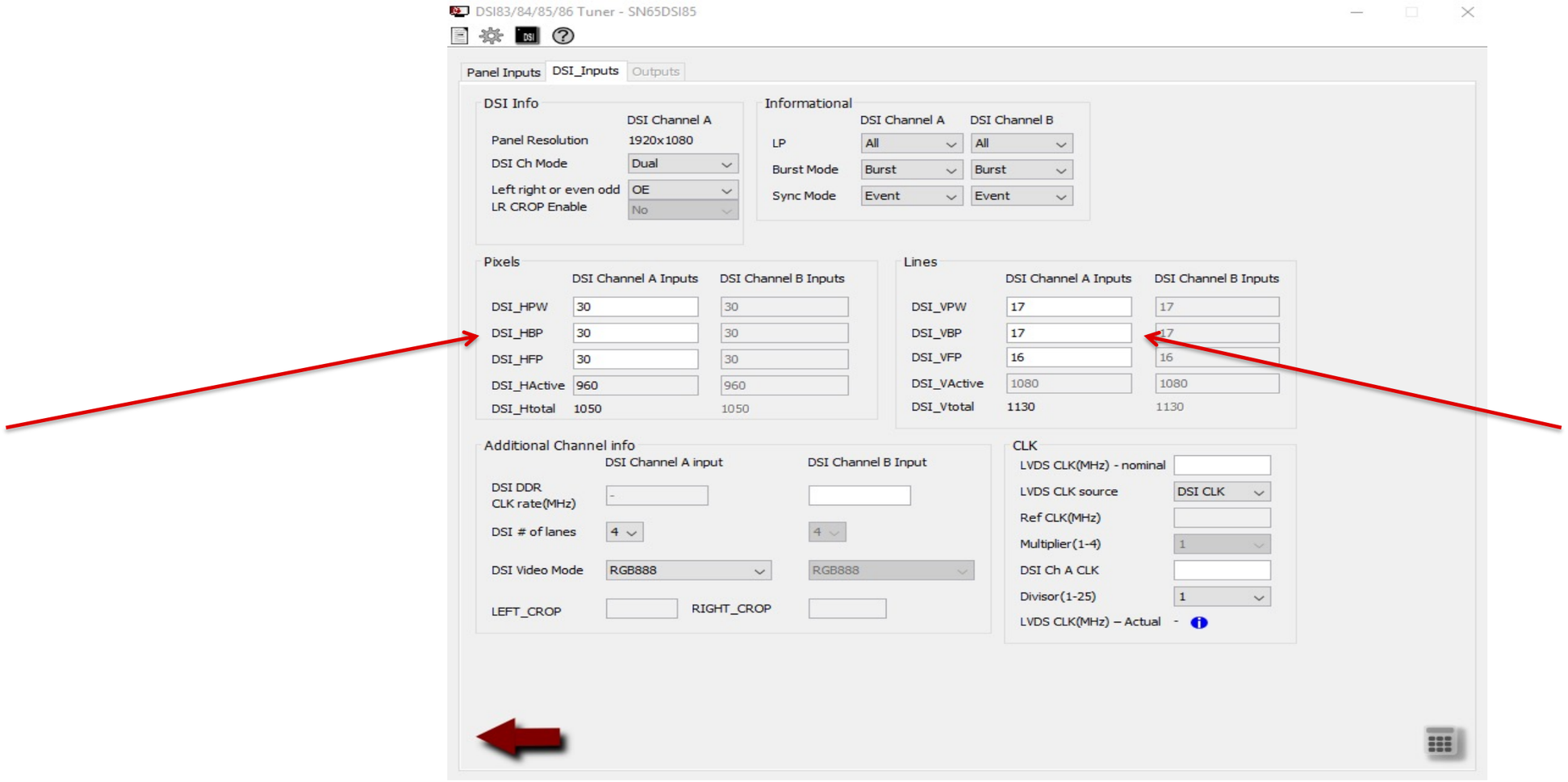
Dual to dual

- The “DSI # of lanes” depends on the required throughput to meet the panel resolution
- Each lane can support up to 1 Gbps



Dual to dual

- Enter the pixel/line information. Typically this will match the panel inputs:



Dual to dual

- Enter the “LVDS CLK(MHz)” – nominal value from the frequency specified in the panel datasheet
- The LVDS CLK range for the SN65DSI83/84/85 is 25 to 154MHz, so make sure you’re within this range

Signal	Item	Symbol	Min	Typ	Max	Unit
Vertical Section	Period	Tv	1092	1130	1818	Th
	Active	Tdisp(v)	1080	1080	1080	Th
	Blanking	Tblk(v)	12	50	738	Th
Horizontal Section	Period	Th	1034	1050	1100	Tclk
	Active	Tdisp(h)	960	960	960	Tclk
	Blanking	Tblk(h)	74	90	140	Tclk
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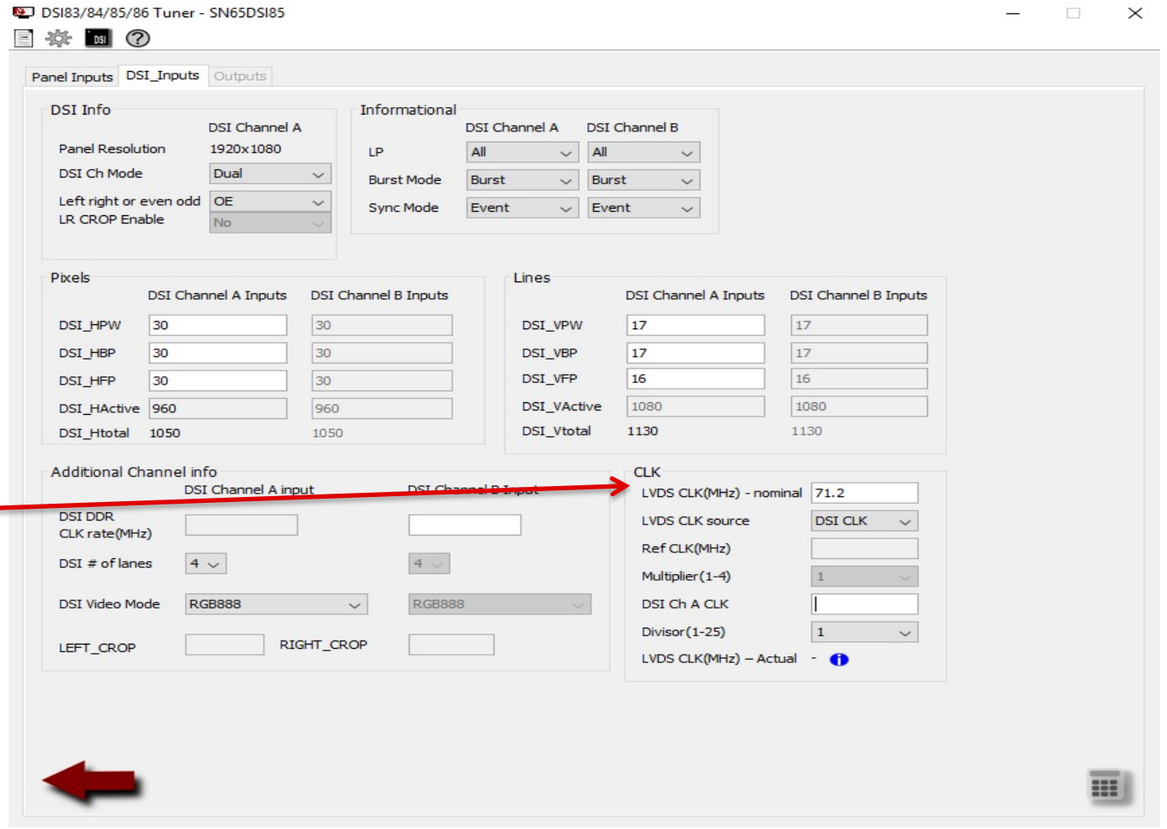
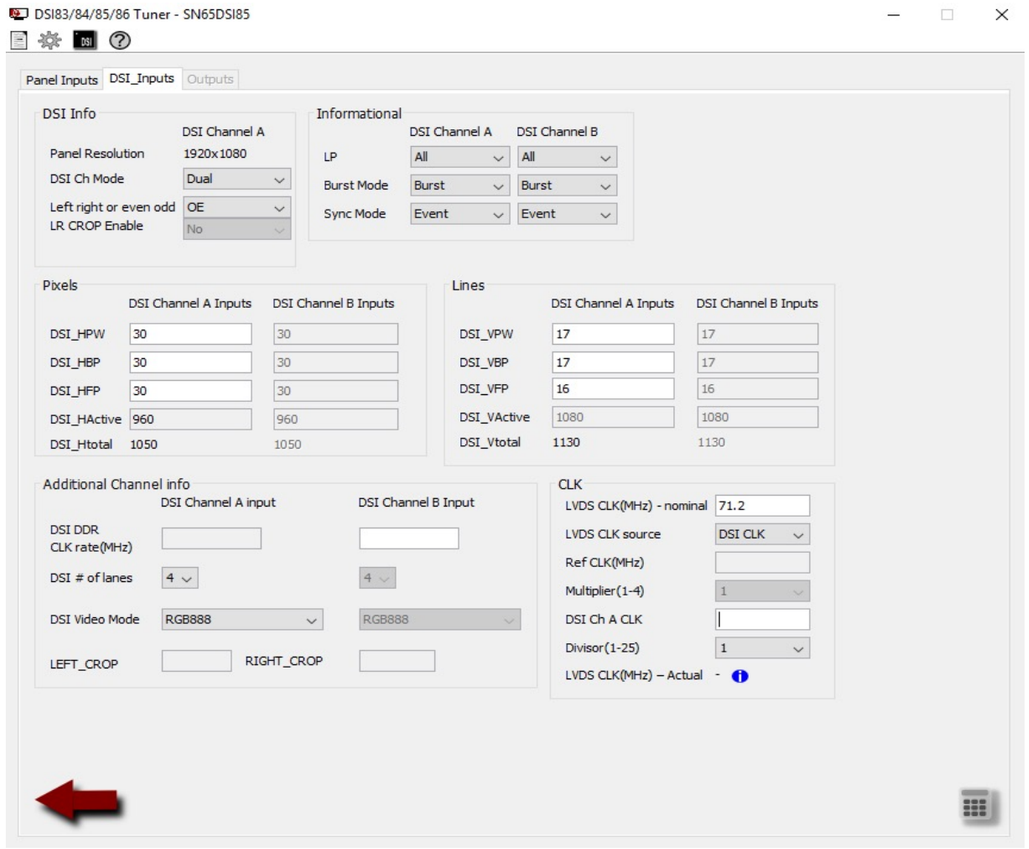
	Frequency	Freq	56.5	71.2	94	MHz
Frame rate	Frame rate	VFreq	50	60	76	Hz
Hsync Frequency	Hsync Frequency	HFreq	55	68	91	KHz



Dual to dual

- The LVDS CLK source can be derived from either the DSI CLK or an external reference clock



Dual to dual

- Assume the DSI CLK will be used as the LVDS CLK source. To calculate the minimum required DSI CLK frequency, use the below equation:

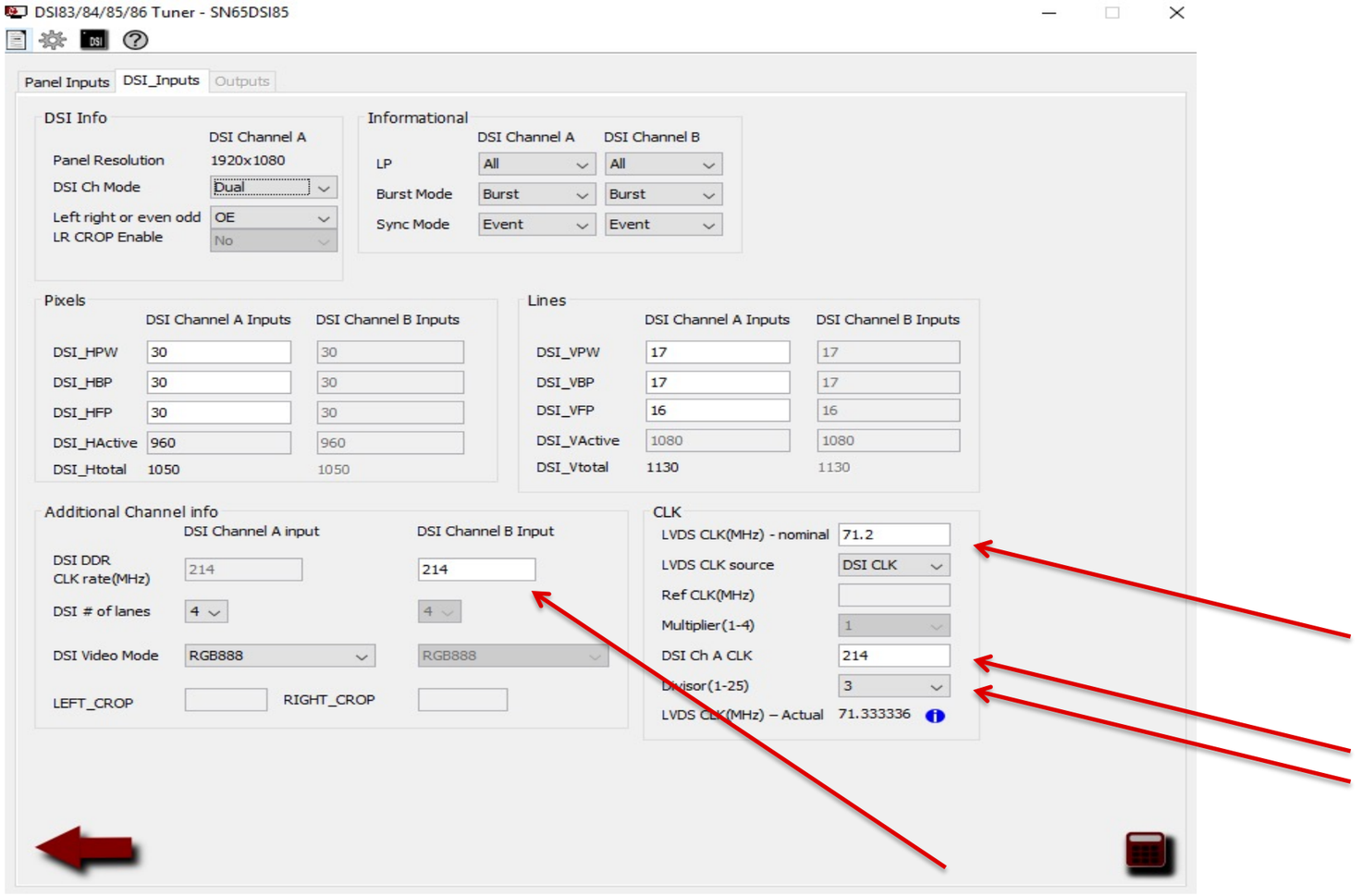
- $$Minimum\ DSICLK\ frequency = \frac{Throughput}{2 \times \#\ of DSI\ Lanes} = \frac{LVDS\ CLK \times bpp}{2 \times \#\ of\ DSI\ Lanes}$$

- For this example:

- $$Minimum\ DSICLK\ frequency = \frac{71.2\ MHz \times 24\ bpp}{2 \times 4} = \frac{1708.8\ Mbps}{2 \times 4} = 214\ MHz$$

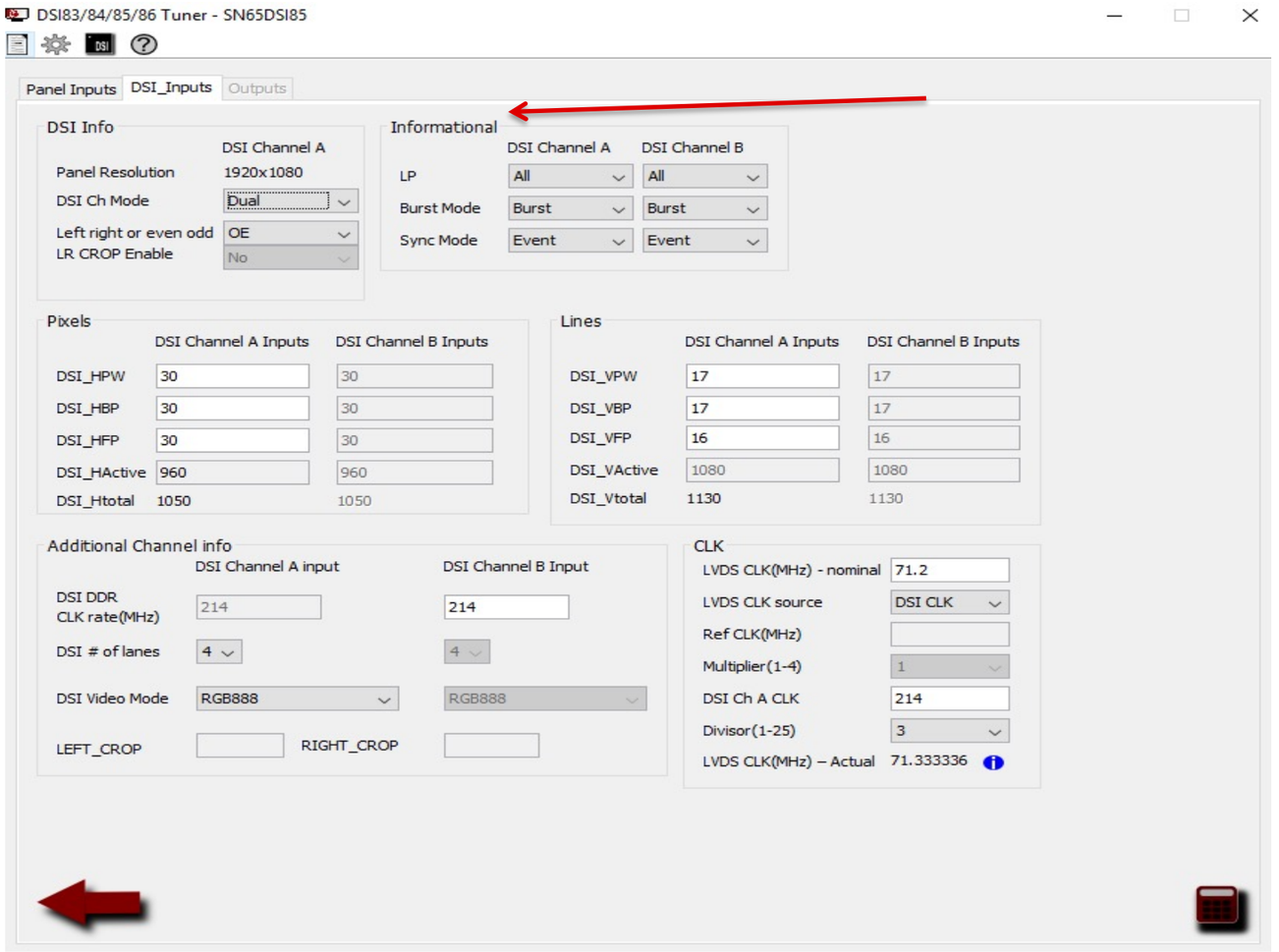
Dual to dual

- Fill out corresponding sections in tool and select the correct divisor:



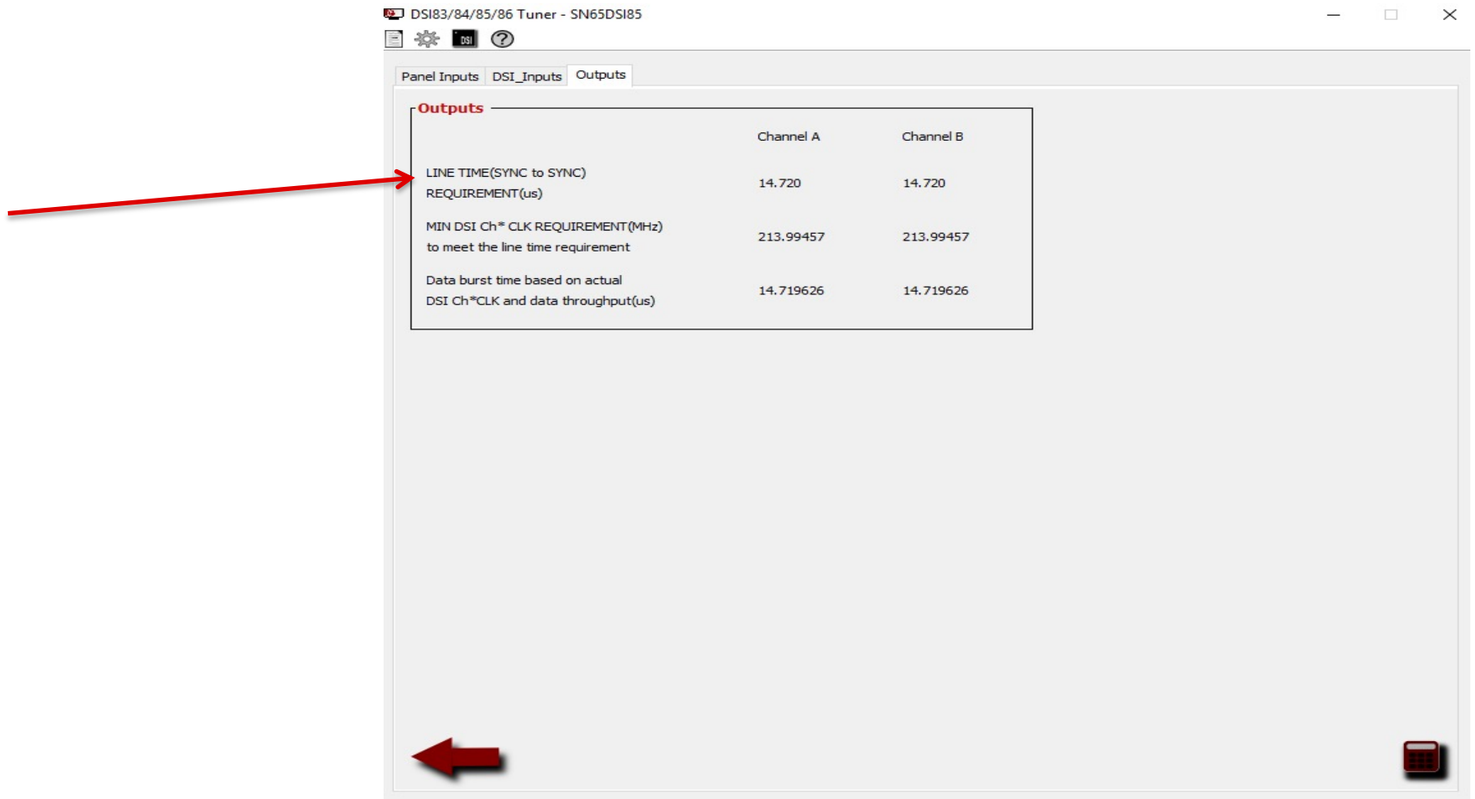
Dual to dual

- The “Informational” section depends on the DSI source



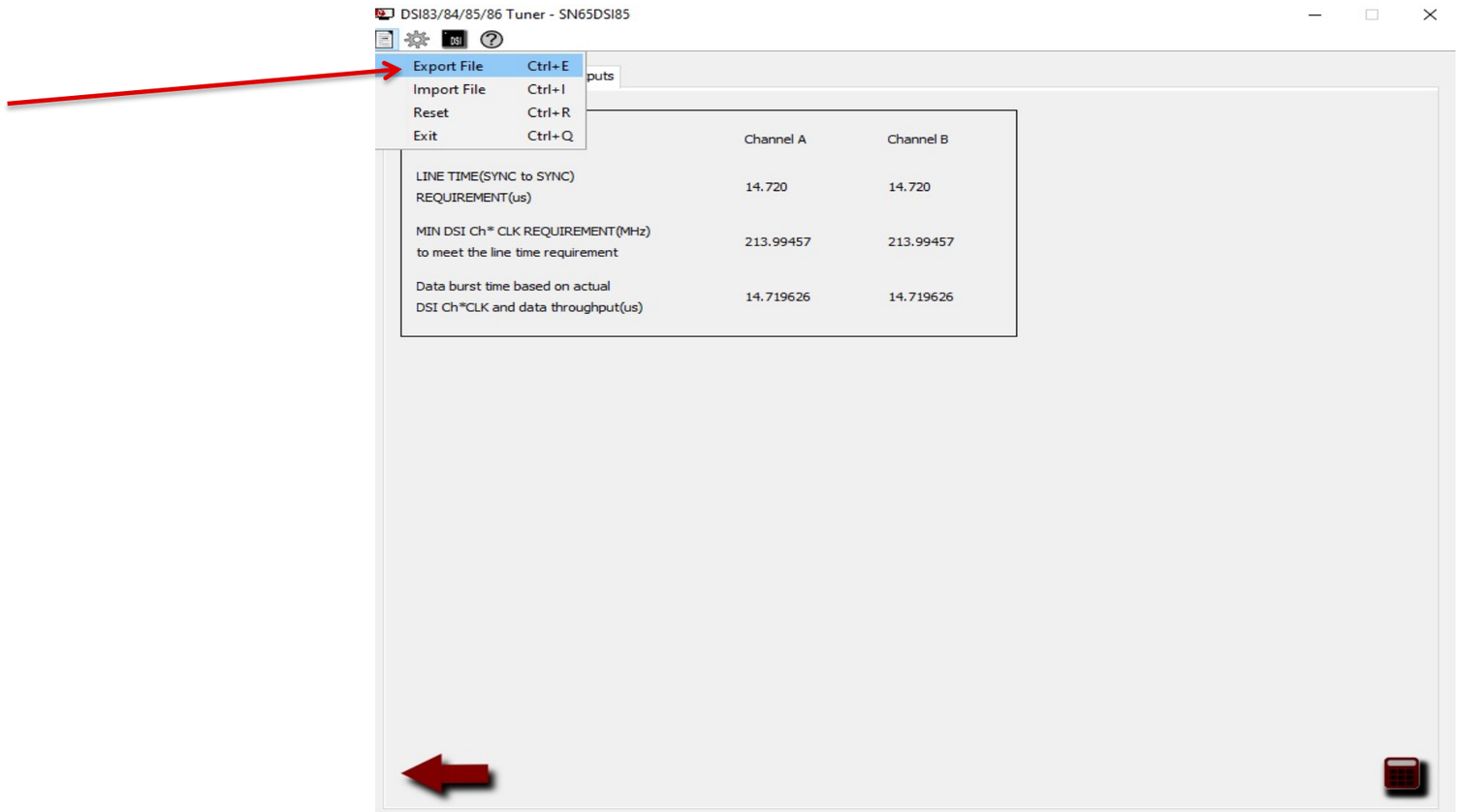
Dual to dual

- Click the calculator icon in the lower right to get to the “Outputs” window
- Make note of the LINE TIME requirement. The line time (horizontal sync to the next horizontal) on the input is preserved when outputting onto the LVDS interface.



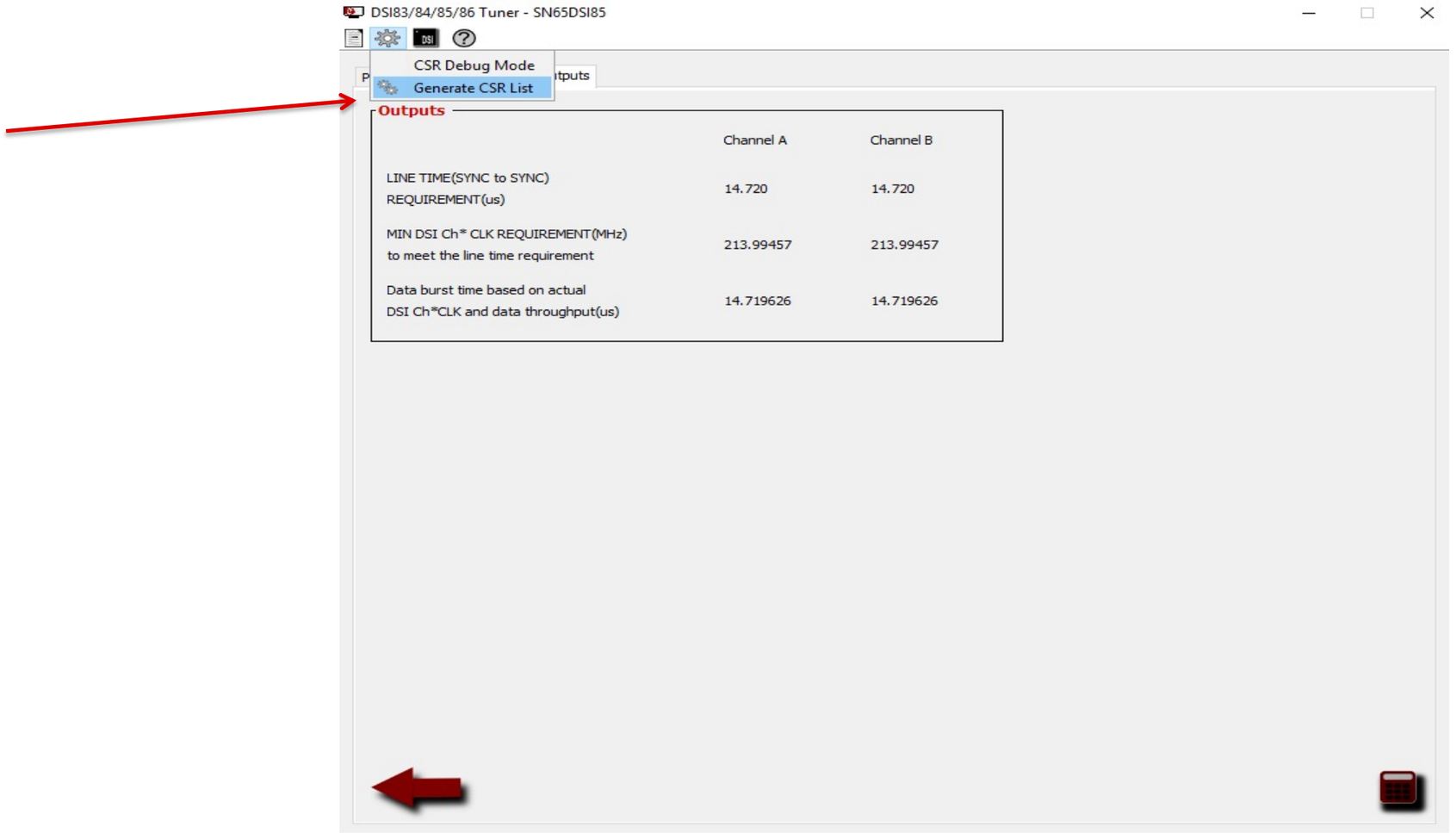
Dual to dual

- Click the icon in the upper left to export/save the .dsi file
- You can import it later without having to re-enter all the settings



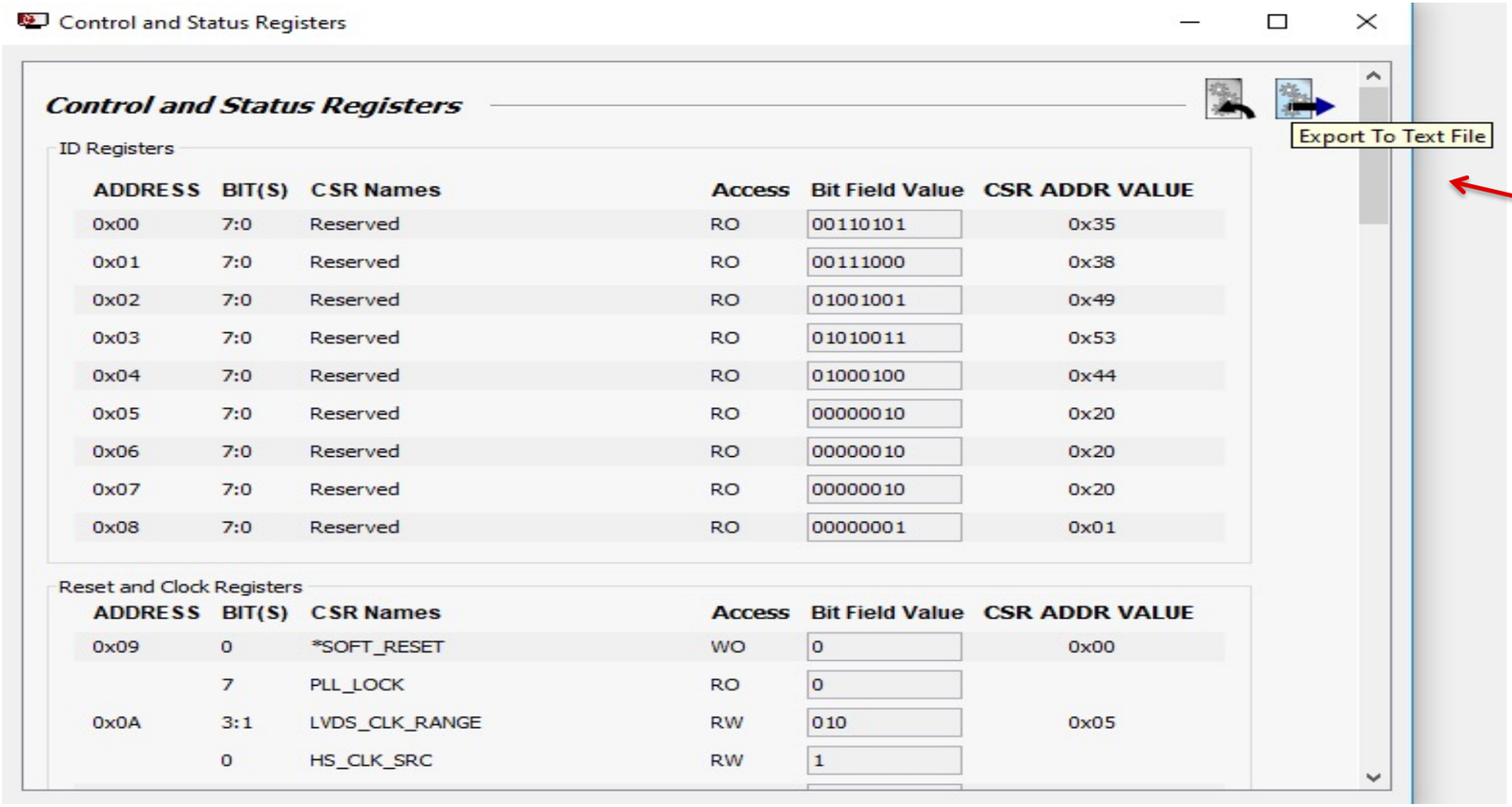
Dual to dual

- Click the icon in the upper left and Generate CSR list



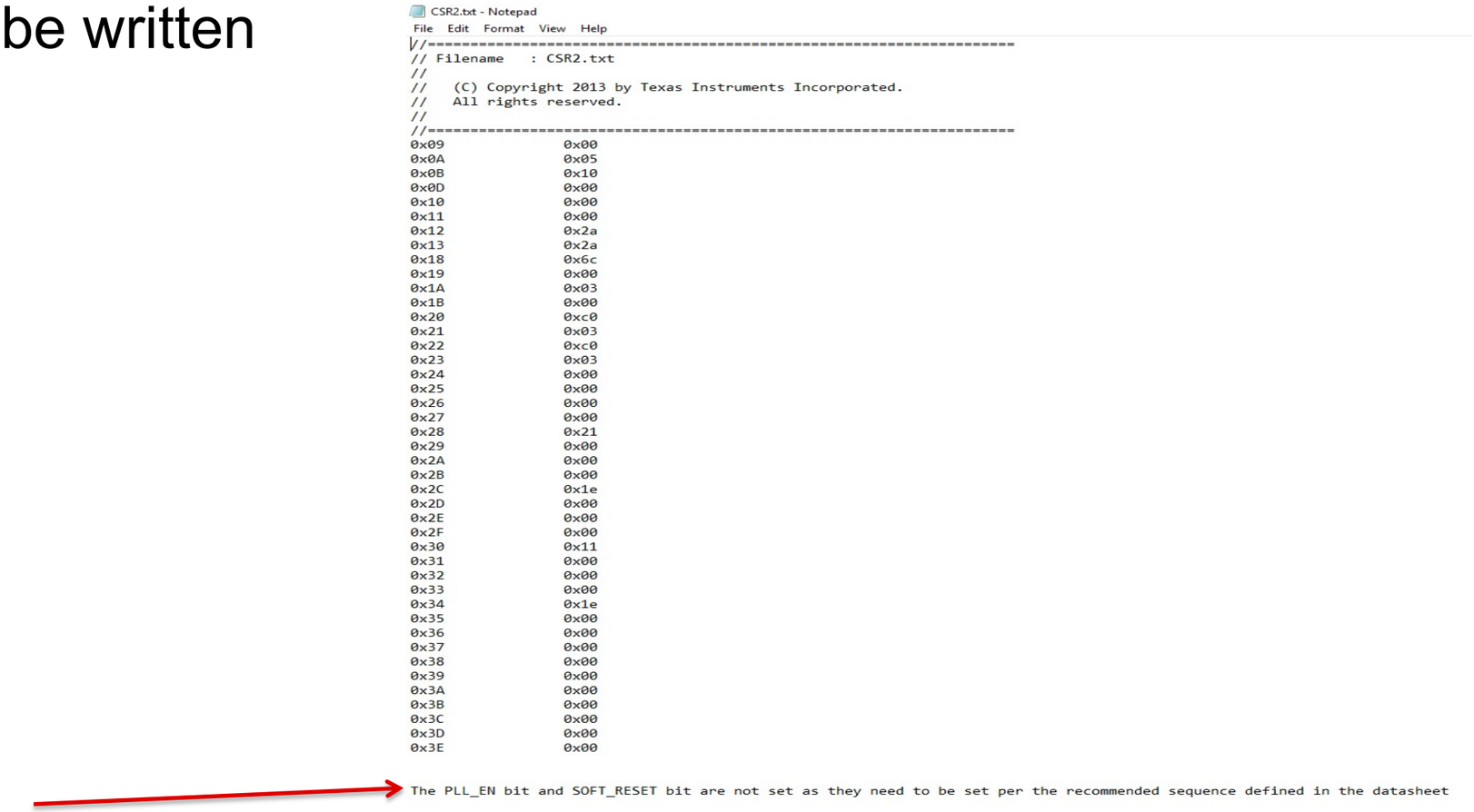
Dual to dual

- When the “Control and Status Registers” window pops up, click the  icon to export the settings to a .txt file



Dual to dual

- Open up the .txt file that was just generated. The column on the left contains the I2C register addresses, and the column on the right contains the values that need to be written



CSR2.txt - Notepad

File Edit Format View Help

```
//=============================================================================
// Filename    : CSR2.txt
//
//   (C) Copyright 2013 by Texas Instruments Incorporated.
//   All rights reserved.
//
//=============================================================================
0x09              0x00
0x0A              0x05
0x0B              0x10
0x0D              0x00
0x10              0x00
0x11              0x00
0x12              0x2a
0x13              0x2a
0x18              0x6c
0x19              0x00
0x1A              0x03
0x1B              0x00
0x20              0xc0
0x21              0x03
0x22              0xc0
0x23              0x03
0x24              0x00
0x25              0x00
0x26              0x00
0x27              0x00
0x28              0x21
0x29              0x00
0x2A              0x00
0x2B              0x00
0x2C              0x1e
0x2D              0x00
0x2E              0x00
0x2F              0x00
0x30              0x11
0x31              0x00
0x32              0x00
0x33              0x00
0x34              0x1e
0x35              0x00
0x36              0x00
0x37              0x00
0x38              0x00
0x39              0x00
0x3A              0x00
0x3B              0x00
0x3C              0x00
0x3D              0x00
0x3E              0x00

The PLL_EN bit and SOFT_RESET bit are not set as they need to be set per the recommended sequence defined in the datasheet
```

Thanks for your time!