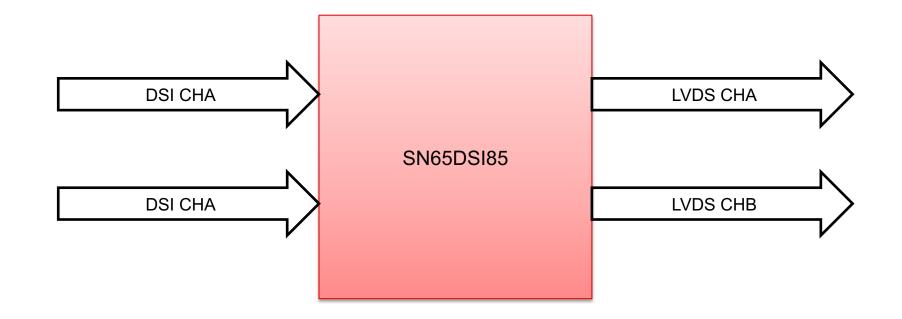
Dual DSI input to Dual-Link LVDS TI Precision Labs – SN65DS183/84/85

Presented and prepared by Ikechukwu Anyiam





• The SN65DSI85 is the only device that can be used for this application

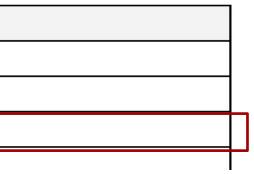




- From display datasheet, identify:
- Resolution:

| Items | Unit | Specification |
|-----------------|------|--------------------------------|
| Screen Diagonal | [mm] | 609.7 (24.0") |
| Active Area | [mm] | 531.36 (H) x 298.89 (V) |
| Pixels H x V | | 1920 x 1080 |
| Divol Ditch | [um] | 276 75 (por one triad) +276 75 |

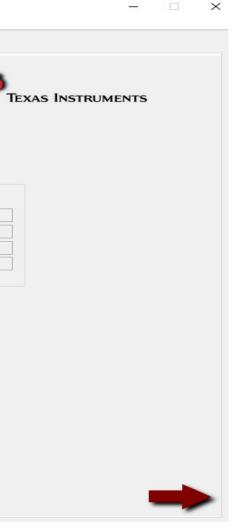
• This is a 1920 x 1080 panel





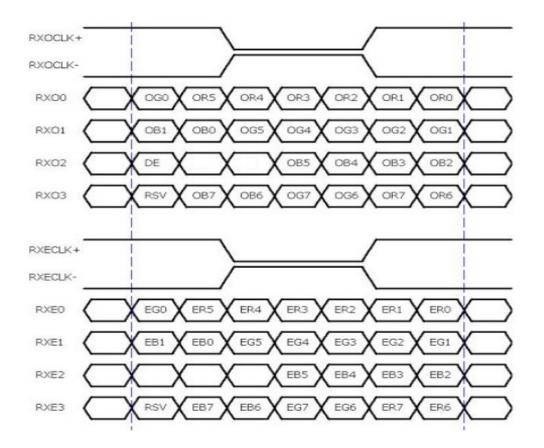
• After changing the "LVDS Mode" to "Dual", fill in the resolution:

| | 💽 DSI83/84/85/86 Tuner - SN65DSI85 | |
|---|--|-------------------------------|
| | Panel Inputs DSI_Inputs Outputs | |
| Notice how the tool | Panel Info Channel A | |
| | Panel Vendor | |
| automatically divides | Panel Model | |
| automatically undes | Resolution 1920 pixels x 1080 lines | |
| | Test Pattern | |
| "LVDS_HActive" by 2. | Pixels LVDS Channel A LVDS Channel B | Lines LVDS Channel A |
| | LVDS_HPW | LVDS_VPW |
| | | |
| | LVDS_HActive 960 | LVDS_VFP LVDS_VActive 1080 |
| | Htotal 960 0 | Vtotal 1080 0 |
| | Additional Panel Info Channel A Channel B | |
| | FORMAT Format 2 V | |
| | Data Enable Polarity Positive Horizontal Sync Polarity Negative | |
| | Vertical Sync Polarity Negative ~ | |
| | Bits Per Pixel 18bpp ~ 18bpp ~ | |
| | | |
| | | |
| | | |
| | | |





- From display datasheet, identify:
- Mapping format:



• This is Format 2 (VESA), 24bpp



• Fill out corresponding section in tool:

| Panel Info Channel Panel Vendor Panel Model Resolution LVDS Mode Dual Test Pattern | pixels x 108 | 0 lines | | | | Texas Instruments |
|---|--------------|----------------|--------------|----------------|---|-------------------|
| Pixels LVDS Cha | nnel A I | LVDS Channel B | Lines | LVDS Channel A | | |
| LVDS_HBP | | | LVDS_VBP | | | |
| LVDS_HFP | | | LVDS_VFP | | | |
| LVDS_HActive 960 | | | LVDS_VActive | | | |
| Htotal 960 | (| 0 | Vtotal | 1080 | 0 | |
| Additional Panel Info | Channel A | Channel B | | | | |
| FORMAT | Format 2 | | | | | |
| Data Enable Polarity | Positive | ~ | | | | |
| Horizontal Sync Polarity | | | | | | |
| Vertical Sync Polarity | Negative | ~ | | | | |
| Bits Per Pixel | 24bpp | ~ 24bpp ~ | | | | |
| | | | | | | |
| | | | | | | |
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- From display datasheet, identify:
- Timing Parameters:

| Signal | Item | Symbol | Min | Тур | Max | Unit |
|------------|------------|----------|------|------|------|-------|
| Vertical | Period | Tv | 1092 | 1130 | 1818 | Th |
| Section | Active | Tdisp(v) | 1080 | 1080 | 1080 | Th |
| Section | Blanking | Tblk(v) | 12 | 50 | 738 | Th |
| Horizontal | Period | Th | 1034 | 1050 | 1100 | Tclk |
| Section | Active | Tdisp(h) | 960 | 960 | 960 | Tclk |
| Section | Blanking | Tblk(h) | 74 | 90 | 140 | Tclk |
| Clock | Period | Tclk | 10.6 | 14.0 | 17.7 | Ns |
| Clock | Frequency | Freq | 56.5 | 71.2 | 94 | MHz |
| Frame rate | Frame rate | VFreq | 50 | 60 | 76 | Hz |
| Hsync | Hsync | HFreq | 55 | 68 | 91 | KHz |
| Frequency | Frequency | initeq | 55 | 00 | 71 | ISTIZ |

- From this, we can see that the total vertical blanking is 50, and the total horizontal blanking is 90
 - -VPW+VBP+VFP=50
 - -HPW+HBP+HFP=90



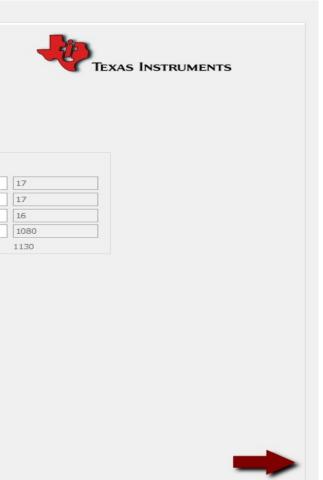
- Fill out corresponding section in tool:
- Horizontal blanking (90) is divided among HPW, HBP, and HFP

• Vertical blanking (50) is divided Among VPW, VBP, and VFP

|] | 🕸 🖬 🕐 | | | | | | | | | |
|----|---|---|--|-------------|--------------------------------|---|---|--|--|--|
| Pa | anel Inputs DSI | Inputs |)utputs | | | | | | | |
| | Panel Info Panel Vendor Panel Model Resolution LVDS Mode Test Pattern | Channel 1920 g Dual | A movels × 108 | 0 line | 25 | | | | | |
| | Pixels LVDS_HPW LVDS_HBP LVDS_HFP LVDS_HActive Htotal | LVDS Channel A LVDS_HPW 30 LVDS_HBP 30 LVDS_HFP 30 LVDS_HFP 30 LVDS_HActive 960 | | | Channel B | | Lines LVDS_VPW LVDS_VBP LVDS_VFP LVDS_VActive Vtotal | LVDS Channel A 17 17 16 1080 1130 | | |
| | Additional Pan FORMAT Data Enable Po Horizontal Sync Vertical Sync Po Bits Per Pixel | olarity c Polarity | Channel A Format 2 Positive Negative 24bpp | > > > | Channel B Format 2 24bpp | ~ | | | | |

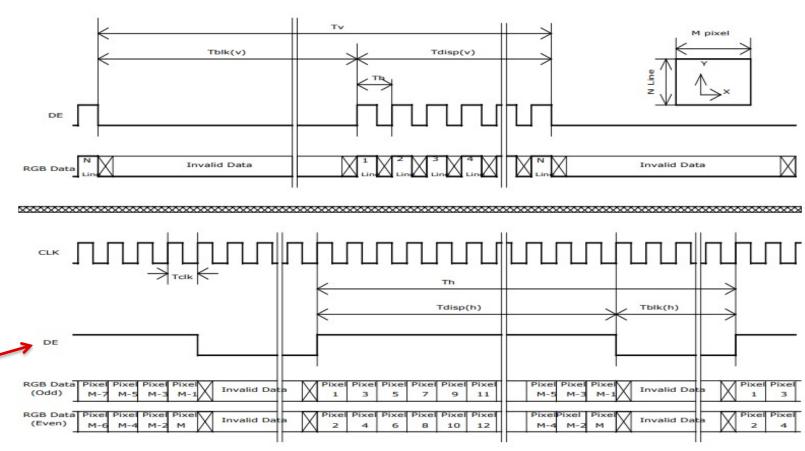
DSI83/84/85/86 Tuner - SN65DSI8⁴

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- From display datasheet, identify:
- HSYNC, VSYNC, and DE polarity:
- This particular display operates in DE mode, so HSYNC/VSYNC polarity don't matter.
- DE is positive during active display so DE polarity is positive





• Fill out corresponding section in tool:

| Panel Info Panel Vendor Panel Model Resolution LVDS Mode Test Pattern | Channel 1920 ; Dual | pixels x 10 | 30 lines | | | | -27 | Texas Instrume |
|--|---------------------------|-------------|----------|-----------|--------------|------------------|------|----------------|
| Pixels | | | | | Lines | | | |
| | LVDS Cha | nnel A | LVDS Cha | annel B | | LVDS Channe | | |
| LVDS_HPW | 30 | | 30 | | LVDS_VPW | 17 | 17 | |
| LVDS_HBP | 30 | | 30 | | LVDS_VBP | 17 | 17 | |
| LVDS_HFP | 30 | | 30 | | LVDS_VFP | 16 | 16 | |
| LVDS_HActive | | | 960 | | LVDS_VActive | all and a second | 1080 | |
| Htotal | 1050 | | 1050 | | Vtotal | 1130 | 1130 | |
| Additional Par | nel Info | Channel A | A Ch | annel B | | | | |
| FORMAT | | Format 2 | | ormat 2 🗸 | | | | |
| Data Enable P | olarity | Positive | ~ | | | | | |
| Horizontal Syr | | Negative | | | | | | |
| Vertical Sync F | | Negative | | | | | | |
| Bits Per Pixel | Chartey | 24bpp | | 4bpp 🗸 | | | | |
| Dits PEI PIXE | | ליעריב | ~ 2 | 4bpp ~ | | | | |
| | | | | | | | | |
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• Switch to "DSI_Inputs" window by either clicking the tab or clicking the arrow:

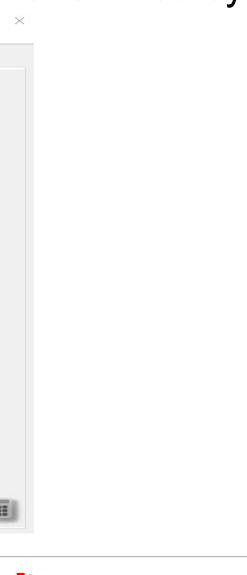
| Panel Info Panel Vendor Panel Model Resolution LVDS Mode Test Pattern | Channel (1920) più Dual (| xels x 10 | 80 lines | | | | -27 | Texas Instruments |
|---|----------------------------------|--|----------|-------------------------|--------------|--------------|------|-------------------|
| Pixels | VDS Chan | nel A | LVDS CH | annel B | Lines | LVDS Channel | • | |
| | 30 | | 30 | | LVDS_VPW | 17 | 17 | |
| | 30 | | 30 | | LVDS_VBP | 17 | 17 | |
| | 30 | | 30 | | LVDS_VFP | 16 | 16 | |
| LVDS_HActive | | | 960 | | LVDS_VActive | | 1080 | |
| Htotal : | 1050 | | 1050 | | Vtotal | 1130 | 1130 | |
| Additional Pane FORMAT Data Enable Pol Horizontal Sync Vertical Sync Po Bits Per Pixel | arity Polarity | Channel A Format 2 Positive Negative 24bpp | | Channel B Format 2 v | | | | |

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- The inputs to this window mainly depend on the DSI source
- The parameters entered must match the actual DSI parameters transmitted by the DSI source
 Image: Station of the sta

| | | DSI Channel | A | | DSI C | hannel A | DSI C | Channel B | | |
|----------------------------------|------------------------|----------------|--------|-----------------|----------|----------|-------|----------------------|-----------------------|--|
| anel Resolution | n | 1920x1080 | | LP | All | ~ | All | \sim | | |
| SI Ch Mode | | Single | \sim | Burst Mode | Burst | t v | Burs | t 🗸 | | |
| eft right or even CROP Enable | | OE No | ~ | Sync Mode | Even | nt ~ | Ever | nt 🗸 | | |
| els | Charles and the second | anal A Tanaka | DELC | and B tanuta | | Lines | | DCI Channel & Januta | DCI Changel B Japanta | |
| | SI Char | nnel A Inputs | DSIC | nannel B Inputs | | | | DSI Channel A Inputs | DSI Channel B Inputs | |
| | | | | | | DSI_VPW | | | | |
| | | | | | 1 | DSI_VBP | | | | |
| SI_HFP | | | | | 1 | | | 1080 | | |
| SI_HActive 1 SI_Htotal 19 | 10.000 C | | 0 | | | DSI_VAct | | 1080 | 0 | |
| SI_HIUTAI IS | 920 | | 0 | | | 001_100 | | 1000 | | |
| ditional Char | | | | | | | | CLK | | |
| | DS. | I Channel A in | put | DSI Ch | annel B | Input | | LVDS CLK(MHz) - no | | |
| SI DDR LK rate(MHz) | - | | | | | | | LVDS CLK source | DSI CLK 🗸 | |
| SI # of lanes | 1 | ~ | | 1 ~ | | | | Ref CLK(MHz) | | |
| | | | | | | | | Multiplier (1-4) | 1 ~ | |
| SI Video Mode | R | GB666 packed | | ✓ RGB66 | 66 packe | ed 🗸 | | DSI Ch A CLK | | |
| FT_CROP | | PI | GHT_CR | ne ar | | | | Divisor(1-25) | 1 ~ | |
| FI_CROP | | | | | | | | LVDS CLK(MHz) - Ad | tual - 🕕 | |
| | | | | | | | | | | |
| | | | | | | | | | | |
| | | | | | | | | | | |



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- Select "Dual" as the "DSI Ch Mode"
- Since the panel is 24bpp, select "RGB888" as the DSI Video Mode

| DSI Info | DSI Channel A | Informational | DSI Channel A | DSI Channel B | |
|--|---------------------|------------------|--------------------|---|------------------------|
| Panel Resolution | 1920×1080 | LP | All ~ | All 🗸 | |
| DSI Ch Mode | Dual 🗸 | Burst Mode | Burst 🗸 | Burst 🗸 | |
| Left right or even odd LR CROP Enable | 0E ~ No ~ | Sync Mode | Event 🗸 | Event 🗸 | |
| Pixels DSI Cha | nnel A Inputs DSI C | Channel B Inputs | Lines | DSI Channel A Input | s DSI Channel B Inputs |
| DSI_HPW | | | DSI_VPW | - | |
| DSI_HPW | | | DSI_VPW DSI_VBP | |] [|
| DSI_HEP | | | DSI_VEP | | |
| DSI_HActive 960 | 960 | | DSI_VAct | ive 1080 | 1080 |
| DSI_Htotal 960 | 960 | | DSI_Vtot | | 1080 |
| DSI DDR CLK rate(MHz) DSI # of lanes 1 | I Channel A input | 1 ~ RGB88 | nnel B Input | CLK LVDS CLK(MHz) - r LVDS CLK source Ref CLK(MHz) Multiplier(1-4) DSI Ch A CLK Divisor(1-25) | DSI CLK ~ |
| LEFT_CROP | RIGHT_CF | 20P | | Divisor(1-25) LVDS CLK(MHz) – / | |





- The "DSI # of lanes" depends on the required throughput to meet the panel resolution
- Each lane can support up to 1 Gbps

| DSI Info | | Informational | | | | | | |
|--|---------------------------|----------------------|------------|----------|---------|--|---------------|---------|
| | DSI Channel A | | DSI Cha | nnel A | DSI Cha | annel B | | |
| Panel Resolution DSI Ch Mode | 1920x1080 | LP | All | ~ | All | ~ | | |
| | | Burst Mode | Burst | ~ | Burst | ~ | | |
| Left right or even odd LR CROP Enable | No | Sync Mode | Event | ~ | Event | ~ | | |
| Pixels | | | _ | ines | | | | |
| | annel A Inputs D | OSI Channel B Inputs | | | D | SI Channel A Inputs | DSI Channel I | 8 Input |
| DSI_HPW | | | | DSI_VPW | | | | |
| DSI_HBP | | | | DSI_VBP | | | | |
| DSI_HFP | | | | DSI_VFP | | | | |
| DSI_HActive 960 | | 960 | | DSI_VAct | ive 1 | 1080 | 1080 | |
| DSI_Htotal 960 | 9 | 960 | | DSI_Vtot | al 10 | 080 | 1080 | |
| Additional Channel in | nfo SI Channel A input | DSI Cha | innel B In | out | | CLK LVDS CLK(MHz) - non | -in al | - |
| DSI DDR CLK rate(MHz) | | | |] | | LVDS CLK source Ref CLK(MHz) | DSI CLK | ~ |
| DSI # of lanes | ~ | 4 🗸 | | | | Multiplier (1-4) | 1 | |
| DSI Video Mode R | GB888 | ~ RGB88 | 8 | | | DSI Ch A CLK | | |
| LEFT_CROP | RIGH | T_CROP | | | | Divisor (1-25) LVDS CLK (MHz) – Act | 1 tual - 🚹 | ~ |



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• Enter the pixel/line information. Typically this will match the panel inputs:

| DSI Info Panel Resolution DSI Ch Mode Left right or even odd LR CROP Enable | DSI Channel A 1920x1080 Dual ~ OE ~ No ~ | Informational LP Burst Mode Sync Mode | DSI Channel All Burst Event | A DSI All Bur Eve | st v | | |
|---|--|--|--------------------------------------|--|---|-----------|--|
| DSI_HPW 30 DSI_HBP 30 DSI_HFP 30 DSI_HFP 30 DSI_HActive 960 DSI_Htotal 1050 Additional Channel int DSI DSI DDR CLK rate(MHz) DSI # of lanes 4 | 30 30 30 960 1050 fo I Channel A input | DSI Cha 4 ~ RGB88 | DSI DSI DSI DSI | VPW _VBP _VFP _VActive _Vtotal | DSI Channel A Inputs 17 17 16 1080 1130 CLK LVDS CLK(MHz) - nor LVDS CLK source Ref CLK(MHz) Multiplier(1-4) DSI Ch A CLK Divisor(1-25) LVDS CLK(MHz) - Activity | DSI CLK ~ | |



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- Enter the "LVDS CLK(MHz)" nominal value from the frequency specified in the panel datasheet
- The LVDS CLK range for the SN65DSI83/84/85 is 25 to 154MHz, so make sure you're within this range DSI83/84/85/86 Tuner - SN65DSI85 🖹 🔆 📶 🕜

Panel Inputs DSI_Inputs Outputs

DSI Channel A

1920x1080

Dual

Informational

DSI Channel A

DSI Channel B

Burst

DSI Info

Panel Resolution DSI Ch Mode

| | | | | | | | Left right or even odd OE V Sync Mode Event Event LR CROP Enable No V V Event V | ~ |
|-----------------------|------------|----------|------|------|------|------|---|----------------------|
| Signal | Item | Symbol | Min | Тур | Max | Unit | | |
| Vertical | Period | Tv | 1092 | 1130 | 1818 | Th | Pixels Lines DSI Channel A Inputs DSI Channel B Inputs DSI Channel B Inputs | nnel A Inpu |
| Section | Active | Tdisp(v) | 1080 | 1080 | 1080 | Th | DSI_HPW 30 30 DSI_VPW 17 | |
| | Blanking | Tblk(v) | 12 | 50 | 738 | Th | DSI_HBP 30 30 DSI_VBP 17 | |
| | Period | Th | 1034 | 1050 | 1100 | Tclk | DSI_HFP 30 30 DSI_VFP 16 | |
| Horizontal Section | Active | Tdisp(h) | 960 | 960 | 960 | Tclk | DSI_HActive 960 960 DSI_VActive 1080 DSI_Htotal 1050 1050 DSI_Vtotal 1130 | |
| Section | Blanking | Tblk(h) | 74 | 90 | 140 | Tclk | Additional Channel info | |
| Clock | Period | Tclk | 10.6 | 14.0 | 17.7 | Ns | | CLK(MHz) - |
| Clock | Frequency | Freq | 56.5 | 71.2 | 94 | MHz | DSI DDR LVDS C CLK rate(MHz) | CLK source |
| Frame rate | Frame rate | VFreq | 50 | 60 | 76 | Hz | DSI # of lanes 4 v 4 v | K(MHz) |
| Hsync | Hsync | HFreq | 55 | 68 | 91 | KHz | DSI Video Mode RGB888 V RGB888 DSI Ch | A CLK |
| Frequency | Frequency | | | | | | LEFT CROP RIGHT_CROP | (1-25) CLK(MHz) - |

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| | DSI Channel B Inputs | |
|----|----------------------|--|
| | 17 | |
| | 17 | |
| | 16 | |
| | 1080 | |
| m | DSI CLK v | |
| | 1 ~ | |
| | 1 ~ | |
| ct | ual - | |
| | | |
| | | |
| | | |

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• The LVDS CLK source can be derived from either the DSI CLK or an external reference clock

| Panel Resolution | | DSI Channel / | 4 | Informational | | | Channel B | | |
|------------------------|-----------|-----------------|--------|-----------------|------------------------|------|----------------------|----------------------|--|
| | | Dual ~ | | Burst Mode | Burst v | | | | |
| Left right or | even odd | OE | ~ | Sync Mode | Event v | | | | |
| LR CROP Ena | able | No | ~ | | | | | | |
| | | | | | 1 | | | | |
| ixels | | | DSI C | hannel B Inputs | Lines | | DSI Channel A Inputs | DSI Channel B Inputs | |
| DSI_HPW | | | 30 | | DSI_VPW | | 17 | 17 | |
| DSI_HBP | | | 30 | | DSI_VBP | | 17 | 17 | |
| OSI_HFP | 30 | | 30 | | DSI_VFP DSI_VActive | | 16 | 16 | |
| SI_HActive | 960 | | 960 | | | | 1080 | 1080 | |
| DSI_Htotal | 1050 | | 1050 | | DSI_Vte | otal | 1130 | 1130 | |
| dditional Cl | nannel in | fo | | | | | CLK | | |
| | DS: | I Channel A inp | out | DSI Cha | annel B Input | | LVDS CLK(MHz) - nor | minal 71.2 | |
| DSI DDR CLK rate(MH | z) | |] | | | | LVDS CLK source | DSI CLK 🗸 | |
| DSI # of lane | | ~ | | 4 ~ | | | Ref CLK(MHz) | | |
| | | | | . ~ | | | Multiplier (1-4) | 1 ~ | |
| DSI Video Mo | de R | GB888 | | ✓ RGB88 | 8 | ~ | DSI Ch A CLK | | |
| LEFT_CROP | | RI | GHT_CR | OP | | | Divisor(1-25) | 1 ~ | |
| | | | | | | | LVDS CLK(MHz) - Ac | tual - 🌓 | |
| | | | | | | | | | |
| | | | | | | | | | |



- Assume the DSI CLK will be used as the LVDS CLK source. To calculate the minimum required DSI CLK frequency, use the below equation:
- Minimum DSICLK frequency = $\frac{Throughput}{2 \times \# of DSI Lanes} = \frac{LVDS CLK \times bpp}{2 \times \# of DSI Lanes}$
- For this example:

• Minimum DSICLK frequency = $\frac{71.2 MHz \times 24 bpp}{2 \times 4} = \frac{1708.8 Mbps}{2 \times 4} = 214 MHz$



• Fill out corresponding sections in tool and select the correct divisor:

| Info | | | | ormational | | | | | | | | |
|---------------|---------|----------------------------|------------|-------------|------------|-----------|---------|---------------|-----------------|------------|-------------|---|
| nel Resolut | tion | DSI Channel A 1920x1080 | | | DSI Cha | | _ | hannel B | | | | |
| I Ch Mode | | Dual | | | All | ~ | All | | ~ | | | |
| ft right or e | | | - DU | rst Mode | Burst | ~ | Burs | t · | ~ | | | |
| CROP Ena | | No | → Sy | nc Mode | Event | Event ~ E | | Event 🗸 | | | | |
| | | | | | | | | | | | | |
| els | | | | | | Lines | | | | | | |
| | DSI Cha | nnel A Inputs | DSI Channe | el B Inputs | | | | DSI Chan | inel A Inputs | DSI Chann | el B Inputs | |
| I_HPW | 30 | | 30 | | | DSI_VPW | | 17 | | 17 | | |
| I_HBP | 30 | | 30 | DSI_VB | | DSI_VBP | 17 | | 17 | | 1 | |
| I_HFP | 30 | 30 30 | | DSI_VFP | | | 16 | | 16 | | j | |
| I_HActive | 960 | | 960 | DSI_VAct | | ive | ve 1080 | | 1080 | | | |
| I_Htotal | | | 1050 | | | DSI_Vtota | al | 1130 | | 1130 | | |
| | | 6 | | | | | | C 1.14 | | | | |
| litional Ch | | ro I Channel A inp | ut | DSI Cha | annel B In | nput | | CLK LVDS C | CLK(MHz) - nomi | nal 71.2 | | |
| I DDR | , 21 | 4 | | 214 | | | | | LK source | DSI CL | K v | |
| K rate(MHz | z) [2] | .4 | | 214 | | | | | K(MHz) | | | |
| I # of lane | s 4 | ~ | | 4 🗸 | | ~ | | | ier(1-4) | 1 | ~ | |
| I Video Mo | da Dr | GB888 | ~ | RGB88 | 8 | | | | ACLK | 214 | | |
| | ue Ri | 30000 | ~ | KGD00 | 0 | ~ | | | (1-25) | 3 | | - |
| FT_CROP | | RIG | GHT_CROP | | | | | | (1-25) | | 336 | - |
| | | | | | | | | LVDSC | LE (MH2) - ACU | Jai 71.555 | JJU 🕕 | |
| | | | | | | | | | | | | |
| | | | | | | | | | | | | |



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• The "Informational" section depends on the DSI source

| nel Inputs D | si_inputs | Outputs | | | 4 | | | | | - | | |
|---------------|--------------|-----------------------|-----------|-------------|-----------|-----------------------------------|-------|---------------------------|---------|-----------|--------|--|
| DSI Info | | DSI Channel A | | ormationa | | annel A | DELC | hannel B | | | | |
| Panel Resolu | ution | 1920x1080 | LF | | All | | All | | | | | |
| | | Dual | T | Burst Mode | Burst | | Burst | | | | | |
| Left right or | even odd | | DU DU | | | ~ | | | | | | |
| LR CROP En | | No | ~ St | nc Mode | Event | Event \checkmark Eve | | ent 🗸 | | | | |
| | | | | | | | | | | | | |
| Pixels | | | | | | Lines | | | | | | |
| | DSI Char | nnel A Inputs | DSI Chann | el B Inputs | | | | DSI Channel A Inputs | DSI | Channel B | Inputs | |
| DSI_HPW | SI_HPW 30 | | 30 | 30 | | DSI_VPW | | 17 1 | | | | |
| DSI_HBP | 30 | | 30 | 30 | | DSI_VBP DSI_VFP DSI_VActive | | 17 1 | | | | |
| DSI_HFP | SI_HFP 30 | | 30 | | | | | 16 | 16 | | | |
| DSI_HActive | 960 | | 960 | | | | | 1080 | 108 | 0 | | |
| DSI_Htotal | | | 1050 | | | DSI_Vtota | al | 1130 | 113 | D | | |
| | | | | | | | | | | | | |
| Additional C | | to I Channel A inp | out | DSI Ch | annel B I | nput | | CLK LVDS CLK(MHz) - no | minal | 71.2 | | |
| DSI DDR | | | | | | _ | | LVDS CLK source | | DSI CLK | ~ | |
| CLK rate(MH | z) 21 | .4 | | 214 | | | | | | DSI CLK | ~ | |
| DSI # of lan | es 4 | ~ | | 4 ~ | | | | Ref CLK(MHz) | | | _ | |
| | | | | | | | | Multiplier (1-4) | | 1 | ~ | |
| DSI Video Mo | ode R(| GB888 | ~ | RGB88 | 38 | ~ | | DSI Ch A CLK | | 214 | | |
| LEFT_CROP | | RI | GHT_CROP | | | | | Divisor(1-25) | | 3 | ~ | |
| LEIT_CROP | | | - | L | | | | LVDS CLK(MHz) - Ac | ctual 7 | 1.333336 | 0 | |
| | | | | | | | | | | | | |
| | | | | | | | | | | | | |
| | | | | | | | | | | | | |



- Click the calculator icon in the lower right to get to the "Outputs" window
- Make note of the LINE TIME requirement. The line time (horizontal sync to the next horizontal) on the input is preserved when outputting onto the LVDS interface. DSI83/84/85/86 Tuner - SN65DSI85



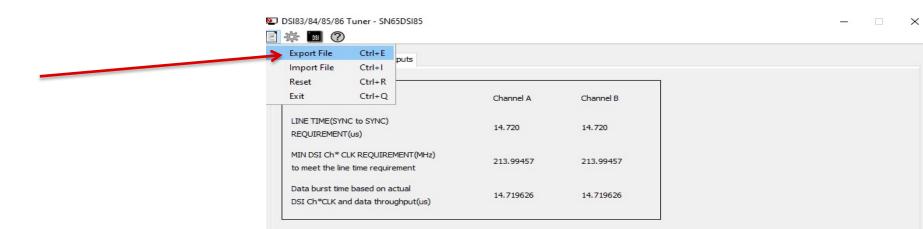


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- Click the icon in the upper left to export/save the .dsi file
- You can import it later without having to re-enter all the settings







• Click the 🐲 icon in the upper left and Generate CSR list

| DSI83/84/85/86 Tuner - SN65DSI85 | | | - | \times |
|---|-----------|-----------|---|----------|
| CSR Debug Mode | | | | |
| Outputs | d 11 | d 15 | | |
| | Channel A | Channel B | | |
| LINE TIME(SYNC to SYNC) REQUIREMENT(us) | 14.720 | 14.720 | | |
| MIN DSI Ch* CLK REQUIREMENT(MHz) to meet the line time requirement | 213.99457 | 213.99457 | | |
| Data burst time based on actual DSI Ch*CLK and data throughput(us) | 14.719626 | 14.719626 | | |
| | | | | |
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• When the "Control and Status Registers" window pops up, click the side icon to export the settings to a .txt file

| ontrol and | Statu | s Registers | | | | A. | | Â |
|---------------|-----------|----------------|--------|------------------------|----------------|----|------|-----------------|
| Registers | | | | | | | Expo | rt To Text File |
| ADDRESS | BIT(S) | CSR Names | Access | Bit Field Value | CSR ADDR VALUE | | | * |
| 0x00 | 7:0 | Reserved | RO | 00110101 | 0x35 | | | |
| 0x01 | 7:0 | Reserved | RO | 00111000 | 0x38 | | | |
| 0x02 | 7:0 | Reserved | RO | 01001001 | 0x49 | | | |
| 0x03 | 7:0 | Reserved | RO | 01010011 | 0x53 | | | |
| 0x04 | 7:0 | Reserved | RO | 01000100 | 0x44 | | | |
| 0x05 | 7:0 | Reserved | RO | 00000010 | 0x20 | | | |
| 0x06 | 7:0 | Reserved | RO | 00000010 | 0x20 | | | |
| 0x07 | 7:0 | Reserved | RO | 00000010 | 0x20 | | | |
| 0x08 | 7:0 | Reserved | RO | 0000001 | 0x01 | | | |
| set and Clock | Registers | s | | | | | | |
| ADDRESS | BIT(S) | CSR Names | Access | Bit Field Value | CSR ADDR VALUE | | | |
| 0x09 | 0 | *SOFT_RESET | WO | 0 | 0x00 | | | |
| | 7 | PLL_LOCK | RO | 0 | | | | |
| 0x0A | 3:1 | LVDS_CLK_RANGE | RW | 010 | 0x05 | | | |





• Open up the .txt file that was just generated. The column on the left contains the I2C register addresses, and the column on the right contains the values that need to be written

| CSR2.tx | rt - Notepad |
|--------------|---|
| | Format View Help |
| // | |
| | name : CSR2.txt |
| 11 | |
| // (C |) Copyright 2013 by Texas Instruments Incorporated. |
| | l rights reserved. |
| 11 | |
| //===== | |
| 0x09 | 0×00 |
| 0x0A | 0x05 |
| 0x0B | 0×10 |
| 0x0D | 0×00 |
| 0x10 | 0×00 |
| 0x11 | 0×00 |
| 0x12 | 0x2a |
| 0x13 | 0x2a |
| 0x18 | 0x6c |
| 0x19 | 0×00 |
| 0x1A | 0x03 |
| 0x1B | 0×00 |
| 0x20 | 0×c0 |
| 0×21 | 0×03 |
| 0x22 | 0×c0 |
| 0x23 | 0x03 |
| 0x24 | 0x00 |
| 0x25 | 0x00 |
| 0x26 | 0×00 |
| 0x27 | 0×00 |
| 0x28 | 0×21 |
| 0x29 | 0×00 |
| 0x2A | 0x00 |
| 0x2B | 0x00 |
| 0x2C | 0x1e |
| 0x2D | 0x00 |
| 0x2E | 0x00 |
| 0x2F | 0×00 |
| 0x30 | 0x11 |
| 0x31 | 0x00 |
| 0x32 | 0x00 |
| 0x33 | 0x00 |
| 0x34 0x35 | 0x1e 0x00 |
| 0x35 | 0x00 |
| 0x30 | 0x00 |
| | 0x00 |
| 0x38 0x39 | 0x00 0x00 |
| 0x3A | 0x00 |
| 0x3B | 0x00 |
| 0x3C | 0x00 |
| 0x3D | 0×00 |
| 0x3E | 0×00 |
| | |
| | |



Thanks for your time!





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