# Advanced topics on BQ40z80 2S – 7S gauge plus protector

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# Agenda

- BQ40z80 overview
- Familiar with the BQ40z50? A quick look at what is new/different with the BQ40z80
- Tools to start your evaluation of the BQ40z80
- Need 5S, 6S or 7S gauging?
- Need more than 2 thermistors for the extra cells? Need an additional ADC input or two?
- Need more GPIOs in your system to turn on/off other devices?
- Need GPIO to use as interrupts for specific flags or status instead of MCU intensive polling?
- Need higher currents and higher capacity?
- Now that you have a larger capacity battery, do you want to show greater resolution on your LED display?
- Do you have a highly capacitive load that needs soft starting to avoid overcurrent?
- Do you have asymmetric load and charging currents?
- Need cell balancing for all 7 cells?

Today I will be going through some of the common challenges for a high cell count battery pack, and show you how the BQ40z80 can help you with these challenges.

- -Need more than 2 thermistors for the extra cells? Need an additional ADC input or two?
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- -Do you have asymmetric load and charging currents?
- -Need cell balancing for all 7 cells?
- I'll address all these topics in the next hour.

2

2

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I'm going to start off with highlighting some of the changes between the BQ40z50 and the BQ40z80, since many of you already know that device. Next, I'll go into the tools we have in place for the BQ40z80 to evaluate the device, as well as start configuring the dataflash settings for your specifica application. After you are familiar with the BQ40z80, we will look at some common challenges:

#### BQ40z80 1S – 7S battery gas gauge with protector

#### **Features**

- · Battery manager with 2-series to 7-series capability
- Advanced Impedance Track<sup>™</sup> gauging with JEITA charge control and cell balancing during charge or at rest
- Suitable for Li-ion, LiFePO4 and NiXX chemistries
- Integrated safety protector
  - Voltage, current, temperature, cell imbalance
  - High-side NMOS FET drivers
- LED support (up to 6)
- Pre-charge and pre-discharge modes included
- Integrated flash memory and lifetime/black box data
- Elliptic curve cryptography (ECC) authentication
- Precision analog front end with dual ADCs
  - High-resolution, 16-bit coulomb counter
    - 15-bit delta-sigma ADC with multiplexer
    - Support for simultaneous CC and ADC
  - Works with 1.8V to 5V I/O systems
- QFN 32pin package (4mm x 4 mm x 0.9mm)

#### **Applications**

- Cordless appliances
- Non-military drones
- Portable robotics and garden tools
- Portable instruments

#### **Benefits**

- High gauging accuracy & multiple complex charging profile suppo
- Provides comprehensive protection for multicell safety
- Continuous cell balancing ensures maximum battery capacity is available at all times
- Lifetime/black box supports analysis of returned battery packs
- Anti-counterfeiting
- Visual display of SOC with LED indication

#### **Typical application schematic**



The BQ40z80 is a fully integrated Impedance Track, single chip gauge that is similar to the BQ40z50. The BQ40z80 supports up to 7S battery packs and has an array of features for fas gauging, protection, and authentication. The BQ40z80 has two ADC's, one multiplexed for voltage measurements, and one dedicated as a coulomb counter.

This information, along with internal temperature is used to compute an accurate battery capacity and state of health over a variety of conditions for a variety of battery chemistries. The device has integrated, programmable safety protections for overvoltage, undervoltage, overcurrent, short-circuit current, overload, and overtemperature. It can enable and disable charge and discharge FETs, pre-charge, and pre-discharge FETs, perform internal or external cell balancing, and even perform permanent fail FUSE blows if needed. All this in a small 32 pin 4mm by 4mm thin QFN package.

#### **BQ40z80** functions



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This chart shows all the new features built on top of the BQ40z50 base functionality. Because the BQ40z80 is scaled up to 7S, it naturally makes sence that high current packs will also be developed with this part. The device can natively support pack capacities up to 29Ah and battery currents up to 32A. With current scaling, the scale factor can be set between 0 and 100, with the scaled current still in 1mA resolution. To reduce losses in the sense resistor, a 1milli-Ohm typical sense resistor is supported, but this can be smaller if larger currents are used.

The BQ40z80 has several multi-function pins that can be configured based on the specific application needs. Most unused pins can be configured as GPIO's, with a the capability of generating interrups on pins through a flag mapping function. The flags may be OR'd or AND'ed together to trigger an interrupt on a particular GPIO pin, with up to eight different flags OR'ded onto a single pin.

Other multi-function pin functions are additional ADC inputs to monitor voltages or temperatures, a dedicated display pin to turn on the LED's, and a presence pin to use for removalbe battery applications to assist in battery detection and entering/exiting lower power states.

A new feature is a pre-discharge pin, which is useful when the load is highly capacitive, such as a motor. The pre-discharge pin allows charging up the cap until a pre-determined voltage is reached, and then turning on the DSG FET. This reduces the chances of having the battery OCD and SCD protections trip when turning on the load, as soft-starts the load and reduces the current spike.

The BQ40z80 also improves the authenitcaion capabilities with Elliptic Curve Cryptography, or ECC, as the encryption method for authentication.

#### **BQ40z80 tools and documentation**



The BQ40z80 is in preview status now, as an Advanced Product Launch. The part will be fully released to production in November 2018, but we already have a lot of information and tools available for you now to start your evaluation and development.

The first place to start is on the BQ40z80 product page on ti.com. On this page you will find the datasheet with detailed information on the device. You can go to the tools and software page and order a BQ40z80 EVM, and also read the EVM user guide. In the guide you will find details on how to configure the jumpers to configure the multi-function pins and registers so the device does just what you want it to do.

For more detail on the registers, you can go to the technical documents tab on the BQ40z80 product page to read the BQ40z80 Technical Reference Manual, or TRM. The TRM is the go-to spot to find details on every Smart Battery Data Specification, or SBS command, Data Flash, Register bit and flag, data flash bit, and all modes and states. The TRM is over 300 pages long, but don't let that intimidate you. The document is searchable, and is a great resource when you are configuring the BQ40z80 using the TI BQStudio tool. I won't go into detail on the tool, but it allows you to read and write the parameters to you need to set up the bq40z80, and the TRM give you definitions, examples, and the required information if you have questions.

(If something doesn't make sense to you in the TRM, you can always ask for help by posting your question to the e2e forum, or looking to see if your question has already been asked and answered)

To anticipate some of the common questions from prior products, I have prepared a few additional documents that can help.

One app note address the manufacture, production, and calibration of the BQ40z80, another app note addresses how to complete a successful learning cycle for the BQ40z80, and another app not introduces two new tools that are helpful if you are going to use the authentication feature of the BQ40z80.

## Need 5S, 6S, or 7S gauging?



Let's jump into the first topic addressed by the BQ40z80 – supporting battery packs with more than 4 cells.

The BQ40z80 supports up to 7S packs, but it takes a little work to get there. If you are only doing a 5S or 6S pack, then your set-up is straightforward in that you connect the cells directly to the ADC (through the resistors, not shown on the simplified schematic), and using the cell configuration register to configure it for 5S or 6S. However, for 7S, since there isn't a VC7 on the device, the top of stack and cell 7 is measured by configureing two multifunction pins to achieve this function.

Pin 15 is configured as VC7EN, which controls duty cycling the external resistor divider to save power. Pin 12 is configured as VC7SENSE to have it be the ADC input so that information is used in calculating the voltage for BAT and cell 7.

These pins are configured in the configuration register called Pin Configuration - pretty simple, right?

## BQ40z80 configuration options for 7S example



The BQ40z80EVM default settings are for the 7S cell configuration. This chart shows the default configuration for the other multi-function pins. Pin 12 and Pin 15, as mentioned, are use to configure for 7S. Pin 16 is used for external cell balancing for the 7<sup>th</sup> cell. I'll go into more detail on that in a bit. Pin 13 is used in conjunction with Pins 20, 21, and 22. Pin 13 is the Display input, which is connected to a pushbutton, that when pressed lights up the LEDs to display the state of charge. I'll also go into a bit more detail on that later. Finally, pin 17 is configured as a pre-discharge pin.

# Setting up the BQ40z80 for high cell applications

|  |   |                                  | Number of<br>Cells                                 |    |   |   |  |                                      | J12  | ? Term   | inal Block  | Con            | nections   |   |  |  |   |  |
|--|---|----------------------------------|--|----|---|---|--|--------------------------------------|--|--|---|----------------|--|---|--|--|---|--|
| Refer to the   |   |                                  |  | 1N |   | 1P  |  | 2P                                   |  | 3P   |   | 4P             |  | 5P  |  | 6P   |   | 7P   |
|  |   |                                  | 1  | ⊕  | -cell1+   | Ð   | short  | ⊕                                    | short  | Ð  | short   | $\oplus$       | short  | ⊕   | short  | ⊕  | short   | Ð  |
| BQ40280 EVIVI  |   |                                  | 2  | Ð  | -cell1+   | Ð   | -cell2+  | ⊕                                    | short  | Ð  | short   | Ð              | short  | Ð   | short  | ⊕  | short   | Ð  |
| user quide   |   |                                  | 3  | ⊕  | -cell1+   | ⊕   | -cell2+  | $\oplus$                             | -cell3+  | Ð  | short   | Ð              | short  | ⊕   | short  | ⊕  | short   | $\oplus$   |
| <u>door guide</u>  |   | ļ                                | 4  | ⊕  | -cell1+   | ⊕   | -cell2+  | ⊕                                    | -cell3+  | Ð  | -cell4+   | Ð              | short  | ⊕   | short  | ⊕  | short   | $\oplus$   |
|  |   |                                  | 5  | Ð  | -cell1+   | Ð   | -cell2+  | Ð                                    | -cell3+  | Ð  | -cell4+   | Ð              | -cell5+  | ⊕   | short  | ⊕  | short   | Ð  |
|  |   |                                  | 6  | Ð  | -cell1+   | Ð   | -cell2+  | Ð                                    | -cell3+  | Ð  | -cell4+   | Ð              | -cell5+  | ⊕   | -cell6+  | ⊕  | short   | Ð  |
| Connect cells and  |   |                                  | 7  | ⊕  | -cell1+   | Ð   | -cell2+  | ⊕                                    | -cell3+  | Ð  | -cell4+   | ⊕              | -cell5+  | Ð   | -cell6+  | ⊕  | -<br>cell7+   | Ð  |
|  |   |                                  |  |    |   |   |  |                                      |  |  |   |                |  |   |  |  |   |  |
| snort the  | _ |                                  |  |    |   |   |  |                                      |  |  |   |                |  |   |  |  |   |  |
| connections for  |   | Genera                           | al Description                                     | Pi | n Config  | uratio  | on Regist  | er Se                                | etting   | Jumpe<br>Conne                                 | ections   |                |  |   | Co   | omme   | ents  |  |
| connections for<br>unused cells  |   | Genera                           | al Description                                     | Pi | n Config<br>[MFP12_   | uratio<br>SEL2<br>DE                            | on Regist<br>::MFP12_3<br>EFAULT   | er Se                                | etting   | Jumpe<br>Conne<br>J20[                         | er<br>ections<br>1,2], J7[1,2   | ]              | Conne  | cts Pi  | Co<br>in 12 as V<br>volt   | ommo<br>7SEN<br>age d  | ents<br>NSE to th<br>livider  | e middle of th   |
| connections for<br>unused cells  | • | Genera                           | al Description<br>V7SENSE<br>TS3                   | Pi | n Config<br>[MFP12_<br>[MFP12_                                  | uratio<br>SEL2<br>DE<br>SEL2                    | on Regist<br>::MFP12_9<br>EFAULT<br>::MFP12_9  | ser Se                               | etting<br>]=000<br>]=001   | Jumpe<br>Conne<br>J20[                         | er<br>ections<br>1,2], J7[1,2<br>J20[2,3]   | ]              | Conne  | cts Pi  | Co<br>in 12 as V<br>volt<br>ects Pin 1   | 7SEN<br>age d<br>2 as <sup>-</sup>   | ents<br>NSE to th<br>livider<br>TS3 to a  | e middle of th<br>10k NTC  |
| connections for<br>unused cells<br>Refer to the EVM  |   | Genera<br>Pin<br>12              | Al Description<br>V7SENSE<br>TS3<br>ADCIN1         | Pi | n Config<br>[MFP12_<br>[MFP12_<br>[MFP12_                       | uration<br>SEL2<br>SEL2<br>SEL2                 | on Regist<br>::MFP12_:<br>EFAULT<br>::MFP12_:<br>::MFP12_:   | ser Se                               | etting  <br>]=000<br>]=001<br>]=010  | Jumpe<br>Conne<br>J20[<br>J20[                 | r<br>ctions<br>1,2], J7[1,2<br>J20[2,3]<br>1,2], J7[2,3   | ]              | Connec<br>C<br>Connec<br>between                           | cts Pi<br>Conne<br>cts Pi<br>0 V a  | Co<br>in 12 as V<br>volt<br>ects Pin 1<br>n 12 to Pi<br>ind 1 V to<br>a  | 7SEN<br>age d<br>2 as <sup>-</sup><br>n 1 of<br>have<br>t this   | ents<br>NSE to th<br>livider<br>TS3 to a<br>f J11. Co<br>the ADC<br>pin   | e middle of th<br>10k NTC<br>nnect a volta<br>read the volt  |
| connections for<br>unused cells<br>Refer to the EVM  |   | Genera<br>Pin<br>12              | Al Description V7SENSE TS3 ADCIN1 GPIO             | Pi | n Config<br>[MFP12_<br>[MFP12_<br>[MFP12_<br>[MFP12_            | uration<br>SEL2<br>SEL2<br>SEL2<br>SEL2         | on Regist  | ser Se<br>SELO<br>SELO<br>SELO       | etting  <br>]=000<br>]=001<br>]=010<br>]=011   | Jumpe<br>Conne<br>J20[<br>J20[<br>J20[         | r<br>cctions<br>1,2], J7[1,2<br>J20[2,3]<br>1,2], J7[2,3<br>1,2], J7[2,3                            | ·]<br>-]<br>-] | Connec<br>Connec<br>between<br>Connects                    | cts Pi<br>Conne<br>cts Pi<br>0 V a<br>Pin 1                               | Co<br>in 12 as V<br>volt<br>ects Pin 12<br>in 12 to Pi<br>ind 1 V to<br>a<br>12 to Pin 1                                       | 7SEN<br>age d<br>2 as <sup>-</sup><br>n 1 of<br>have<br>t this   | ents<br>NSE to th<br>livider<br>TS3 to a<br>f J11. Co<br>the ADC<br>pin<br>11. Use t  | e middle of th<br>10k NTC<br>nnect a voltag<br>; read the volt<br>his pin as a C   |
| connections for<br>unused cells<br>Refer to the EVM<br>guide for setting<br>the multi-function |   | Genera<br>Pin<br>12<br>Pin       | Al Description V7SENSE TS3 ADCIN1 GPIO VC7EN       | Pi | n Config<br>[MFP12_<br>[MFP12_<br>[MFP12_<br>[MFP12_<br>[MFP15_ | uration<br>SEL2<br>SEL2<br>SEL2<br>SEL2<br>SEL2 | MFP12_<br>FAULT<br>MFP12_<br>MFP12_<br>MFP12_<br>MFP12_<br>1:MFP12_<br>1:MFP15_<br>FAULT             | SELO<br>SELO<br>SELO<br>SELO         | etting     1       ]=000     1       ]=010     1       ]=011     1       0]=00     1                   | Jumpe<br>Conne<br>J20[<br>J20[<br>J20[         | r<br>cctions<br>1,2], J7[1,2<br>J20[2,3]<br>1,2], J7[2,3<br>1,2], J7[2,3<br>J6[1,2]                 | ·]<br>-]<br>-] | Connect<br>Connects<br>Connects<br>Connects<br>the voltage | cts Pi<br>Conne<br>cts Pi<br>0 V a<br>Pin 1<br>s Pin<br>e divi            | Co<br>in 12 as V<br>volt<br>ects Pin 1<br>ind 1 V to<br>a<br>12 to Pin 1<br>15 (VC7E<br>der so a s<br>is applied               | 2 as <sup>2</sup><br>2 as <sup>2</sup><br>n 1 of<br>have<br>t this<br>I of J <sup>2</sup><br>EN) to<br>caleo<br>d to V | ents<br>NSE to the<br>livider<br>TS3 to a<br>f J11. Co<br>the ADC<br>pin<br>11. Use to<br>the gate<br>d voltage<br>(CTSENS)             | e middle of th<br>10k NTC<br>nnect a voltag<br>read the volt<br>his pin as a G<br>of Q6 to ena<br>of the top of s                  |
| Refer to the EVM<br>guide for setting<br>the multi-function                                    |   | Genera<br>Pin<br>12<br>Pin<br>15 | Al Description V7SENSE TS3 ADCIN1 GPIO VC7EN /DISP | Pi | n Config<br>[MFP12_<br>[MFP12_<br>[MFP12_<br>[MFP15_<br>[MFP15_ | SEL2<br>SEL2<br>SEL2<br>SEL2<br>SEL2<br>SEL2    | MFP12_<br>MFP12_<br>MFP12_<br>MFP12_<br>MFP12_<br>MFP12_<br>IMFP12_<br>IMFP15_<br>EFAULT<br>I:MFP15_ | SELO<br>SELO<br>SELO<br>SELO<br>SELO | etting     ]       ]=000     ]       ]=001     ]       ]=010     ]       ]=011     ]       0]=00     ] | Jumpe<br>Conne<br>J20[<br>J20[<br>J20[<br>J20[ | r<br>ctions<br>1,2], J7[1,2<br>J20[2,3]<br>1,2], J7[2,3<br>1,2], J7[2,3<br>J6[1,2]<br>2,3], J8[1,2] |                | Connect<br>Connects<br>Connects<br>Connects<br>the voltage | cts Pi<br>Conne<br>cts Pi<br>0 V a<br>Pin 1<br>s Pin 1<br>s Pin<br>e divi | Co<br>volt<br>ects Pin 1:<br>n 12 to Pi<br>nd 1 V to<br>a<br>12 to Pin 1<br>15 (VC7E<br>der so a s<br>is applied<br>cts Pin 15 | 7SEN<br>age d<br>2 as 7<br>n 1 of<br>have<br>t this<br>I of J<br>EN) to<br>caled<br>d to V                             | ents<br>NSE to the<br>livider<br>TS3 to a<br>f J11. Co<br>the ADC<br>pin<br>11. Use to<br>the gate<br>d voltage<br>cC7SENS<br>SP) to TF | e middle of th<br>10k NTC<br>nnect a voltag<br>read the volt<br>his pin as a C<br>of Q6 to ena<br>of the top of s<br>E<br>5 and S3 |

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8

In the BQ40z80 EVM user guide, there is a lot of good information on how to configure the EVM. When using the EVM, you may not have a battery pack ready to use, or you may want to use a power supply as a battery stack. A simple way to do that is to connect resistors between the VC terminals and then place the voltage source from ground to the top of stack. When doint this, you won't be able to source or sink, but you will be able to see the voltage measurement at each cell, and configure and calibrate the BQ40z80. The EVM Guide has a simple table that shows you the configuration for each multifunction pin with the corresponding register setting, jumper connection, and any additional comments to help get that EVM set up correctly.

If you are using less than 7S, then short together the higher cell terminal block connections on the EVM as shown.

### Setting up the BQ40z80 for high cell systems



When using BQStudio, you configure the settings in dataflash. To do this, go to the DataMemory tab, then go to the Configuration section, and then to Pin Configuration. You can set the multi-function pins to the desired function. As mentioned, the default configuration is to have VC7EN and V7Sense configured to be used for enabling and measuring the 7<sup>th</sup> cell. You also have to have the cell configuration reflect the number of cells used in the system. In this case, it is shown to have setting 7, which means a 7S configuration.

#### Reading voltages, cell currents, cell powers for cells 5-7

#### Refer to <u>BQ40z80 Technical Reference Manual (TRM)</u>

#### 18.1.63 ManufacturerAccess() 0x007B DAStatus3

This command returns the cell voltages, cell currents, and cell powers for cells 5–7 on *ManufacturerBlockAccess()* or *ManufacturerData()*.

| Status   | Condition   |
|----------|---|
| Activate | 0x007B to ManufacturerBlockAccess() or ManufacturerAccess() |

Action: Output 18 bytes of data on *ManufacturerBlockAccess()* or *ManufacturerData()* in the following format: aaAAbbBBccCCddDDeeEEffFFggGGhhHHiilljj where:

| Value | Description   | Unit |
|-------|---|------|
| AAaa  | Cell Voltage 5  | mV   |
| BBbb  | Cell Current 5. Simultaneous current measured during Cell Voltage 5 measurement | mA   |
| CCcc  | Cell Power 5. Calculated using Cell Voltage 5 and Cell Current 5 data           | cW   |
| DDdd  | Cell Voltage 6  | mV   |
| EEee  | Cell Current 6. Simultaneous current measured during Cell Voltage 6 measurement | mA   |
| FFff  | Cell Power 6. Calculated using Cell Voltage 6 and Cell Current 6 data           | cW   |
| GGgg  | Cell Voltage 7  | mV   |
| HHhh  | Cell Current 7  | mA   |
| llii  | Cell Power 7. Calculated using Cell Voltage 7 and Cell Current 7 data           | cW   |

The TRM provides information on how to read information about voltages, currents, and powers for all the cells. A new ManufacturerAccess command returns this information for cells 5 through 7. However, we provide the bqStudio graphical user interface to simplify this for evaluation.

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### Using BQStudio to read voltages, currents, power



Using BqStudio, go to the Registers tab, and then scroll down to where the cell voltages, cell currents, and cell powers are displayed. You can also use bqStudio to log this data for analysis.

# **Calibrating currents**

- Refer to <u>BQ40z80 Manufacture</u>, <u>Production</u>, and Calibration
- · CC offset calibration is not required
- · Board offset calibration is not required
- 1. Apply a known current of 0 mA, and ensure no current is flowing through the sense resistor connected between the SRP and SRN pins.
- 2. If ManufacturerStatus()[CAL] = 0, send 0x002D to ManufacturerAccess() to enable the [CAL] flag.
- 3. Send 0xF082 to ManufacturerAccess() to enable raw cell voltage output on ManufacturerData().
- 4. Poll ManufacturerData() until ZZ increments by 2 before reading data.
- 5. Obtain the ADC conversion readings of current from ManufacturerData():
   ADC<sub>cc</sub> = AAaa of ManufacturerData()
- Is ADC<sub>cc</sub> < 0x8000? If yes, use ADC<sub>cc</sub>; otherwise, ADC<sub>cc</sub> = -(0xFFF AAaa + 0x0001).
  6. Average several readings for higher accuracy. Poll *ManufacturerData()* until ZZ increments to indicate that updated values are available:
- ADC<sub>cc</sub> = [ADC<sub>cc</sub>(reading n) + ... + ADC<sub>cc</sub>(reading 1)]/n
- 7. Read Coulomb Counter Offset Samples from data flash.
- 8. Calculate offset value:
- CC offset = ADC<sub>CC</sub> × (Coulomb Counter Offset Samples)
- 9. Write the new CC Offset value to data flash.
- 10. Re-check the current reading and if it is not accurate, repeat steps 1 10.
- 11. Send 0x002D to ManufacturerAccess() to clear the [CAL] flag if all calibration is complete.

#### 2.5 Current Calibration

A diagram of current calibration is shown in Figure 5.



Figure 5. Current Calibration

2.5.1 CC Offset Calibration

NOTE: Due to hardware improvements in this device, CC Offset calibration is not necessary. Only run the CC Offset Calibration procedure if current is observed when no current should be present.

#### 2.5.2 Board Offset Calibration

NOTE: Due to hardware improvements in this device, Board Offset calibration is not necessary. Only run the Board Offset Calibration procedure if board offset current is observed.



12

To calibrate the device, you can do it manually following the process in the app note for BQ40z80 manufacture, production and calibration. No CC offset calibration is necessary on the bq40z80, but just in case it is, the app note has how to do that. Also, there should not be an board offset calibration required either, but again, just in case you experience that in your system, we have detailed instruction on how to perform that in the app note.



An easier way it to do all the calibration with the BQStudio GUI. When you click on the Calibration tab, a window will pop up that shows all the calibration options. The device firmware comes programmed with a value that is likely close to the final gain value, but it needs to be calibrated to your specific board. The instructions for calibrating the current are simple:

\*Connect and measure a 2-A current source from 1N (–) and Pack– (+) to calibrate without using the FETs. (TI does not recommend calibration using the FETs.)

\*Enter –2000 in the Applied Current field and select the Calibrate Current box.

\*Press the Calibrate Gas Gauge button to calibrate.

\*Deselect the Calibrate Current box after current calibration has completed.



Calibrating voltages is also needed, and can be accomplished on the same Calibration tab. All of the voltage calibration can be done at the same time.

\*Measure the voltage from 1P to 1N (VSS) and enter this value in the Applied Cell 1 Voltage field and select the Calibrate Voltage box.

\*Measure the voltage from 6P to 1N (VSS) and enter this value in the Applied VC6-VSS Voltage field and select the Calibrate Battery Voltage box.

\*Measure the voltage from Pack+ to Pack– and enter this value in the Applied Pack Voltage field and select the Calibrate Pack Voltage box. If the voltage is not present, then turn the charge and discharge FETs on by entering a 0x0022 command in the Manufacturer Access register on the Register screen.

\*If the device is configured for 7S, measure the voltage from 7P to 1N (VSS) and enter this value in the Applied Cell-7 Positive Terminal Voltage field and select the Calibrate Battery Voltage box.

\*Press the Calibrate Gas Gauge button to calibrate the voltage measurements.

\*Deselect the Calibrate Voltage boxes after voltage calibration has completed.

\*Note that calibration of the temperature sensors can also be done as well. The BQ40z80 has up to four TS inputs, and all can be calibrated on this screen.

#### How to use MFPs as ADC or thermal sense pins

- The BQ40z80 has many multi-function pins
- Pins 12 and 13 can be configured as ADC or TS pins
- The EVM jumpers can easily be configured to change the behavior of these pins
- The Pin Configuration Register in BQStudio controls the behavior

| Gener   | al Description | Pin Configuration Register Setting     | Jumper<br>Connections | Comments  |
|---------|----------------|--|-----------------------|---|
| V7SENSE | V7SENSE        | [MFP12_SEL2:MFP12_SEL0]=000<br>DEFAULT | J20[1,2], J7[1,2]     | Connects Pin 12 as V7SENSE to the middle of the<br>voltage divider  |
| Pin     | TS3            | [MFP12_SEL2:MFP12_SEL0]=001            | J20[2,3]              | Connects Pin 12 as TS3 to a 10k NTC   |
| 12      | ADCIN1         | [MFP12_SEL2:MFP12_SEL0]=010            | J20[1,2], J7[2,3]     | Connects Pin 12 to Pin 1 of J11. Connect a voltage<br>between 0 V and 1 V to have the ADC read the voltage<br>at this pin |
|         | GPIO           | [MFP12_SEL2:MFP12_SEL0]=011            | J20[1,2], J7[2,3]     | Connects Pin 12 to Pin 1 of J11. Use this pin as a GPIO   |
|         | /DISP          | [MFP13_SEL2:MFP13_SEL0]=000<br>DEFAULT | J21[1,2], J14[1,2]    | Connects Pin 13 (/DISP) to TP5 and S3   |
| Din     | TS4            | [MFP13_SEL2:MFP13_SEL0]=001            | J21[2,3]              | Connects Pin 12 as TS4 to a 10k NTC   |
| 13      | ADCIN2         | [MFP13_SEL2:MFP13_SEL0]=010            | J21[1,2], J14[2,3]    | Connects Pin 13 to Pin 5 of J11. Connect a voltage<br>between 0 V and 1 V to have the ADC read the voltage<br>at this pin |
|         | GPIO           | [MFP13_SEL2:MFP13_SEL0]=011            | J21[1,2], J14[2,3]    | Connects Pin 13 to Pin 5 of J11. Use this pin as a GPIO   |

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15

In order to use all four TS inputs, the multifunction pins must be configured appropriately on the EVM.

The BQ40z80 has two dedicated TS inputs, which may not be enough for applications with a high cell count, so the multifunction pins can be used as TS3 and TS4 as well.

Make sure the jumper connections on the board, as well as the register settings are configured properly.

The pin configuration register in BqStudio controls the behavior.

The TS inputs can be configured to report as a FET temperature in DAStatus2() by setting the corresponding flag in Temperature Mode and DA Configuration[FTEMP].

When configured this way, the TS input is not used in the gauging or aldvanced charge algorithm simulations.

## The MFP's can also be configured as GPIO's

| Refer to section 13 of the <u>TRM</u> for configuration details              |
|--|
| Use Pin Configuration to use these as GPIOs                                  |
| GPIO capabilities are dependent on the pin                                   |
| GPIOs can be input or output   |
| GPIOs behavior in Sealed Mode can be read only or controlled                 |
| GPIOs can be configured as output low, output high, or high-Z                |
| GPIOs can be configured to generate interrupts using a flag mapping function |

|   | PARAMETER   | CONDITIONS   | MIN                                       | TYP               | MAX                         | UNIT                |  |
|---|---|--|---|-------------------|-----------------------------|---------------------|--|
| Low-Voltag                                  | ge General Purpose I/O (Multifunction Pins  | 12 and 13 configured as GPIO)  | 1   |                   |                             |                     |  |
| VIH   | High-level input  |  | 0.65 ×<br>V <sub>REG</sub>                |                   |                             | V                   |  |
| VIL   | Low-level input   |  |   |                   | 0.35 ×<br>V <sub>REG</sub>  | V                   |  |
|   | Output veltage high   | Output High, Pull-up Enabled, I <sub>OH</sub> = -1.0 mA  | 0.75 ×                                    |                   |                             | N                   |  |
| VOH   | Output voltage high   | Output High, Pull-up Enabled, I <sub>OH</sub> =<br>-10 μA  | V <sub>REG</sub>                          |                   |                             | v                   |  |
| V <sub>OL</sub>                             | Output voltage low  | Output Low, I <sub>OL</sub> = 1mA  |   |                   | 0.2 ×<br>V <sub>REG</sub>   | V                   |  |
| CIN   | Input capacitance   |  |   | 5                 |                             | pF                  |  |
| I <sub>LKG</sub>                            | Input leakage current   |  |   |                   | 1                           | μA                  |  |
| High-Volta<br>as VC7EN)                     | ge General Purpose I/O (Multifunction pins<br>(Pin 16 configured as PDSG)   | 15, 16, 17 configured as GPIO, PRES  | , DISP, or S                              | HUTDN)            | (Pin 15 c                   | onfigured           |  |
| VIH   | High-level input  |  | 1.3                                       |                   |                             | V                   |  |
| VIL   | Low-level input   |  |   |                   | 0.55                        | V                   |  |
| V   | Output voltage high   | Output enabled, $\lor_{BAT}$ > 5.5 $\lor,$ $I_{OH}$ = –0 $\mu A$   | 3.5                                       |                   |                             | V                   |  |
| ¥ OH  | Oulput Voltage high   | Output enabled, $\lor_{BAT}$ > 5.5 $\lor,$ $I_{OH}$ = –10 $\mu A$  | 1.8                                       |                   |                             | v                   |  |
| V <sub>OL</sub>                             | Output voltage low  | Output disabled, I <sub>OL</sub> = 1.5 mA  |   |                   | 0.4                         | V                   |  |
| CIN   | Input capacitance   |  |   | 5                 |                             | pF                  |  |
| I <sub>LKG</sub>                            | Input leakage current   |  |   |                   | 1                           | μA                  |  |
| R <sub>O</sub>                              | Output reverse resistance   | Between GPIO, PRES, DISP,<br>SHUTDN, VC7EN, PDSG, and PBI  | 8   |                   |                             | kΩ                  |  |
| General Pu                                  | urpose I/O (Multifunction Pins 20, 21, 22 co  | nfigured as GPIO) (Pin 20 configured   | as PDSG)                                  |                   |                             |                     |  |
| 1/  | High-level input  |  | 1.45                                      |                   |                             | V                   |  |
| VIH   | riigii-level ilipat   |  |   |                   | 0.55                        | V                   |  |
| VIH<br>VIL                                  | Low-level input   |  |   |                   | 0.55                        |                     |  |
| VIL<br>VOH                                  | Low-level input   | Output enabled, V <sub>BAT</sub> > 3.0 V, I <sub>OH</sub> =<br>-22.5 mA  | V <sub>BAT</sub> –<br>1.6                 |                   | 0.55                        | V                   |  |
| VIL<br>VIL                                  | Low-level input   | Output enabled, V <sub>BAT</sub> > 3.0 V, I <sub>OH</sub> =<br>-22.5 mA<br>Output disabled, I <sub>OL</sub> = 3 mA   | V <sub>BAT</sub> –<br>1.6                 |                   | 0.55                        | V<br>V              |  |
| VIL<br>V <sub>IL</sub><br>V <sub>OH</sub>   | Low-level input<br>Output voltage high<br>High level output current protection  | Output enabled, V <sub>BAT</sub> > 3.0 V, I <sub>OH</sub> =<br>-22.5 mA<br>Output disabled, I <sub>OL</sub> = 3 mA   | V <sub>BAT</sub> −<br>1.6<br>−30          | -45               | 0.55                        | V<br>V<br>mA        |  |
| VIH<br>VIL<br>VOH<br>I <sub>SC</sub><br>IOL | Low-level input<br>Output voltage high<br>High level output current protection<br>Low level output current                      | Output enabled, ∨ <sub>BAT</sub> > 3.0 ∨, I <sub>OH</sub> =           -22.5 mA           Output disabled, I <sub>OL</sub> = 3 mA           ∨ <sub>BAT</sub> > 3.0 ∨, ∨ <sub>OL</sub> > 0.4 ∨ | V <sub>BAT</sub> −<br>1.6<br>−30<br>15.75 | -45<br>22.5       | 0.55<br>0.4<br>-60<br>29.25 | V<br>V<br>mA<br>mA  |  |
| VIH<br>VIL<br>VOH<br>ISC<br>IOL<br>CIN      | Low-level input<br>Output voltage high<br>High level output current protection<br>Low level output current<br>Input capacitance | Output enabled, ∨ <sub>BAT</sub> > 3.0 ∨, I <sub>OH</sub> =           -22.5 mA           Output disabled, I <sub>OL</sub> = 3 mA           ∨           VBAT > 3.0 ∨, ∨ <sub>OL</sub> > 0.4 ∨ | V <sub>BAT</sub> −<br>1.6<br>−30<br>15.75 | -45<br>22.5<br>20 | 0.55<br>0.4<br>-60<br>29.25 | V<br>MA<br>mA<br>pF |  |



Since the BQ40z80 can be used in a wide variety of applications, and the applications can have a wide variety of requirements for system level function, one of the new additions to the BQ40z80 is the ability to configure several pins, up to eight, as general purpose input/output pins, or GPIO.

The capabilities of the GPIO depend on the pin chosen, and the capabilities are detailed in the BQ40z80 datasheet.

There are two low-voltage GPIO on pins 12 and 13. There are three high-voltage GPIO on pins 15, 16, and 17.

There are 3 GPIO on pins 20, 21, and 22 that are normally configured as LED outputs, so they can sink higher current than the other GPIO.

The GPIO can be configured as input or output, and can be configured as output low, output high, or high-z.

The default configuration of all the MFP's is as high-z, to enable a safe state for configuration during production.

# **Using GPIOs**

#### 18.43 0x48 GPIORead()

This read-only command returns an 8-bit field, with each bit providing the input level read from each of the eight pins that can be configured as GPIOs. The command returns valid data for all pins configured as GPIO, including those configured to drive an output.

| SBS  | Nama       |    | Access |    | Protocol | Tune | Min  | Max   | Default | Unit |
|------|------------|----|--------|----|----------|------|------|-------|---------|------|
| Cmd  | Name       | SE | US     | FA | FIOLOCOT | Type | MIII | IVIAX | Delault |      |
| 0x48 | GPIORead() | R  | R      | R  | Word     | U2   | —    | 65535 | 0       | —    |

#### 18.44 0x49 GPIOWrite()

as GPIO, including those configured to drive an output.

This write-only command is used to set the output drive of each GPIO pin configured as a GPIO. The data associated with pins not configured as GPIOs is not impacted. The format of the command is a 16-bit field, with 2-bits associated with each GPIO pin. These two bits set the output drive status as: 00 = drive output low, 01 = drive output high, 10 = set output high-Z, and 11 = set output high-Z.

| SBS  | Name        |    | Access |    | Protocol | Type | Min   | Max   | Default | Unit |
|------|-------------|----|--------|----|----------|------|-------|-------|---------|------|
| Cmd  | Name        | SE | US     | FA | FIOLOCOI | Type | WIIII | IVIAA | Delaun  | Unit |
| 0x49 | GPIOWrite() | W  | W      | W  | Word     | U2   | _     | 65535 | 0       | —    |

| 15         | 14         | 13          | 12                        | 11          | 10           | 9               | 8             |  |
|------------|------------|-------------|---------------------------|-------------|--------------|-----------------|---------------|--|
| RL         | 2          | R           | L1                        | R           | L0           | RH2             |               |  |
| LEDCNTLC/0 | SPIO RSVD  | LECDNTLB/   | GPIO RSVD                 | LEDCNTLA/PD | SG/GPIO RSVD | VC7EN/DISP/GPIO |               |  |
| 7          | 6          | 5           | 4                         | 3           | 2            | 1               | 0             |  |
| RH         | 1          | RI          | RH0                       |             | or AD3       | RC2 0           | or AD2        |  |
| CB7EN/PDSG | /GPIO RSVD | PRES/SHUTDN | PRES/SHUTDN/DISP/GPIO TS1 |             | DCIN2/GPIO   | V7SENSE/TS3     | 3/ADCIN1/GPIO |  |

Using the GPIO's is straight-forward. Use the GPIORead() command to reutn an 8-bit field, with each bit providing the input level read from each of the eight pins that can be configured as GPIOs. The command returns valid data for all pins configured

Use the GPIOWrite() command to set the output drive of each GPIO pin configured as a GPIO. The format of the command is a 16-bit field, with 2-bits associated with each GPIO pin. This is shown in this map. These two bits set the output drive status as 00 = drive output low, 01 = drive output high, 10 or 11 = set output high-Z.

17

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#### **Example of GPIO as an interrupt**

| OperationStatus()[XCHG]<br>- Set FlagMapSetUp0[FLAG_POL:0] = 0 for no<br>change in the polarity of the flag<br>- Set FlagMapSetUp0[FLAG_GPIO2:0] = 0x7 for<br>the RC2 pin<br>- Set FlagMapSetUp0[FLAG_OR] = 1 for the OR<br>operation<br>- Set FlagMapSetUp0[FLAG_OD] = 0 for driven-<br>high/driven low | <ul> <li>Set FlagMapSetUp0[FLAG_EN] = 1 to enable the control</li> <li>Set FlagMapSetUp0[FLAG_REG2:0] = 0x02 for OperationStatus()</li> <li>Set FlagMapSetUp0[FLAG_BIT4:0] = 0x00 for</li> <li>OperationStatus()[PRES]</li> <li>Set FlagMapSetUp0[FLAG_POL:0] = 0 for no change in the polarity of the flag</li> <li>Set FlagMapSetUp0[FLAG_GPIO2:0] = 0x7 for the RC2 pin</li> <li>Set FlagMapSetUp0[FLAG_OR] = 0 for the OR operation</li> <li>Set FlagMapSetUp0[FLAG_OD] = 0 for driven-high/driven-low</li> </ul> |
|--|---|
| <ul> <li>Set <i>FlagMapSetUp0[FLAG_EN]</i> = 1 to enable the control</li> <li>Set <i>FlagMapSetUp0[FLAG_REG3:0]</i> = 0x02 for <i>OperationStatus()</i></li> <li>Set <i>FlagMapSetUp0[FLAG_BIT4:0]</i> = 0x0E for</li> </ul>   | <ul> <li>Set FlagMapSetUp0[FLAG_GPI02:0] = 0x7 for the RC2 pin</li> <li>Set FlagMapSetUp0[FLAG_OR] = 1 for the OR operation</li> <li>Set FlagMapSetUp0[FLAG_OD] = 0 for driven-high/driven low</li> <li>Configure the third control register FlagMapSetUp2 to map</li> <li>OperationStatus()[PRES]</li> <li>Set FlagMapSetUp0[FLAG_EN] = 1 to enable the control</li> </ul>   |
| <ul> <li>either OperationStatus()[PRES] and</li> <li>either OperationStatus()[XCHG] is set or</li> <li>BatteryMode()[CF] is set</li> <li>Configure the first control register FlagMapSetUp0</li> <li>to map OperationStatus()[XCHG]</li> </ul>   | <ul> <li>Set FlagMapSetUp0[FLAG_EN] = 1 to enable the control</li> <li>Set FlagMapSetUp0[FLAG_REG2:0] = 0x00 for BatteryMode()</li> <li>Set FlagMapSetUp0[FLAG_BIT4:0] = 0x07 for BatteryMode()[CF]</li> <li>Set FlagMapSetUp0[FLAG_POL:0] = 0 for no change in the polarity of the flag</li> </ul>   |
| Example: Configure <i>FlagMapSetUp0.2</i> to trigger the active high interrupt on RC2 (pin 12) only when   | <ul> <li>Configure the second control register <i>FlagMapSetUp1</i> to map<br/><i>BatteryMode()[CF]</i></li> </ul>  |

The bq40z80 supports generating interrupts on pins configured as GPIOs. It includes a flag mapping function for these pins, which is a bank of eight control registers, *FlagMapSetUp0..8*, that enable up to eight separate flags in the device to be mapped to one or more GPIO pins. Flags may be OR'ed or AND'ed together to trigger an interrupt on a particular GPIO pin. For example, up to eight different flags can be OR'ed onto a single GPIO pin or up to seven flags are OR'ed together then AND with the 8th flag to trigger an interrupt.

On this page is an example for using a GPIO as an interrupt based on three specific conditions. In this case, I am using FlagMapSetUp0.2 to trigger the active high interrupt on Pin 12 only when the battery is interted and either XCHG is set or CF is set.

OperationStatus[Pres] tells me when the presence pin is pulled low, indicating the battery is inserted into the system.

OperationStatus[XCHG] tells me when when charging is disabled. If XCHG is set to 1, then I know that charging is disabled.

OperationStatus[CF] tells me the status of the condition flag. If CF is set to 1, then I know that MaxError is greater than the Max Error Limit, and a condition cycle is needed.

\*The first step is to set the flag\_EN bit to 1, to enble the control

\*Next is to set flag\_reg bits to select which register contains the flag. There are registers available are batterymode, batterystatus, operationstatus, chargingstatus, tempstatus, gaugingstatus, Itstatus, safetystatus, and Pfstatus. In this case, OperationStatus is set by selecting 0x02.

\*Next is to use Flag\_Bit to select which bit in the resister is used. In this case 0x0E is selected for the XCHG bit. Since I don't want to change the polarity of the bit when monitoring it, I leave the FLAG\_POL bit set to 0.

\*In order to map the interrupt to Pin 12, I set FLAG\_GPIO to 0x7.

\*Now for the logic – I have the FLAG\_OR set to 1 for the OR operation, and the FLAD\_OD set to 0 to select driven high/driven low. The other option is to set it to 1 and have it be high-z/driven low.

\*I follow the same process for the CF bit.

\*Finally, I configure the PRES bit in a like manner.

As you can see, this is a very powerful addition to the BQ40z80, and provides a way to have interrupts generated without having to poll the device for status. For many applications that are on a dock or in a lower power mode much of the time, this can have

a large impact on the total run time, as well as the robustness of the system.

#### Need higher currents and/or capacity?



So with higher cell counts, it is likely that the capacity and currents are also higher than with the bq40z50. Although the BQ40z50 and BQ40z80 natively support pack capacities up to 29Ah and battery currents up to 32A, the BQ40z80 includes a scale factor that can be set between 0 and 100 to "scale up" the currents seen by the coulomb counter. Setting the scale factor to 0 disables the scaling. When using scaling, reading the higher current is done with the CurrentLong function. All other currents and capacities are reported as non-scaled values and the host must multiply the value by the scale factor. All protections must be divided by the scale factor. The design capacity mAh and design capacitycWh must be scaled in data flash, and all current and capacity parameters in the data flash are divided by the scale factor. The scale factor. The scale factor is also used to calibrate the pack, so if -4000mA is entered as the actual current, it does not need to be scaled.

#### Do you want more resolution on the LED display?

| BQ40750     | Range      | Parameter<br>name | Example<br>threshold | Behavior   |
|-------------|------------|-------------------|----------------------|--|
| supports up | 90 to 100% | CHG<br>Thresh 6   | 90%                  | LED6 on solid if above 90%, off if SOC below threshold |
| to 5 LEDs   | 80 to 90%  | CHG<br>Thresh 5   | 80%                  | LED6 on solid if above 80%, off if SOC below threshold |
|             | 60 to 80%  | CHG<br>Thresh 4   | 60%                  | LED6 on solid if above 60%, off if SOC below threshold |
| BQ40z80     | 40 to 60%  | CHG<br>Thresh 3   | 40%                  | LED6 on solid if above 40%, off if SOC below threshold |
| supports up | 20 to 40%  | CHG<br>Thresh 2   | 20%                  | LED6 on solid if above 20%, off if SOC below threshold |
| to 6 LEDs   | 0 to 20%   | CHG<br>Thresh 1   | 0%                   | LED6 on solid if above 0%, off if SOC below threshold  |
|             |            |                   |                      |  |



20

The BQ40z80 has an LED display that shows various status information when the display button is pressed. The LED display is available in sleep mode, but disabled during device shutdown or under CUV conditions. The LED can be used even under PF conditions if configured that way. With the BQ40z80, up to 6 LEDs can be driven in charlieplexing mode from three LED outputs. The LEDs show the relative state of charge or absolute state of charge depending on the LEDMODE setting. The display stays on for LED Hold Time. These can be configured in the dataflash.

The BQ40z80 even has alarms that can be set for the LEDs to flash if certain SOC thresholds are reached.

## How to get 12 effective steps with BQ40z80

- Use BLINKMIDPT = 1
- Segments will blink until they reach the midpoint between thresholds
- LED blink period is adjustable



| Range      | Parameter<br>name | Example<br>threshold | Behavior   |
|------------|-------------------|----------------------|--|
| 95 to 100% | CHC Throah 6      | 00%                  | LED6 on solid if above 95%, off if SOC below threshold |
| 90 to 95%  | CHG Milesii o     | 90 %                 | LED6 on blink if above 90%, off if SOC below threshold |
| 85 to 90%  | CHG Thresh 5      | 80%                  | LED6 on solid if above 85%, off if SOC below threshold |
| 80 to 85%  | CHO Miesir 5      | 0078                 | LED6 on blink if above 80%, off if SOC below threshold |
| 70 to 80%  | CHG Thresh 4      | 60%                  | LED6 on solid if above 70%, off if below               |
| 60 to 70%  | ono miesir 4      | 0070                 | LED6 on blink if above 60%, off if SOC below threshold |
| 50 to 60%  | CHG Thresh 3      | 40%                  | LED6 on solid if above 50%, off if below               |
| 40 to 50%  | ono miesiro       | 4070                 | LED6 on blink if above 40%, off if SOC below threshold |
| 30 to 40%  | CHG Thresh 2      | 20%                  | LED6 on solid if above 30%, off if below               |
| 20 to 30%  | ono miesirz       | 2070                 | LED6 on blink if above 20%, off if SOC below threshold |
| 10 to 20%  | CHG Thresh 1      | 0%                   | LED6 on solid if above 10%, off if below               |
| 0 to 10%   | ono mean r        | 070                  | LED6 on blink if above 0%, off if SOC below threshold  |

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21

Additionally, the LED can be configured to blink until the midpoint of each LED segment is reached by setting BLINKMIDPT to 1. This effectively gives twice the number of segments to show the state of charge, or 12 levels from empty to full.

#### How to use the PDSG function with capacitive loads



Some loads, like motors, have starting caps that can demand large currents during startup. This large current may trip protections in the pack, effectively shutting down the system. To solve this dilemma, the BQ40z80 has a way to pre-charge the output, effectively softstarting the load to make sure the over-current protections aren't reached. The pre-charge function is similar in the charge direction, directly driving the pre-charge PFET. However, the pre-discharge is only able to drive an NFET, which in turn drives the PFET for pre-discharge. The PDSG Level is set to determine when the PDSG FET turns off, and is in terms of a percent of the top o fo the cell stack, or BAT voltage. When the PDSG Level is reached, or the PDSG Timeout is reached, the PDSG FET turns off and the DSG FET turns on. The PDSG current is adjustable through the resistor from the PDSG PFET to PACK.



### Asymmetric loads and charging currents?

The BQ40z80EVM is configured where the CHG and DSG FETs are in series. This means that when charging, current flows through both FETs, and when discharging, current flows through both FETs. The gauge implements protection for the CHG FET so that in series configuration, if the CHG FET is off and the DSG FET is on, and if discharge current greater than Charge *Current Threshold* is detected, the CHG FET is turned on quickly to protect the CHG FET body diode from discharge current flowing through it. This is the proper operation for FETs configured in series, but what about parallel configuration? Why would you need that?



In many high cell applications, the discharge current may be an order of magnitude greater than the charge current. For example, it is not uncommon for cordless vacuum cleaners to approach 20A discharge currents, yet only charge at 2A or less. In this case, if the DSG and CHG FETs are in series, they both need to be sized for the highest current to minimize power loss as well as control temperature of the FET. The bq40z80 includes support for a circuit configuration where the CHG and DSG FETs are in parallel rather than in series, allowing for the charge FET to be higher Rdson, smaller packaging, and lower cost. This also saves the power loss through the CHG FET during discharge, getting the most out of the battery for the load.

In Parallel configuration, if the CHG FET is off and the DSG FET is on, then the CHG FET is not turned on if discharge current is detected since these paths are completely independent.

The BQ40z80 EVM does not support the parallel configuration right now, but a TI design is planned for the future.



**Cell balancing with 7S configuration** 

Finally, what if you need cell balancing for all the cells in your application?

Good news that the BQ40z80 has internal cell balancing for 6 cells, and supports external cell balancing for the 7<sup>th</sup> cell. All 7 cells can be set up for external cell balancing if higher balance currents are needed. Refer to section 8 of the TRM for details on the cell balancing, which provides the calculations needed to set the balance time based on the internal or external balancing circuits. Cells 1-6 are calculated, and there is a separate calculation for the 7<sup>th</sup> cell.

Thanks for taking the time to learn how the BQ40z80 2S-7S battery pack manager can solve some of the common challenges for high cell count applications. If you have other challenges you need help with, please submit them on e2e.ti.com. Thanks!