High VOLT Interactive

Where power supply design meets collaboration

How to protect SiC MOSFETs… the best way!

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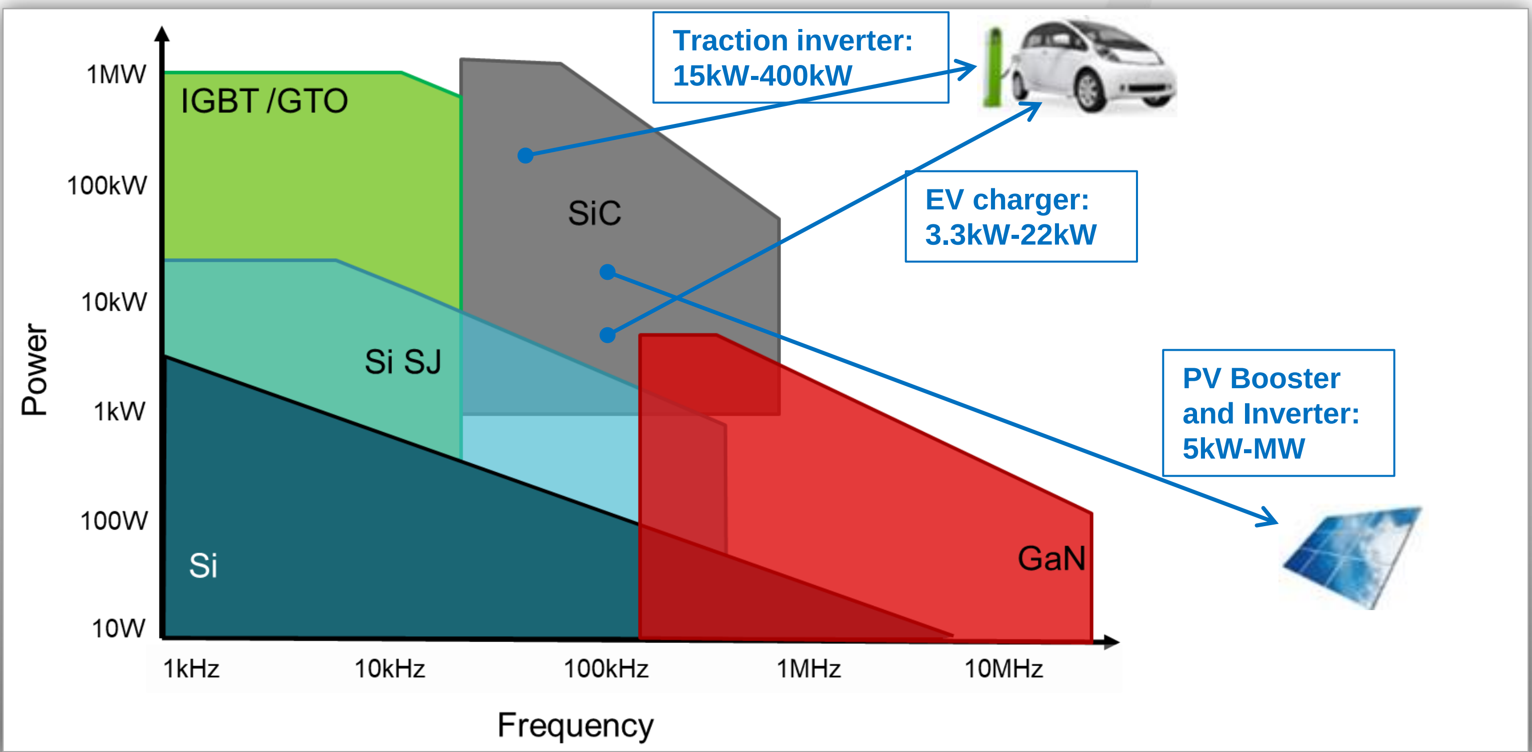
What will I get out of this session?

- What are SiC MOSFET advantages compared with Si MOSFET and IGBT
- Different short circuit current sensing and protection methods
- How to safely turn off MOSFET under short circuit

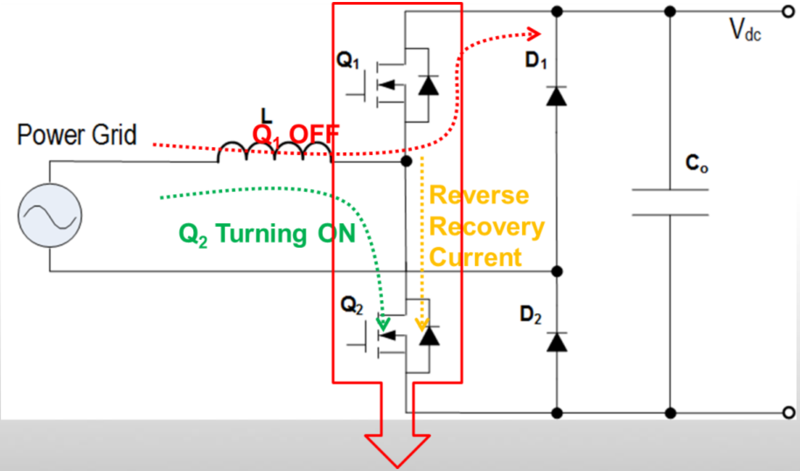
- Relevant part numbers:
  - UCC2152x
  - ISO585X
- Relevant reference designs:
  - TIDA-01604&5
  - ISO5852SDWEVM-017
  - TIDA-00917
- Relevant applications:
  - Solar Inverter, HEV/EV Traction Inverter, EV On-Board Charger, Charging Pile

SiC MOSFET Application Positioning

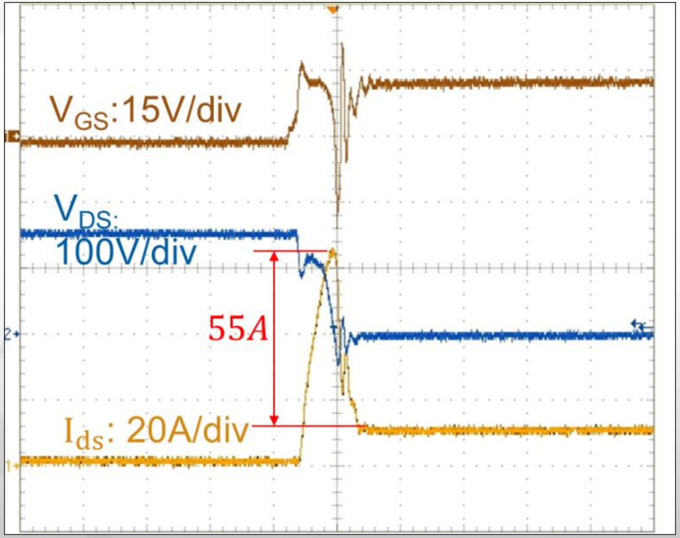


SiC MOSFET Advantages over Si MOSFET

1) **Lower specific Rds(on) especially for >650V devices; 2) Low body diode reverse recovery.**



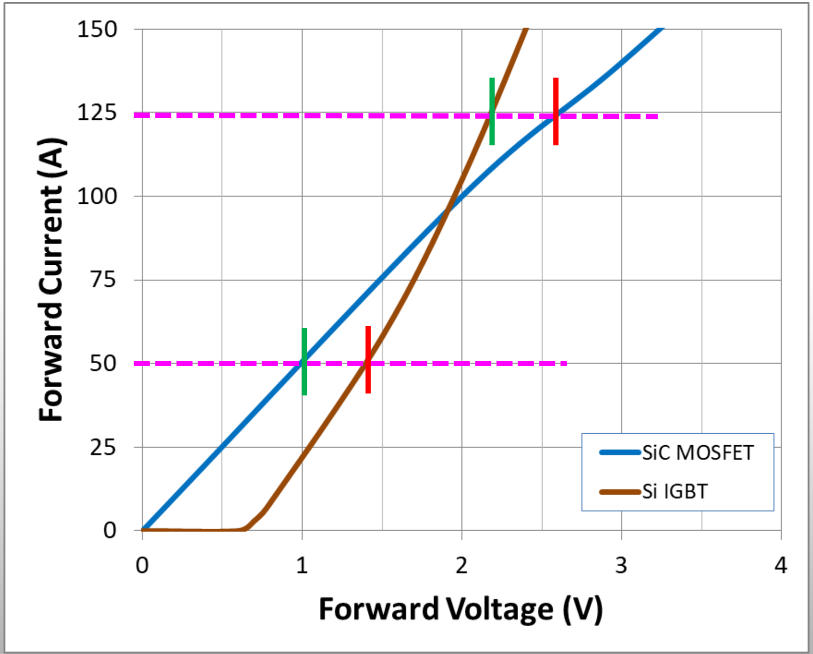
Use SiC , GaN devices or Si IGBT!

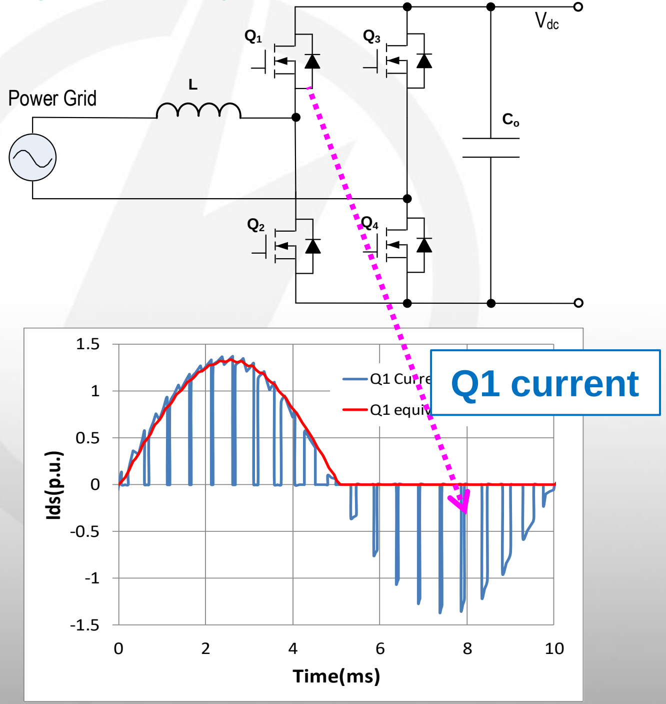


SJ-MOSFET Reverse Recovery at Vdd=150V, Idd=10A

SiC MOSFET Advantages over Si IGBT: Conduction

1) No 0.5-1.0V knee voltage; 2) Has "body diode"; 3) 3rd quadrant operation mode.





SiC MOSFET Advantages over Si IGBT: Switching

❑ Low switching loss:

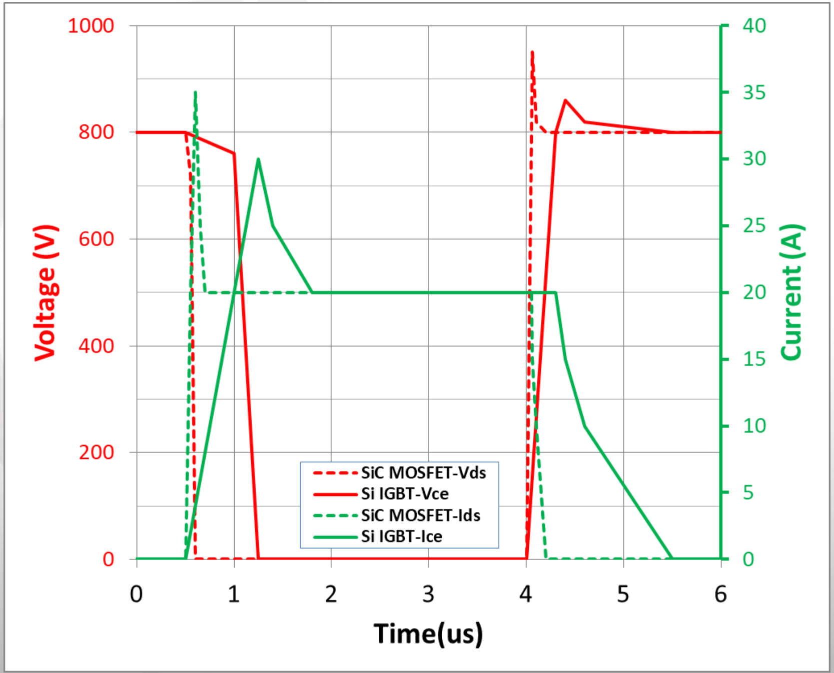
MOSFET (unipolar) vs IGBT (bipolar)- fundamental difference;

❑ Switch loss less increase at elevated temperatures:

For 1000V SiC MOSFET, Esw@25˚C = Esw@150˚C

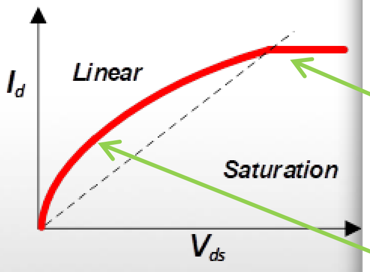
❑ Low reverse recovery for the body diode:

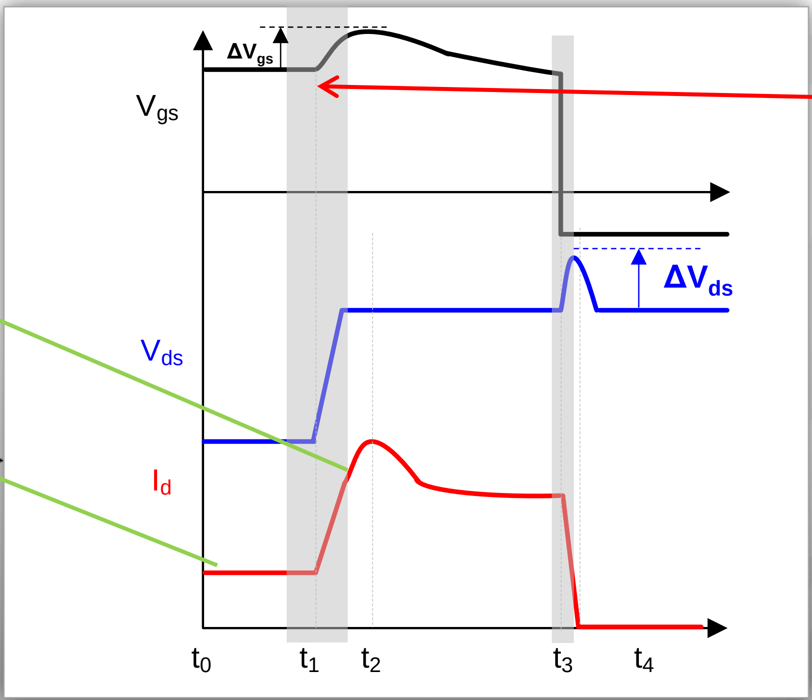
Silicon PiN diode has significant reverse recovery which has reverse recovery loss and also adds more turn on loss.

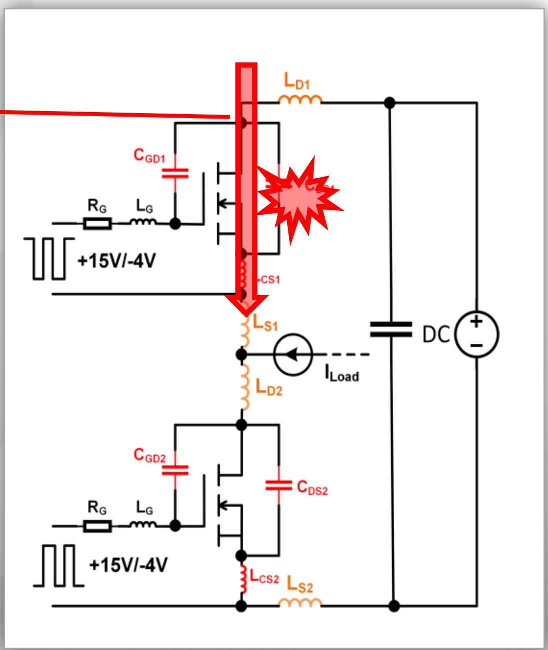


Typical switching waveforms

Overcurrent/Short Circuit Fault

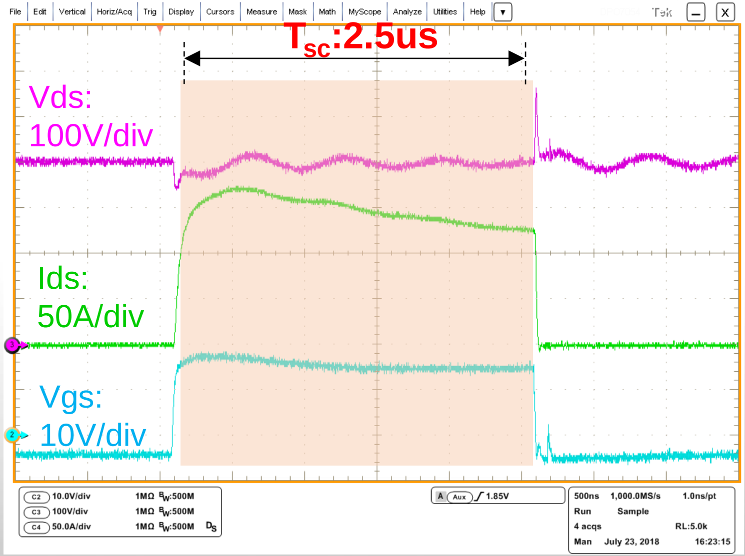






Short circuit happens at t1:

Overcurrent/Short Circuit Fault Mechanism: Thermal limitation

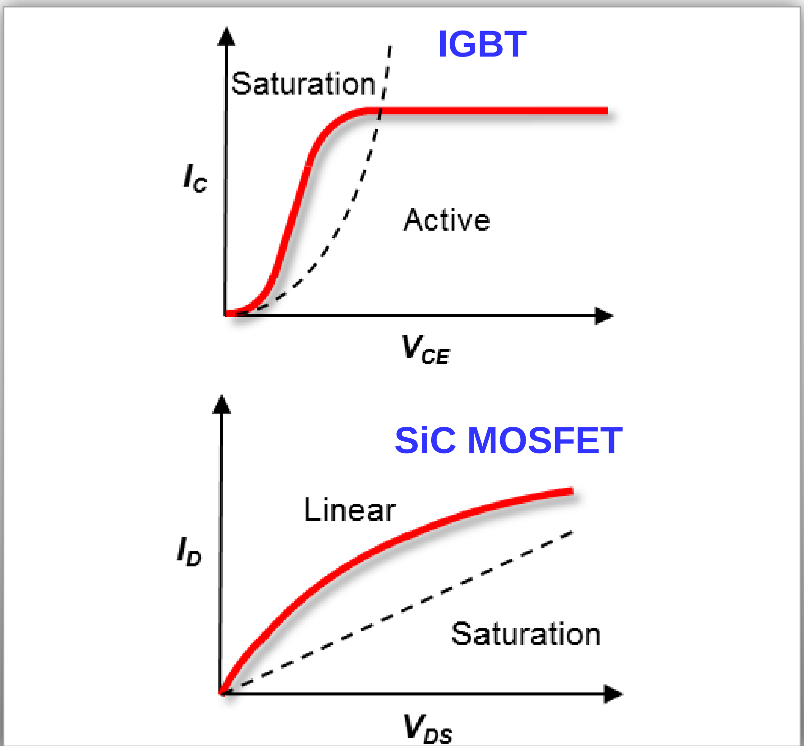


- The short circuit withstand time t_{sc} is determined by the critical energy
  - minimal dissipated energy leading to device failure for one short circuit pulse

$$E_c = \int_{t_1}^{t_3} V_{ds} \cdot I_d \cdot dt$$

  - Vds is the DC link volatge, Id will be the device saturation current.
- SiC MOSFET short circuit withstand time is shorter than IGBT due to smaller chip size, less thermal capacity.

Overcurrent/Short Circuit Fault Mechanism: Thermal limitation



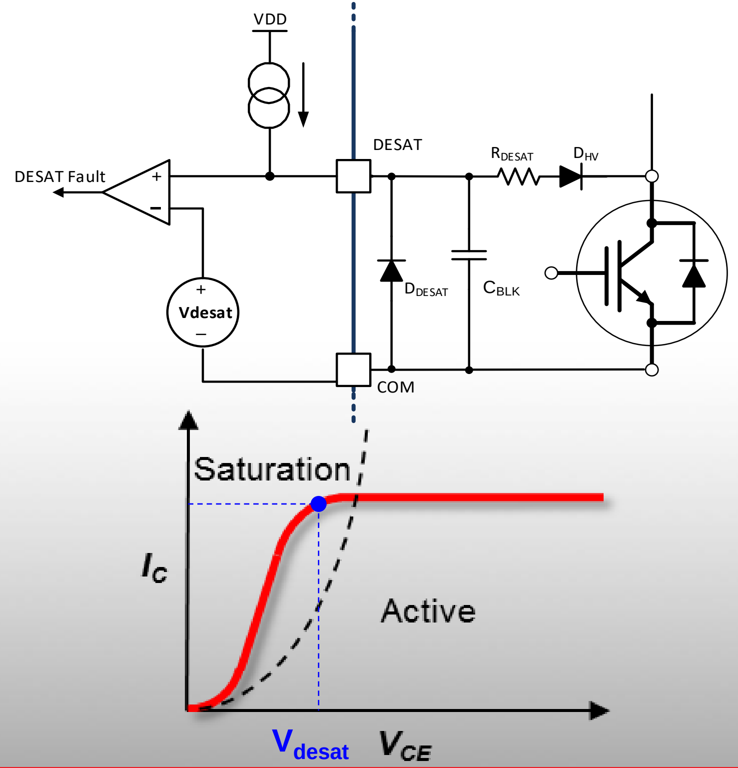
- ***IGBT self-limits the current increase with lower saturation current***
  - shape transient from saturation region to active region, collector current is limited to a constant value in active region
- ***SiC MOSFET has large linear region with high saturation current***
  - In the case of SiC, I_d continues to increase with increase in V_{ds}, eventually resulting in faster breakdown
- ***For same rated current & voltage, IGBT reaches active region for significantly lower VCE as compared to SiC MOSFET***

Question: From thermal limitation point of view, what is the typical SiC MOSFET short circuit withstand time (for example 1200V MOSFET in TO247 package used for 800V dc bus)?

- A) <1us
- B) 1-3us
- C) 3-10us
- D) >10us

Answer: B) 1-3us (under typical Vds and recommended Vgs conditions)

Overcurrent/Short Circuit Protection Method: DESAT



- Desaturation circuit detects the V_{ds} of MOSFET or V_{ce} of IGBT, protection is triggered when detected voltage is above pre-set reference voltage
- Blanking time is needed to prevent false trigger during switching turn on transients

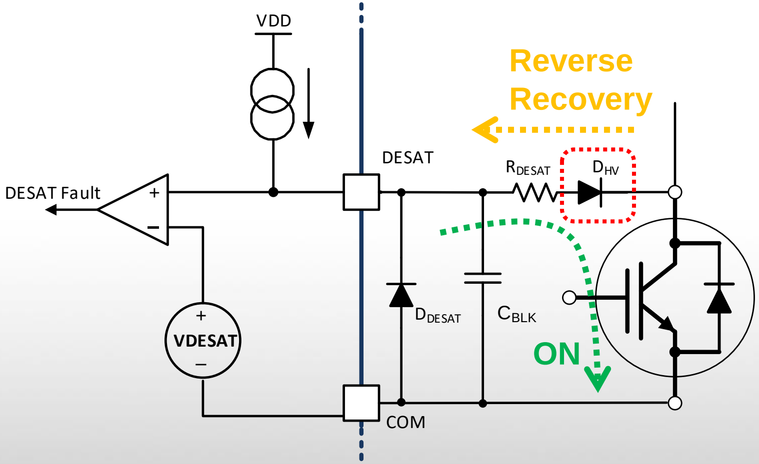
$$t_{DS\_BLK} = \frac{V_{DESAT} \times C_{BLK}}{I_{CHG}}$$

- Real detection voltage on the device terminals is lower than pre-set reference voltage

$$V_{DS\_DET} = V_{desat} - V_{D_{HV}} - I_{desat} \times R_{desat}$$

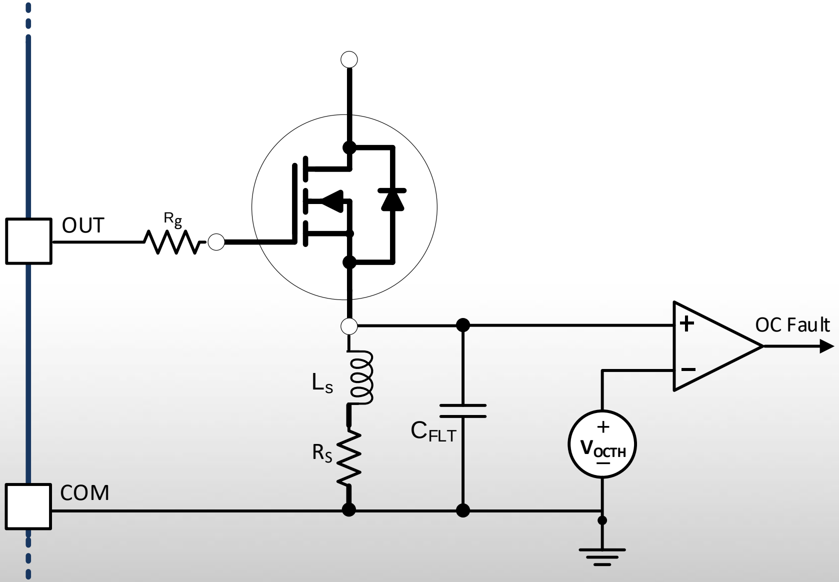
- DESAT threshold voltage varies between different devices due to the output characteristics, especially IGBT and SiC MOSFET

Overcurrent/Short Circuit Protection Method: DESAT



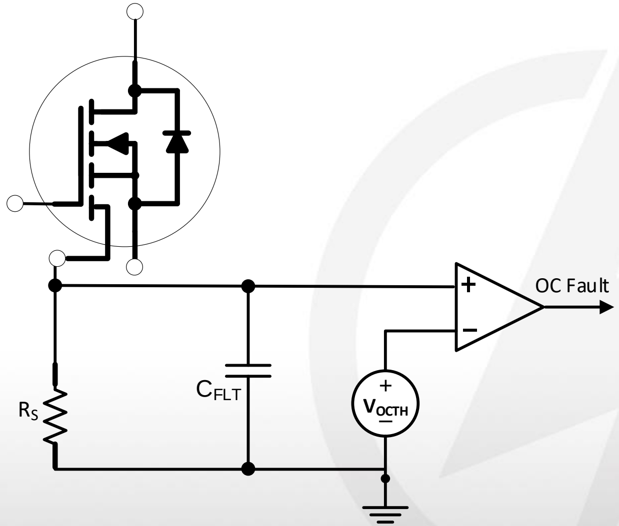
- Advantages
  - Simple circuits
  - low loss
  - Programmable protection time
- Challenges of DESAT protection method
  - High voltage fast reverse recovery diodes add cost
  - Multiple high voltage diodes are needed to share blocking voltage for above 1200V applications
  - Blanking time makes the protection time too long for SiC MOSFET
  - Parallel diode D_{desat} is needed to prevent the negative voltage on DESAT pin
  - Indirect current sensing can be challenging for SiC MOSFET

Overcurrent/Short Circuit Protection Method: Shunt Resistor



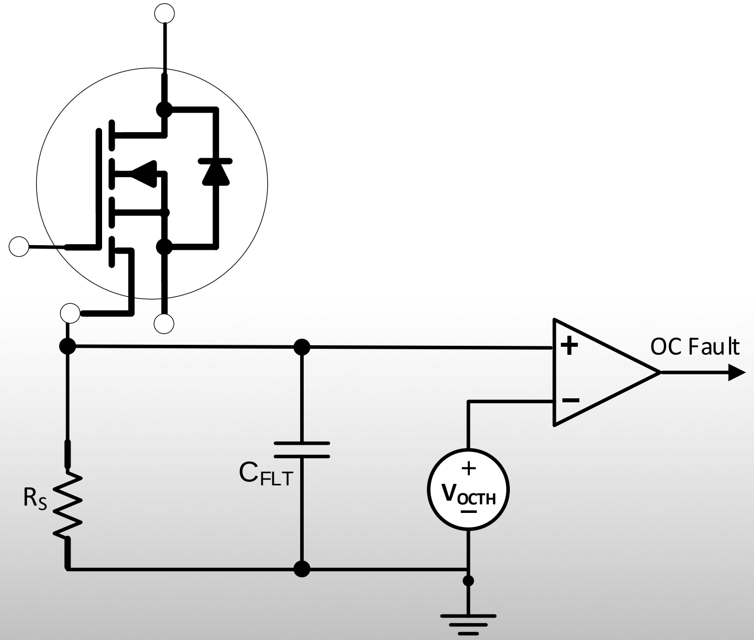
- Advantages
  - Accurate for both AC and DC
  - Fast protection speed
  - Low cost
- Challenges of shunt resistor
  - High power loss in high power applications
  - Weak noise immunity due to gate loop noise caused by parasitic inductance of shunt resistor and PCB trace

Overcurrent/Short Circuit Protection Method: SenseFET / Current Mirror



- SenseFET / Current mirror is used to scale down main current, tens of mV voltage is measured on sense resistor
- Accuracy is determined by current scaling circuit and sensing resistor
- More commonly used in automotive applications

Overcurrent/Short Circuit Protection Method: SenseFET / Current Mirror



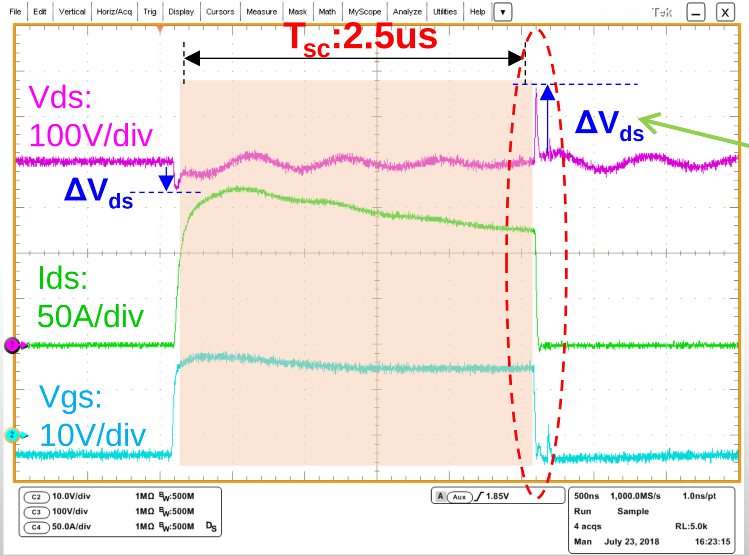
- Advantages
  - Fastest protection speed
  - Accurate for both AC and DC
- Challenges of SenseFET / Current mirror
  - Module needs to be customized to integrate SenseFET / Current mirror
  - Higher cost

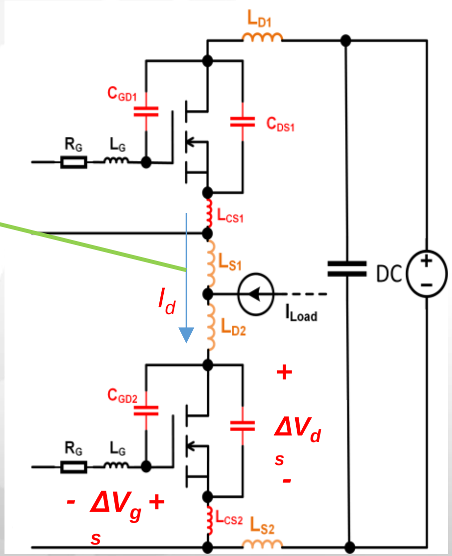
Overcurrent/Short Circuit Protection Method: Comparison

Method	DESAT	Shunt Resistor	SenseFET / Current Mirror
Response time	Slow	Fast	Fast
Accuracy	Good for IGBT; Medium for SiC MOSFET	High, depends on shunt quality 3% without calibration, 1% with calibration	Medium, depends on scaling accuracy and external resistor selection
Losses	Negligible	High and depends on Rs value	Low
Cost	Medium	Low	High

- Shunt Resistor method is not desired for high power applications due to high loss;
- SenseFET/Current Mirror works best for SiC MOSFET for its low noise and fast speed, but senseFET is not always available;
- Desat method works good for IGBT, but may have limitations for SiC MOSFET, especially for the drivers designed fro IGBT.

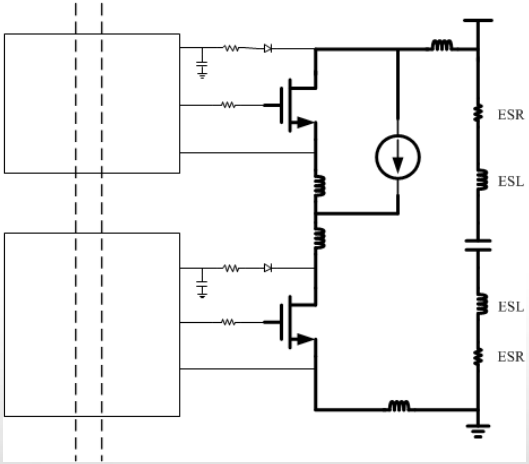
Overcurrent/Short Circuit Safe Turn-off: Avalanche limitation

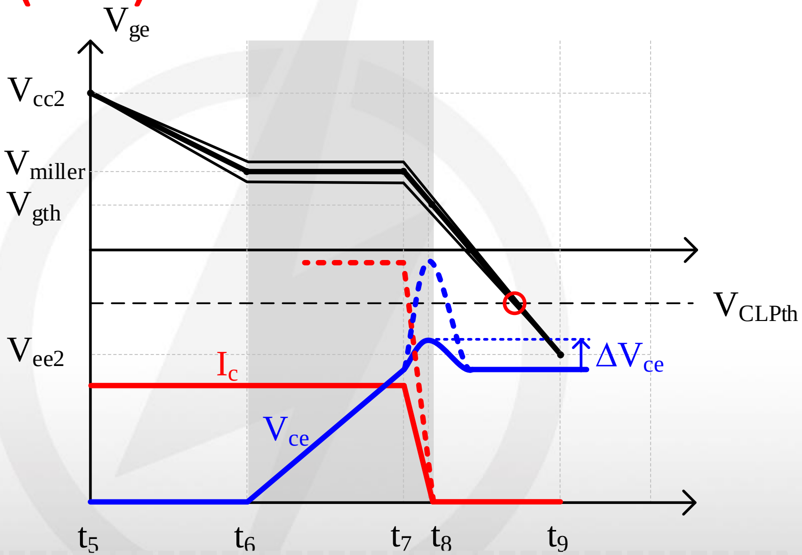




- ***Voltage and avalanche limit:*** Device avalanche can be caused by the overshoot voltage on V_{ds}

SiC MOSFET Protection: Soft Turn-Off (STO) & 2L Turn-Off



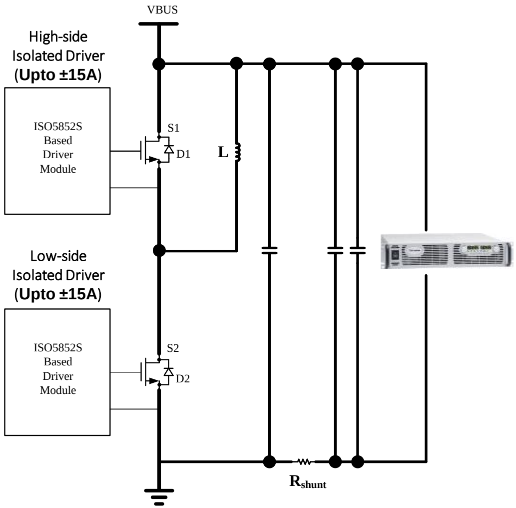


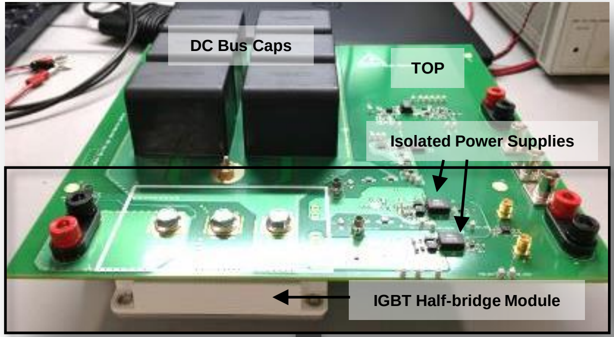
- There are parasitic inductances in the power loop.
- Parasitic inductances together with di/dt cause voltage spikes.
- The di/dt rate is much higher under short circuit fault that a preventive turn-off measure needs to be taken in order to limit the loop inductance induced voltage spike.
- Effectively, there are two ways to slow down the turn-off process: *reduce di* or *extend dt*.

Short-Circuit Protection: Hardware Validation

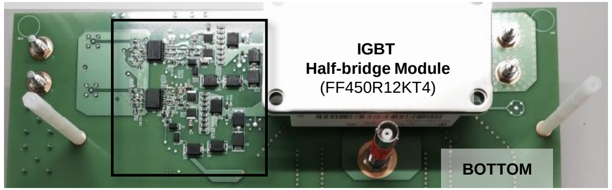
Evaluation Hardware

Schematic for Double-Pulse Test Setup



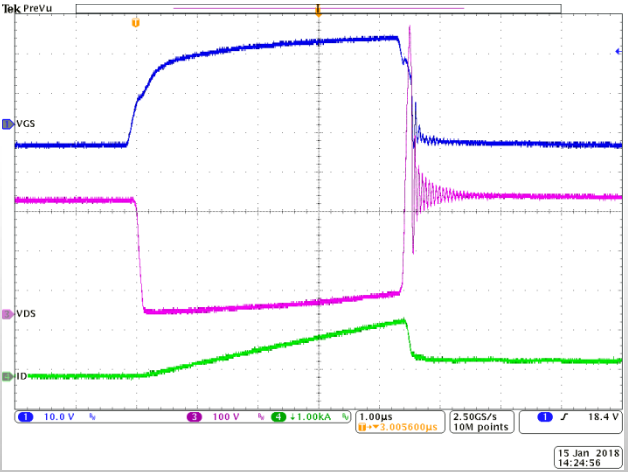


Isolated Half-bridge Drive Stage
using ISO5852S-Q1 + 15A Buffer Driver



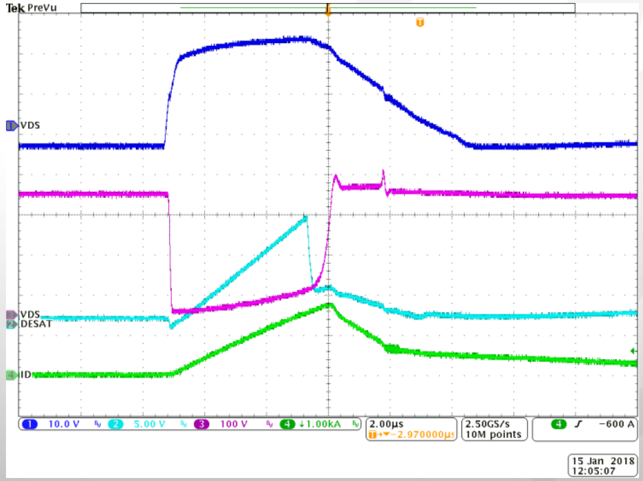
Short Circuit Protection for SiC MOSFETs: with or without Soft turn-off

VDS(100V/div), IC(1kA/div), VGS(10V/div)



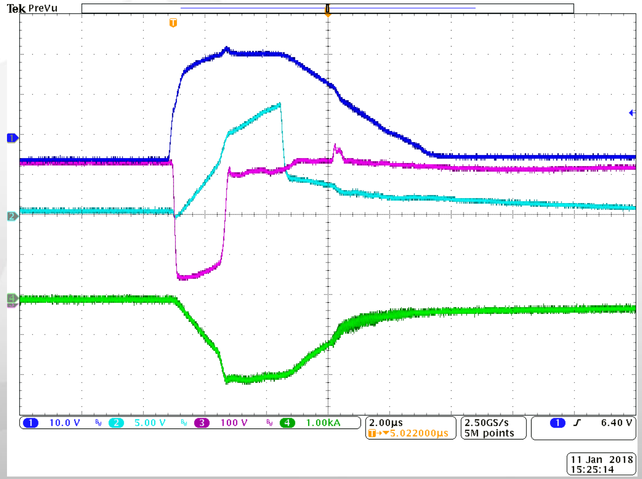
Hard Turn-off

VDS(100V/div), IC(1kA/div), VGS(10V/div), VDESAT(5V/div)



Soft Turn-off for Hard SC

VDS(100V/div), IC(1kA/div), VGS(10V/div), VDESAT(5V/div)



Soft Turn-off for SC under Load

Summary and key takeaways

- SiC MOSFET has superior performance than Si IGBTs for both conduction and switching;
- There are mainly three methods for the fault current sensing and then protection, sense FET is good for SiC MOSFETs but cost is high;
- De-sat method used for Si IGBT needs to be re-designed for SiC MOSFETs;
- Soft/two level turn off is also desired for turning off SiC MOSFET under short circuit.