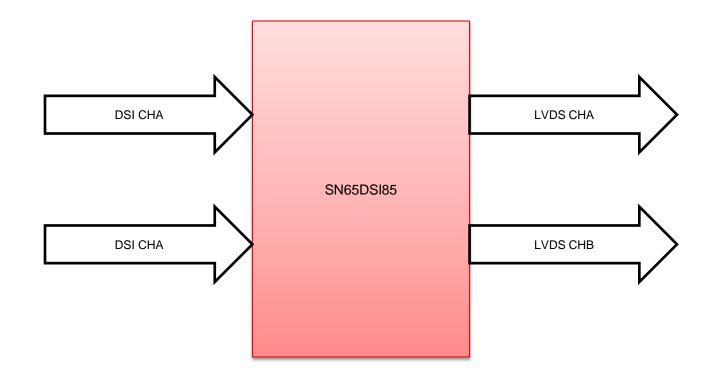
SN65DSI83/84/85- Two Single DSI Input to Dual-Link LVDS

Ikechukwu (I.K.) Anyiam



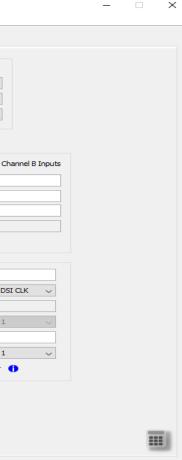
- Please watch the "Single DSI Input to Single-Link LVDS" video before watching this video
- Only the SN65DSI85 can be used for this demo





• Select "Dual" as the LVDS Mode and "Two Single" as the DSI Ch Mode

anel Inputs DSI_Inputs Outputs	Panel Inputs DSI_Inputs Outputs
Panel Info Channel A Channel B Panel Vendor Panel Model	DSI Info DSI Channel A DSI Channel B UP All All Burst Mode Burst Burst
Resolution pixels x LVDS Mode Dual v Test Pattern	Left right or even odd OE Sync Mode Event Event LR CROP Enable No Image: Sync Mode Event Event Pixels DSI Channel A Inputs DSI Channel B Inputs DSI Channel A Inputs DSI Channel A Inputs DSI Channel A Inputs DSI_HBP Image: Sync Mode DSI_VPW Image: Sync Mode Image: Sync Mode DSI_HBP Image: Sync Mode DSI_VPW Image: Sync Mode Image: Sync Mode DSI_HBP Image: Sync Mode Image: Sync Mode Image: Sync Mode Image: Sync Mode DSI_HBP Image: Sync Mode Image: Sync Mode Image: Sync Mode Image: Sync Mode DSI_HBP Image: Sync Mode Image: Sync Mode Image: Sync Mode Image: Sync Mode DSI_HBP Image: Sync Mode Image: Sync Mode Image: Sync Mode Image: Sync Mode DSI_HBP Image: Sync Mode Image: Sync Mode Image: Sync Mode Image: Sync Mode DSI_HActive Image: Sync Mode Image: Sync Mode Image: Sync Mode Image: Sync Mode
Htotal 0 0 Htotal 0 0 Additional Panel Info Channel A Channel B FORMAT Format 2 v Format 2 v Data Enable Polarity Positive v Positive v Horizontal Sync Polarity Negative v Negative v Vertical Sync Polarity Negative v Negative v Bits Per Pixel 18bpp v 18bpp v	DSI_Htotal 0 0 0 0 Additional Channel info DSI Channel A input DSI Channel B Input LVDS CLK(MHz) - nominal DSI DDR - - - LVDS CLK(MHz) - nominal DSI # of lanes 1 1 Multiplier (1-4) Multiplier (1-4) DSI Video Mode RGB666 packed RGB666 packed DSI Ch A CLK LEFT_CROP RIGHT_CROP LVDS CLK(MHz) - Actual





 Enter the same settings from the "Single DSI Input to Single-Link LVDS" demo to both Channel A and Channel B on the "Panel Inputs" window

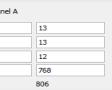
		▶ DSI83/84/85/86 Tuner - SN65DSI85
Panel Inputs DSI_Inputs Outputs		Panel Inputs DSI_Inputs Outputs
Panel Info Channel A Panel Vendor Panel Model Resolution 1024 pixels x 768 lines LVDS Mode Single ~ Test Pattern	TEXAS INSTRUMENTS	Panel Info Channel A Channel B Panel Vendor
Pixels LVDS Channel A LVDS Channel B LVDS_HPW 107	Lines LVDS Channel A LVDS_VPW 13 LVDS_VBP 13 LVDS_VFP 12 LVDS_VActive 768 Vtotal 806	Pixels LVDS Channel A LVDS Channel B LVDS_HPW 107 107 LVDS_HBP 107 107 LVDS_HFP 106 106 LVDS_HFP 106 106 LVDS_HActive 1024 1024 Hotal 1344 1344 Additional Panel Info Channel A Channel B FORMAT Format 1 Format 1 Data Enable Polarity Positive Negative Vertical Sync Polarity Negative Negative Bits Per Pixel 24bpp 24bpp

Settings from "Single DSI Input to Single-Link LVDS" video

New settings











 Enter the same settings from the "Single DSI Input to Single-Link LVDS" demo to both Channel A and Channel B on the "DSI_Inputs" window

768 LP A Burst Mode E	All SI Channel B All SI Channel B Burst SI Channel B Burst SI Channel B Event SI Channel B Event SI Channel B Event SI Channel B Burst SI Channel B Event SI Channel B	DSI Info Panel Resolut DSI Ch Mode Left right or o LR CROP Ena	Two Single ~	Informational DSI Chan LP All Burst Mode Burst Sync Mode Event	Anel A DSI Channel B All ~ Burst ~ Event ~
	Lines	Pixels		Lines	
Channel A Inputs DSI Channel B Inputs	DSI Channel A Inputs DSI Channel B Inputs		DSI Channel A Inputs DSI Channel B Input	_ _	I Channel A Inputs DSI Channel B Inputs
	DSI_VPW 13		107 107	DSI_VPW 13	
	DSI_VBP 13		107 107	DSI_VBP 13 DSI_VFP 12	
+	DSI_VActive 768		106 106	DSI_VActive 76	
•	DSI_Vtotal 806	DSI_HActive DSI_Htotal		DSI_Vtotal 80	
nel info DSI Channel A input DSI Channel 195 1 4 1 RGB888 RGB666 p RIGHT_CROP 1	LVDS CLK source DSI CLK ~ Ref CLK(MHz) Multiplier (1-4) 1 ~	Additional Ch DSI DDR CLK rate(MH: DSI # of lane DSI Video Mo LEFT_CROP	DSI Channel A input DSI C 2) 195 195 24 \log 4 \l		CLK LVDS CLK(MHz) - nominal 65 LVDS CLK source DSI CLK ~ Ref CLK(MHz) Multiplier(1-4) 1 DSI Ch A CLK 195 Divisor(1-25) 3 ~ LVDS CLK(MHz) - Actual 65.0 ()

Settings from "Single DSI Input to Single-Link LVDS" video

New settings



• Observe the "Outputs" window, and follow the same procedure as in the previous examples to generate the CSR settings

Panel Inputs DSI_Inputs Outputs				
Outputs]	
	Channel A	Channel B		
LINE TIME(SYNC to SYNC) REQUIREMENT(us)	20.677	20.677		
MIN DSI Ch* CLK REQUIREMENT(MHz) to meet the line time requirement	194.99927	194.99927		
Data burst time based on actual DSI Ch*CLK and data throughput(us)	20.676924	20.676924		
			1	



Thanks for your time!



