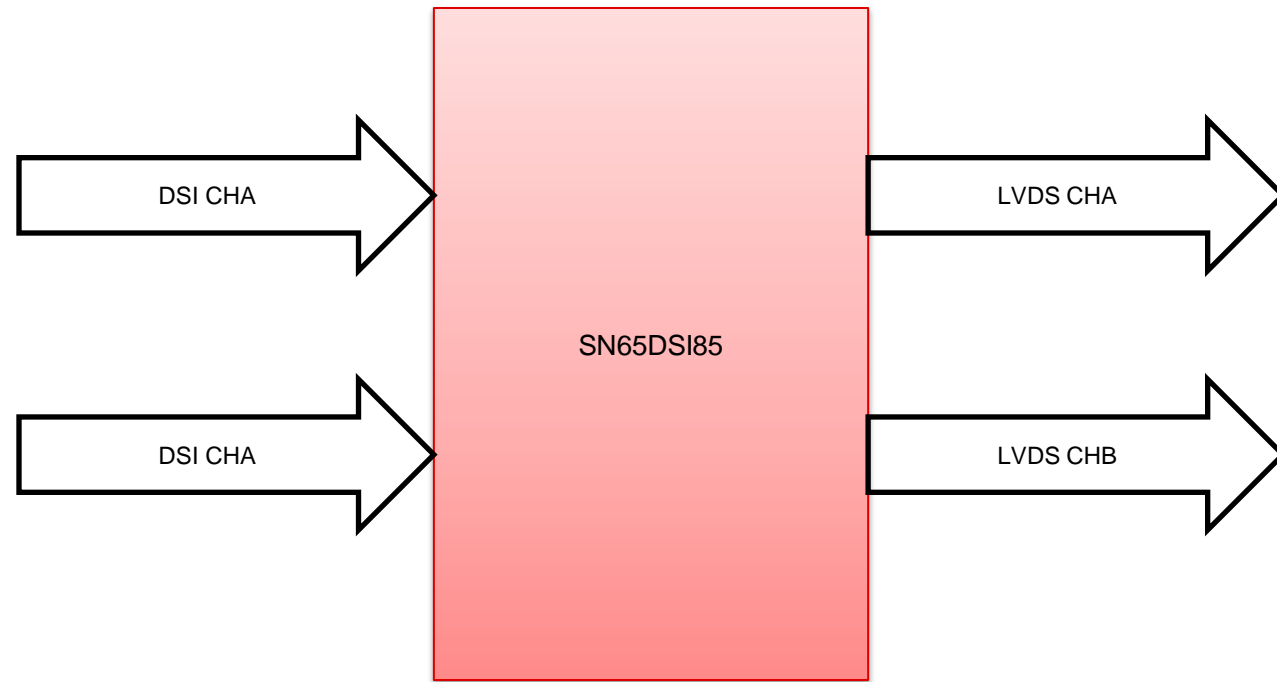


SN65DSI83/84/85- Two Single DSI Input to Dual-Link LVDS

Ikechukwu (I.K.) Anyiam

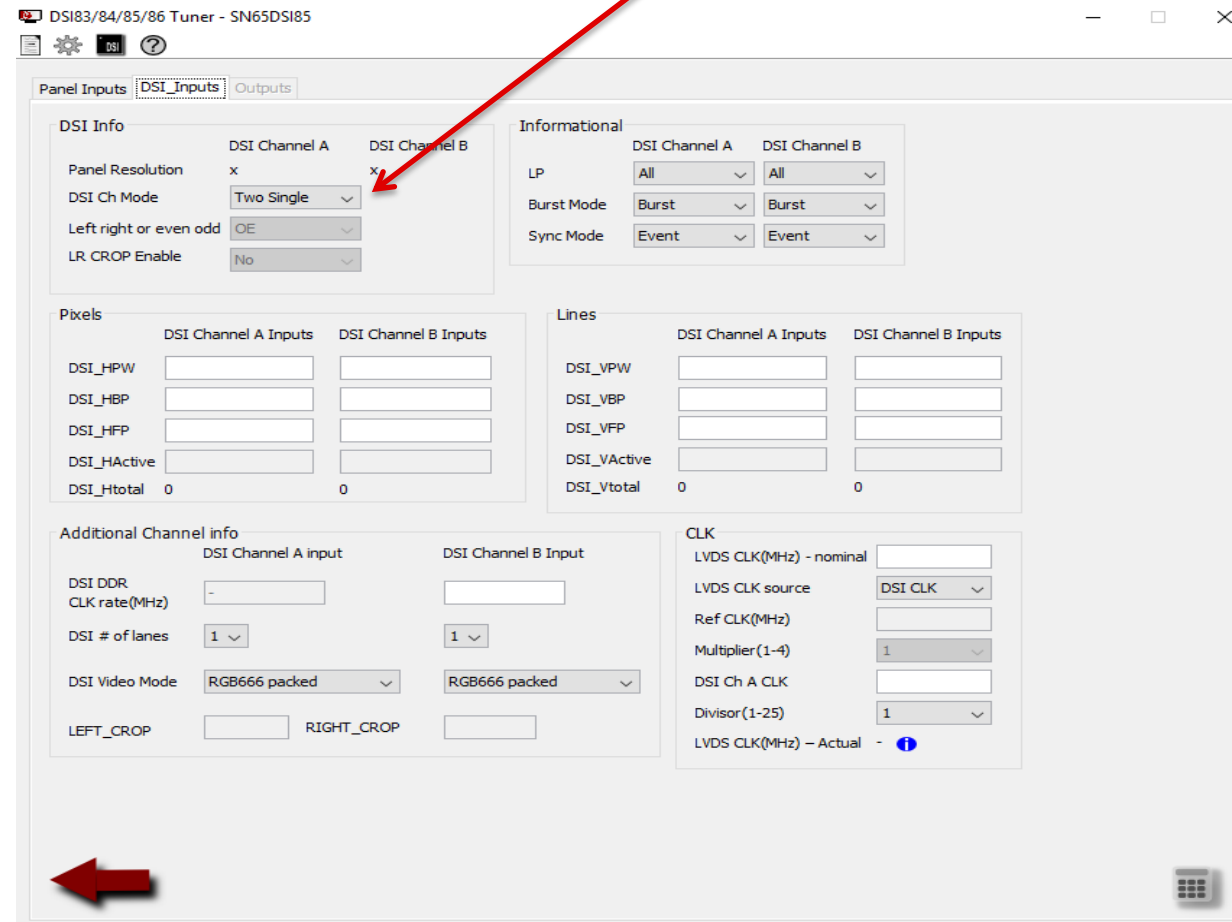
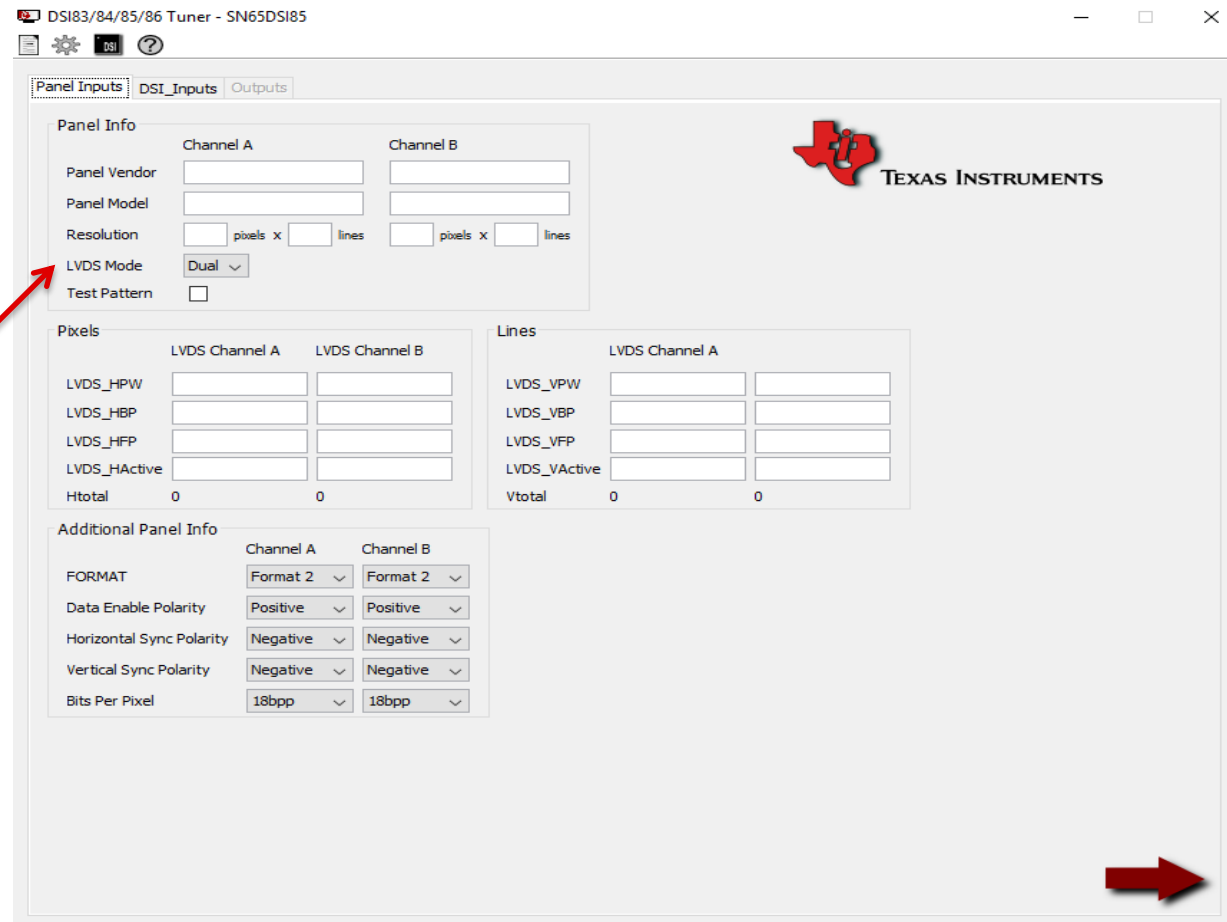
Two single to dual

- Please watch the “Single DSI Input to Single-Link LVDS” video before watching this video
- Only the SN65DSI85 can be used for this demo



Two single to dual

- Select “Dual” as the LVDS Mode and “Two Single” as the DSI Ch Mode



Two single to dual

- Enter the same settings from the “Single DSI Input to Single-Link LVDS” demo to both Channel A and Channel B on the “Panel Inputs” window

DSI83/84/85/86 Tuner - SN65DSI83

Panel Inputs | DSI_Inputs | Outputs

Panel Info

Channel A

Panel Vendor:

Panel Model:

Resolution: 1024 pixels x 768 lines

LVDS Mode: Single

Test Pattern:

Pixels

	LVDS Channel A	LVDS Channel B
LVDS_HPWW	107	
LVDS_HBP	107	
LVDS_HFP	106	
LVDS_HActive	1024	
Htotal	1344	0

Lines

	LVDS Channel A
LVDS_VPW	13
LVDS_VBP	13
LVDS_VFP	12
LVDS_VActive	768
Vtotal	806

Additional Panel Info

Channel A

FORMAT: Format 1

Data Enable Polarity: Positive

Horizontal Sync Polarity: Negative

Vertical Sync Polarity: Negative

Bits Per Pixel: 24bpp

Settings from “Single DSI Input to Single-Link LVDS” video



DSI83/84/85/86 Tuner - SN65DSI85

Panel Inputs | DSI_Inputs | Outputs

Panel Info

Channel A | Channel B

Panel Vendor: |

Panel Model: |

Resolution: 1024 pixels x 768 lines | 1024 pixels x 768 lines

LVDS Mode: Dual

Test Pattern:

Pixels

	LVDS Channel A	LVDS Channel B
LVDS_HPWW	107	107
LVDS_HBP	107	107
LVDS_HFP	106	106
LVDS_HActive	1024	1024
Htotal	1344	1344

Lines

	LVDS Channel A
LVDS_VPW	13
LVDS_VBP	13
LVDS_VFP	12
LVDS_VActive	768
Vtotal	806

Additional Panel Info

Channel A | Channel B

FORMAT: Format 1 | Format 1

Data Enable Polarity: Positive | Positive

Horizontal Sync Polarity: Negative | Negative

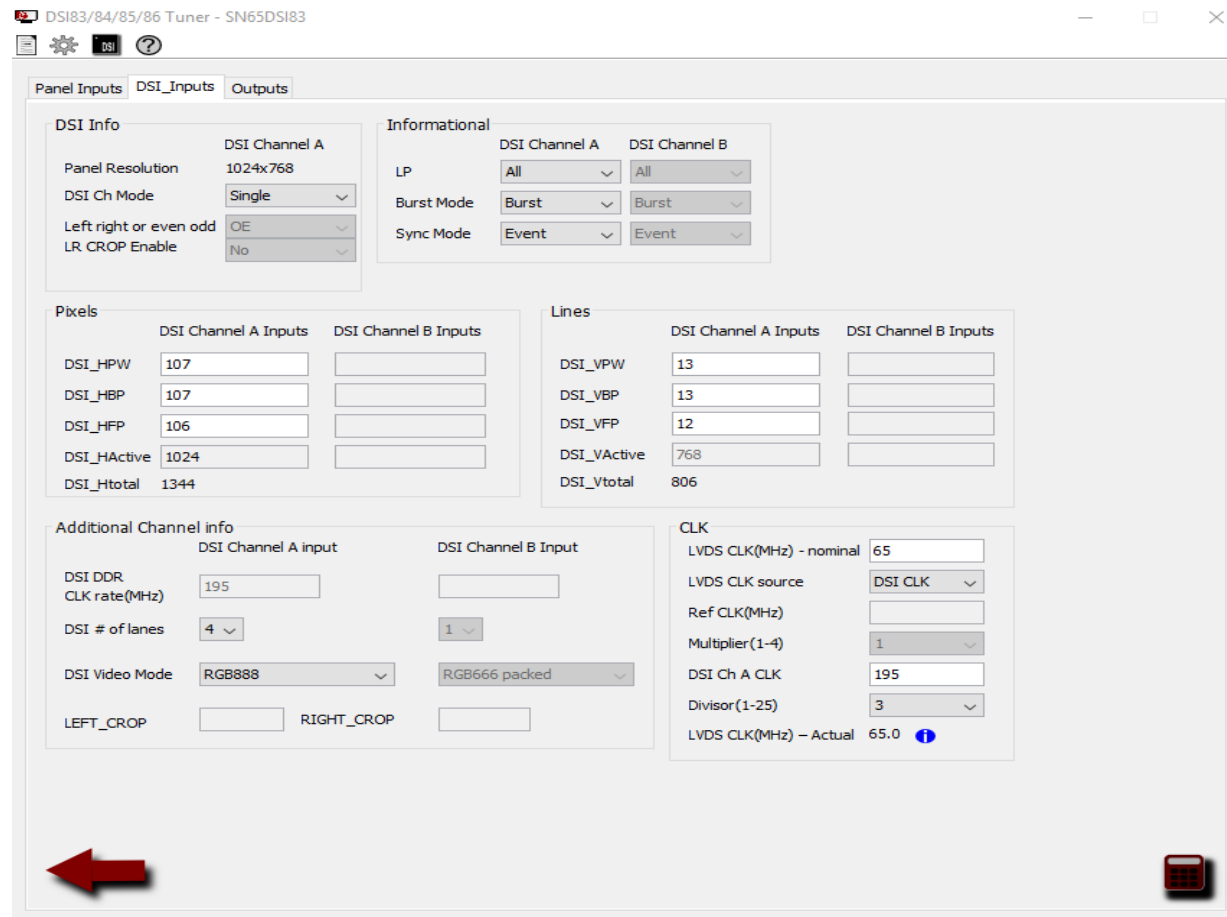
Vertical Sync Polarity: Negative | Negative

Bits Per Pixel: 24bpp | 24bpp

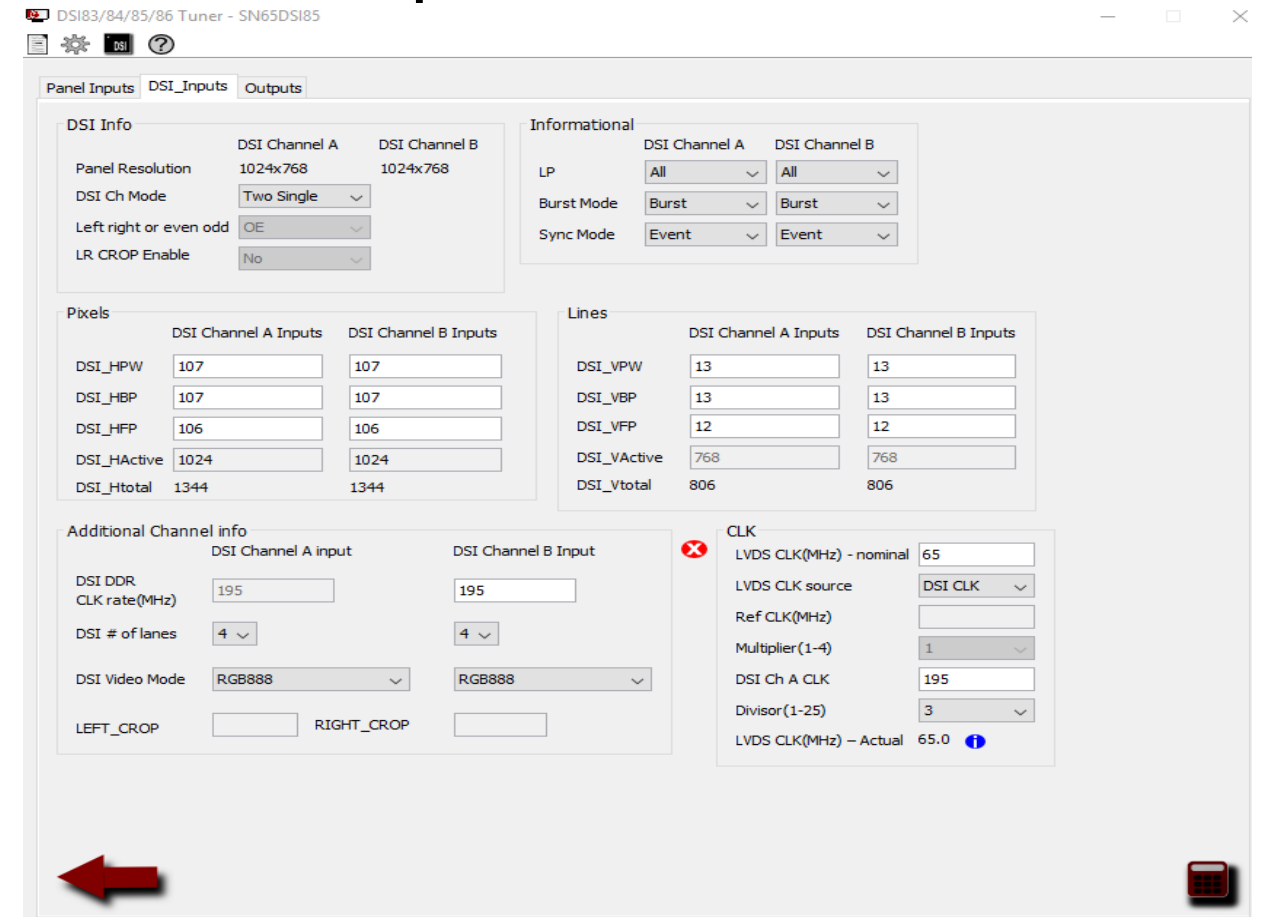
New settings

Two single to dual

- Enter the same settings from the “Single DSI Input to Single-Link LVDS” demo to both Channel A and Channel B on the “DSI_Inputs” window



Settings from “Single DSI Input to Single-Link LVDS” video



New settings

Two single to dual

- Observe the “Outputs” window, and follow the same procedure as in the previous examples to generate the CSR settings

Outputs	Channel A	Channel B
LINE TIME(SYNC to SYNC) REQUIREMENT(us)	20.677	20.677
MIN DSI Ch* CLK REQUIREMENT(MHz) to meet the line time requirement	194.99927	194.99927
Data burst time based on actual DSI Ch*CLK and data throughput(us)	20.676924	20.676924

Thanks for your time!