High VOLT Interactive

Where power supply design meets collaboration

Gate Driver Design – from Basics to Details

Wei Zhang

What will I get out of this session?

- **PURPOSES:**
  - What is the difference: low side, high and low side driver, and isolated gate driver?
  - How to maximize the gate driver performance – from basic to details
    - Parasitics in the gate driver
    - Hard/soft switching
    - High dv/dt and di/dt
    - Isolated gate driver

- Part numbers mentioned:
  - Low side: UCC2751x, UCC2752x, UCC27x24
  - H-/L- Side: UCC2771x, UCC272xx
  - Isolated: UCC2152x, UCC2122x UCC53xx
- Reference designs mentioned:
  - TIDA-01160, TIDA-01159
- Relevant end equipment:
  - EV/HEV, UPS, telecom, servers, solar, motor drive

Where are gate driver ICs used?

Gate driver applications

Li-ion battery portables

Adaptors and chargers

Server/telecom/UPS

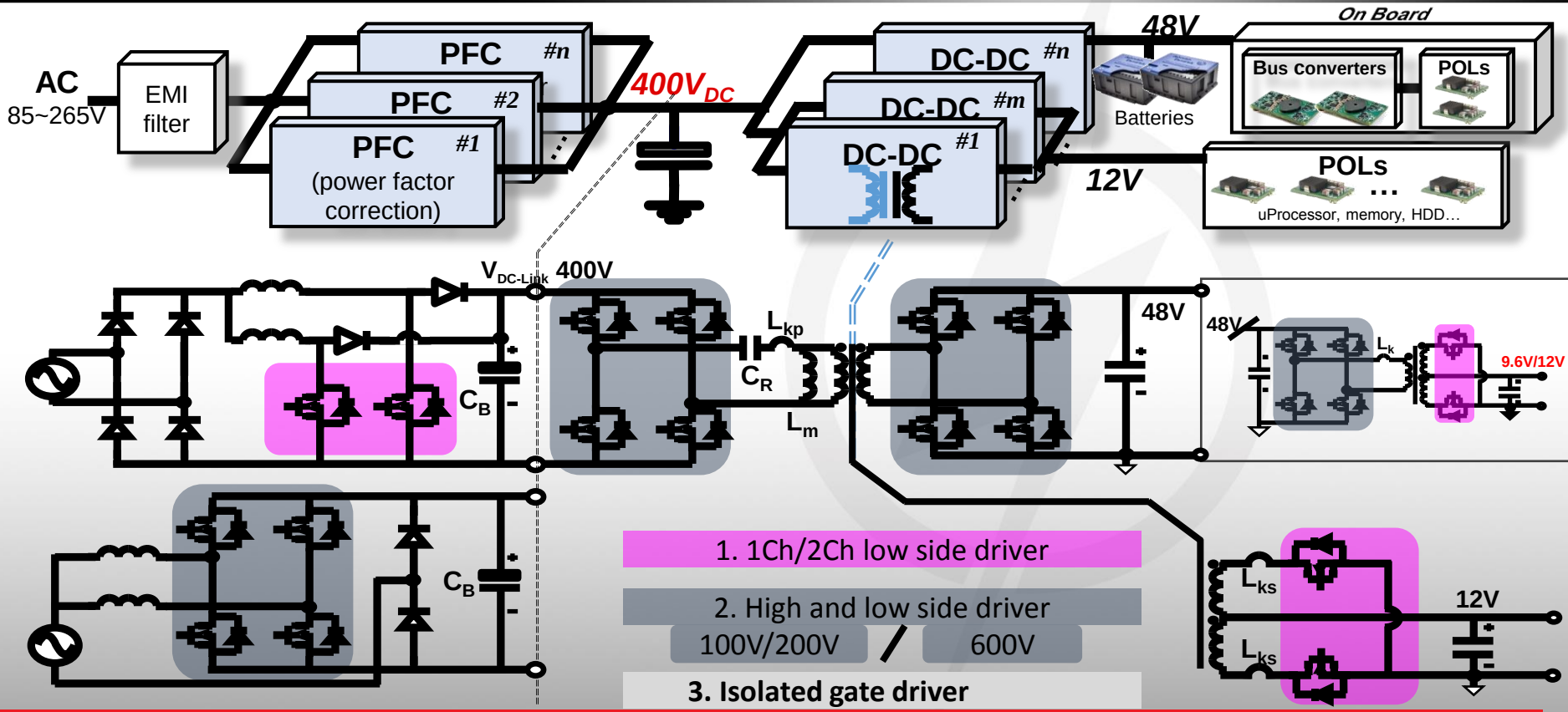
Electric vehicles class D audio

Solid state lighting (SSL)

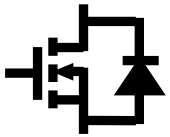
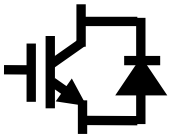
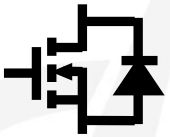
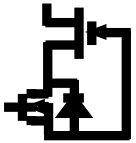
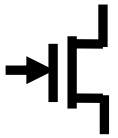
Renewables

Motor drive (VFD)

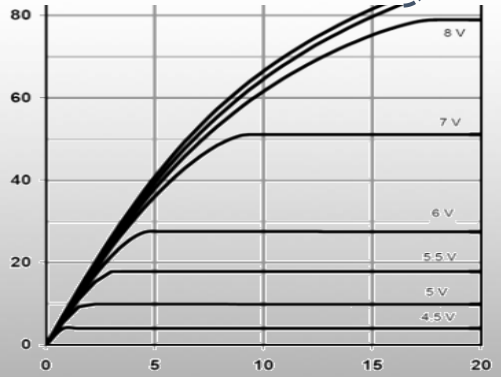
Gate Driver in Server / Telecom



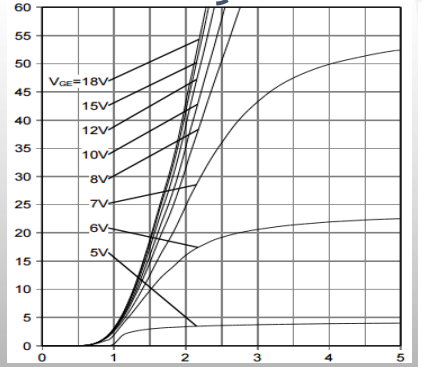
What are the Power Devices?

	Si-MOSFET	IGBT	SiC-MOSFET	GaN	
					
				Nom-ON	Nom-OFF
Voltage ratings	20~650V	≥650V	≥650V	≤650V	
Optimal V_{GS} Max.limit	0~15V (±20V)	-10~15V (±20V)	-5~20V (-10~25V)	-5~10V (±18V)	-4~6V (-10~7V)

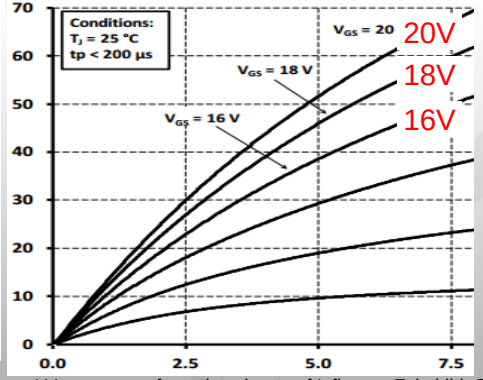
Si-MOSFET 10V



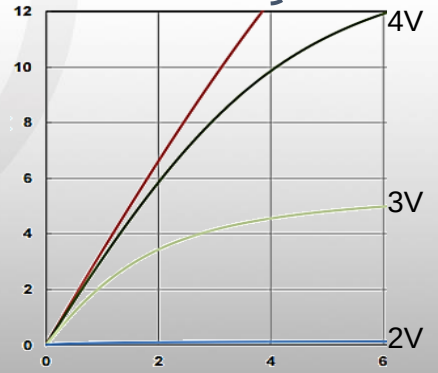
IGBT 12V



SiC-MOSFET

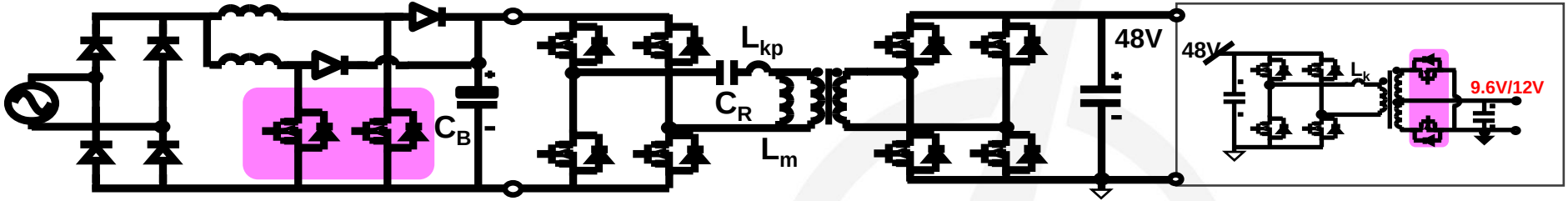


GaN 5V

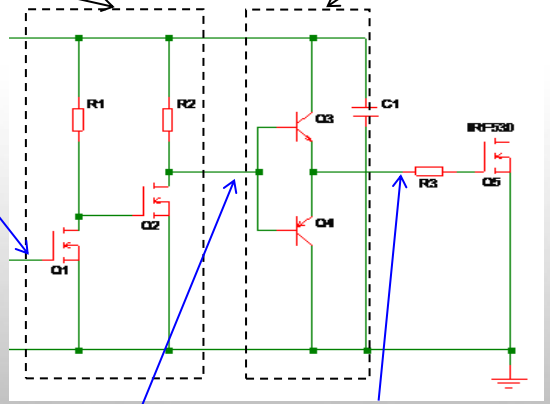


- I-V curves are from datasheets of Infineon, Fairchild, ST, CREE, EPC

Discrete vs Driver IC?



Level shift circuit + NPN/PNP totem pole



3.3V/5V PWM signal from microcontroller or DSP

Micro/DSP

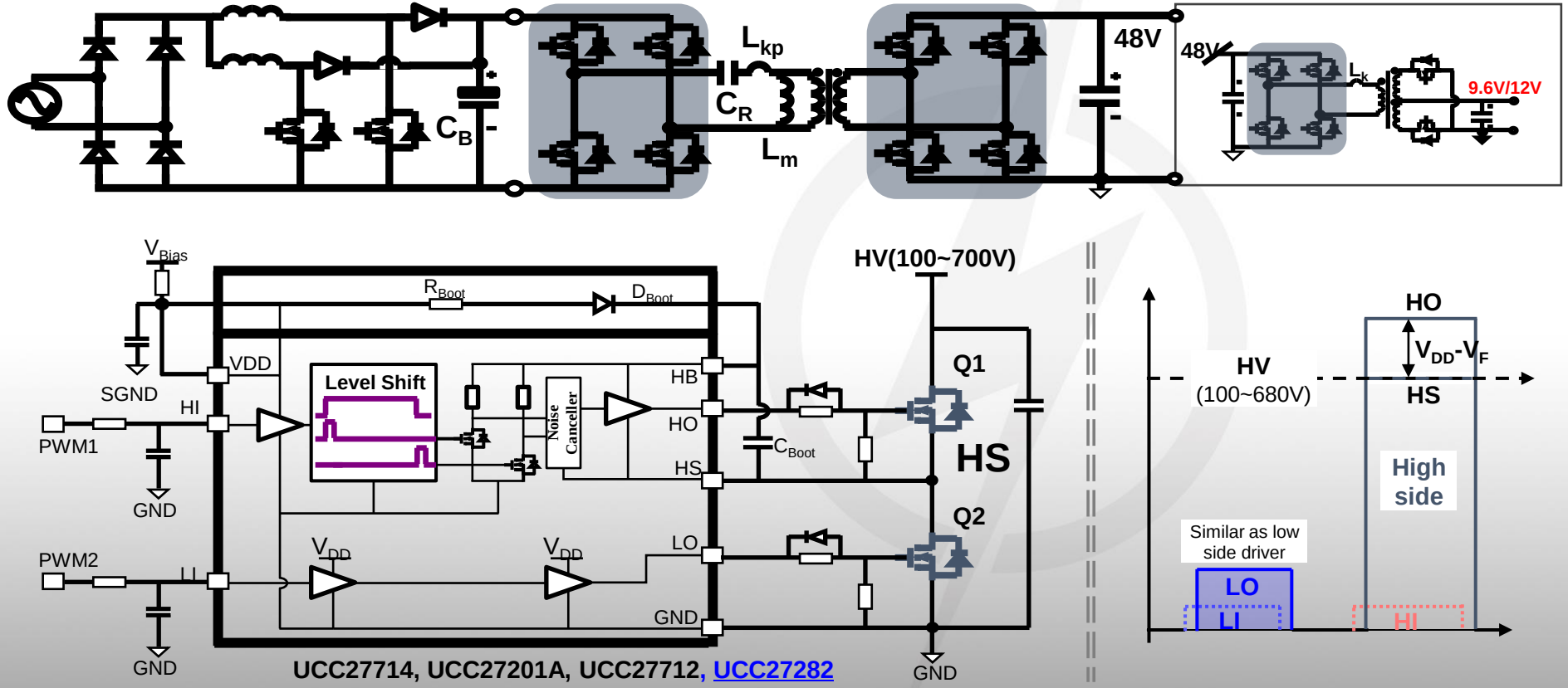
Level shifted 12V signal

12V with high peak source/sink current

Now

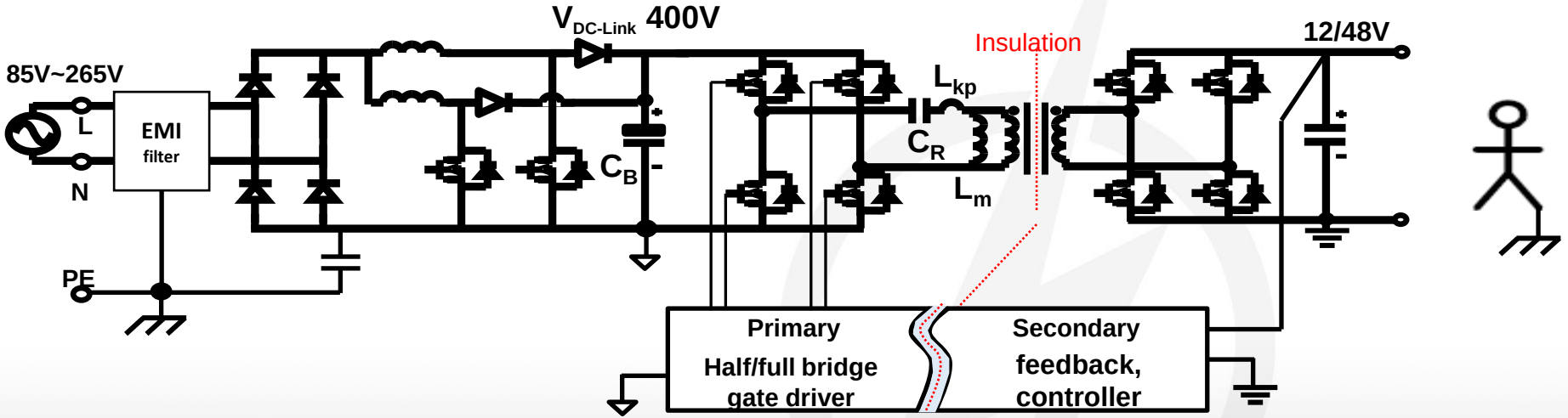
- Reduces BOM component count
- Reduces PCB space
- Protects from spurious signals during power up (such as UVLO)
- Improves reliability

How does a Half-Bridge Driver Operate?



UCC27714, UCC27201A, UCC27712, UCC27282

Why ISOLATION?



IEC 60950-1 ed. 2.0, Table 5B

Working voltage V, peak or DC	Test voltage for electric strength based on peak working voltage		
	Functional insulation (V_{RMS})	Basic insulation (V_{RMS})	Reinforced insulation (V_{RMS})
≤210	1000	1000	1500
≤420	1500	1500	3000

What is Functional, Basic, Reinforced Isolation?

Isolation	Definition
Functional	Insulation that is necessary only for the **correct functioning** of the equipment
Basic	Insulation to provide **basic protection against electric shock**
Supplementary	Independent insulation applied in addition to BASIC insulation in order to reduce the risk of electric shock in the event of a failure of the BASIC insulation
Double	Insulation comprising both BASIC insulation and SUPPLEMENTARY insulation
Reinforced	**Single insulation system** that provides a degree of protection against electric shock equivalent to DOUBLE insulation under the conditions specified in this standard

Isolation Req. Exp. per IEC-60950

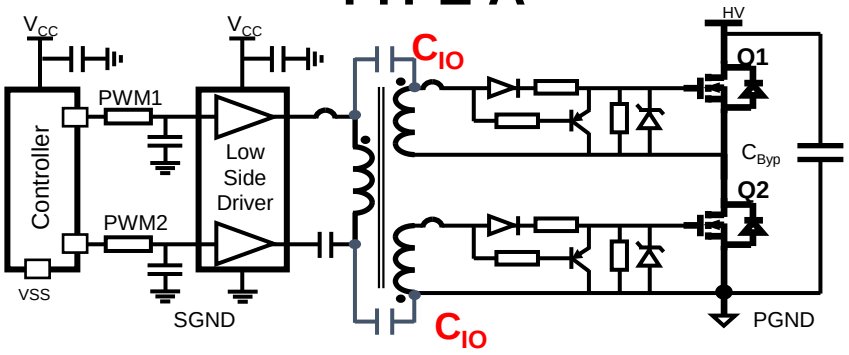
According to Figure 2H of IEC60950-1

Isolation Req. Exp. per IEC-60950

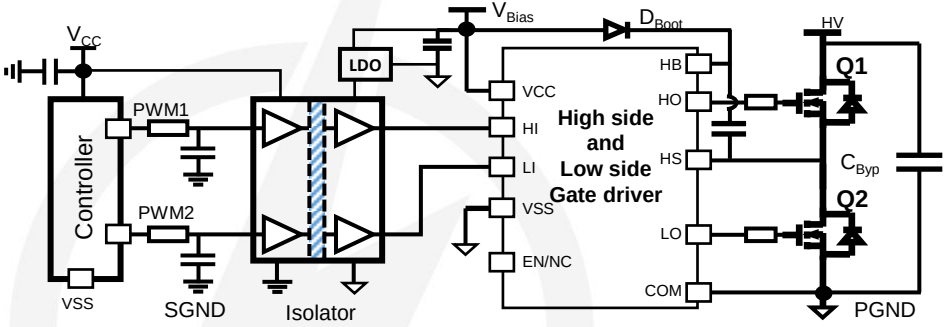
According to Figure 2H of IEC60950-1

Transformer vs. Driver IC

TYPE A



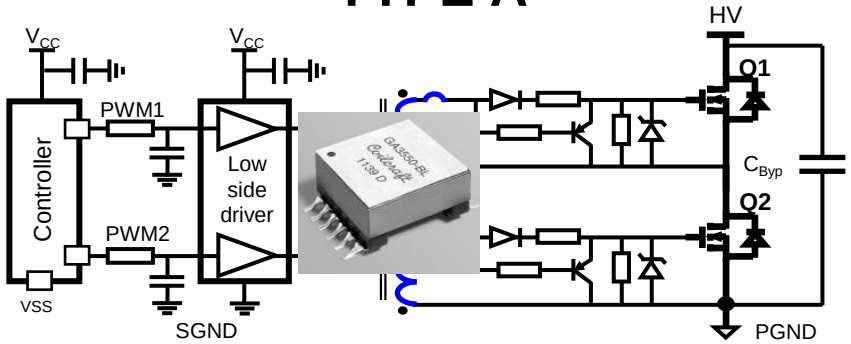
TYPE B



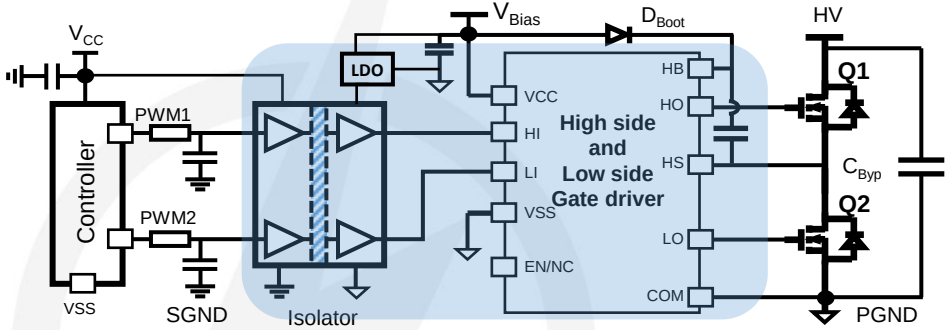
	Type A	Type B
T_{Prop}	≈20ns	≈100ns
Bias power	NO	Yes
C_{IO}	≥10pF	<1pF
Parasitics	Large (L_{LK})	Very small
Overshoot	Large	Small
Size	Bulky	Small

Transformer vs. driver IC?

TYPE A



TYPE B



		W (mm)	L (mm)	H (mm)	Area (mm²)	Vol (mm³)
Type A	UCC27324	5	6.2	1.75	31	54.25
	GA3550-BL	17.4	24.13	10	420	4200
				SUM	451	4254

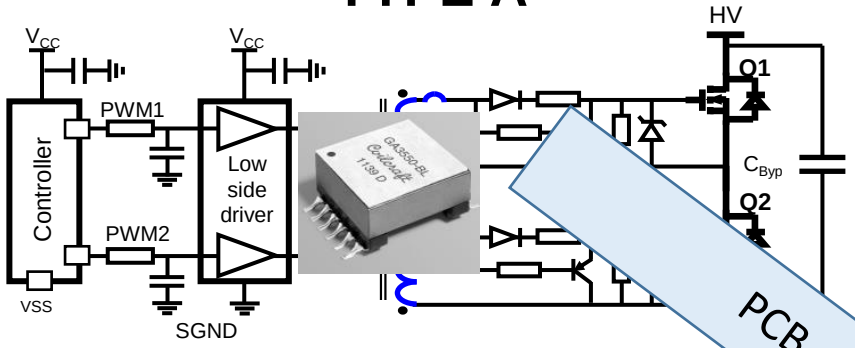
Type B	ISO7520C	10.5	10.6	2.65	111.3	295
	UCC27714	8.75	6.2	1.75	54.25	95
	MURS360	8.1	6.1	2.4	49.41	119
				SUM	215	509

TYPE C: ISO driver

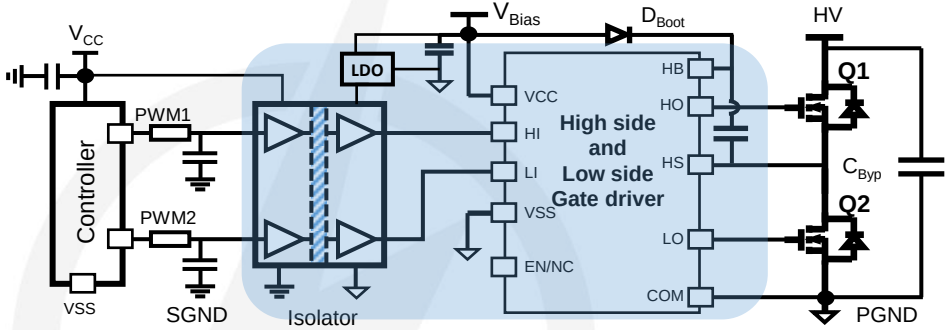
- CMTI>100V/ns
- 5kVrms reinforced isolation
- T_{Prop}: 19ns typ.
- Match./T_{PWD} < 5ns
- 110mm²

Transformer vs. driver IC?

TYPE A



TYPE B



PCB area reduction – 76%

		W (mm)	L (mm)	H (mm)	Area (mm²)	
Type A	UCC27324	5	6.2	1.75	31	54
	GA3550-BL	17.4	24.13	10	420	4200
				SUM	451	4254

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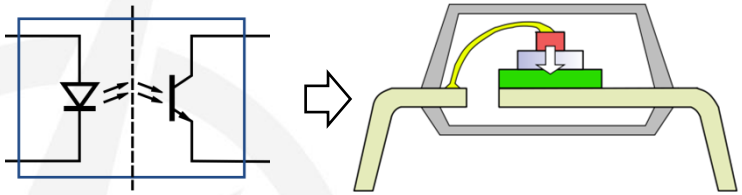
TYPE C: ISO driver

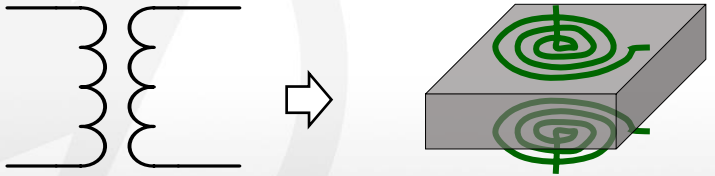
- CMTI>100V/ns
- 5kVrms reinforced isolation
- : 19ns typ.
- WD < 5ns
- 110

Popular ISOLATION methods

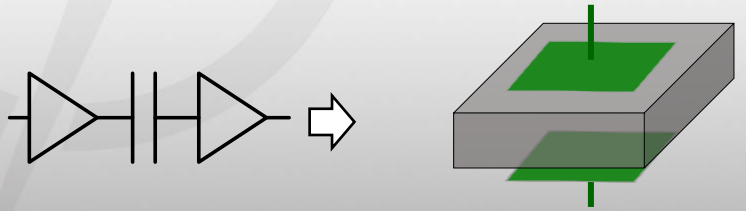
- A) Optocoupler
  - Signal transfer between two isolated circuits using light – LED + phototransistor, ~1970s



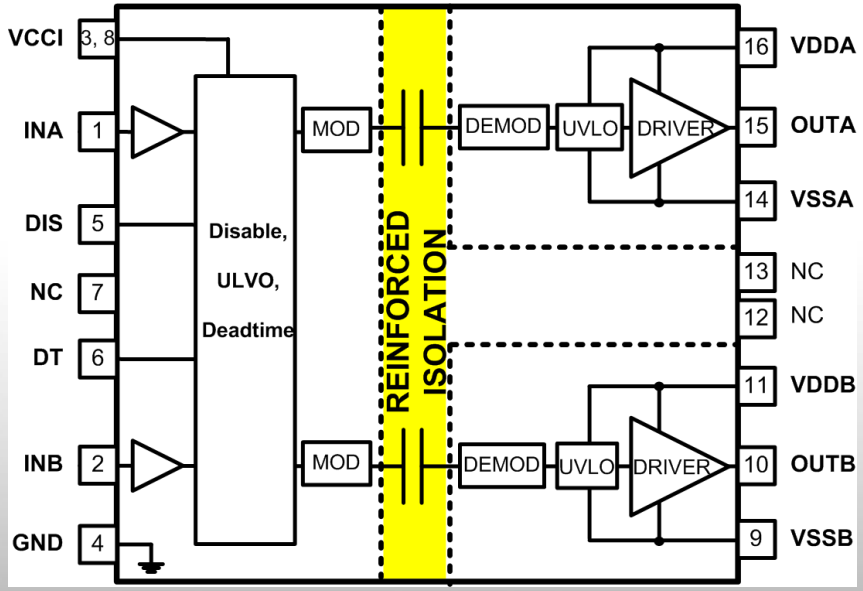
- B) Transformer
  - Integrated micro-transformer and electronic circuitry, ~2001



- C) Capacitor
  - Signal transmission through capacitive isolation with on-off-keying (OOK) modulation, ~2004



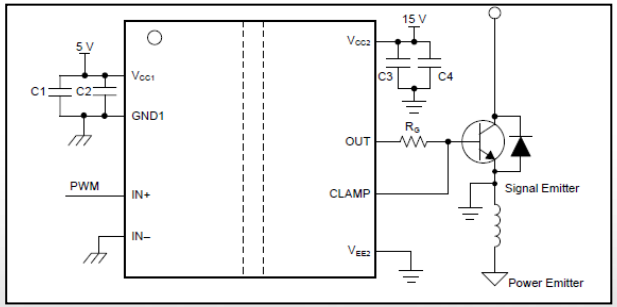
UCC2122x, UCC2x520: 2-ch. Isolated Gate Driver



- 6A/4A sink/source
- 19ns propagation delay
- >100V/ns
- Up to 3~18V wide input range and 6.5~30V wide output voltage range
- Programmable overlap, and interlock/delay time from 0ns~5µs
- Output fail safe low with active pull down
- UVLO options: 5V, 8V, 12V
- 3.0kV, 5.7kV basic / reinforced isolation
- Pin-2-pin compatible to industry standard
- UL, VDE, CQC certified

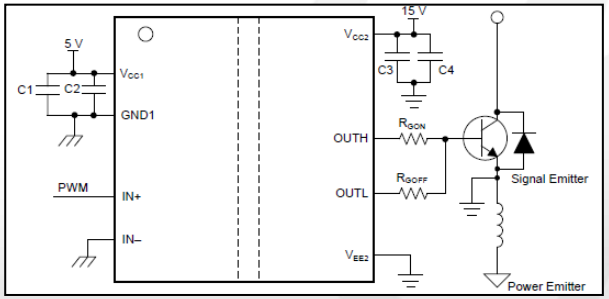
UCC53xx single ch. isolated gate driver

Miller clamp:
3-kV – UCC5310M and UCC5350M
5-kV – UCC5310M



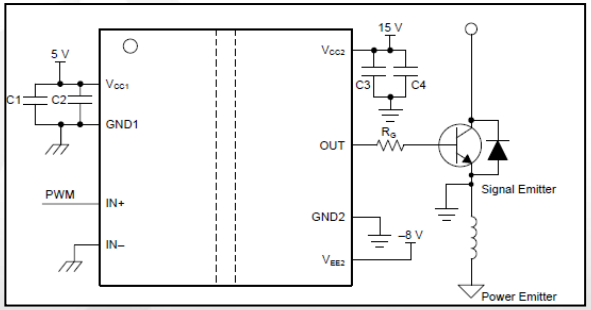
- Features active Miller clamping which prevents false turn-on of the power transistors induced by the Miller current
- Tie clamp pin to gate of FET

Split output:
3-kV – UCC5320S, UCC5350SB, UCC5390S
5-kV – UCC5320S



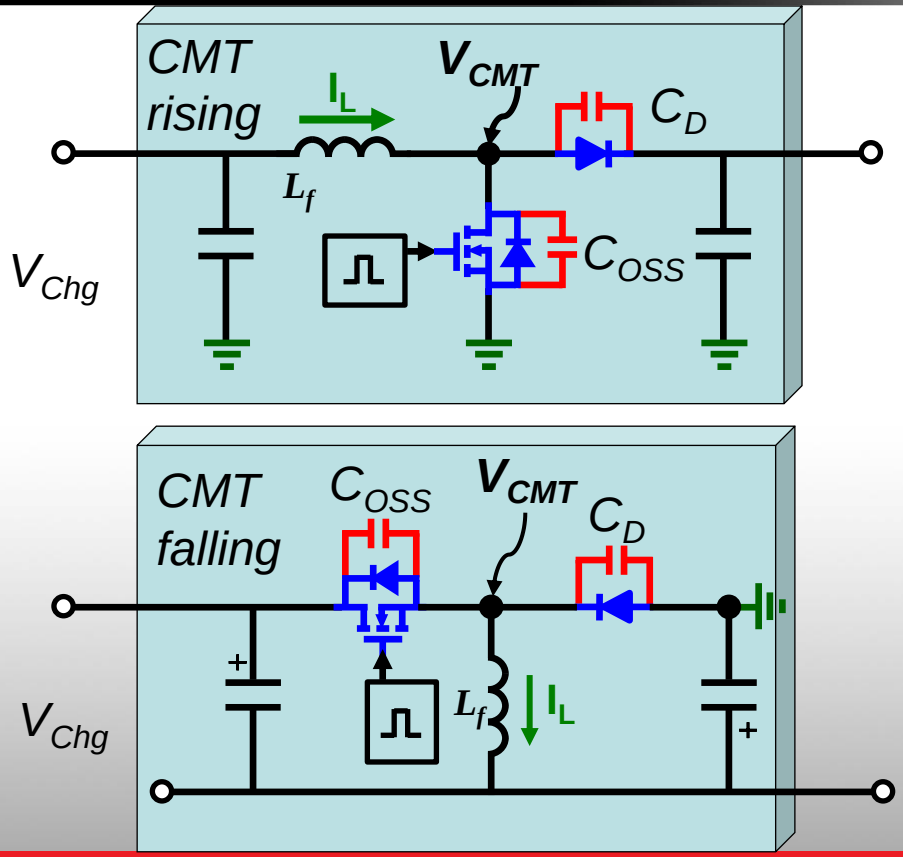
- Two outputs OUTH and OUTL can be used to separately control rise and fall times of power transistor
- Rise and fall times are controlled by series resistors: R_{GON} and R_{GOFF}

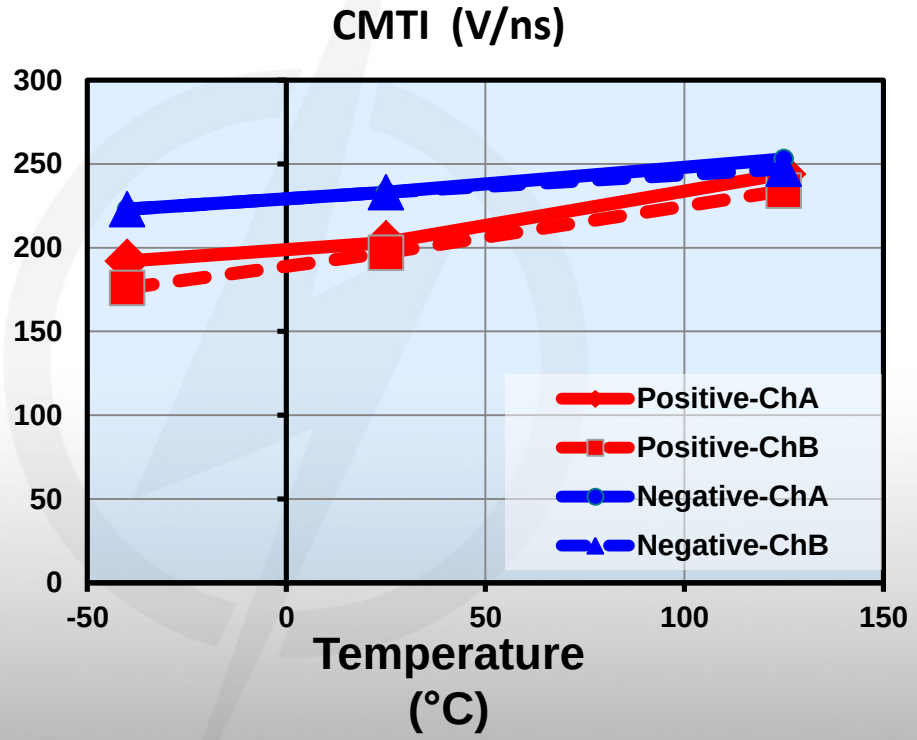
Emitter – UVLO control:
3-kV – UCC5320E and UCC5390E
5-kV – UCC5390E



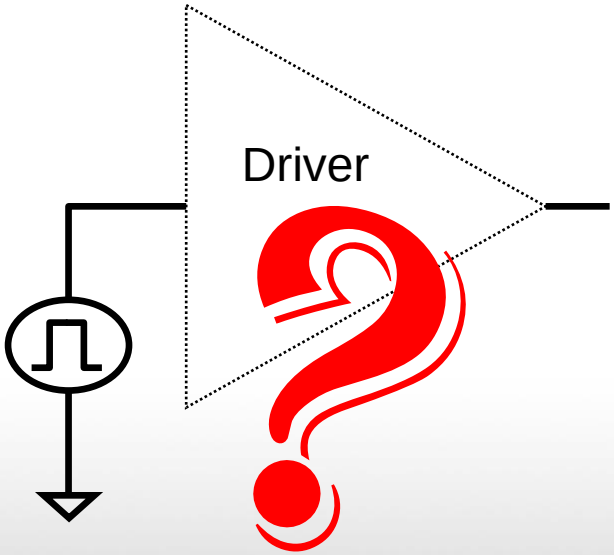
- UVLO protection by monitoring the voltage between the V_{CC2} and GND2 pins to prevent the power transistors from operating in a saturation region

CMTI Measurement for UCC21520





Gate Driver Design is Simple?

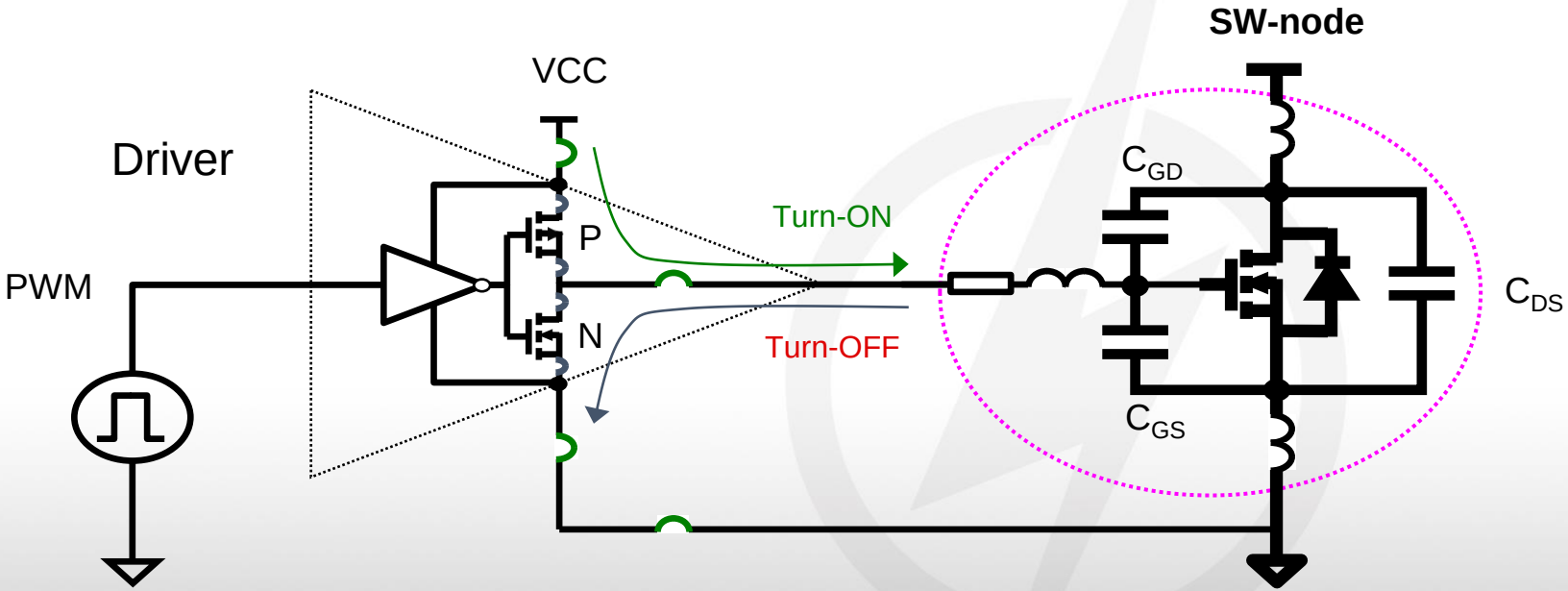


1. Parasitics in gate driver?
2. Gate driver soft/hard switching difference?
3. Strong gate driver and MOSFET nonlinear C_{oss}?
4. Common mode transient immunity(CMTI), dv/dt and di/dt through parasitics L and C?
5. How to separate power ground noise by PCB layout?
6. Power supply for isolated gate driver in UPS, server and Telecom system
7. TIDA and experimental waveforms

Gate driver deep dive

Very critical role in converter efficiency and reliability

What are the Parasitics?



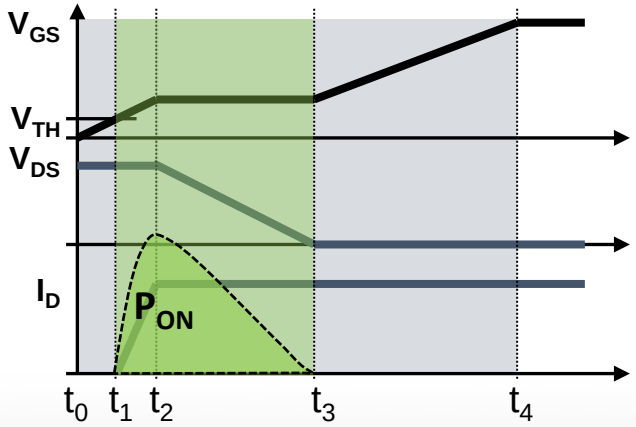
$$C_{ISS} = C_{GS} + C_{GD}$$

$$C_{RSS} = C_{GD}$$

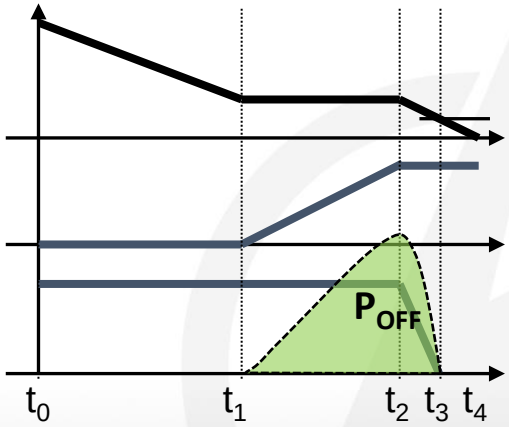
$$C_{OSS} = C_{GD} + C_{DS}$$

Turn-ON/OFF process

Turn-ON



Turn-OFF

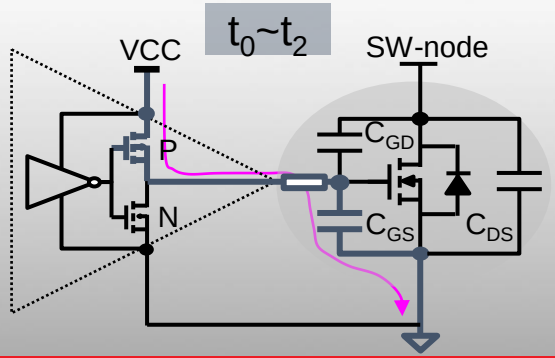


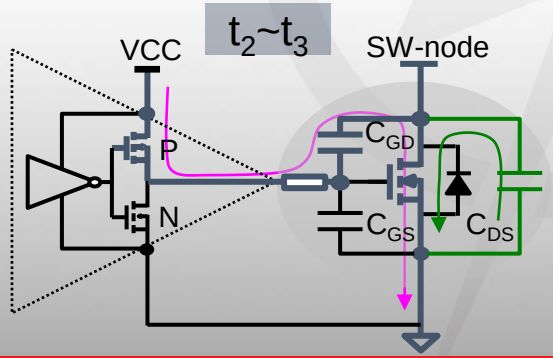
Switching on loss

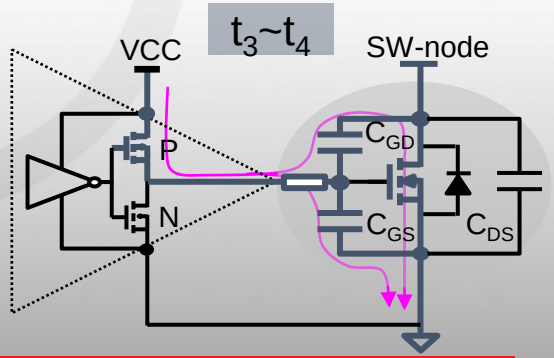
$$\int_{t_1}^{t_3} V_{DS}(t) \cdot I_D(t) dt + E_{OSS}$$

$$t_{1\sim3} \propto \frac{1}{I_{Drv}}$$

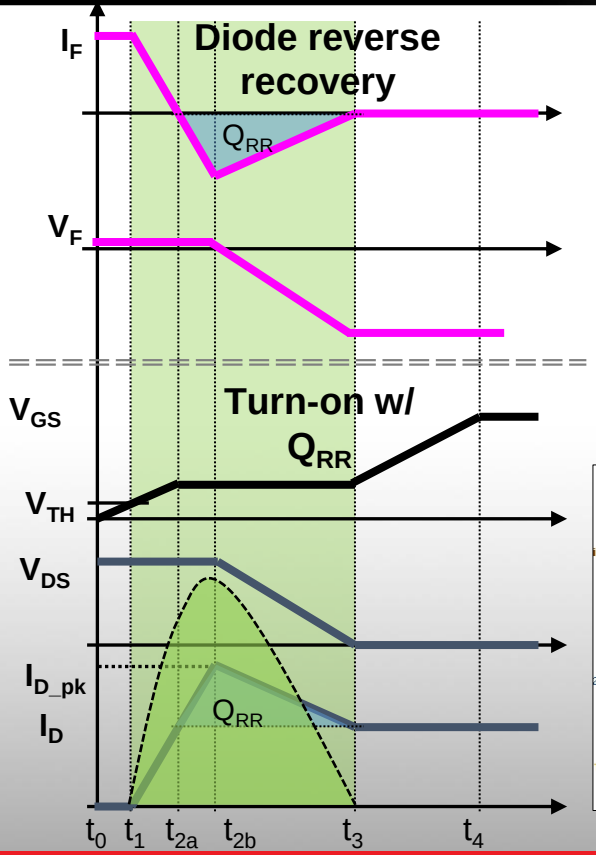
Stronger driver → lower switching loss



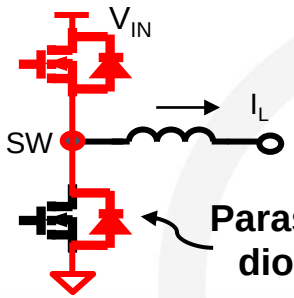


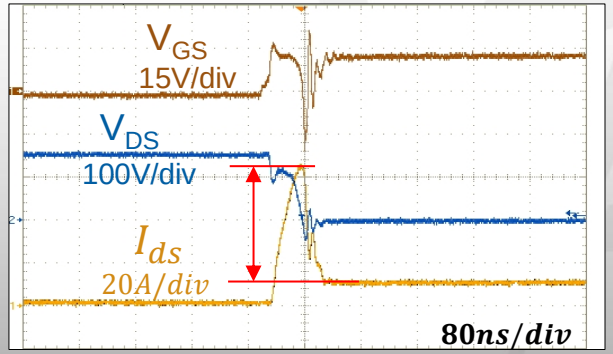


Turn-ON with Reverse Recovery

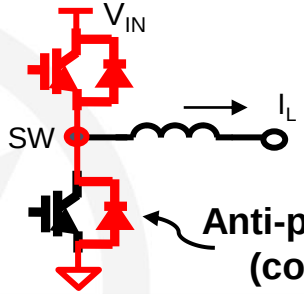


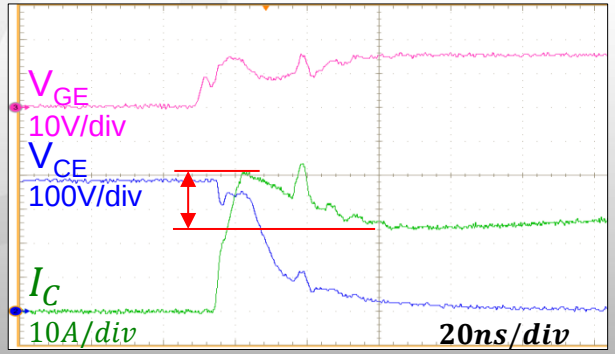
SJ-MOSFET



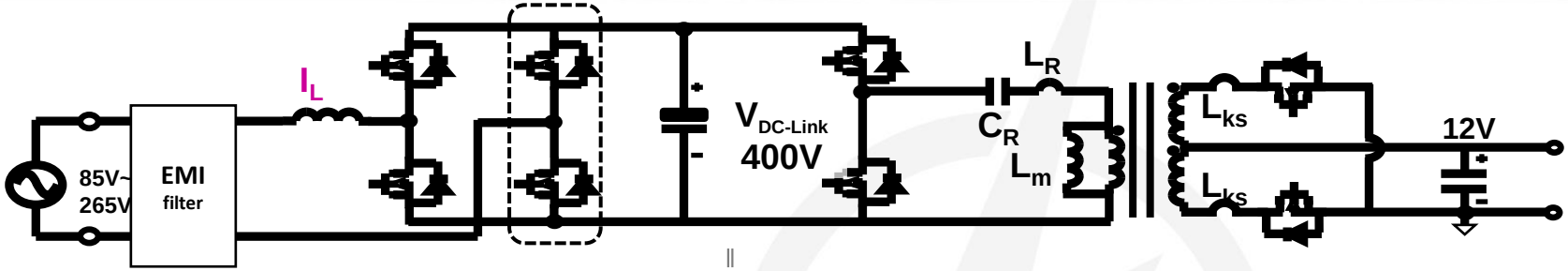


IGBT

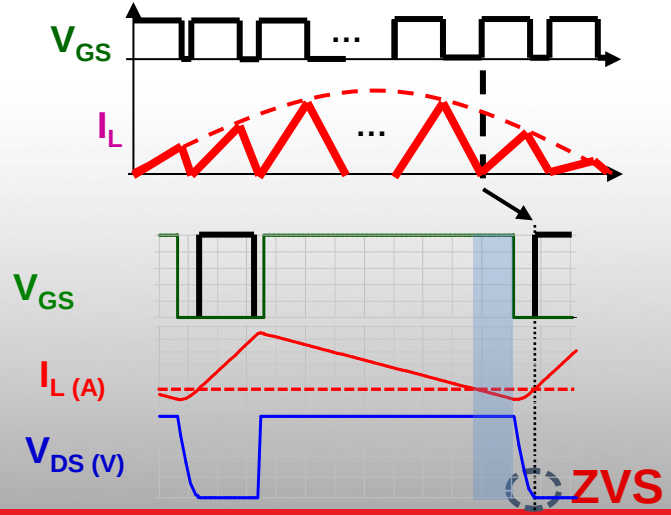




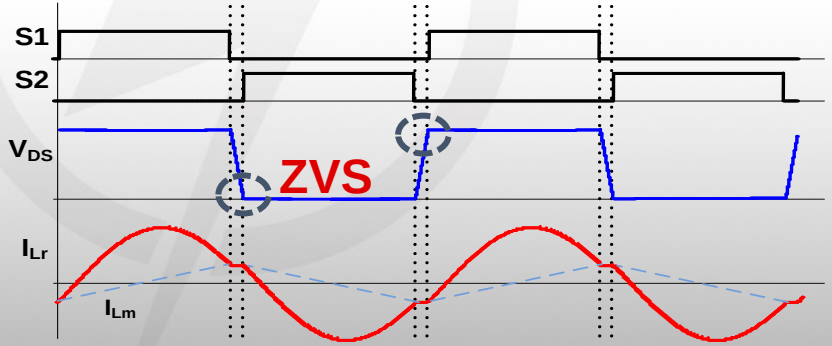
Soft Switching



CRM totem pole PFC

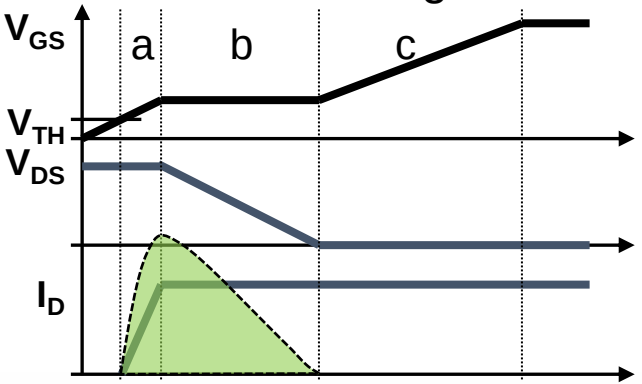


LLC converter + center-tap rectifier

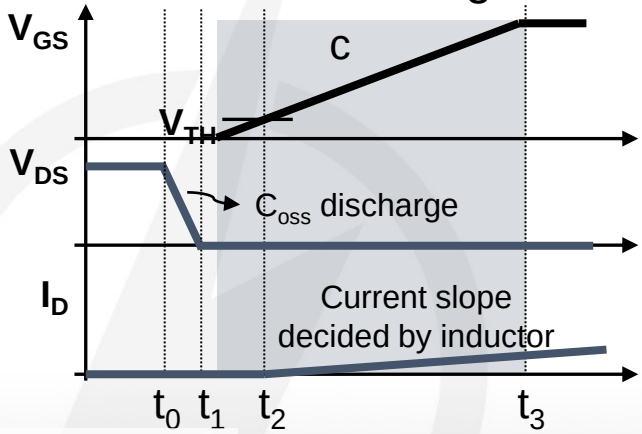


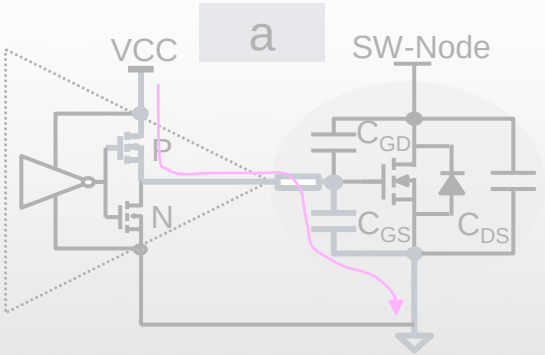
Gate Driver for Soft Switching

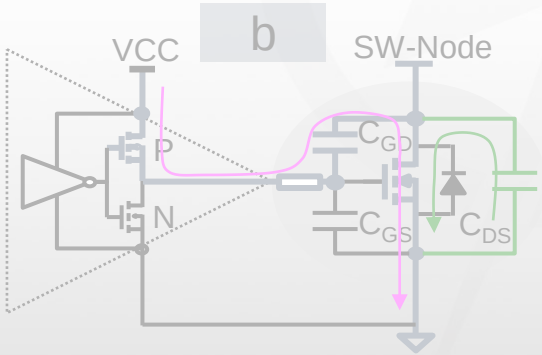
Hard-switching

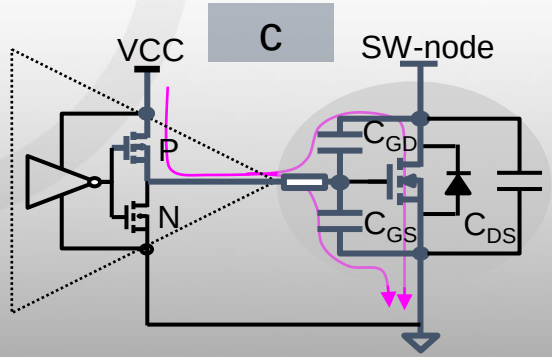


Soft-switching

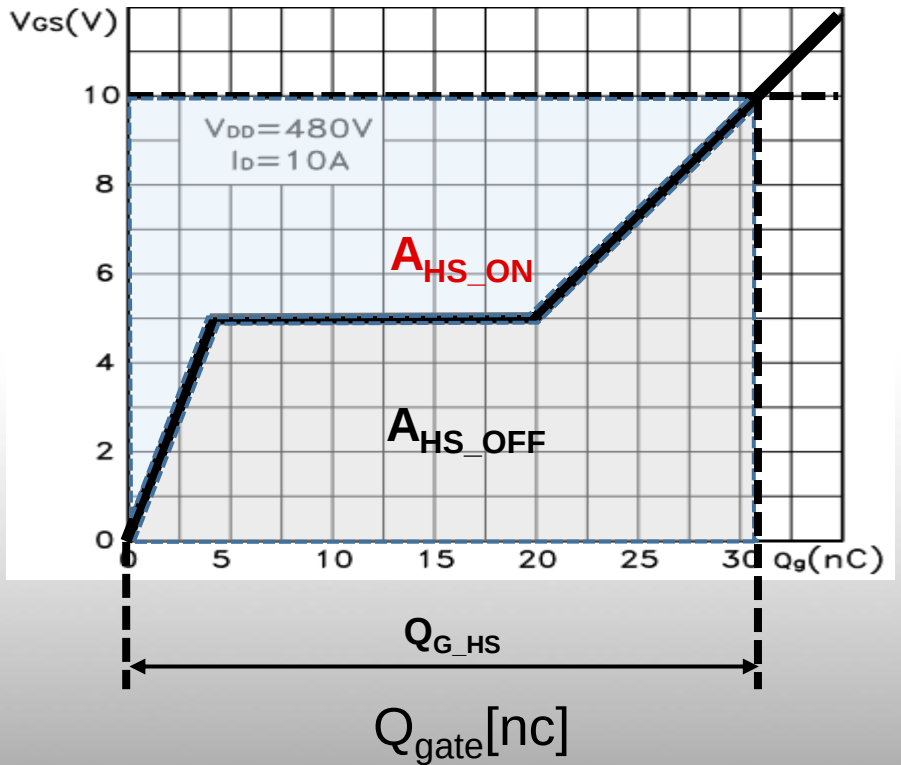




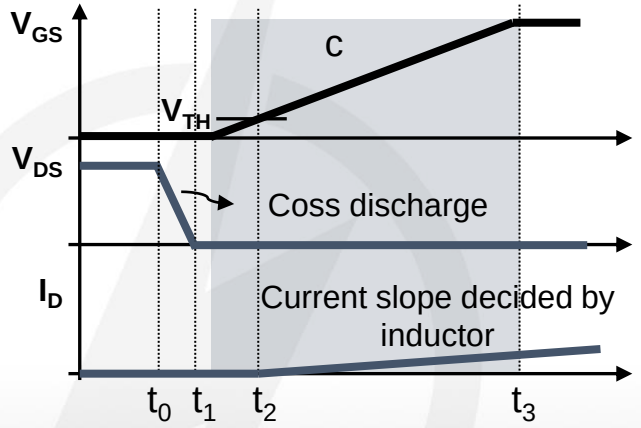




Gate Driver for Soft Switching



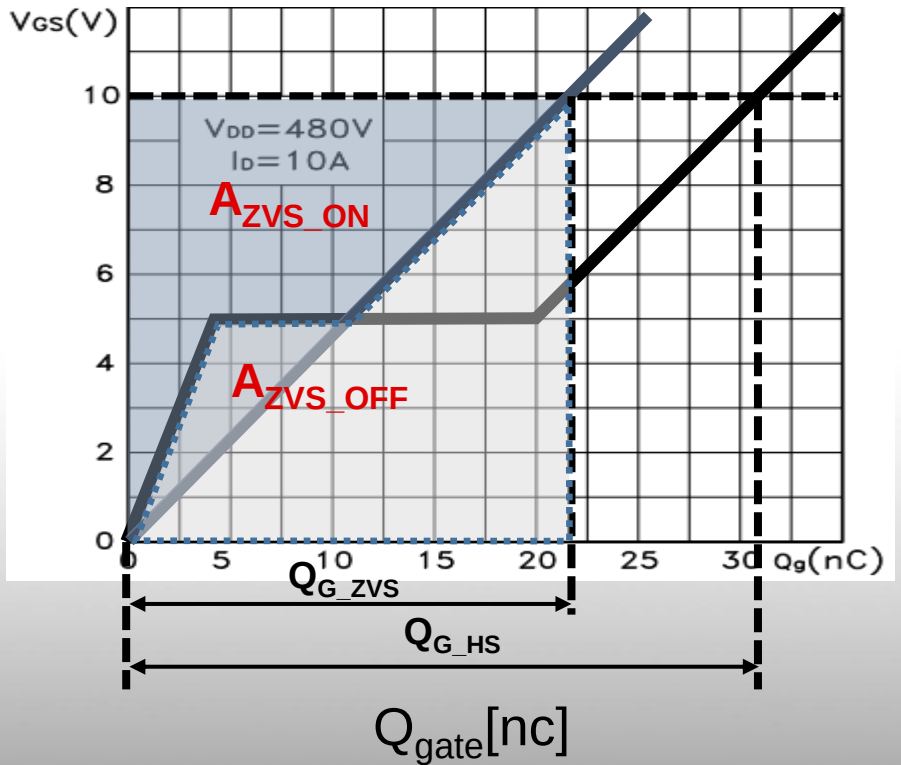
Soft-switching



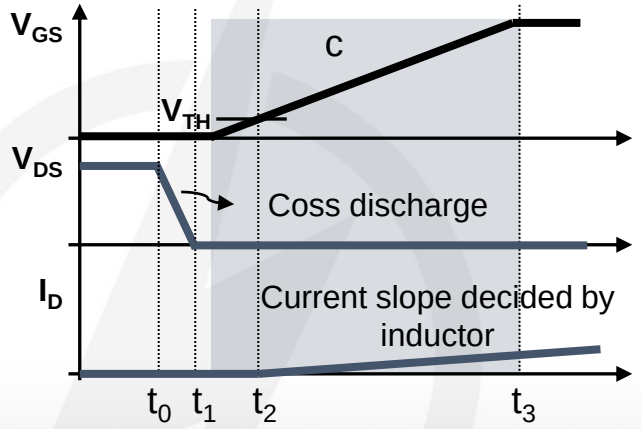
$$E_{G\_HS} = A_{HS\_ON} + A_{HS\_OFF} = V_{GS} \cdot Q_{G\_HS}$$

$$P_{GateDrv} = E_G \cdot f_{SW}$$

Gate Driver for Soft Switching



Soft-switching

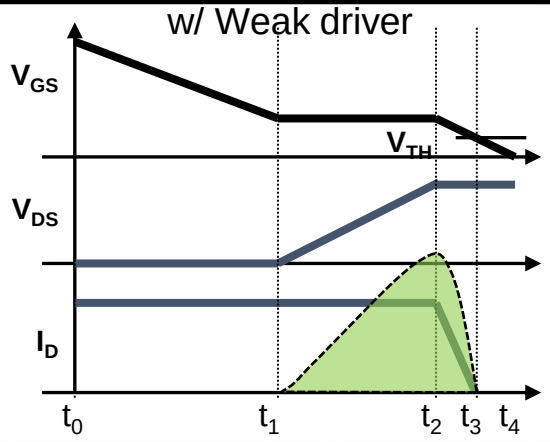


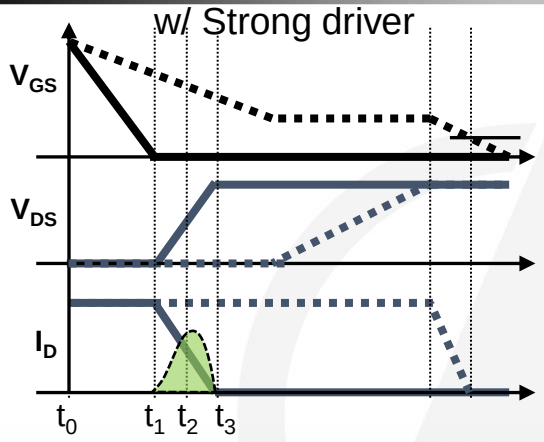
$$E_{G\_HS} = A_{HS\_ON} + A_{HS\_OFF} = V_{GS} \cdot Q_{G\_HS}$$

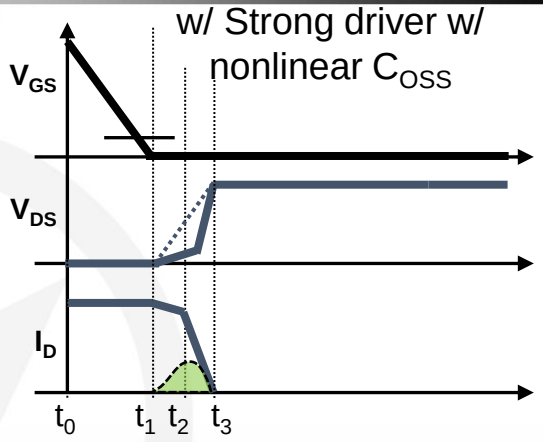
$$E_{G\_ZVS} = A_{ZVS\_ON} + A_{ZVS\_OFF} \approx V_{GS} \cdot Q_{G\_ZVS}$$

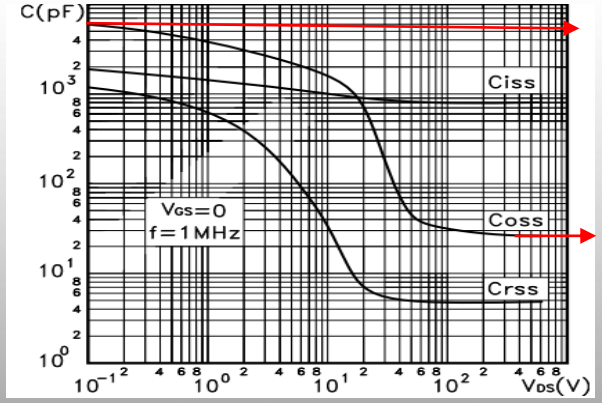
$$P_{GateDrv} = E_G \cdot f_{SW}$$

Strong Turn-OFF







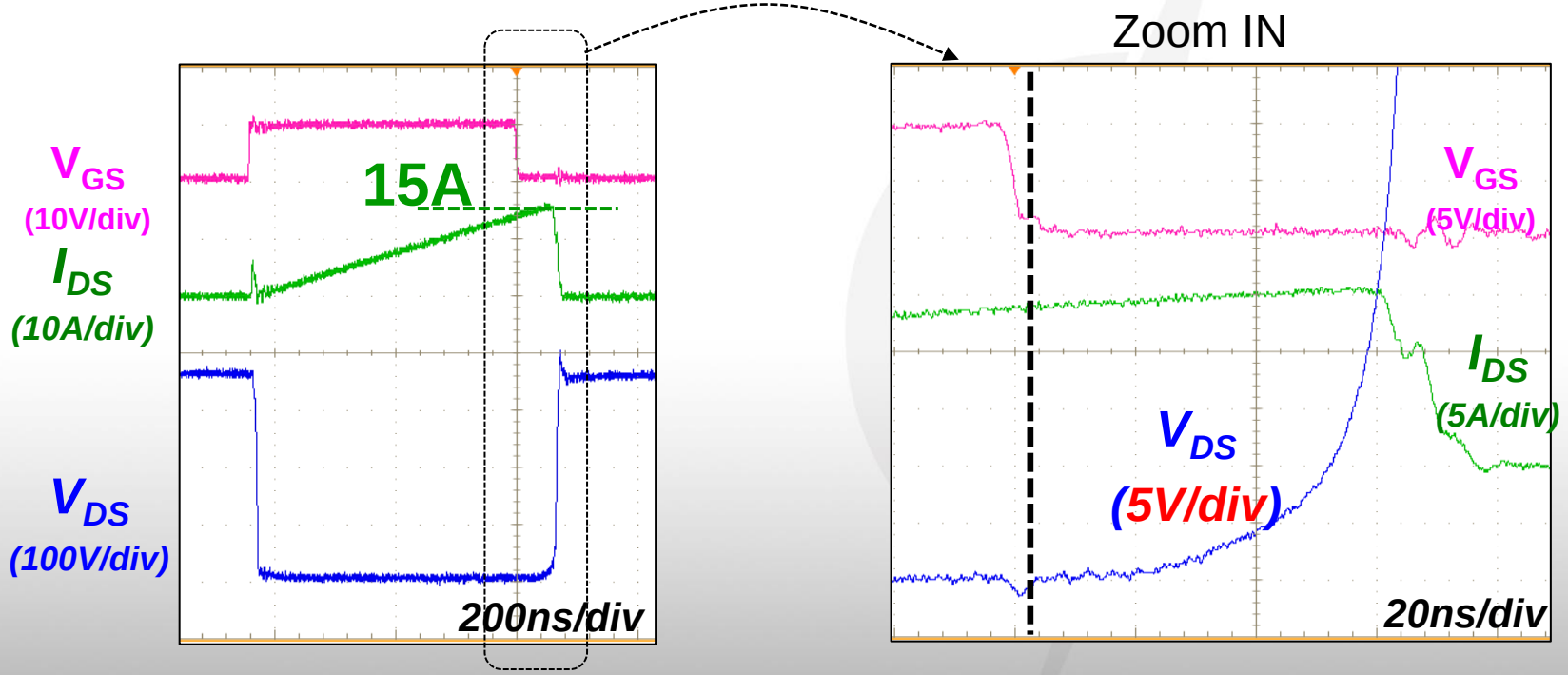


C_{OSS}(0V) =6nF

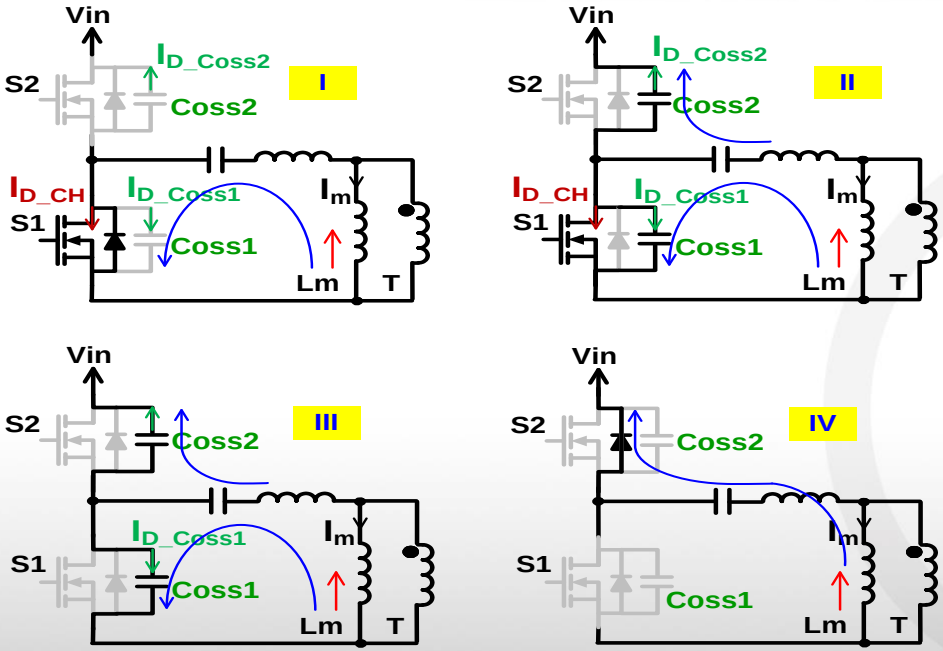
C_{OSS}(400V) <30pF

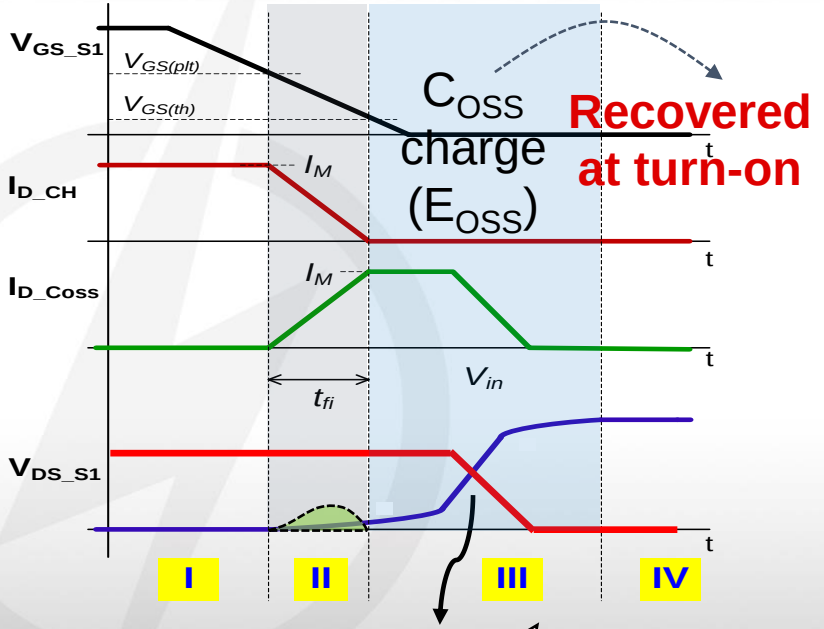
- Switching behavior is not controlled by gate current, but by C_{OSS} and load current
- Large C_{OSS} at low voltage performs as natural snubber
- Small C_{OSS} at high voltage shortens V-I overlap
- Fast dv/dt and di/dt, other bad things

Strong Turn-OFF



Strong Driver for LLC Turn-OFF



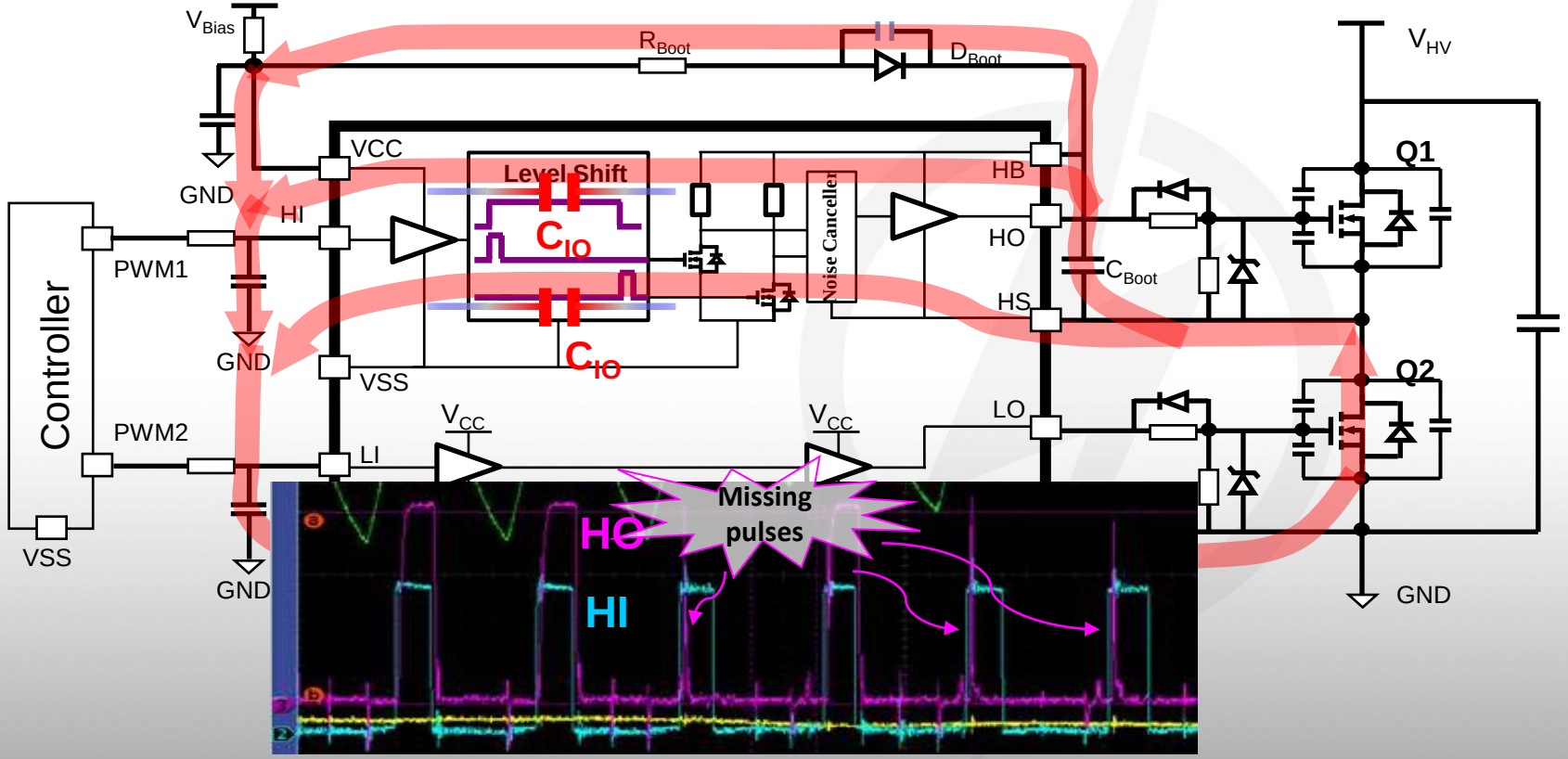


In period II, $V_{DS\_S1} << V_{DS\_S2}$; $C_{oss1} >> C_{oss2}$

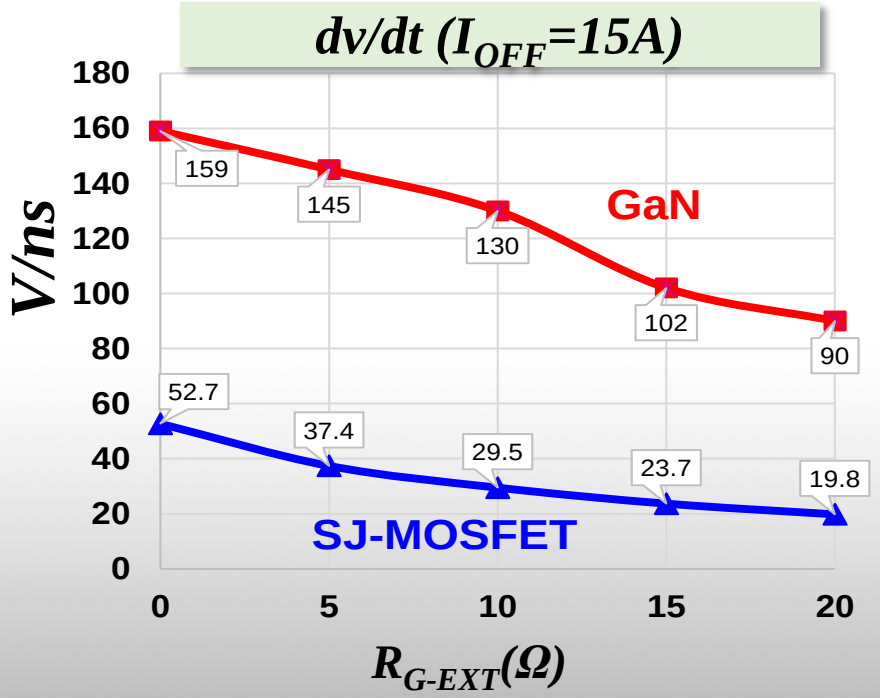
$$I_{D\_Coss} = I_{D\_Coss1} + I_{D\_Coss2} \approx I_{D\_Coss1}$$

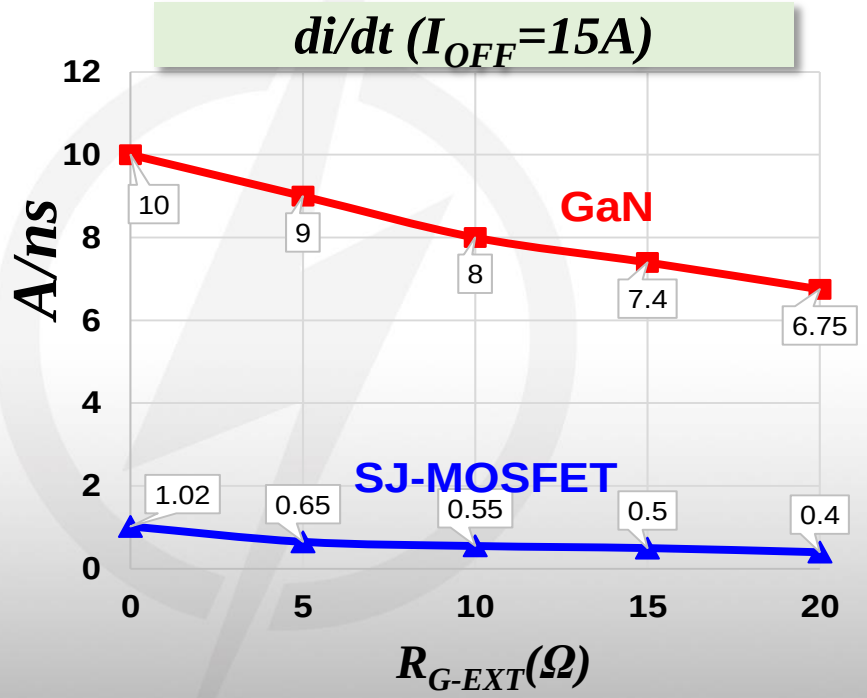
High dv/dt, di/dt

dv/dt and its influence

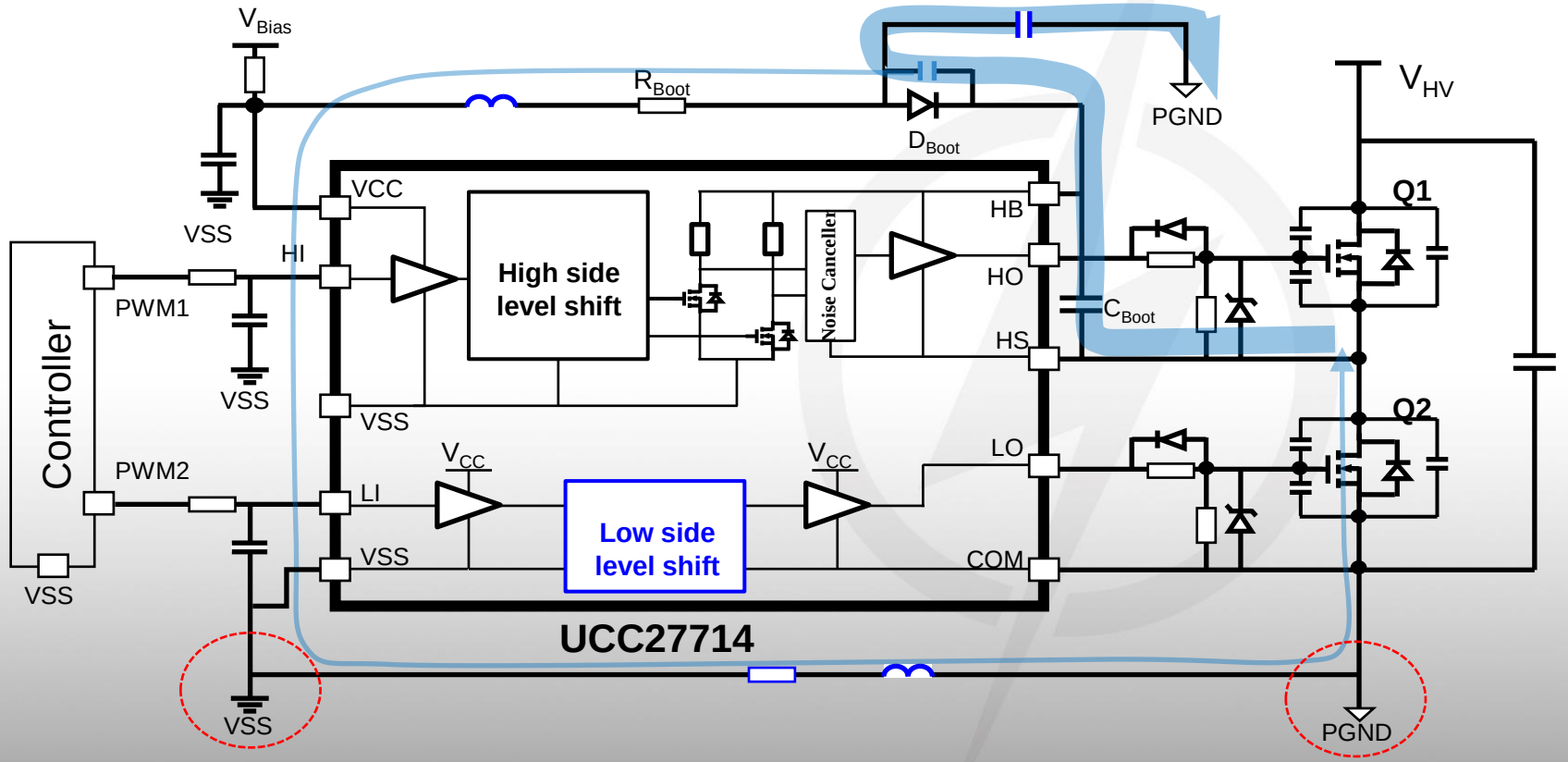


High dv/dt and di/dt: GaN vs. Si





Separate Power Ground Noise



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[5] “An introduction to LLC resonant half-bridge converter”, AN2644, ST
[6] Bo Yang, et al., “LLC Resonant Converter for Front End DC/DC Conversion”
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THANK YOU