SN65DSI83/84/85- Debugging and Troubleshooting Tips

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Initialization sequence

- Ensure that the initialization sequence in the datasheet is being followed

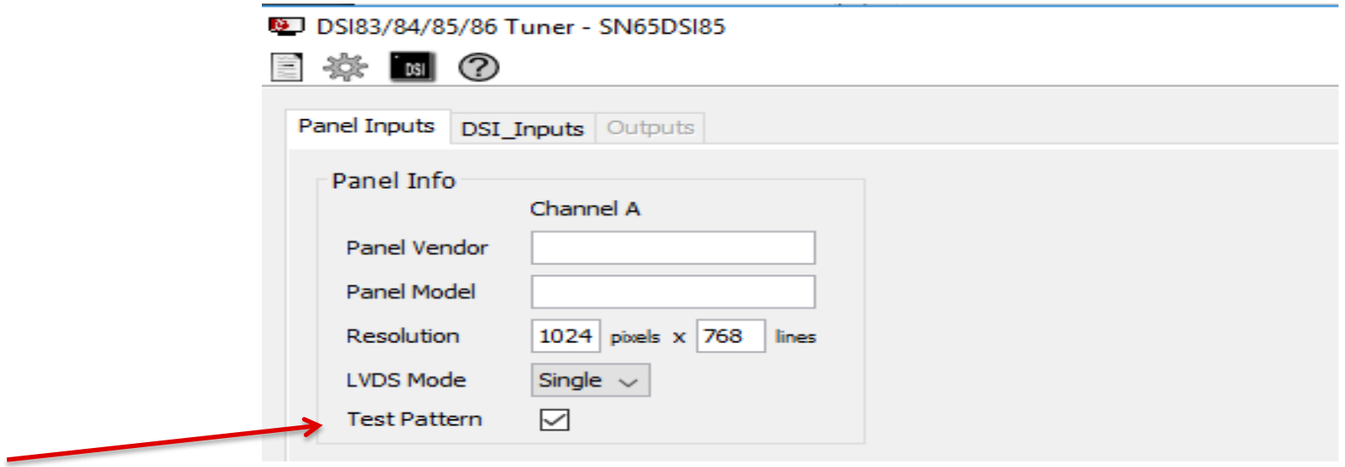
INITIALIZATION SEQUENCE NUMBER	INITALIZATION SEQUENCE DESCRIPTION
Init seq 1	Power on
Init seq 2	After power is applied and stable, the DSI CLK lanes MUST be in HS state and the DSI data lanes MUST be driven to LP11 state
Init seq 3	Set EN pin to Low
Wait at least 10 ms	
Init seq 4	Tie EN pin to High
Wait at least 10 ms	
Init seq 5	Initialize all CSR registers to their appropriate values based on the implementation (The SN65DSI8x is not functional until the CSR registers are initialized)
Init seq 6	Set the PLL_EN bit (CSR 0x0D.0)
Wait at least 10 ms	
Init seq 7	Set the SOFT_RESET bit (CSR 0x09.0)
Wait at least 10 ms	
Init seq 8	Change DSI data lanes to HS state and start DSI video stream

Test pattern

- Check to see if the test pattern can be displayed correctly to help isolate the issue

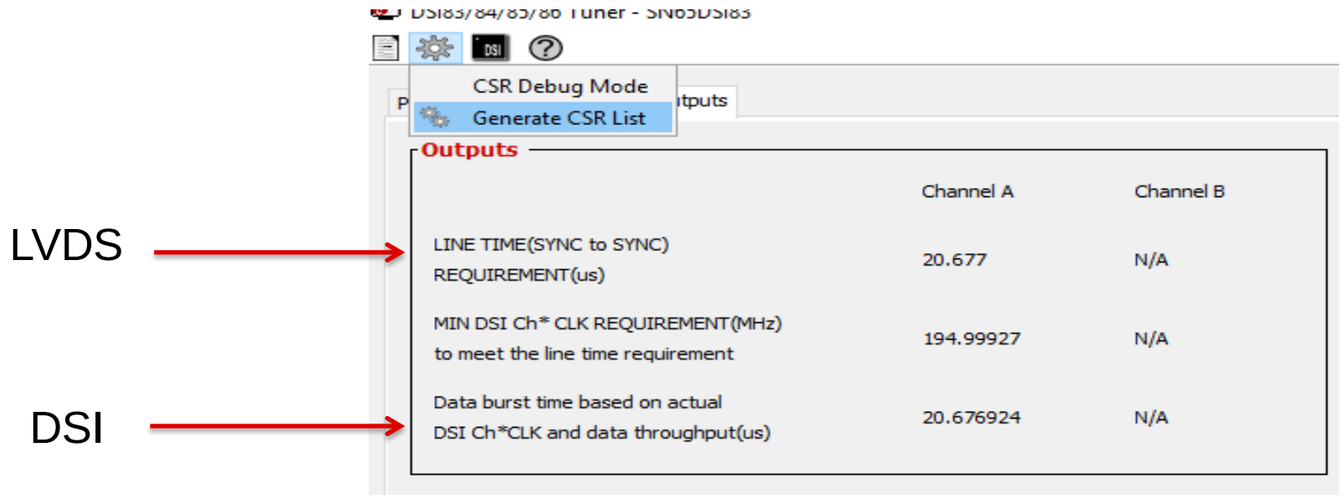
- The test pattern does not use the DSI input (except the DSI CLK as an option)

- The test pattern output can be configured with the DSI-Tuner. There are also instructions in the datasheet



Line time

- Ensure the line time is being met on the DSI side
- The line time (horizontal sync to the next horizontal sync timing from the processor) on the input is preserved when outputting onto the LVDS interface.



DSI clock

- If the DSI CLK is used to derive the LVDS CLK, then the DSI CLK **must operate in HS free-running (continuous) mode**

- If an external REFCLK is used as the source for the LVDS CLK, then the DSI CLK is allowed to stop during the blanking periods

Register configuration

- Verify the registers have been configured correctly for the application
- Video input timing, register configuration and the panel timing requirements all have to match up for video streaming to work without errors
- Use the DSI-Tuner for the majority of the configuration, and reference the register map in the datasheet
- Ensure the data mapping between the LVDS outputs and the display is correct

Checking error register

- Check 0xE5 (and 0xE6 if the SN65DSI85 is used) for any errors

- **Clear this register by writing 0xFF to it before reading it**
  - Some errors may get erroneously set during the initialization sequence

Additional resources

- SN65DSI8xEVM: http://www.ti.com/tool/sn65dsi85evm
  - User's Guide: http://www.ti.com/lit/ug/sllu221/sllu221.pdf
- Hardware Implementation and Schematic/Layout Guidelines: http://www.ti.com/lit/an/slla340a/slla340a.pdf
- DSI-Tuner: http://www.ti.com/tool/DSI-TUNER
- DSI-Tuner Manual: http://www.ti.com/lit/an/slla332b/slla332b.pdf
- Troubleshooting guide: http://www.ti.com/lit/an/slla356/slla356.pdf
- Support: https://e2e.ti.com/

Thanks for your time!