Introduction to **Processor SDK Radar – Part 2**

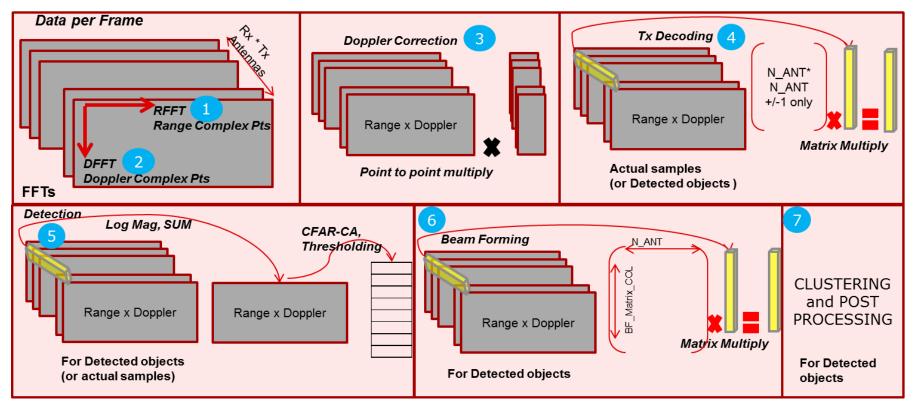


Agenda

- What is Processor SDK Radar?
 - Radar SDK Software Stack
- Processor SDK Radar Processing Chain
 - Algorithm Blocks (FFT, Peak Detection, Beam Forming)
 - Cascade Radar Data Processing Chain
- Getting Started with Processor SDK Radar

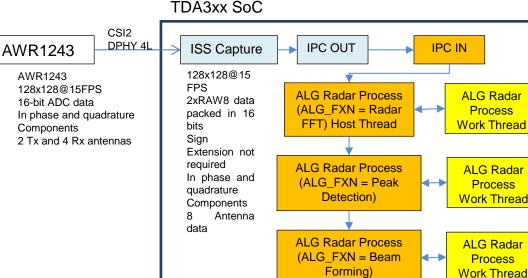


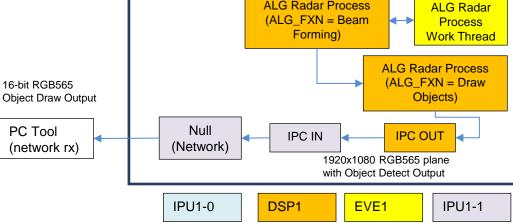
Radar Data Processing flow

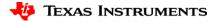


Single Chip AWR1243 based Object Detection using Processor SDK – Radar on TDA3xx

- This usecase demonstrates the EVE object detection computation.
- The data flow shows a radar data capture for a configuration of 128 samples per chirp and 128 chirps per frame @ 15 FPS for 4 Rx Antenna and 2 Tx Antenna.







Radar Process Algorithm Link

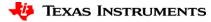
Alg Plugin (Framework)

Library API

| Alg Link | | | | | | | | |
|--------------|-------------|-----------------------------|---------------------------|--|--|--|--|--|
| FFT Algorith | Im Function | Peak Detect Alg Function | Beam Form Alg Function | | | | | |
| Range FFT | Doppler FFT | Peak Detector | Beam forming | | | | | |

- A single radar algorithm link exposes the FFT, Peak Detection and Beam forming algorithm modules.
- This is achieved by the concept of "Algorithm Function".
- The Algorithm link takes care of buffer management for single input and single output queue.
- Processor SDK Radar Users can develop their own Radar Processing algorithms and use the algorithm plugin and algorithm function infrastructure to create their own Radar processing

PROCESSOR_SDK_RADAR_xx_xx_xx_vision_sdk\apps\src\rtos\radar\src\alg_plugins



Algorithm Modules (FFT)

Sub-function within API

| | | FFT | | |
|--------------------------|-----------|-----------|-----|-----------------------|
| Interference zero out | DC offset | windowing | FFT | Doppler correction |

• Kernels

- FFT: 64, 128, 256, 512, 1024 point FFT kernels (16-bit fixed point with shift control at each stage, overflow detection)
- Interference zero out
- DC offset
- Windowing
- Doppler correction

• Applet

- XDAIS based interface
- Control to enable/disable interference zero out, DC offset, windowing and Doppler correction
- DMA based data flow using internal memories for data processing



Algorithm Modules (Peak Detector)

Sub-function within API

| Peak Detector | | | | | | | | | |
|---------------|------------------------|----------------------|--|--|--|--|--|--|--|
| Tx decoding | Log magnitude & SUM | CFAR-CA detection | | | | | | | |

- Kernels
 - Tx decoding
 - Log magnitude, sum
 - CFAR-CA detection

PROCESSOR_SDK_RADAR_xx_xx_xx_ti_components\alg orithms\eve_sw_xx_xx_xx\apps\peak_detection

Applet

- XDAIS based interface
- Control to enable/disable Tx decoding
- Control for energy computation for detection to be sum of log magnitude vs direct energy sum
- Control for cell sum direction (range vs doppler)
- DMA based data flow using internal memories for data processing



Algorithm Modules (Beam forming)

Sub-function within API

| Beam forming | | | | | | | | | |
|-----------------|-----------------------|----------------------|--|--|--|--|--|--|--|
| Matrix multiply | Energy computation | Peak localization | | | | | | | |

- Kernels
 - Matrix multiply
 - Energy computation
 - Peak Localization

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Applet

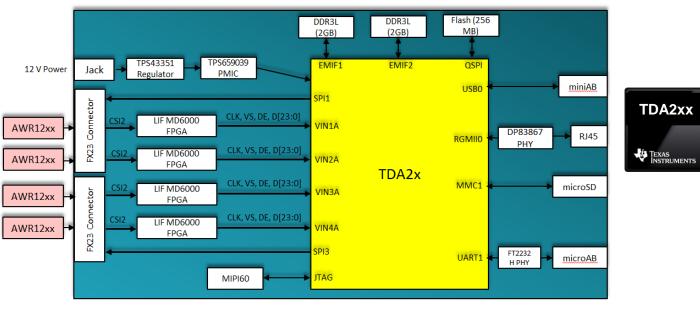
- XDAIS based interface
- DMA based data flow using internal memories for data processing



System architecture: Cascade FMCW radars

MIMO cascade with synchronous radars

2 PCB system, Up-to 192 radar virtual array combinations Radar front-end few inches from processors

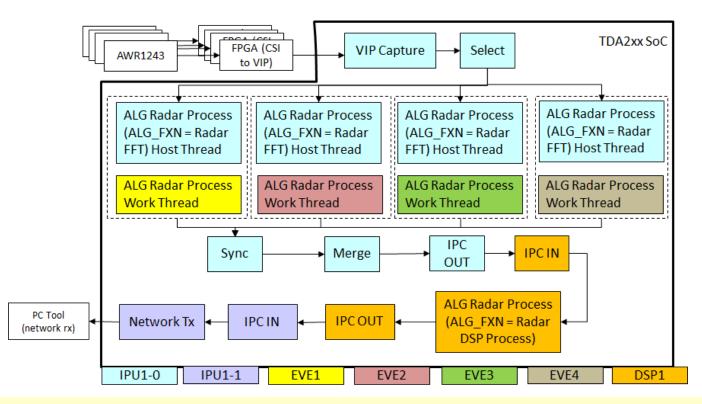


AWR1243 mmWave Sensors Highly configurable frequency modulated continuous wave radio frequency transceivers with 76-81 GHz band which support up to 3 transmit (Tx) and 4 receive (Rx) chains

Highly optimized and scalable family of TI ADAS devices. Mix of TI's fixed and floating-point TMS320C66x digital signal processor (DSP), Vision/Vector AccelerationPac (EVE), ARM Cortex-A15 MPCore[™] and dual-Cortex-M4 processors.



4-Chip Cascade Radar Data Flow



PROCESSOR_SDK_RADAR_03_05_00_00\vision_sdk\docs\Radar\ProcessorSDKRadar_DataSheet.pdf



Radar System Planner

• Excel Based Utility to analyze the Radar processing requirements on TDA devices.

| Configurations | | | | | | | | | | | | | | | |
|-------------------------------------|---------------|---------------|--------------|------------|---------|---------------|----------|---------------|-------------|----------|------------|-------------|----|-------------|-------------|
| Range Dimension | 1024 | DDR BW = 95 | OCMC BW = 0 | DDF | BW = 0 | OCMC BW = 0 | c | DR BW = 0 | OCMC BW = 0 | DE | OR BW = 95 | OCMC BW = 0 | | DDR BW = 95 | OCMC BW = 0 |
| Doppler Dimension (per Tx) | 128 | Interfe | rence Zero | | | | 1 F | | | | | | | | |
| Rx | 4 | | | | D | C Offset | | Range | Window | | Rai | nge_FFT | | Doppl | er_Window |
| Tx | 3 | | out | | | | 1 | | | 1 | | | | | _ |
| Frames/sec | 15 | EVE | 0.00% | EVE | | 0.62% | E | VE | 1.2 | 4% EV | /E | 0.0 | 0% | EVE | 11.69 |
| Multiplexing across Tx | Yes | | | | | | | | | | | | | | 1 |
| Detection Method | CFAR-CA | | K | | | | | | | | | - | | | - |
| Detection/dwells | 20 | DDR BW = 0 | OCMC BW = 0 | DDF | BW = 95 | OCMC BW = 0 | E | DR BW = 0 | OCMC BW = 0 | DE | OR BW = 8 | OCMC BW = 0 | | DDR BW = 9 | OCMC BW = 0 |
| Number of Angles (Angle resolution) | 120 | | * | | | | T T | | | | | | | | |
| System Overhead | 5% | Den | nlan FFT = | | l- | | | Free | ~ | | 1.00.1 | An amituda | | | |
| virtual Anteenas | 12 | Dop | pler_FFT = | | Doppie | er Correction | | Ener | gySum | | LOG N | lagnitude | | CFAR-C | A Detection |
| #Raw samples/dwell (cube size) | 1572864 | | | | | | | | | | | | | | |
| Plane size (range * doppler) | 131072 | EVE | 0.00% | EVE | | 11.30% | E | VE | | 0% EV | /E | | 0% | EVE | |
| #Object samples/dwell | 240 | | < | | | | | | | _ | | | | | - |
| BeamForming Matrix Column | 120 | | | | | | | | | | | | | | |
| Sample size (in bytes) | 4 | DDR BW = 1 | CMC BW = 0 | DDF | BW = 1 | OCMC BW = 0 | - | | | | | _ | | | |
| | | A | . Fatimation | | Deat | Duccessing | | Color Legends | EVE | C66x | M4 | | | | |
| | | Azimuti | n Estimation | | Post | Processing | L | COIDI Legenus | LVL | COOX | 1014 | | | | |
| | | D/F | 09/ | | | 08 | | | | | | | | | |
| | | EVE | 0% | C66 | ĸ | 0% | | | | | | | | | |
| | | | | | | | | | | | | | | | |
| SOC Utilizati | on Summary | | [| ļ ļ | | | | | | | | | | | |
| Processing/Memory subsystem | Freq(MHz) #co | ores %Loading | | | | SOC Ut | ilizatio | on Summa | ary | | | | | | |
| EVE | 500 | 1 25% | 6 | 35% | | | | | | | | | | | |
| C66x | 500 | 2 09 | 6 | 30% | | | | | | | | | | | |
| M4 | 212 | 1 309 | 4 | | | | | | | | | | | | |
| DDR3 BW | 532 | 1 249 | | 25% | | | | | | | | | | | |
| | | | | 20% | | | _ | | | | | | | | |
| DCMC BW | 266 | 1 09 | 6 | | | | | | | %Loading | | | | | |
| OCMC Memeory Size (KB) | 0 | | | 15% | | | | | | %Loading | | | | | |
| Serve Memeory Size (RD) | 0 | | | | | | | | | | | | | | |
| | | | | 10% | | | | | | | | | | | |
| Cells to control - user input | | | | 5% | | | | | | | | | | | |
| Derived (computed) information | | | | 570 | | | | | | | | | | | |
| | | | | 0% | | | | | | | | | | | |
| | | | | | | | | | | | | | | | |
| | | | | 1 | * EVE | 2 * C66x | 1 * M4 | 1 * DDR3 BW | 1 * OCMC BW | | | | | | |

Looking for Support?

- Use TI E2E forum to get additional support
- Kindly post queries/feedback on below forum
 - https://e2e.ti.com/support/arm/automotive_processors



Thank you





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