The McASP Primer

Bonus material: 48 kHz frame sync, Audio FIFO configuration

How do I generate a 48 kHz frame sync with McASP?

- Keep in mind that McASP only has integer clock dividers.
- Work backwards, starting with the frame sync, since that is your target. AFSX/AFSR = 48 kHz (fs). What must be the frequency of the ACLKX/R?
- In the case of I2S, we have two slots per frame. Each slot consists of 32 bits; Even if the data payload is only 16 bits or 24 bits, we'll encapsulate it within a 32-bit word. Based on this logic, we need a bit clock (ACLKX/ACLKR) of:

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2 slots * 32 bits per slot * 48 kHz = **3.072 MHz**

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- In order to generate all audio clocks internally, AUXCLK must be running at one of these three frequencies.

- If one of the above AUXCLK rates is not available, then an external master clock must be provided to AHCLKX or AHCLKR. The bit clock divider and frame sync generator may then be used to generate the desired clocks.

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- WNUMEVT/RNUMEVT should be configured large enough to allow for the CPU/DMA to burst many samples at once, though it should be small enough so as to avoid over/underflows. Often these are configured equal to half the FIFO depth. For example, for a 64-word FIFO, it is common to configure WNUMEVT=RNUMEVT=32.

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- The DMA needs to be configured such that in response to an AFIFO event it transfers WNUMEVT/RNUMEVT words. A common configuration for devices with EDMA would be to configure the transfer as AB-synchronized with ACNT=4 and BCNT=WNUMEVT (or RNUMEVT).

For more information

- McASP Design Guide: Tips, Tricks, and Practical Examples
  http://www.ti.com/lit/sprack0

- For questions about this training, refer to the E2E Community Forums at
  http://e2e.ti.com