PMIC or discrete: How to design multi-rail power supply for embedded processors & FPGAs

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Agenda

- **Introduction to high-performance processing platform**
  - Use cases for embedded processors & FPGAs
- **Power requirements of embedded processors & FPGAs**
  - Typical requirements for each power rail
  - Care-abouts for power sequencing
- **How to Design a robust power tree for processing platform**
  - Discrete solution
  - PMIC
- **Selection and architecture - PMIC or discrete**
  - Pros and cons
- **Reference designs**

Embedded processors are everywhere

Embedded processors play a KEY role for the next generation of Industry 4.0 & IoT-related applications

Human machine interface

Robotics

Smart appliances

Building control

Machine vision

Connectivity

Artificial intelligence

Applications are getting ‘smarter’ -- appliances

With more features combined into one application, higher-level requirements are coming for embedded processors

★ Real-time performance ★ Graphic accelerators ★ Rich peripherals ★ Scalability Platform

Display and user interface

- Bigger screen and increased resolution
- Audio/video and graphics capabilities
- Touch interface
- Gesture recognition

Highly integrated features

- Multiple sensors integrated
- Machine vision with camera & ToF
- Voice recognition
- AI and machine learning

Connectivity

- WIFI, BLE, ZigBee, 5G connectivity
- Cloud connectivity for post processing, Analysis, Diagnosis, etc.
- High bandwidth gateway and router

TI Products – Sitara™ Processors

Single processor platform for industrial applications

Sitara processors

Scalable + Flexible

- Industrial-grade processors
- Single scalable platform unified by Processor SDK
- PRU-ICSS, DSP acceleration, 2D/3D and video acceleration
- Rich peripherals with security enablers
- Customer proven ease-of-use

Processor SDK

Cutting-edge software

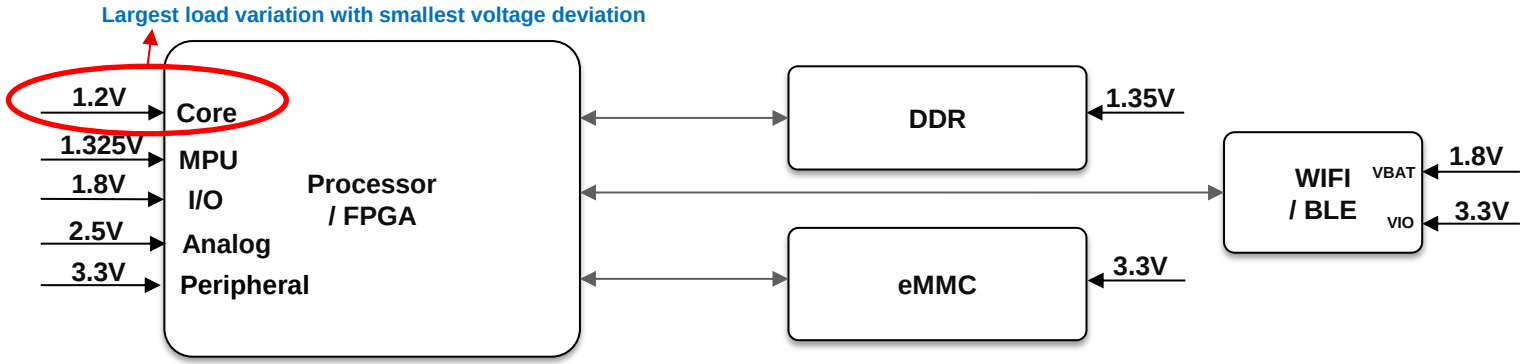
- Common Linux, Linux-RT and RTOS SDK for all Sitara processors
- LTS Linux brings quality, stability, easy migration
- Application-specific libraries and system demos eases customer's software development

Reference Designs
Online reference designs

TI E2E™ community

www.ti.com/sitara

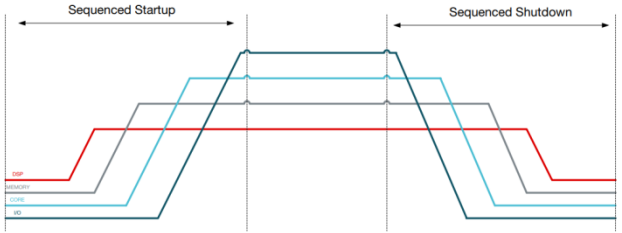
Multi-rail power supply for a processor and FPGA



High-performance power rails

- Critical voltage regulation
  - DC set point accuracy
  - Transient response
- High efficiency over wide load
- Occupied space
- PCB layout

Strict power up and down sequencing



☹ Improper power sequencing can cause reliability problems:
Such as Characteristics degradation, Inrush currents and Latch-up.

Multi-rail power supply -- An example for specs requirements

AM335x, DDR3L, eMMC, WL1837MOD					
Sequence	Power Supply	Device	Nominal Rating	Grouping	Max Current [mA]
4-up, 1-down	VDD_CORE	AM335x	1.1V ±4%	1.1-V Core	400
4-up, 1-down	VDD_MPU	AM335x	1.325V ±4%	1.325V MPU	1000
1-up, 4-down	VDDS	AM335x	1.8V ± 5%	1.8-V IO	605
1-up, 4-down	VIO	WL1837MOD	1.62~1.95	1.8-V IO	< 400
1-up, 4-down	VDDS_SRAM_MPU_BB, VDDS_SRAM_CORE_BG, VDDA_ADC, VDDS_PLL_DDR, VDDS_PLL_MPUVDDS_PLL_CORE_LCD, VDDS_OSC, VDDA1P8V_USB0, VDDA1P8V_USB1	AM335x	1.8V ± 5%	1.8-V Analog	135
2-up, 3-down	VDDA_USB0, VDDA_USB1, VDDSHVx	AM335x	3.3V ± 5%	3.3-V Analog and IO	370
2-up, 3-down	VBAT	WL1837MOD	3.3	3.3-V	850
2-up, 3-down	V_NAND	NAND Flash	3.3	3.3-V	80
2-up, 3-down	Other peripheral	Board	3.3V	3.3V-Others	<500
3-up, 2-down	VDDS_DDR,V_DDR3L	DDR3L	1.35	1.35-V Core	250

Voltage regulation -- DC accuracy

Influencing parameters:

- Reference voltage Vref accuracy
- Feedback divider resistors tolerances
- Load and line regulation due to Error's Amplifier finite gain

V_{OUT}	Load regulation	V_{OUT} = 3.3 V PWM mode operation	0.05 %	/ A
V_{OUT}	Line regulation	3V ≤ V_{IN} ≤ 17 V, V_{OUT}= 3.3 V, I_{OUT} = 1000 mA PWM mode operation	0.02 %	/ V

- Non ideal Vout sensing and PCB traces effects (DC losses)

DC accuracy formula :

$$\Delta V_{out}/V_{out} \cong \pm 2T_R\left(1 - \frac{V_{ref}}{V_{out}}\right) + T_{V_{ref}} + Load\ Regulation$$

T_R = Tolerance of Resistors in %
$T_{V_{ref}}$ = Tolerance of Reference Voltage in %
V_{ref} = Reference Voltage of IC
V_{out} = Set point output voltage

Example:

TPS62480 for Xilinx Zynq XC7Z020

Power rail requirements	
Core Voltage	1V
Tolerance	5%
Max current	6A
Transient (typical)	50% load ≥1A/us

Calculation:

TPS62480 Datasheet	
Vref	0.6V
Tolerance Vref	1%
Tolerance resistors	0.1%
Load regulation	0.02%/A
Tolerances	1.08%
Load regulation @6A	0.12%
Total	**1.20%**

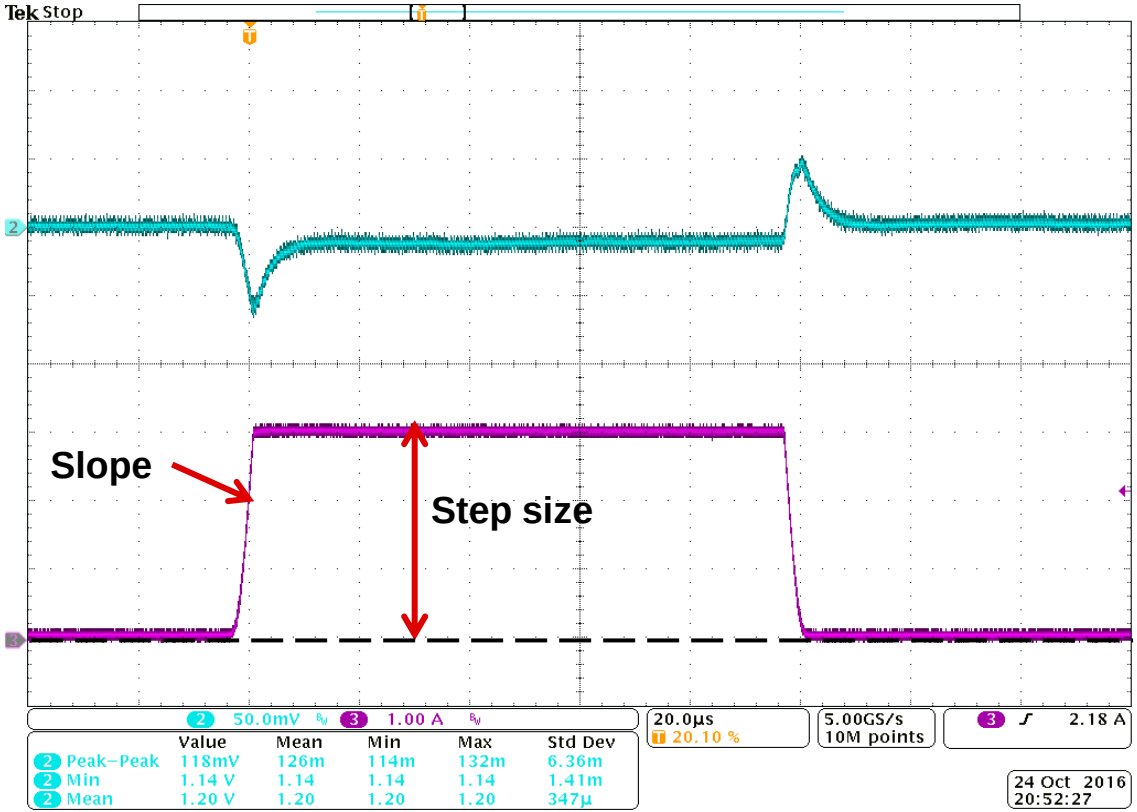
3.8% Margin

Voltage regulation -- Transient response

Influencing parameters:

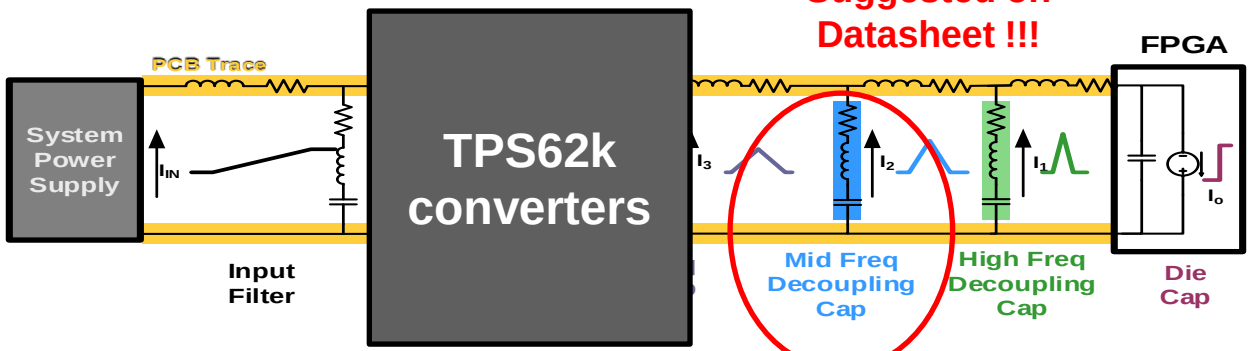
- Slope (A/us)
- Step size (A)
- Loop control topology
  - Voltage control mode
  - Current control mode
  - Hysteretic
  - DCS-control
- Output filter

Often occurs when processors transition from sleep mode to full-power operation



Voltage regulation -- Faster transient response

- No external compensation needed, enables faster design cycles.
- Optimized internal compensation minimizes transient response.
- Only output capacitors must be selected, according to datasheet's guidelines.



High=-bandwidth converter **eliminates the need of low freq. bulk cap**

Complete and **effective decoupling network**

Ceramic X5R and X7R dielectrics are great choices

https://training.ti.com/power-distribution-soc-and-fpga-applications

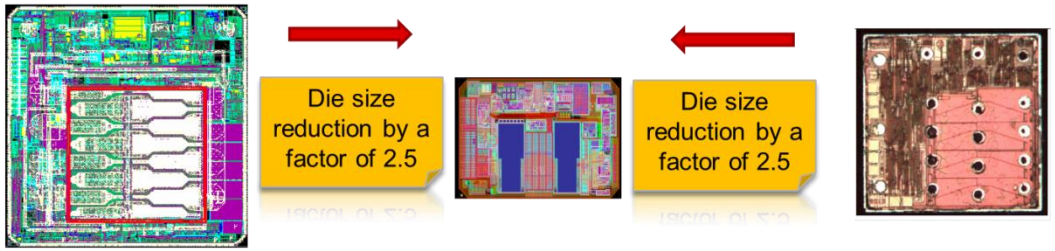
* From BSR-LPDC team's materials

Occupied space -- Compact design required

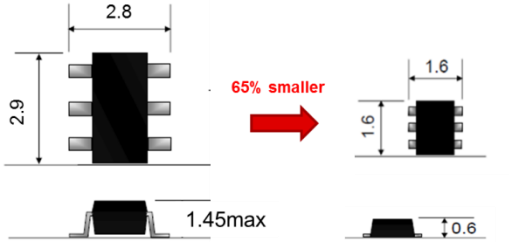
TPS62085 – 3A buck (LBC7)
- RDSon 31mΩ/23mΩ
- Die size 2.4mm²

TPS6282x – 3A buck (LBC9)
- RDSon 26mΩ/25mΩ
- Die size 0.96mm²

MP2131 – 3A buck
- RDSon 50mΩ/40mΩ
- Die size 2.4mm²



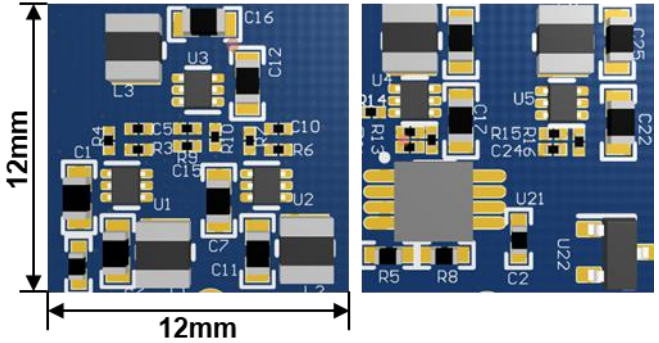
6x6 QFN48
7x7 QFP48



SOT23
Package size: 8.1mm²

SOT563
Package size: 2.6mm²

LBC 9 new level of performance and cost

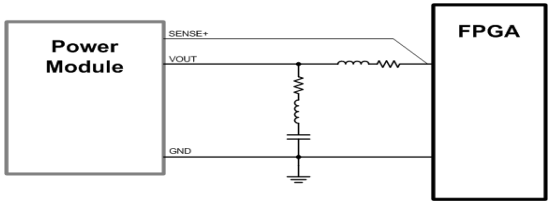


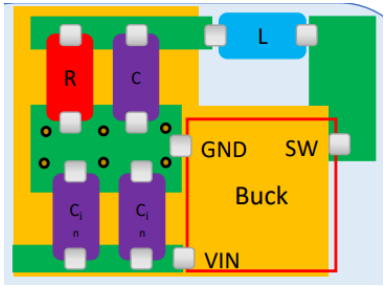
5-Rail Power Supply Design Board

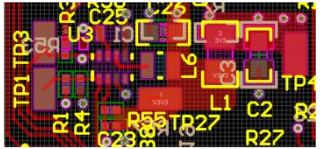
PCB layout -- Minimize DC loss

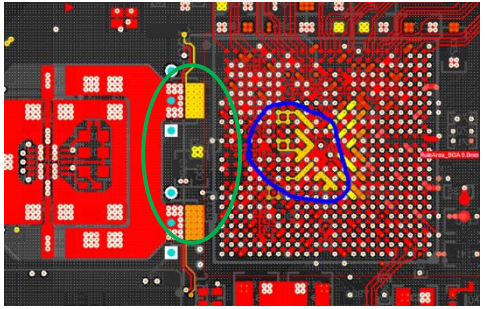
DC loss is the voltage drop due to non ideal sensing. This issue can be reduced by means of:

- **Remote sense**
  - R1 is connected as close as possible to the FPGA core supply pin (note: FPGAs have usually more than one core supply pin and they are often found in BGA packaging formats).
- **Wide/thick copper traces**
  - Reduced output resistance.
- **Place power supply close to FPGA supply input**
  - Shorter traces reduce resistance, as well as inductive loops.







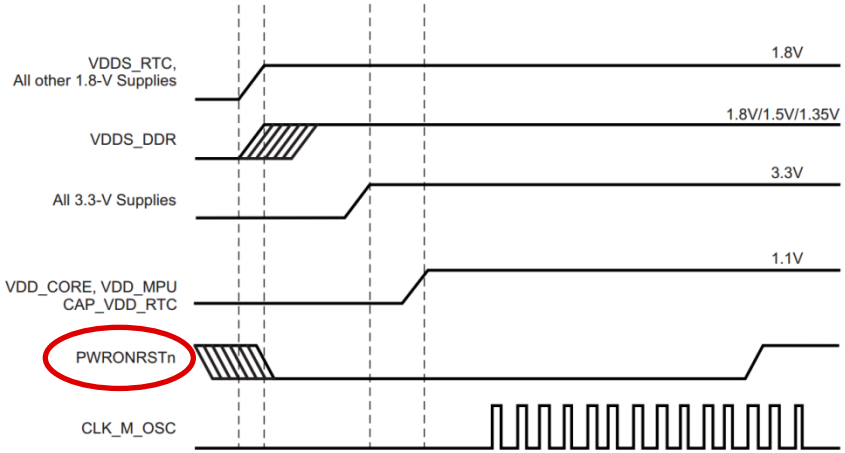


Power sequencing -- Not only sequencing

Example:

Power supply request for Sitara™ AM335x processors

(Power-supply sequencing with RTC feature disabled)



Power up sequencing

Power-down sequencing besides the reverse order of power-up sequencing:

- PWRONRSTn should be taken low at first
- Difference between VDDS and VDDSHVx <2V
- VDDS >= 1.5V after all other supplies fully ramp down

PWRONRSTn input terminal should be taken low, which stops all internal clocks before power supplies are turned off. All other external clocks to the device should be shut off.

The preferred way to sequence power down is to have all the power supplies ramped down sequentially in the exact reverse order of the power-up sequencing. In other words, the power supply that has been ramped up first should be the last one that should be ramped down. This ensures there would be no spurious current paths during the power-down sequence. The VDDS power supply must ramp down after all 3.3-V VDDSHVx [1-6] power supplies.

If it is desired to ramp down VDDS and VDDSHVx [1-6] simultaneously, it should always be ensured that the difference between VDDS and VDDSHVx [1-6] during the entire power-down sequence is <2 V. Any violation of this could cause reliability risks for the device. Further, it is recommended to maintain VDDS ≥1.5V as all the other supplies fully ramp down to minimize in-rush currents.

If none of the VDDSHVx [1-6] power supplies are configured as 3.3 V, the VDDS power supply may ramp down along with the VDDSHVx [1-6] supplies or after all the VDDSHVx [1-6] supplies have ramped down. It is recommended to maintain VDDS ≥1.5V as all the other supplies fully ramp down to minimize in-rush currents.

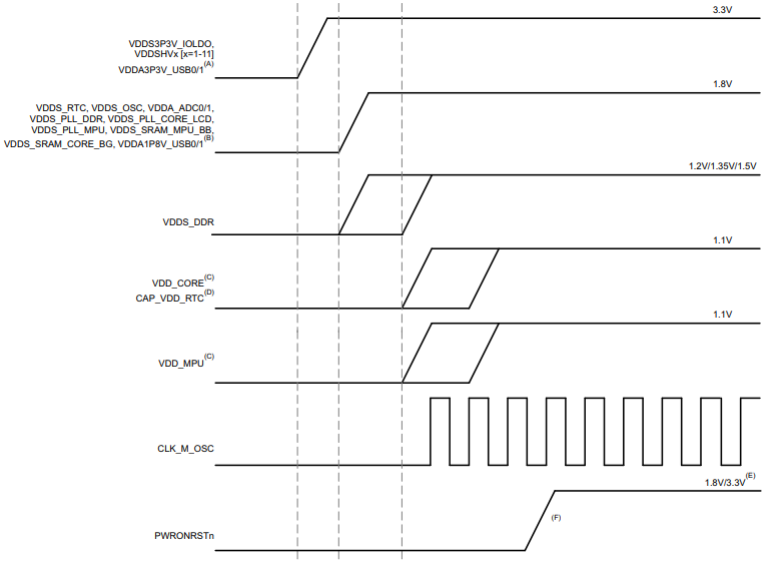
Power down sequencing

Power sequencing -- Simplified power-down sequencing

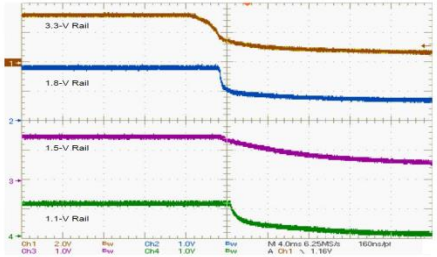
Example:

Power supply request for Sitara AM437x processors

(Simplified power sequencing with RTC feature disabled
Dual-Voltage IOs configured as 3.3V)



Power up sequencing



PWRONRSTn input terminal should be taken low, which stops all internal clocks before power supplies are turned off. All other external clocks to the device should be shut off.

The preferred way to sequence power down is to have all the power supplies ramped down sequentially in the exact reverse order of the power-up sequencing. In other words, the power supply that has been ramped up first should be the last one that is ramped down. This ensures there would be no spurious current paths during the power-down sequence. The VDDS, VDDS_CLKOUT power supply must ramp down after all 3.3-V VDDSHVx [x=1-11] power supplies.

If it is desired to ramp down VDDS, VDDS_CLKOUT and VDDSHVx [x=1-11] simultaneously, it should always be ensured that the difference between VDDS, VDDS_CLKOUT and VDDSHVx [x=1-11] during the entire power-down sequence is <2 V. Any violation of this could cause reliability risks for the device. Further, it is recommended to maintain VDDS, VDDS_CLKOUT ≥1.5V as all the other supplies fully ramp down to minimize in-rush currents.

If none of the VDDSHVx [x=1-11] power supplies are configured as 3.3 V, the VDDS, VDDS_CLKOUT power supply may ramp down along with the VDDSHVx [x=1-11] supplies or after all the VDDSHVx [x=1-11] supplies have ramped down. TI recommends maintaining VDDS, VDDS_CLKOUT ≥1.5V as all the other supplies fully ramp down to minimize in-rush currents.

When using simplified power-down sequence, there are no power-down requirements between the VDDS, VDDS_CLKOUT and VDDSHVx [x=1-11] supplies and are ramped down together without any reliability concerns.

Power down sequencing

Power sequencing -- Uncontrolled power off

Controlled power off

Powering off device by pressing the POWER BUTTON:

- Common way to power off a machine.
- Easy to monitor when this event occurs.
- Enough reaction time for controllers to execute power-down cycle.

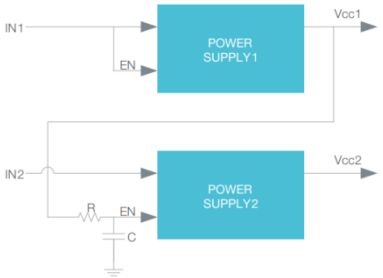
Uncontrolled power off

Occurs when pulling out the plug or power outage

- Unexpected way to power off a machine.
- Hard to monitor when this event occurs.
- Short reaction time for controllers to execute power-down cycle.

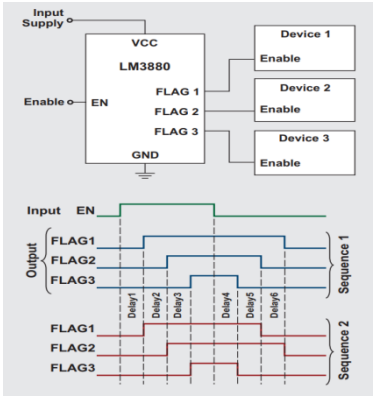
Power sequencing -- Ways to achieve sequencing

Discrete solution



RC-Delay Circuit
to delay the EN pin of device 2

⊗ **Not support power-down sequencing**



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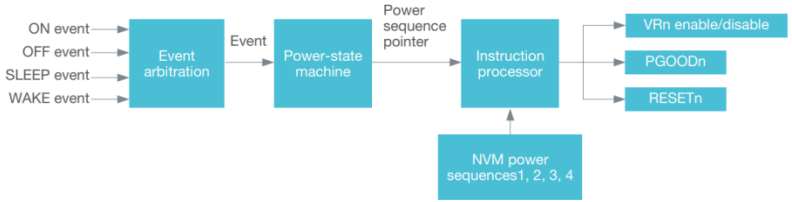
Analog Up/Down Sequencer

⊗ **Fixed numbers of Flags**

☺ **Flexibility configuration**

PMIC



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Instruction processor-based sequencing:

- Instruction processor executes instructions from memory
- ENABLE, DISABLE, and WAIT are present on NVM
- Event (power-up, power-down, faults, resets) sets memory pointer to fetch related instructions
- Generate power good and resets after an execution cycle

⊗ **Cost associated with NVM is intensive**

☺ **Flexibility configuration**