EOS and ESD on ADC
TI Precision Labs – ADCs

Presented by Alex Smith

Prepared by Dale Li

TEXAS INSTRUMENTS

ESD vs. EOS – What's the Difference?

ESD

- Electrostatic discharge
- Short duration event (1-100ns)
- High voltage (kV)
- Fast edges
- Both "in-circuit" and "out-of-circuit"

EOS

- Electrical overstress
- Longer duration event
  - Milliseconds or more
  - Can be continuous
- Lower voltage
  - May be just beyond absolute maximum ratings
- "In-circuit" event only

TEXAS INSTRUMENTS

EOS from Fault or Overdriven

Fault Conditions

- ✓ Harsh electrical environment

- ✓ High voltage circuit in the system

- ✓ Improper power up sequencing

- ✓ Hot-swap connection and disconnection

- ✓ Loss of power supply but input signal is applied

- ✓ Apply bipolar signal to unipolar input ADC

- ✓ Miswiring

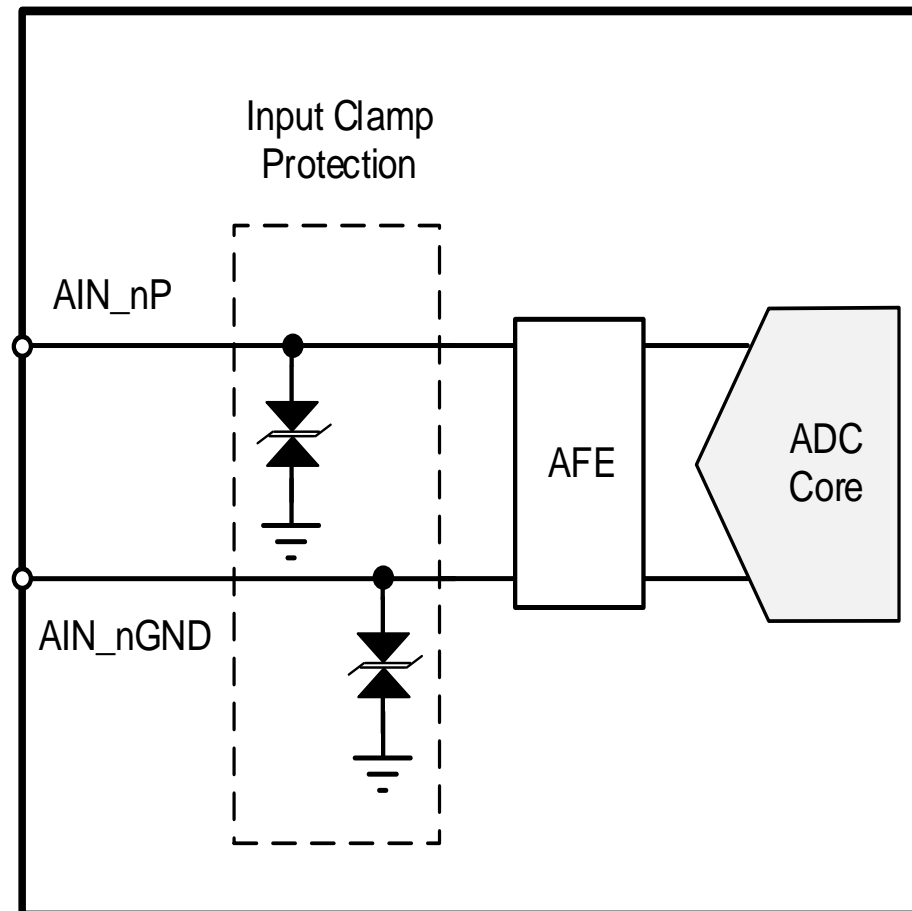- ✓ Other conditions violating the absolute maximum specifications

Transient

Transient

Ground

TEXAS INSTRUMENTS
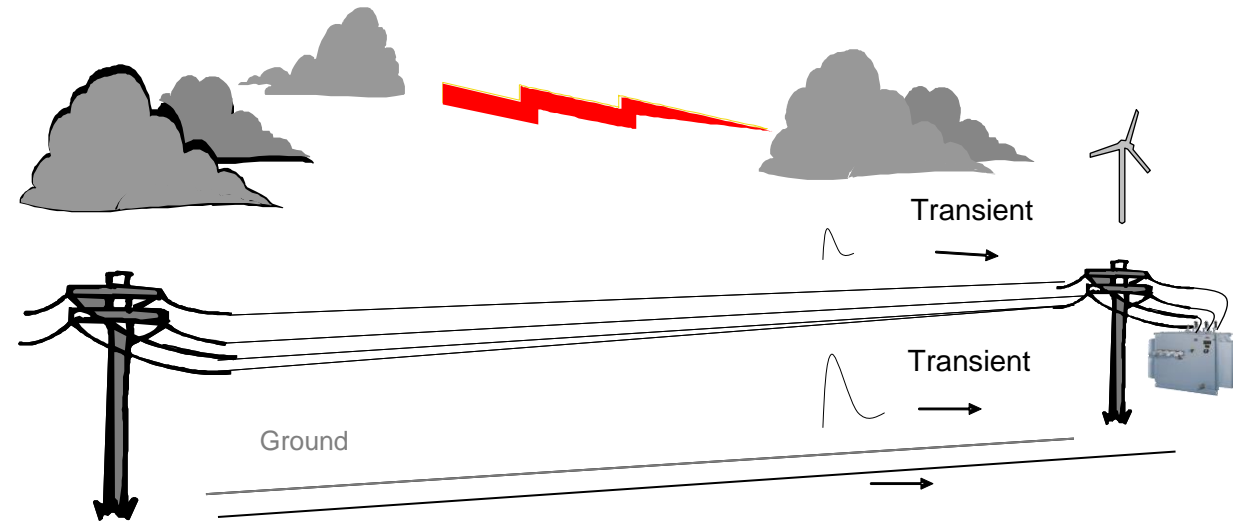
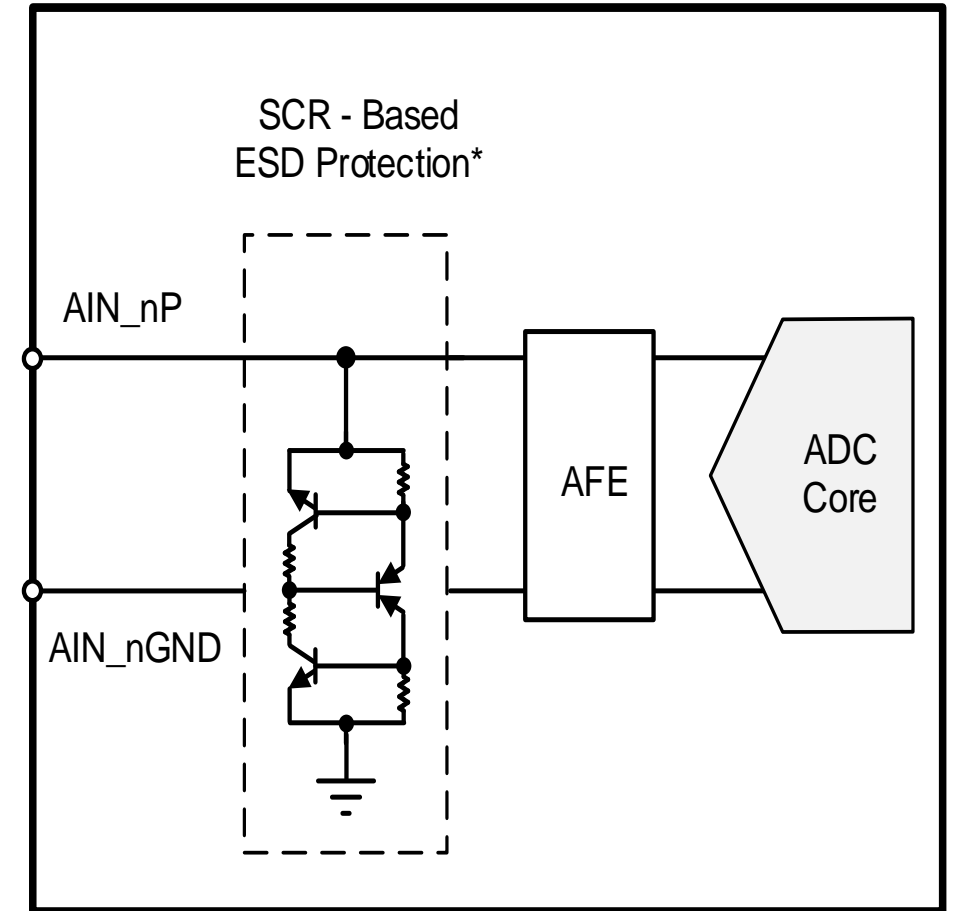# Internal Clamp/Protection on Data Converters

1. Input Steering diodes:
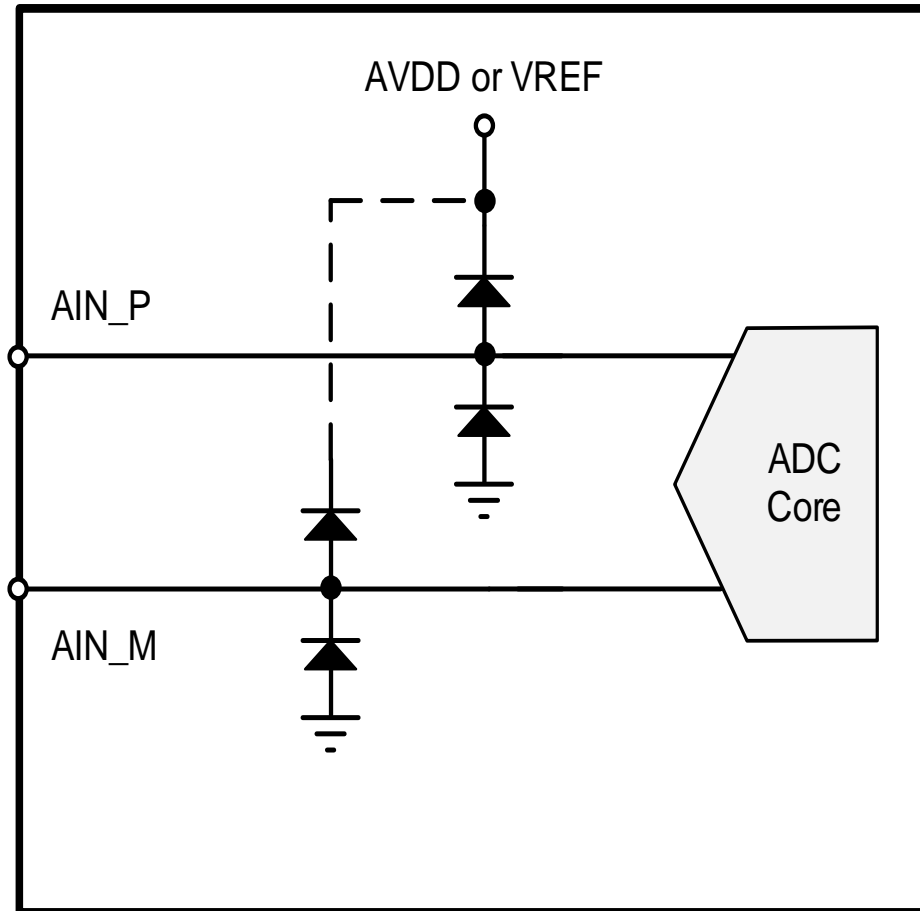
2. Back-to-Back Zener diode:

3. SCR-Based input:

*Bi-directional SCR example

TEXAS INSTRUMENTS
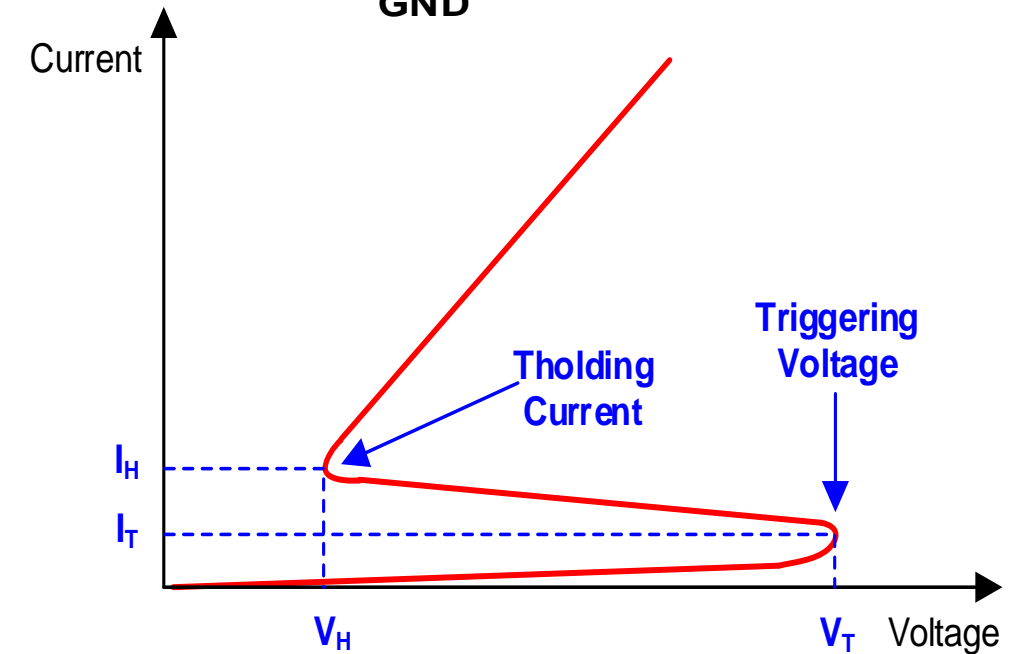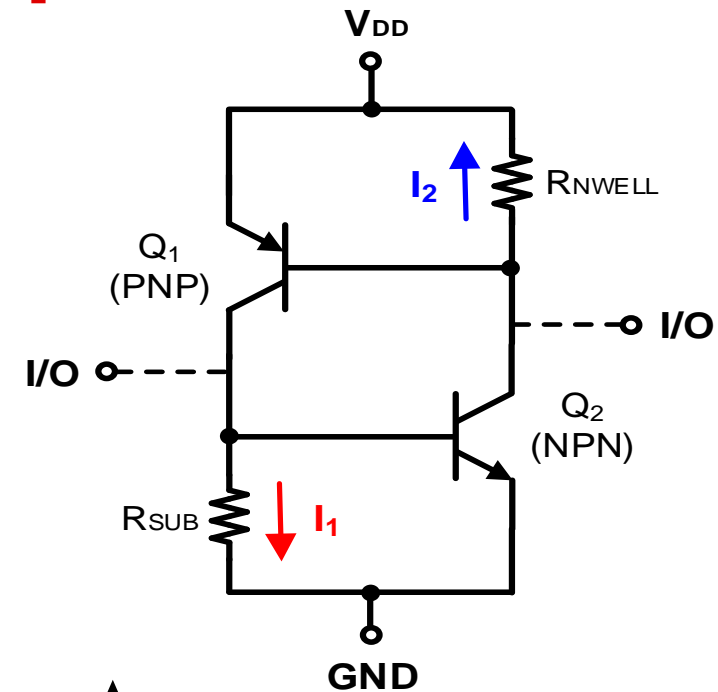
SCR-Based ESD Structure and Latch-up
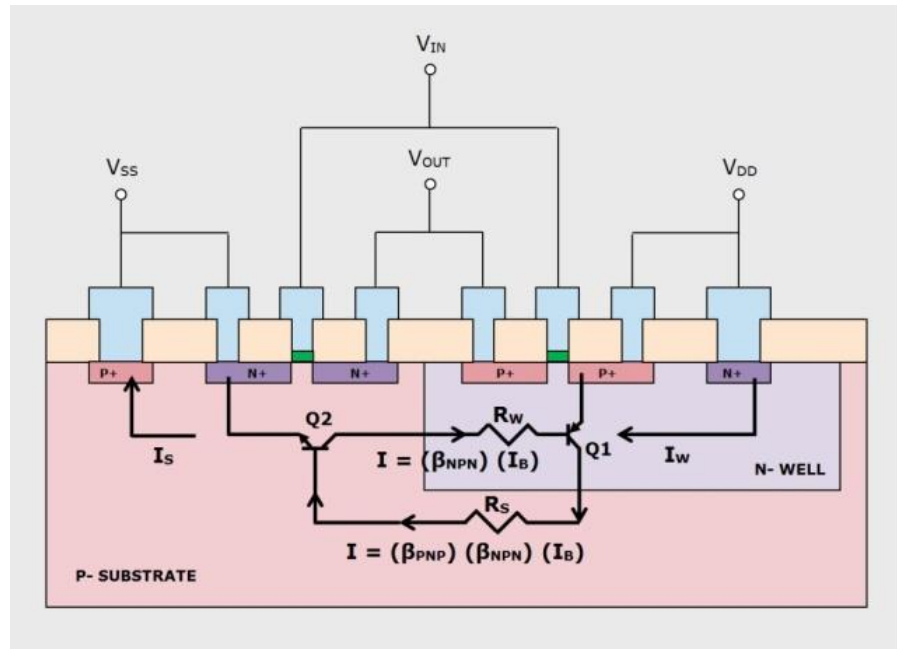
Cross section of typical SCR design structure

Equivalent circuit of SCR

- **SCR** (silicon controlled rectifier) is a parasitic structure. Overshoot and undershoot outside the normal operating voltage and current levels can cause Latch-up and damage the device.

- **Trigger Latch-up**:
  - ✓ Applied voltage > V_H and applied current > I_H

- **Terminate Latch-up state**:
  - ✓ A latch-up remains even after applied signal has been removed and requires a **power supply shut down** to remove the low impedance path.

TEXAS INSTRUMENTS

Why use SCR-Based ESD protection
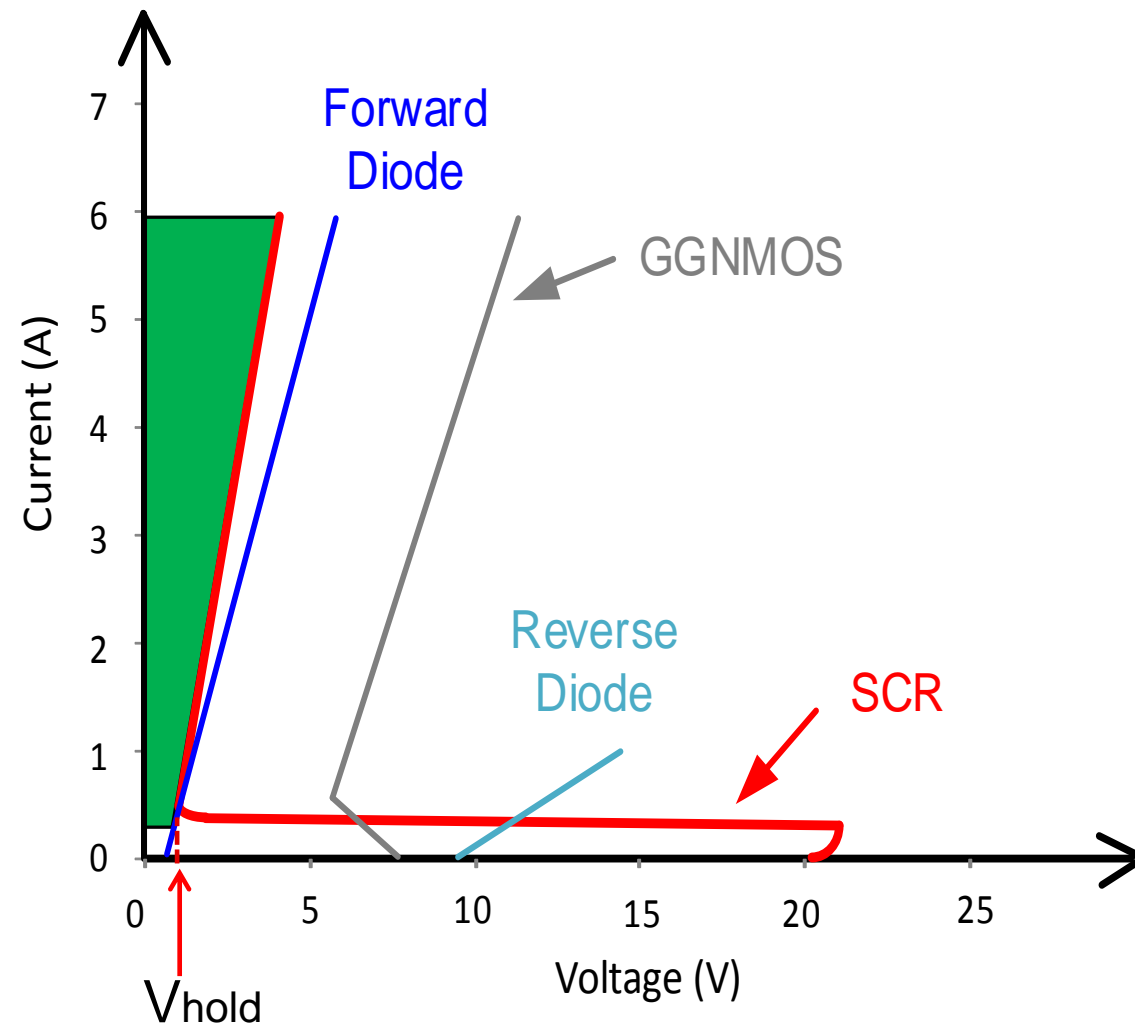
- Input Signal Voltage > Power Supply.
- SCR is used as effective input ESD protection element to sustain a higher ESD level within a smaller layout area because:

  ➢ Lower holding voltage
  ➢ Significantly lower power dissipation
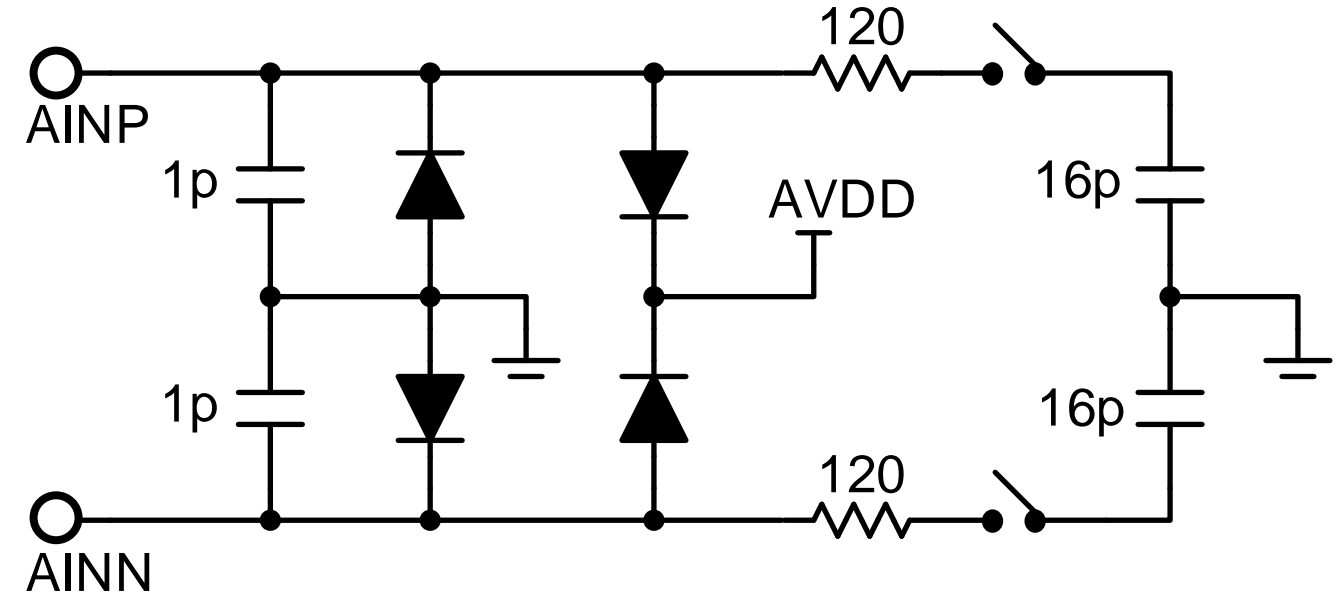 ➢ Robust ESD protection

* Electrostatic Discharge Protection Circuit for High-Speed Mixed-Signal Circuits by Hossein Sarbishaei.

TEXAS INSTRUMENTS

Input Diode to REF/AVDD

ADS8860 Input Stage
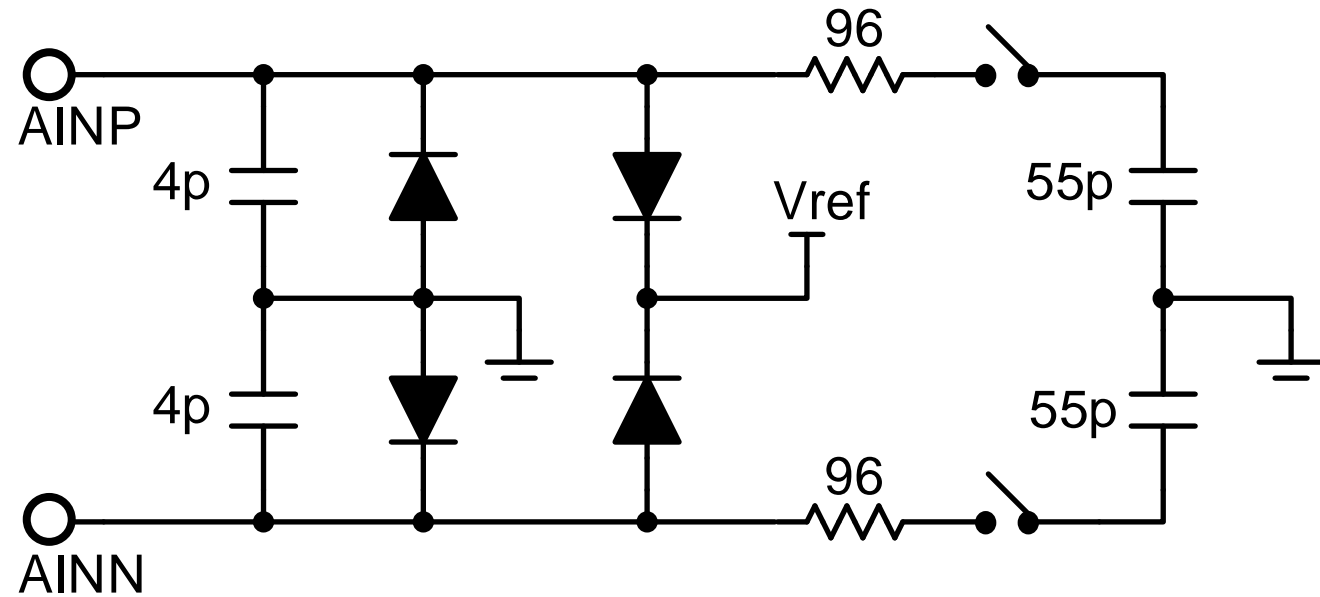
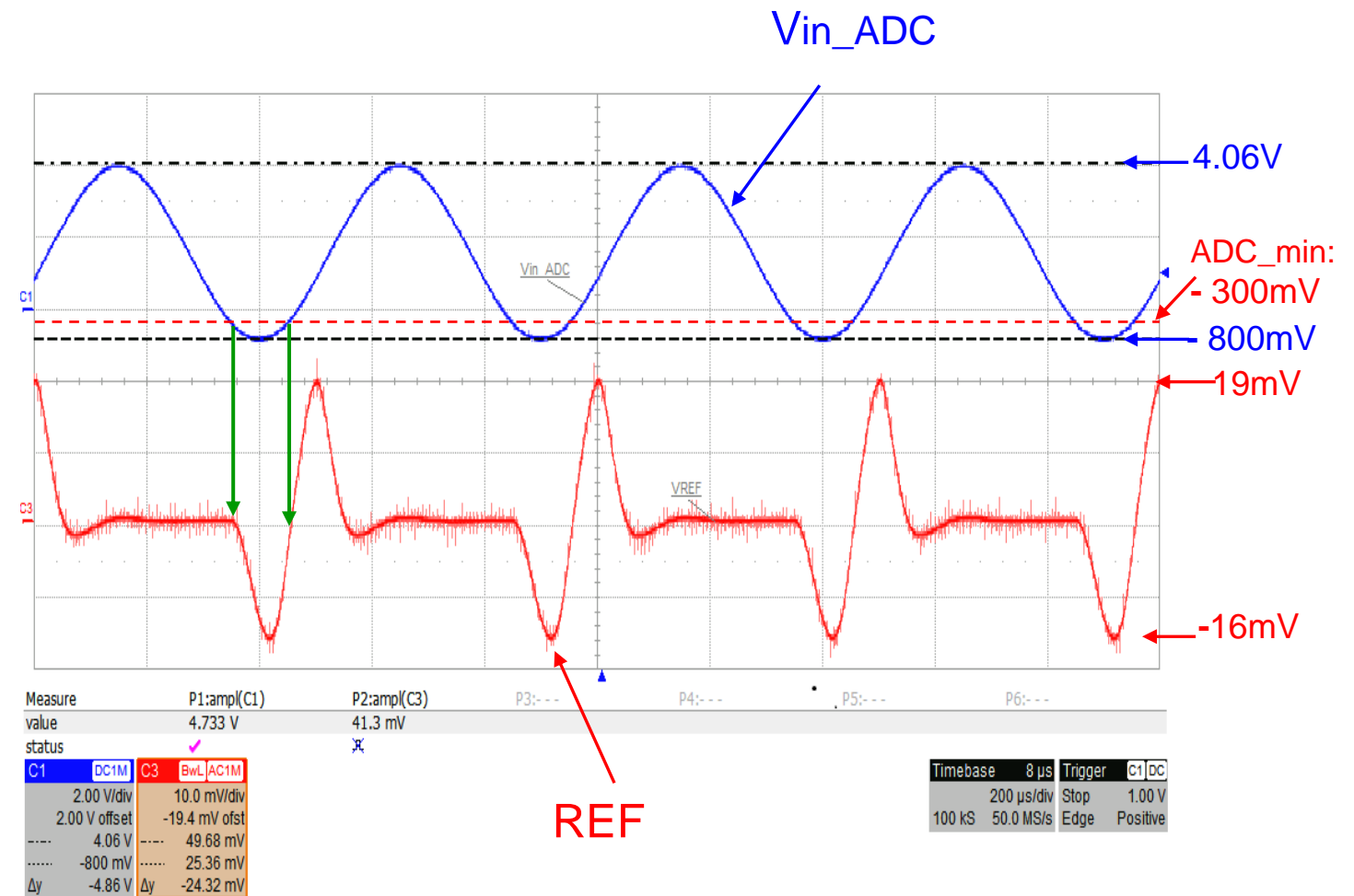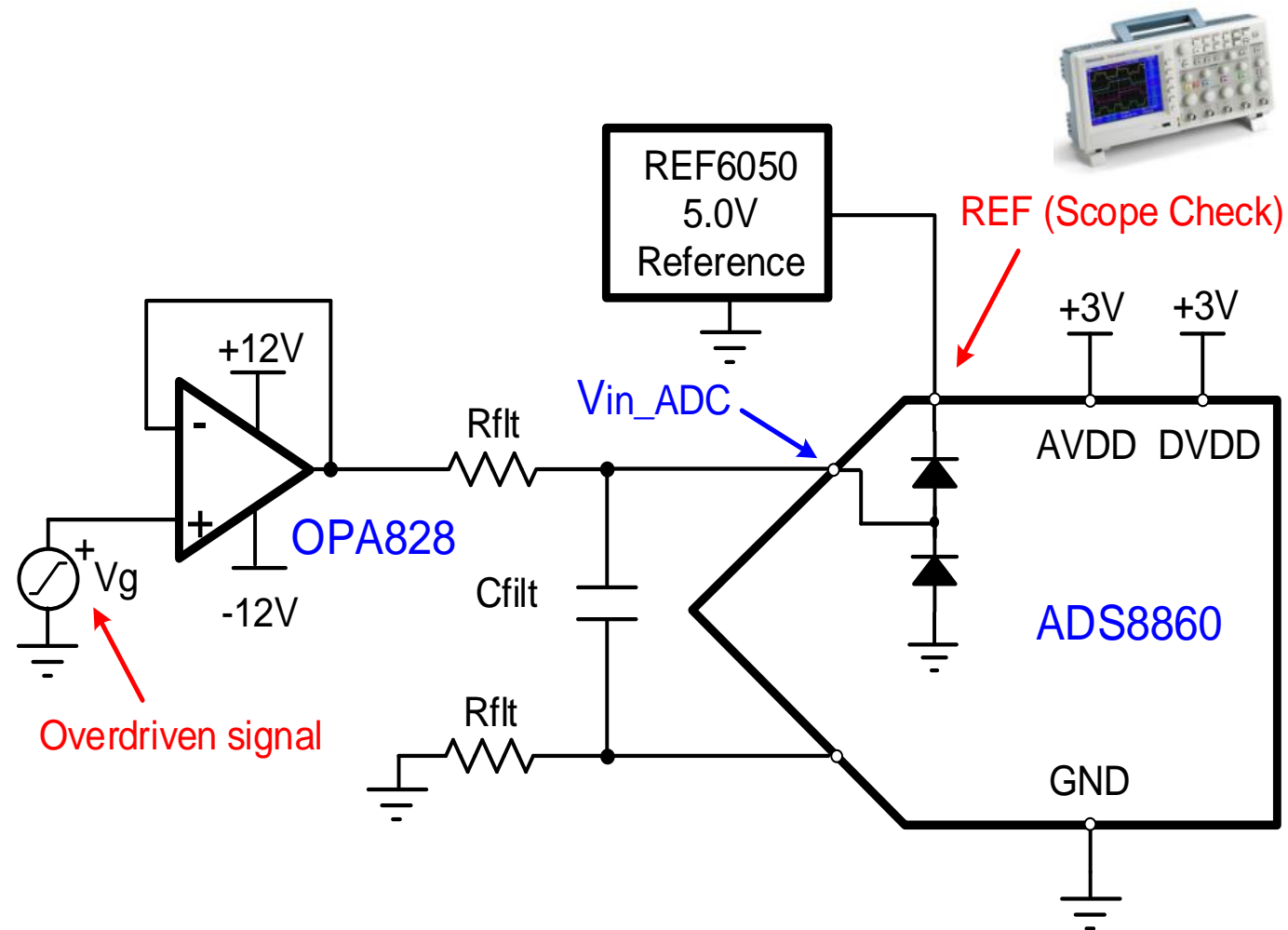**ADS9224R Input Stage**

- Internal diodes are connected to REF: ADS8860,ADS9110,ADS8900B…

- Internal diodes are connected to AVDD: ADS9224R,ADS8168…

- Absolute Maximum Input Range:
  - Analog input voltage is limited to -0.3V to REF+0.3V (or AVDD+0.3V)
  - Input current is generally limited to -10mA to 10mA
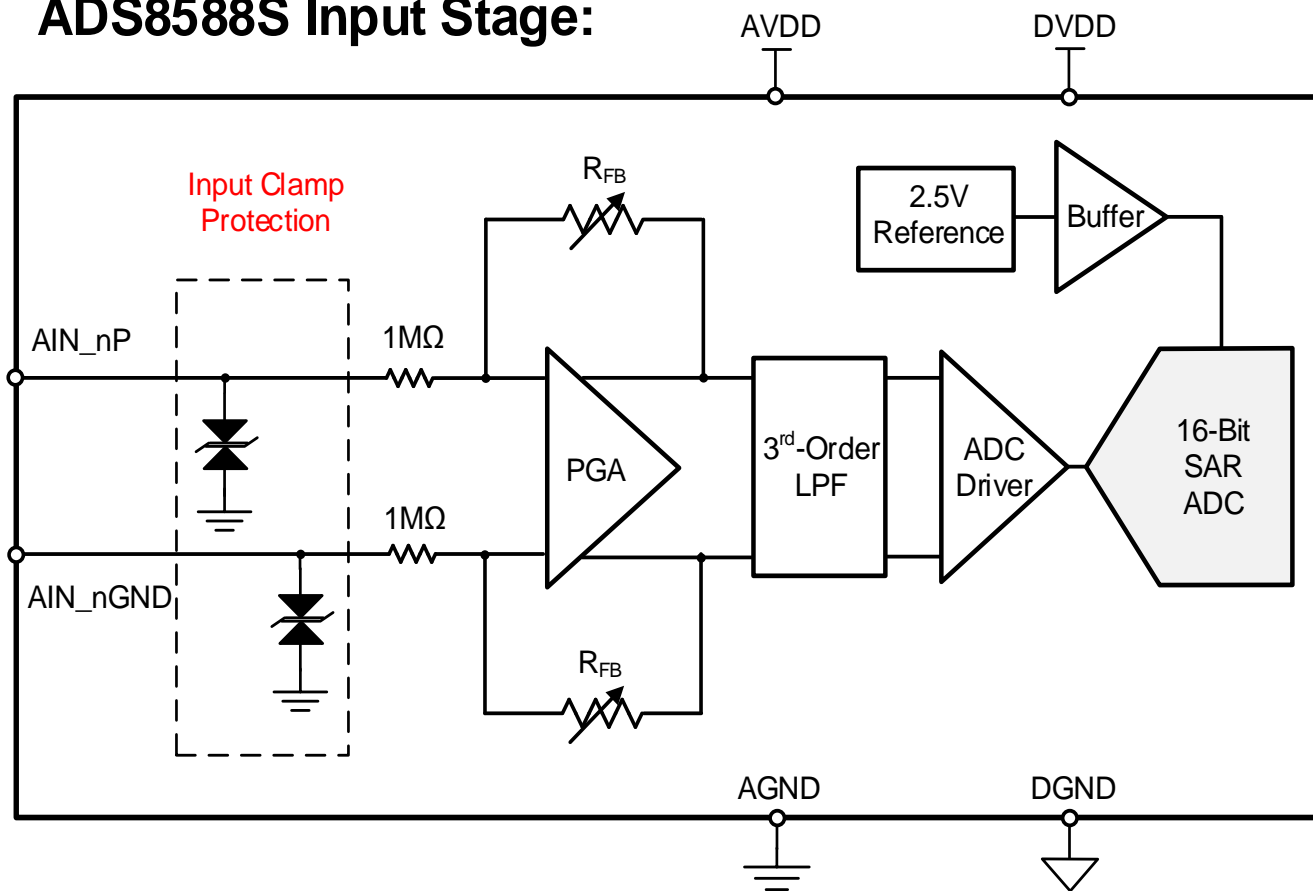
TEXAS INSTRUMENTS

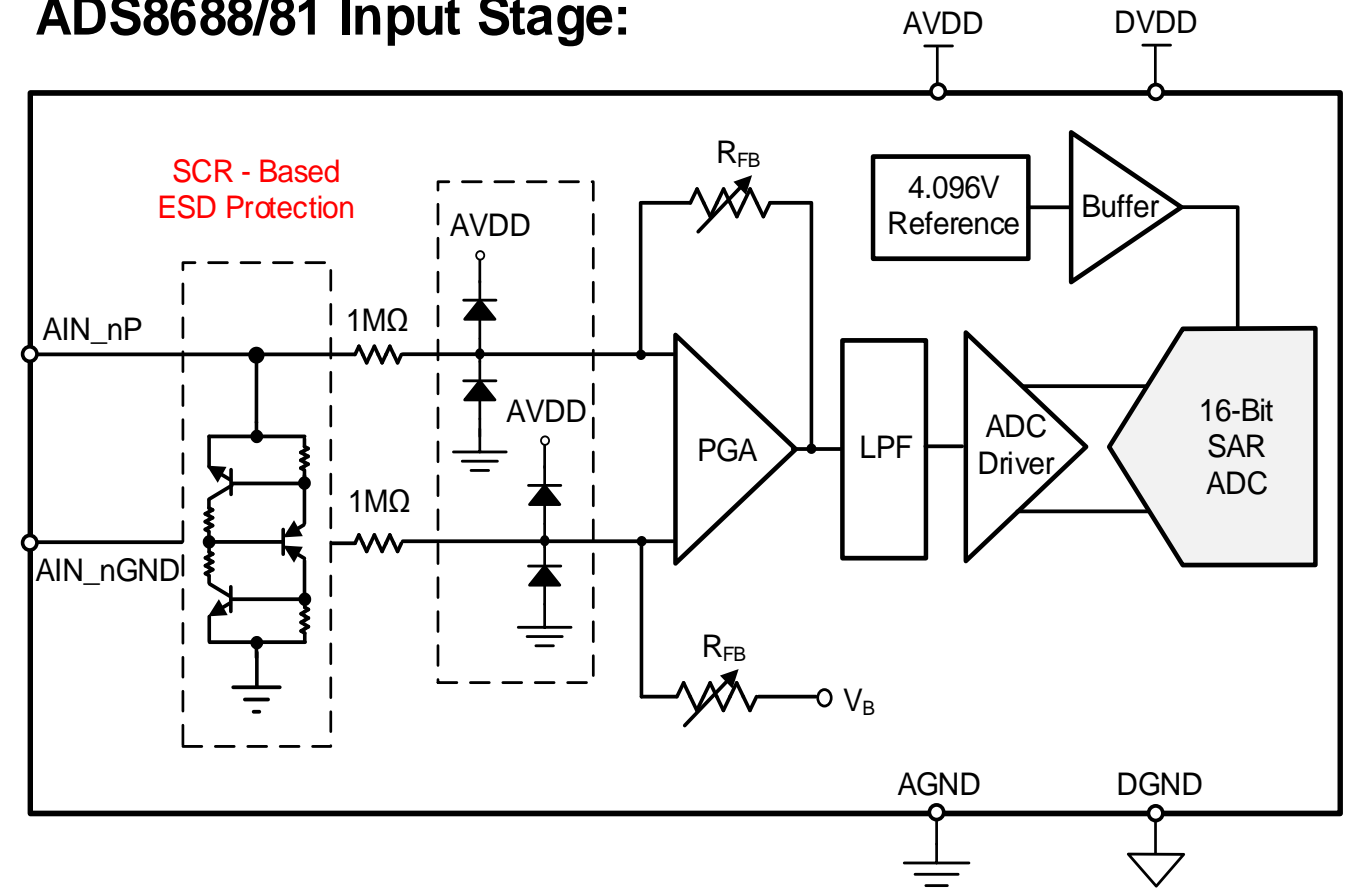# Input ESD Diode turns on and Impacts Voltage Reference

- When input signal is overdriven, a disturbance is found on REF signal (or AVDD) which can degrade the performance if the REF (or AVDD) is shared.
- The higher overdriven signal, the worse disturbance impact.

TEXAS INSTRUMENTS

Input Protection on ADC with AFE

ADS8588S Input Stage: AVDD DVDD — Input Clamp Protection — R_{FB} — 2.5V Reference — Buffer — AIN_nP — 1MΩ — AIN_nGND — 1MΩ — PGA — 3rd-Order LPF — ADC Driver — 16-Bit SAR ADC — R_{FB} — AGND DGND

ADS8688/81 Input Stage: AVDD DVDD — SCR - Based ESD Protection — R_{FB} — 4.096V Reference — Buffer — AIN_nP — 1MΩ — AVDD — AVDD — AIN_nGND — 1MΩ — PGA — LPF — ADC Driver — 16-Bit SAR ADC — R_{FB} — V_B — AGND DGND

- Typically 5V supply voltage and ±12V input range, so ESD diode to supply will not work

- Clamp is implemented with back-to-back Zener diodes or SCR input.

➢ ABS MAX Input voltage limit: ±15V on ADS8588S, and ±20V on ADS8681/8688
➢ ABS MAX Input current Max Limit = ±10mA

9

TEXAS INSTRUMENTS

Thanks for your time! Please try the quiz.

Questions: EOS and ESD on ADC

1. For the circuit shown below, what kind of internal ESD structure is **NOT** practical?

    a.   Input ESD steering diodes

    b.   Back-to-back Zener diodes

    c.   SCR type ESD structure
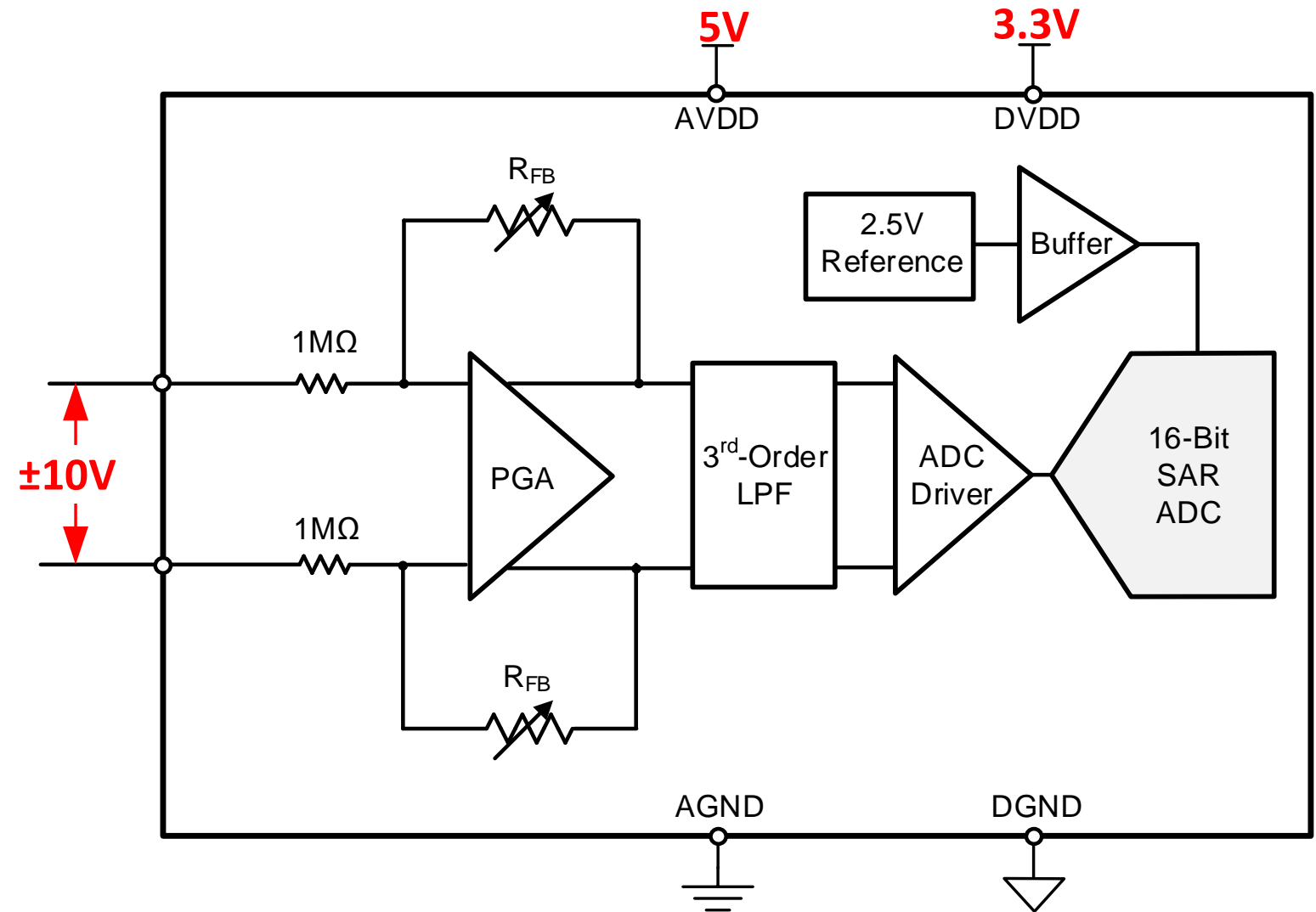
Questions: EOS and ESD on ADC

2. (T/F) The internal ESD protection structures are designed primarily to protect the device during assembly and test (i.e. out of circuit events).

    a. True

    b. False

3. Which type of ESD structure will trigger on and remain on until power is cycled?

    a. Input ESD steering diodes

    b. Back-to-back Zener diodes

    c. SCR type ESD structure

Questions: EOS and ESD on ADC

4. Which of the following does **NOT** apply to ESD?
   a. High voltage (kV)
   b. Fast edges
   c. Long duration event of milliseconds or more.
   d. Both "in-circuit" and "out-of-circuit"

5. For the circuit below, what is the maximum input voltage?
   a. 5.0V
   b. 5.3V
   c. 7V
   d. 12V
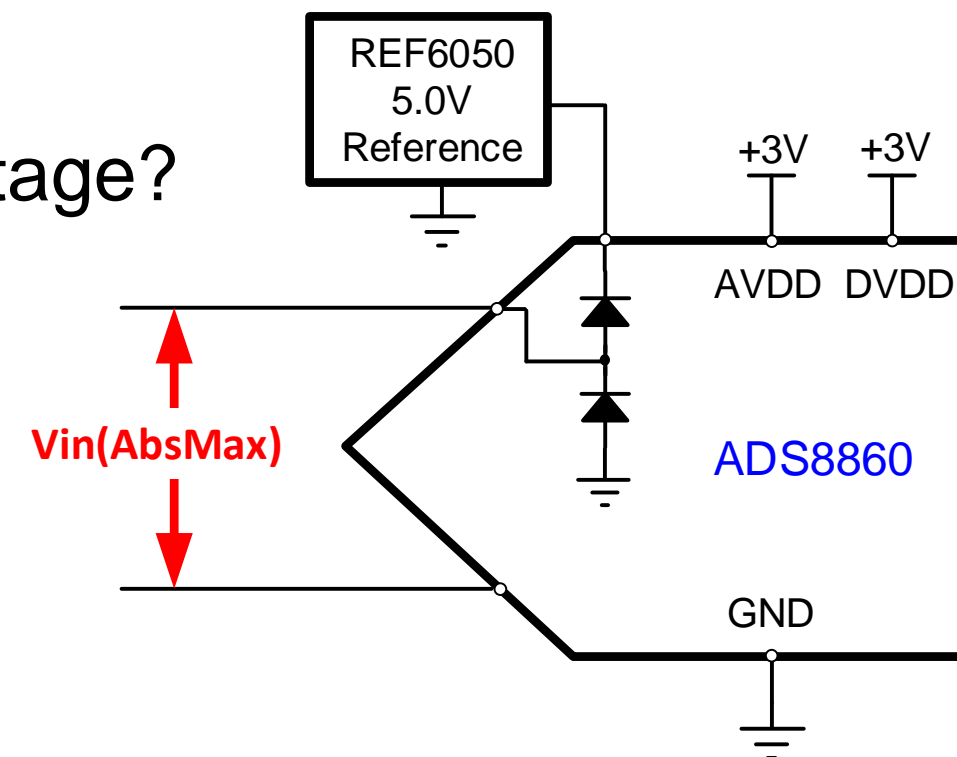
Thanks for your time!

© Copyright 2019 Texas Instruments Incorporated. All rights reserved.