

Presented by: Joseph Serritella

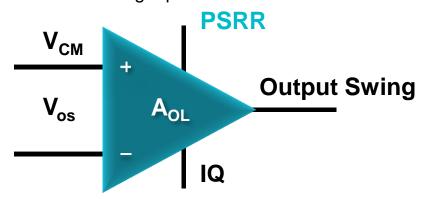
Prepared by: Joseph Serritella, Daryl Hiser, Ray Ochotorena, Mark Irwin



## **OPAMP** verification

#### **OPAMP Electrical Characterization:**

- Characterizing the electrical behavior of an integrated circuit is critical during application troubleshooting
  - Non-conformances can be identified by comprehending device level characteristics in addition to system performance
- OPAMP electrical characterization series will review following topics:
  - Voltage offset (V<sub>OS</sub>)
  - V<sub>CM</sub> / Common mode rejection ratio (CMRR)
  - Power supply rejection ratio (PSRR)
  - Output swing
  - Quiescent current
  - Open loop gain (A<sub>OL</sub>)



# **Prerequisites**

#### **Electrical characterization: PSRR**

- Power supply rejection ratio measurements methods are reviewed
- Following prerequisites are recommended prior to proceeding though the handbook

### **Prerequisites:**

#### **TI-Precision Labs (TIPL) courses:**

**PSRR: TIPL - Op Amps: Power Supply Rejection** 

ti.com/training-power-supply-rejection

#### **Pocket Reference:**

**Training: Analog Engineer's Pocket Reference** 

ti.com/analogrefguide

#### **Application handbook:**

A-B-A: Board Level Troubleshooting

ti.com/board-level-troubleshooting

#### **Simulation tools:**

Simulations are presented within the handbook. It is recommended to install TINA-TI

TINA-TI can be downloaded for free on ti.com: http://www.ti.com/tool/tina-ti



## **OPAMP** test loops

#### **Overview:**

- Analyzing datasheet parameters may appear a challenging task!
- Multiple parameters can be derived easily from offset (V<sub>OS</sub>).
  - PSRR, CMRR, and AOL can be calculated by monitoring shifts

#### False Summing Junction (FSJ):

- Accurate VOS measurements can be obtained through test loops
  - Benefits:

- Disadvantages:
- Simplistic

 Feedback resistor load in parallel with other added loads

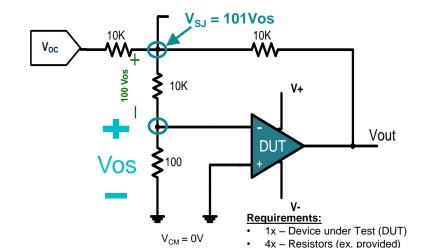
StableSmall

- Loop drive function of DUT V<sub>OS</sub>
- Majority of DC parameters determined with 4 resistors!

#### **Measuring VOS:**

- VOS: differential input voltage required to force output to mid-supply
  - best measured at the summing junction (V<sub>SJ</sub>)
- Output control voltage (VOC): Calibrate the out voltage to zero volts
  - Know as offset correction factor (derived from Kirchhoff's Voltage Law):

$$V_{oc} = -(V_{out} + VOS(302)) + 2VCM$$



#### **Example:**

- V+ = +10V
- V- = -10V
- $V_{OUT} = 0V$
- $V_{OC} = 0V$  (ideal opamp)

#### **Results:**

- V<sub>SJ</sub>= 1.01mV
- 1.01mV = (101)Vos =  $V_{SJ}$

Resistor values can be varied depending on device

$$10\mu V = Vos$$



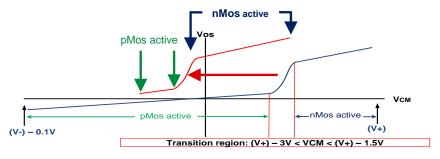
# Power supply rejection ratio – OPA192

#### **Bench setup and measurements:**

- PSRR: Change in V<sub>OS</sub> divided by the change in V<sub>Supply</sub>
  - Consider the transition region for rail to rail amps
  - The nMos active region remains constant as supply delta varies
- Refer to data sheet for PSRR test conditions versus supply range

$$PSRR\left(\frac{V}{V}\right) = \left(\left|\frac{\Delta VOS}{\Delta V_{Supply}}\right|\right)$$

$$PSRR(dB) = -20 \times LOG\left(PSRR\left(\frac{V}{V}\right)\right)$$

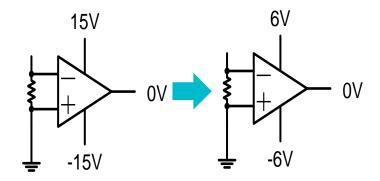


**Figure:** representative  $V_{CM}$  versus  $V_{OS}$  graph. The red line represents the common voltage range of a decreased supply voltage

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR Power- ratio	supply rejection	T <sub>A</sub> = -40°C to +125°C		±0.3	±1.0	μV/V

# Power supply rejection ratio

#### **Bench Setup and Measurements:**



### Offset Voltage (1):

- DUT: OPA192IDGK
- V + = +15V
- V- = -15V
- V<sub>OUT1</sub> = 0V

## Offset Voltage (2):

- DUT: OPA192IDGK
- V + = +6V
- V- = -6V
- V<sub>OUT2</sub> = 0V