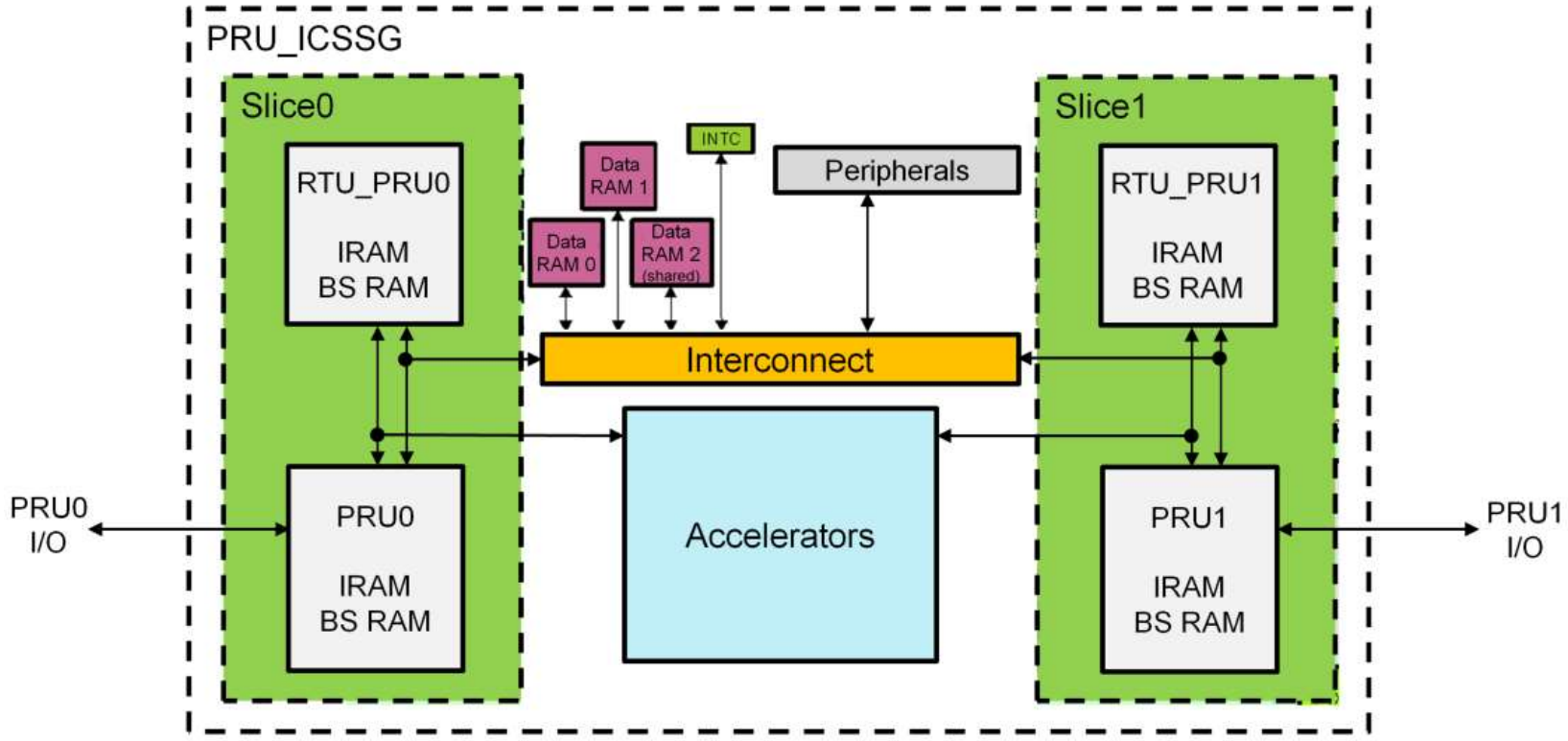
Programmable Real-time Unit for Gigabit Industrial Communication Subsystem (PRU_ICSSG)

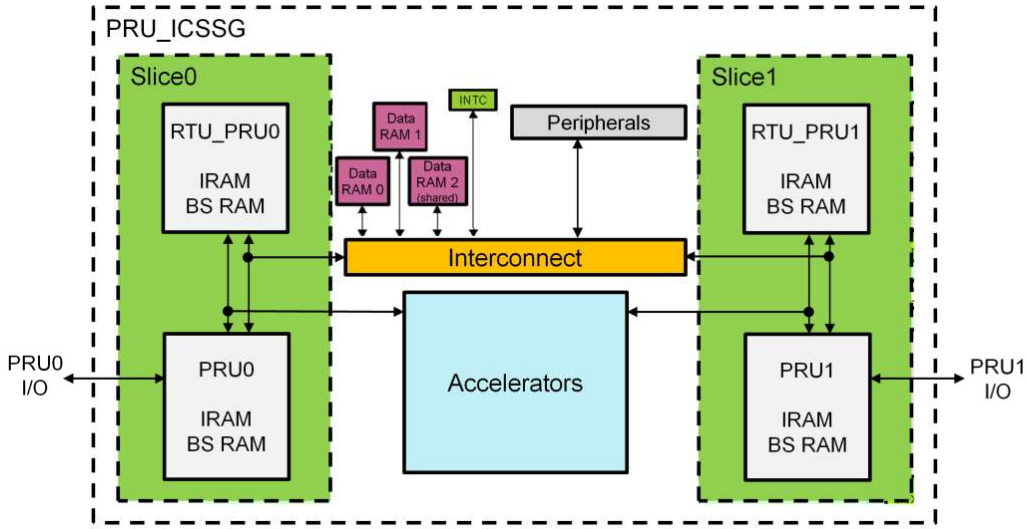
Cores, I/Os, & Peripherals

PRU_ICSSG Block Diagram



Cores & Clock Speed

- Four 32-bit RISC cores
  - 2 Programmable Real-Time Units (PRUs)
  - 2 Auxiliary Programmable Real-Time Units (RTU_PRUs)
    - RTU_PRUs have no dedicated I/Os
    - Smaller IRAM than PRU cores
    - Access to all Shared ICSS resources & SoC resources, similar to PRU cores



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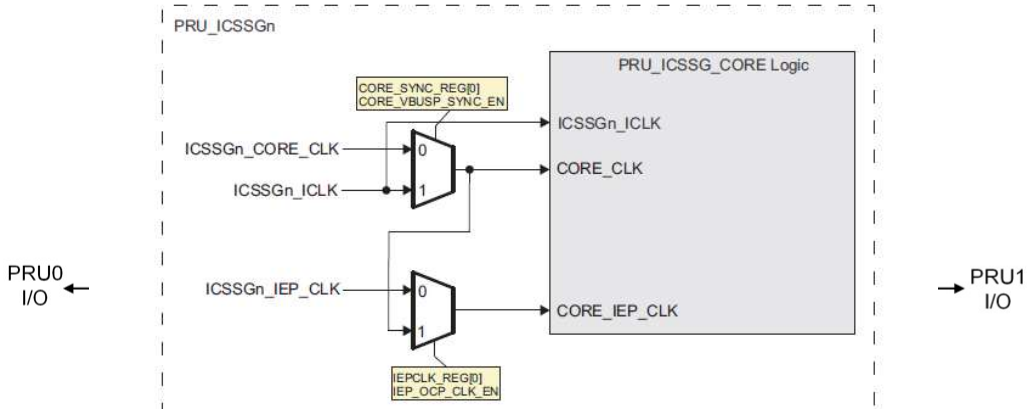
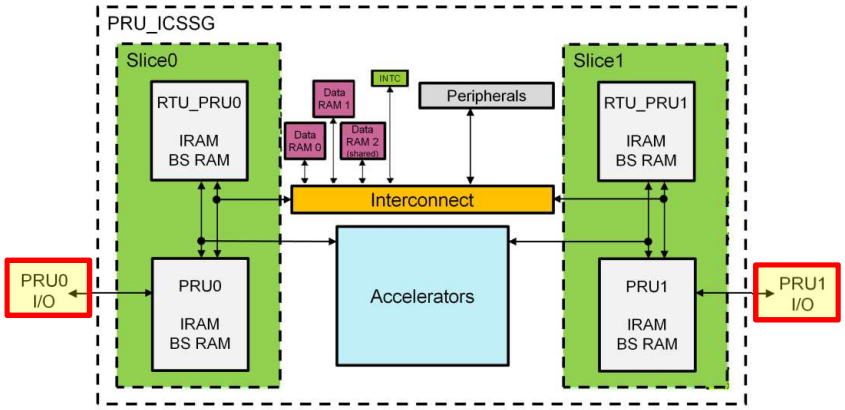
- All 4 cores run at max of 250MHz clock speed
  - CORE_CLK options:
    200MHz (default) / 225MHz / 250MHz
  - CORE_VBUSP_SYNC_EN bitfield enables:
    - High speed (250MHz)
    - New “sync mode” with lowest latency

Figure 6-113. PRU_ICSSG CORE Clock Diagram



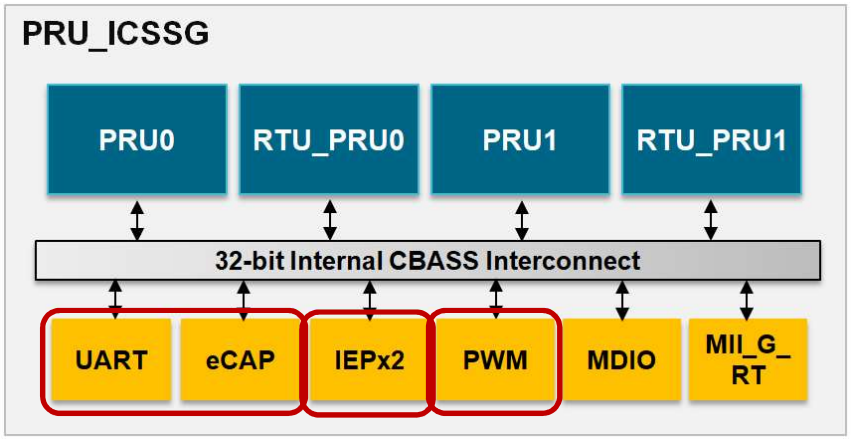
GPI/O Enhancements

- Only PRU cores have I/Os pinned out
  - Up to 30 inputs and 32 outputs per PRU core
- Direct Output
  - Optional bidirectional support on GPOs
    - Enabled in device level CTRLMMR
    - I/O direction controlled by IEP's DIGIO_DATA_OUT_EN registers
- Shift In/Out GPI/O mode
  - Additional configuration options to provide greater flexibility
- Sigma Delta
  - Counter size increased (24 →28-bit)
  - Added Fast Detect logic to monitor min/max ones in a 32-bit sliding window



Feature	PRU-ICSSG
General Purpose Outputs	
Direct Output	Upgraded
Shift out	Upgraded
General Purpose Inputs	
Direct Input	Same
16-bit Parallel Capture	Same
28-bit Shift	Upgraded
3 Ch. Peripheral Interface (EnDAT)	Same
9 Ch. Sigma Delta	Upgraded (not 100% backwards compatible with PRU-ICSS firmware)

PRU_ICSSG Peripherals



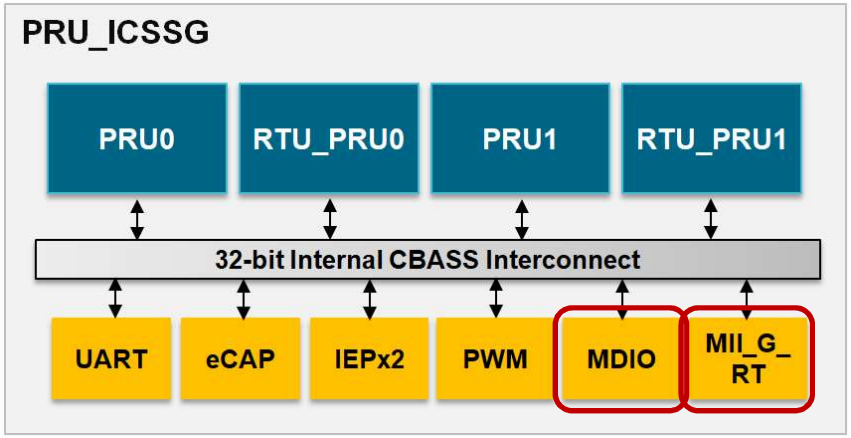
- UART and eCAP
  - Identical to previous PRU-ICSS devices
- Industrial Ethernet Peripheral (IEP)
  - Additional IEP instance
  - New IEP timer modes:

Mode	Description
Slave mode	IEP1 master counter can come from IEP0 counter

Feature	PRU-ICSSG
Peripherals	
UART	Same
eCAP	Same
IEP	Upgraded
PWM	New
MDIO	Upgraded
MII_G_RT	Upgraded

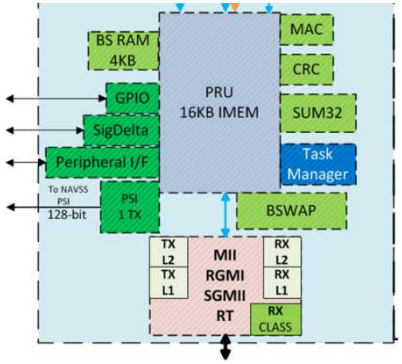
- PWM
  - Up to 4 sets of 3 phased motor control with 12 p programmable PWM outputs
  - Flexible PWM trip generation with minimal later
  - Diagnostic capability to read back trip source and timestamp for multiple events

PRU_ICSSG Peripherals



- MDIO
  - Adds Clause 22 and Clause 45 Support
  - Additional configuration options

- MII_G_RT
  - 1Gb Ethernet speeds
  - RGMII/SGMII support with real-time trigger
  - MII RX_L2 with hardware filter
  - MII TX_L2 pre-emption FIFO
  - RX classifier with ingress filter and per port policing per stream/filter



For more information

- PRU Training Series: https://training.ti.com/pru-training-series
- PRU-ICSS Feature Comparison: http://www.ti.com/lit/sprac90
- PRU_ICSSG Getting Starting Guide on Linux: http://www.ti.com/lit/sprace9
- PRU Read Latencies: http://www.ti.com/lit/sprace8
- PRU-ICSS / PRU_ICSSG Migration Guide http://www.ti.com/lit/spracj
- For questions about this training, refer to the E2E Community Forums at http://e2e.ti.com