High VOLT Interactive

Where power supply design meets collaboration

隔離式閘極驅動器概論

張巍, 系統工程師
德州儀器

What will you get out of this session?

- **PURPOSES:**
  - What are the gate driver application
  - What are the differences: low-side, high-side and low-side, and isolated gate driver?
  - How to maximize the gate driver performance – from basic to details
    - Parasitics in the gate driver
    - Hard/soft switching
    - High dV/dt and di/dt
    - Isolated gate driver

- Part numbers mentioned:
  Low side: UCC27511A, UCC27524A
  H-/L- Side: UCC27282, LMG1210, UCC27710
  Isolated: UCC21540, UCC23513, UCC21710,

- Relevant End Equipment:
  Telecom, servers, solar inverters, motor drive, EV/HEV, UPS

Where are gate driver ICs used?

Gate driver applications

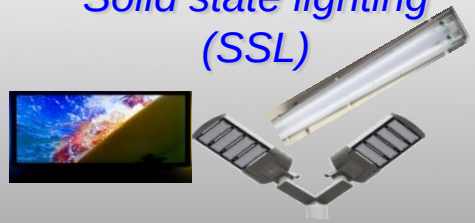
Li-ion battery portables

Adaptors and chargers

Server/telecom/UPS

Electric vehicles class D audio

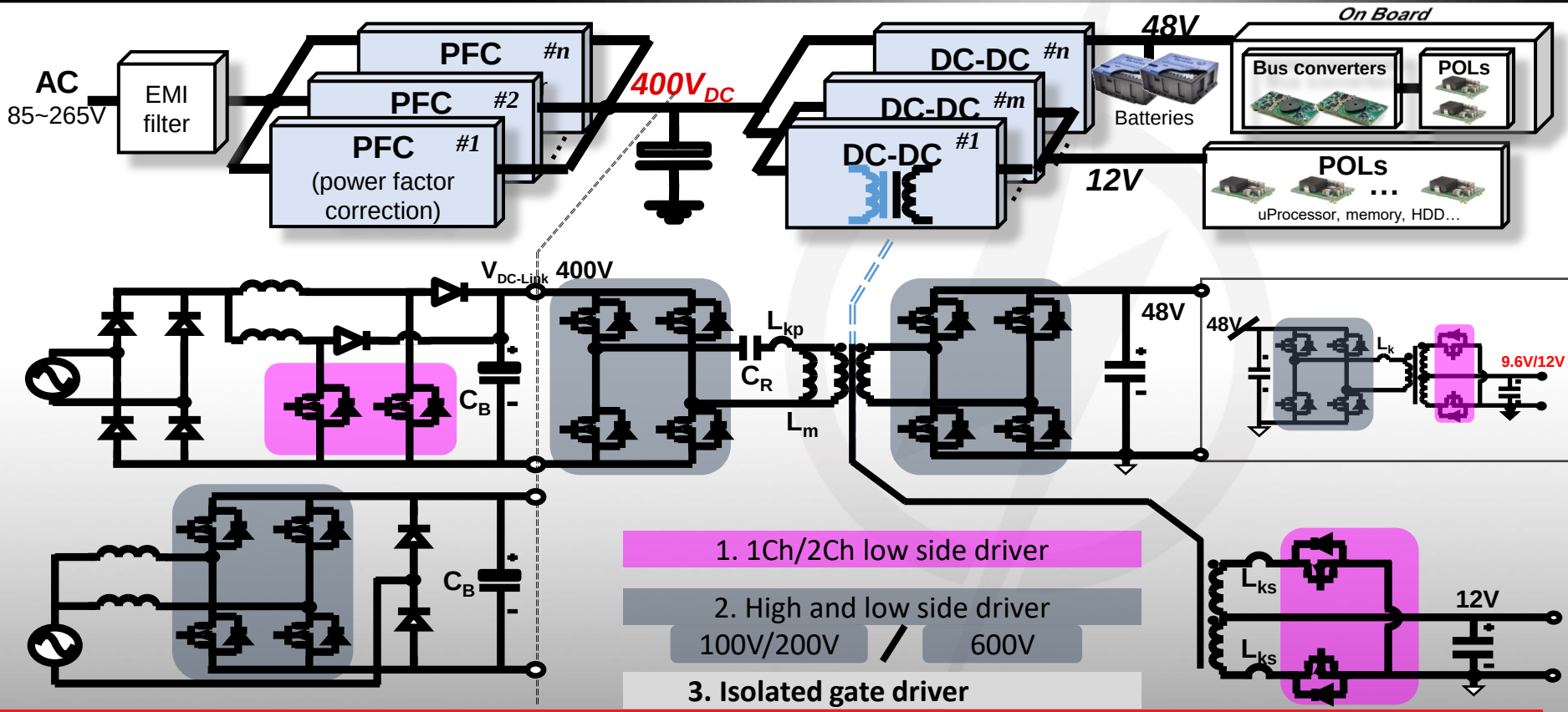
Solid state lighting (SSL)



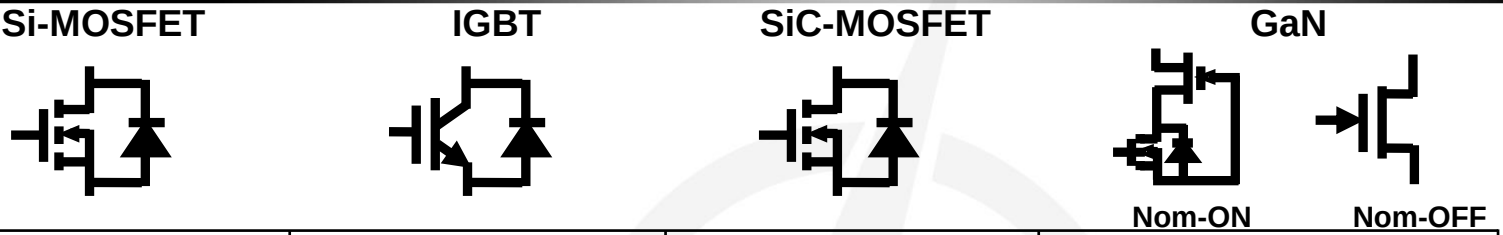
Renewables

Motor drive (VFD)

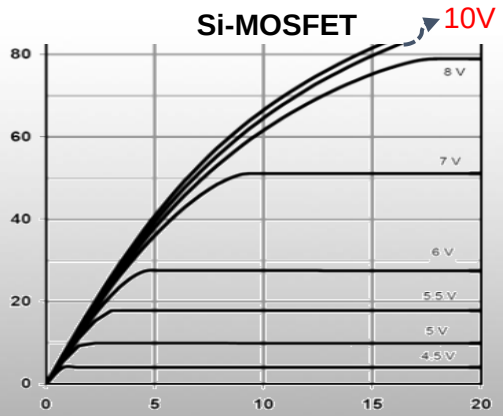
Gate Driver in Server / Telecom

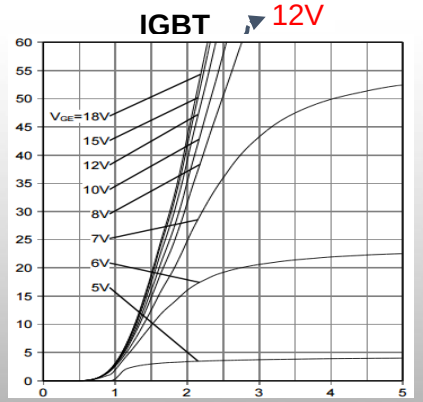


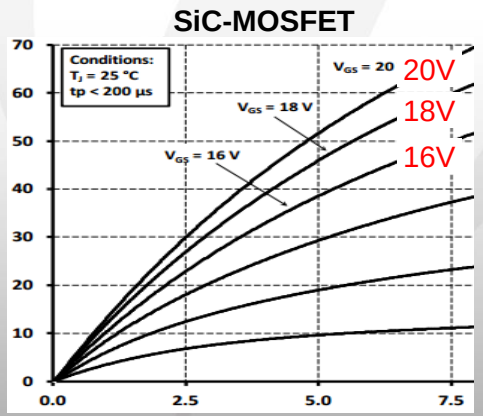
What are the Power Devices?

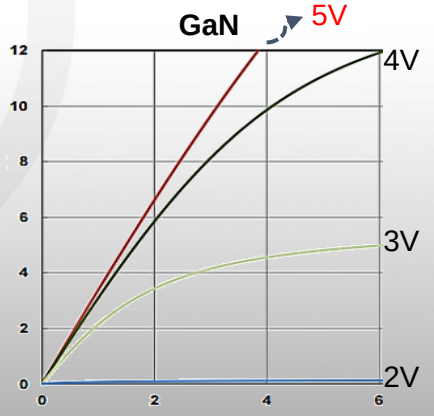


	Si-MOSFET	IGBT	SiC-MOSFET	GaN	
Voltage ratings	20~650V	≥650V	≥650V	≤650V	
Optimal V_{GS} Max.limit	0~15V (±20V)	-10~15V (±20V)	-5~20V (-10~25V)	-5~10V (±18V)	-4~6V (-10~7V)





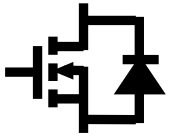




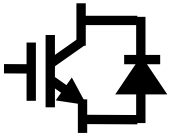
- I-V curves are from datasheets of Infineon, Fairchild, ST, Wolfspeed, EPC

What are the Power Devices?

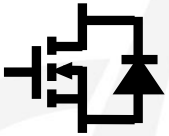
Si-MOSFET



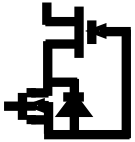
IGBT



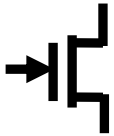
SiC-MOSFET



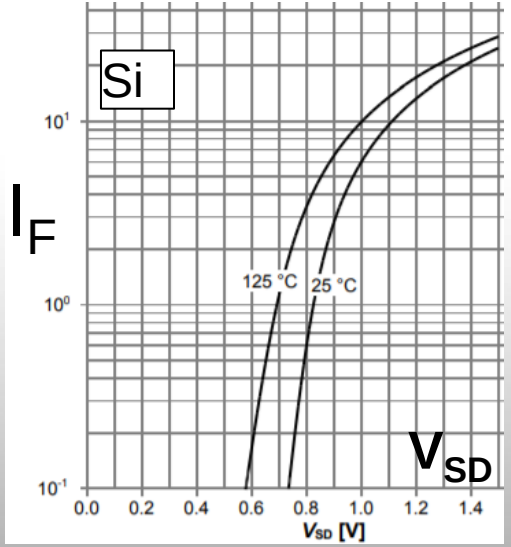
GaN

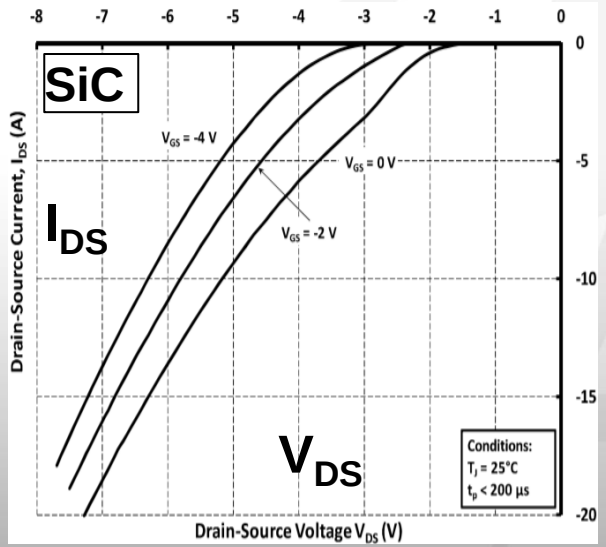


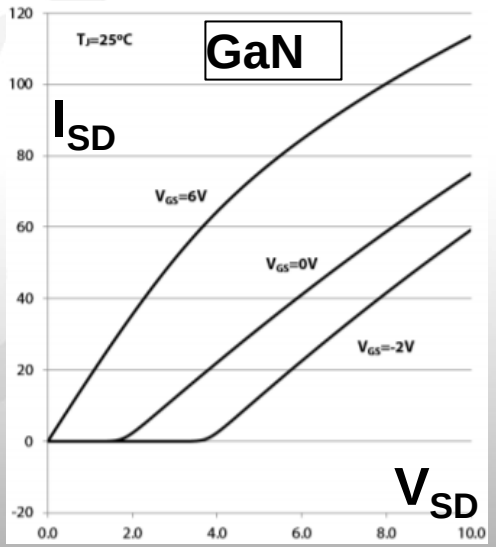
Nom-ON



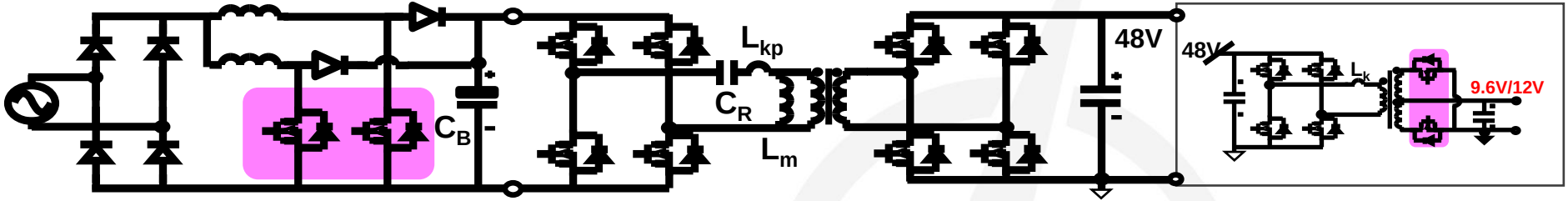
Nom-OFF







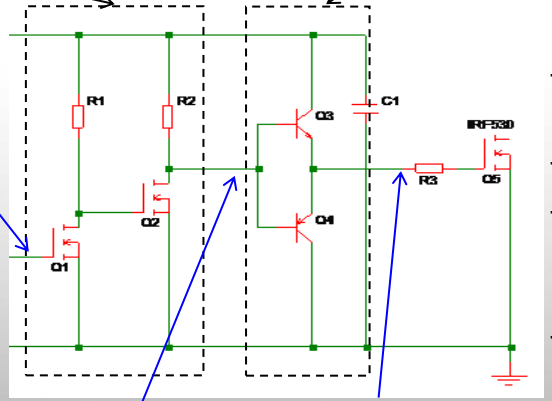
Discrete vs Driver IC?



Level shift circuit + **NPN/PNP totem pole**

3.3V/5V PWM signal from microcontroller or DSP

Micro/DSP



Level shifted 12V signal

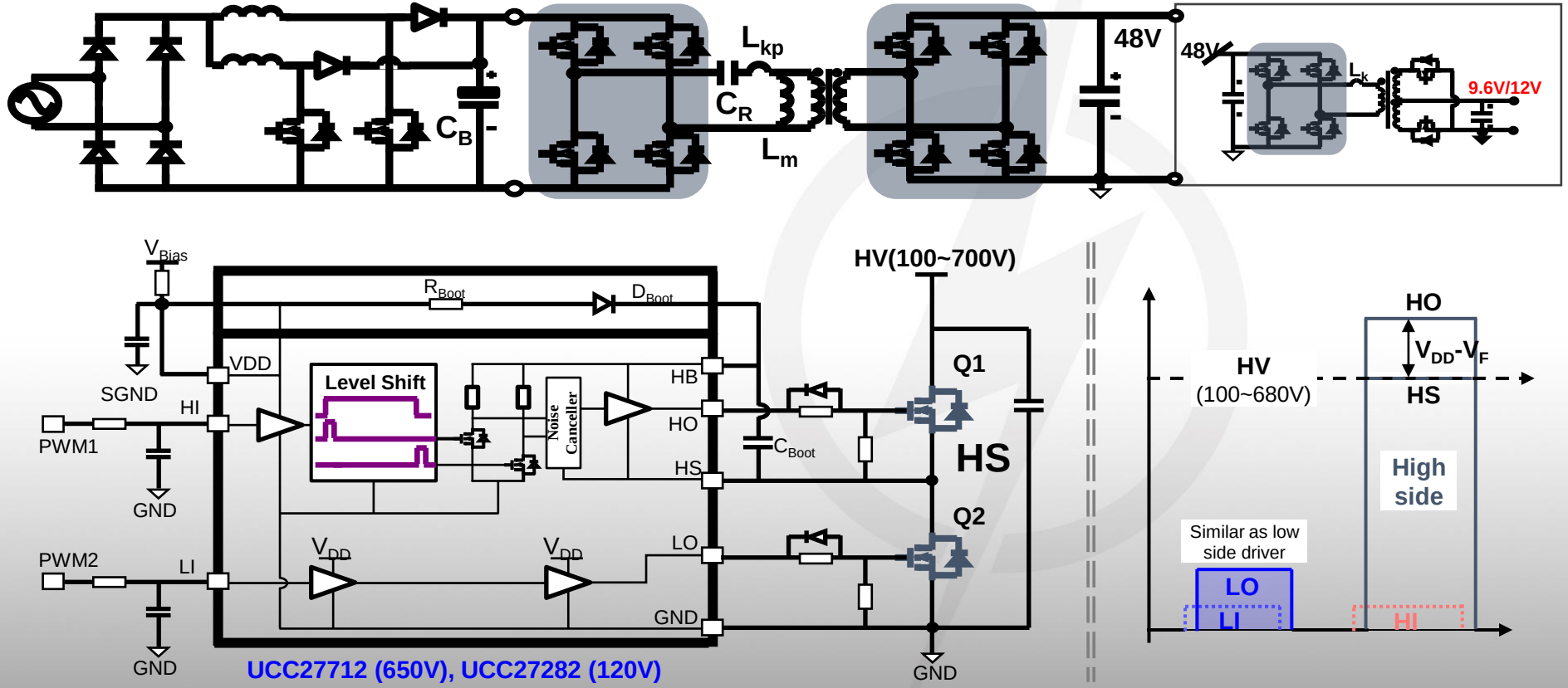
12V with high peak source/sink current

Now

- **Reduces BOM component count**
- **Reduces PCB space**
- **Protects from spurious signals during power up (such as UVLO)**
- **Improves reliability**

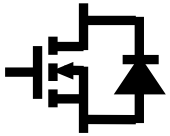
- **UCC27511A - Single**
- **UCC27524A - Dual**
- **UCC27531 – SiC or IGBT**

How does a Half-Bridge Driver Operate?

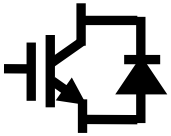


What are the Power Devices?

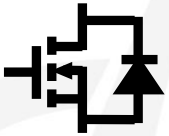
Si-MOSFET



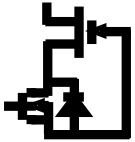
IGBT



SiC-MOSFET



GaN



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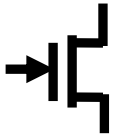

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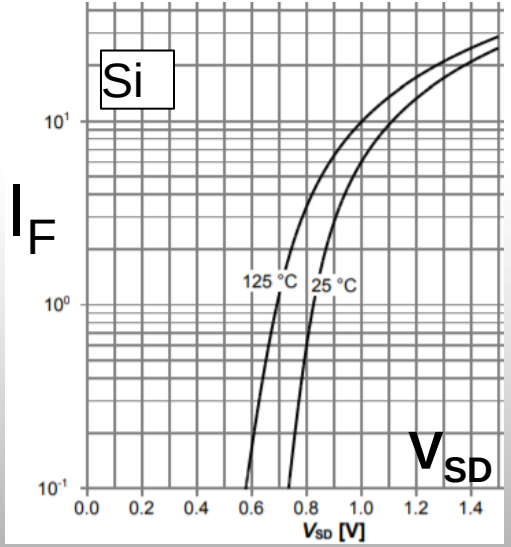
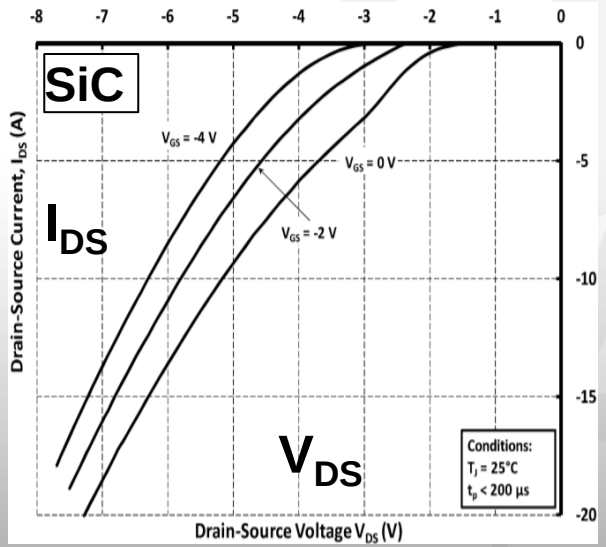
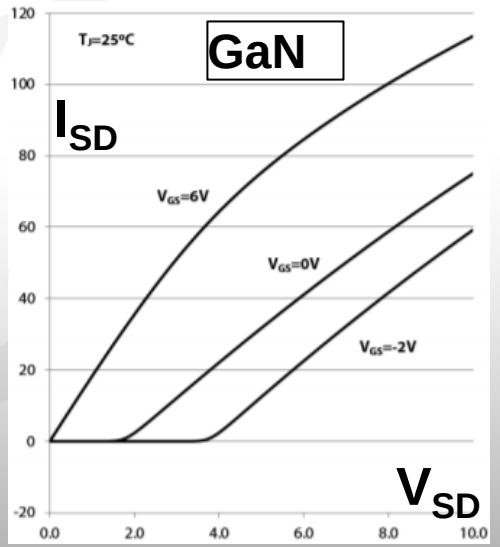
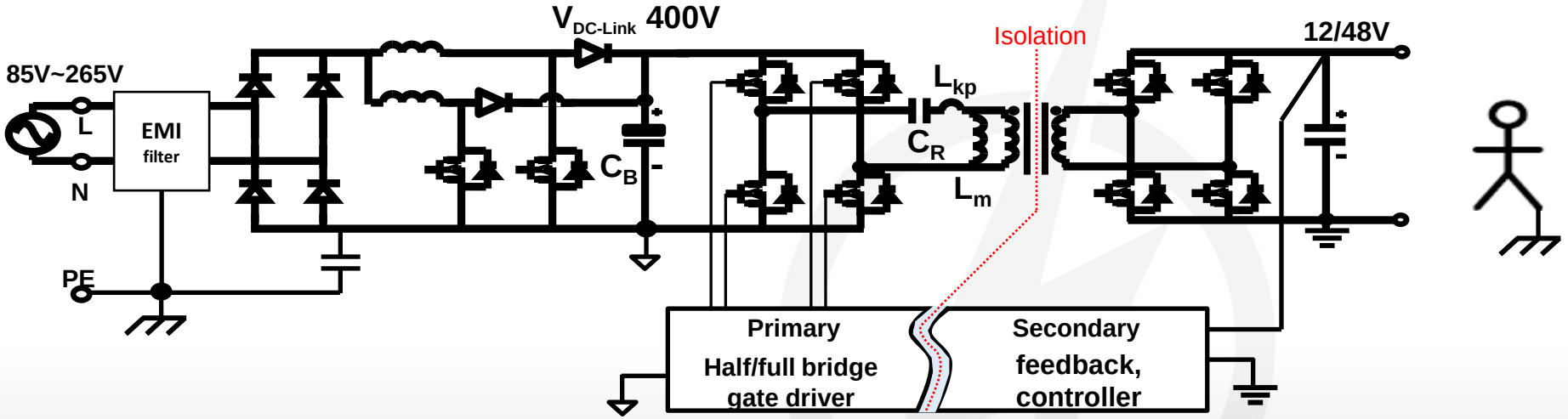






Why ISOLATION?



IEC 60950-1 ed. 2.0, Table 5B

Working voltage V, peak or DC	Test voltage for electric strength based on peak working voltage		
	Functional Isolation (V_{RMS})	Basic Isolation (V_{RMS})	Reinforced Isolation (V_{RMS})
≤210	1000	1000	1500
≤420	1500	1500	3000

What is Functional, Basic, Reinforced Isolation?

Isolation	Definition	Featured Drivers
Functional	Isolation that is necessary only for the **correct functioning** of the equipment	**UCC21220A, UCC21222**
Basic	Isolation to provide **basic protection against electric shock**	**UCC21220A, UCC21222**
Reinforced	**Single Isolation system** that provides a degree of protection against electric shock equivalent to DOUBLE isolation under the conditions specified in this standard	**UCC21540, UCC21520**

Isolation Req. Exp. per IEC-60950

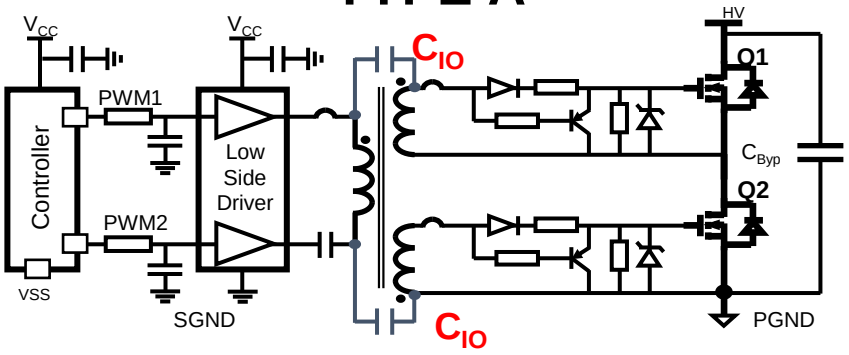
According to Figure 2H of IEC60950-1

Isolation Req. Exp. per IEC-60950

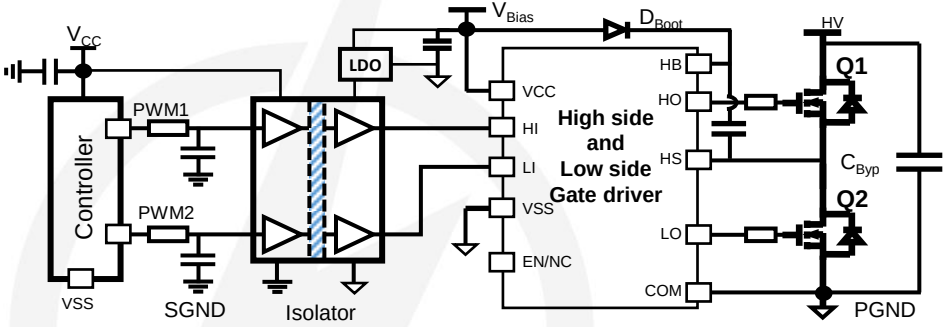
According to Figure 2H of IEC60950-1

Transformer vs. Driver IC

TYPE A



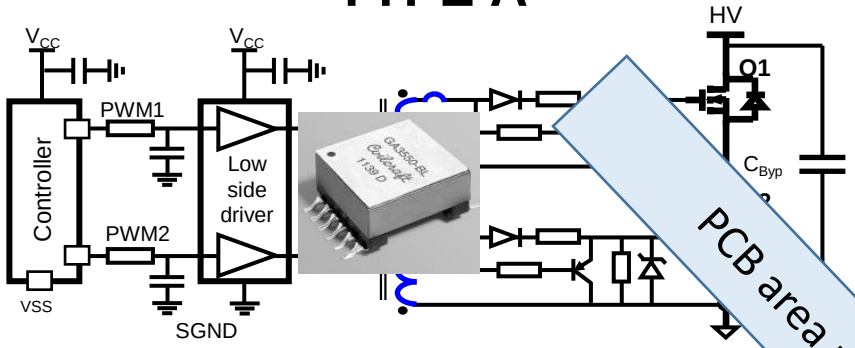
TYPE B



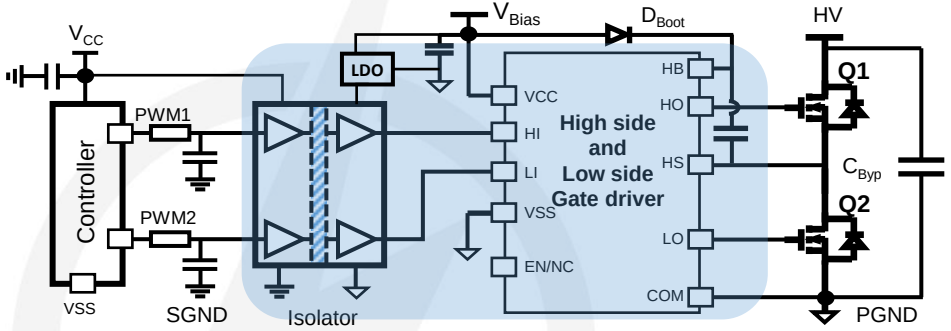
	Type A	Type B
T_{Prop}	≈20ns	≈100ns
Bias power	NO	Yes
C_{IO}	≥10pF	<1pF
Parasitics	Large (L_{LK})	Very small
Overshoot	Large	Small
Size	Bulky	Small

Transformer vs. driver IC?

TYPE A



TYPE B



PCB area reduction – 76%

		W (mm)	L (mm)	H (mm)	Area (mm²)	
Type A	UCC27324	5	6.2	1.75	31	5
	GA3550-BL	17.4	24.13	10	420	4200
				SUM	451	4254

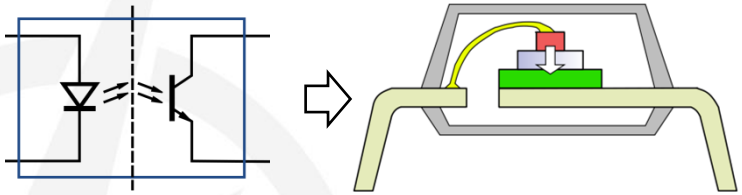
Type B	ISO7520C	10.5	10.6	2.65	111.3	295
	UCC27714	8.75	6.2	1.75	54.25	95
	MURS360	8.1	6.1	2.4	49.41	119
				SUM	215	509

TYPE C: ISO driver

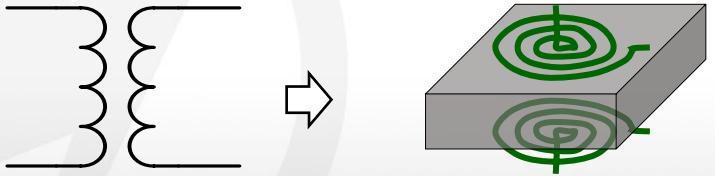
- CMTI>100V/ns
- 5kVrms reinforced isolation
- T_{Prop}: 19ns typ.
- Match./T_{PWD} < 5ns
- 110mm²

Popular ISOLATION methods

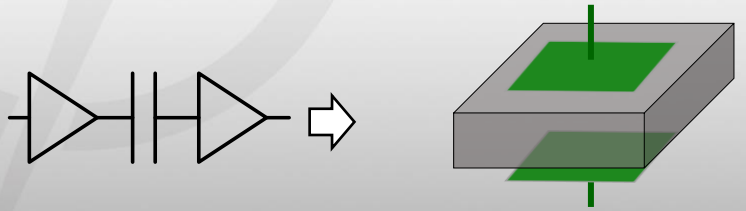
- A) Optocoupler
  - Signal transfer between two isolated circuits using light – LED + phototransistor, ~1970s



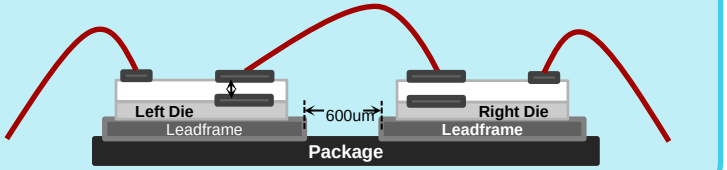
- B) Transformer
  - Integrated micro-transformer and electronic circuitry, ~2001



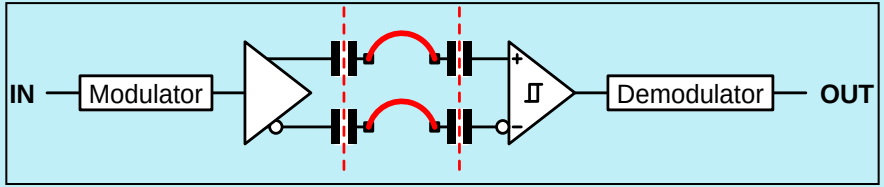
- C) Capacitor
  - Signal transmission through capacitive isolation with on-off-keying (OOK) modulation, ~2004



TI Reinforced Isolation Technology



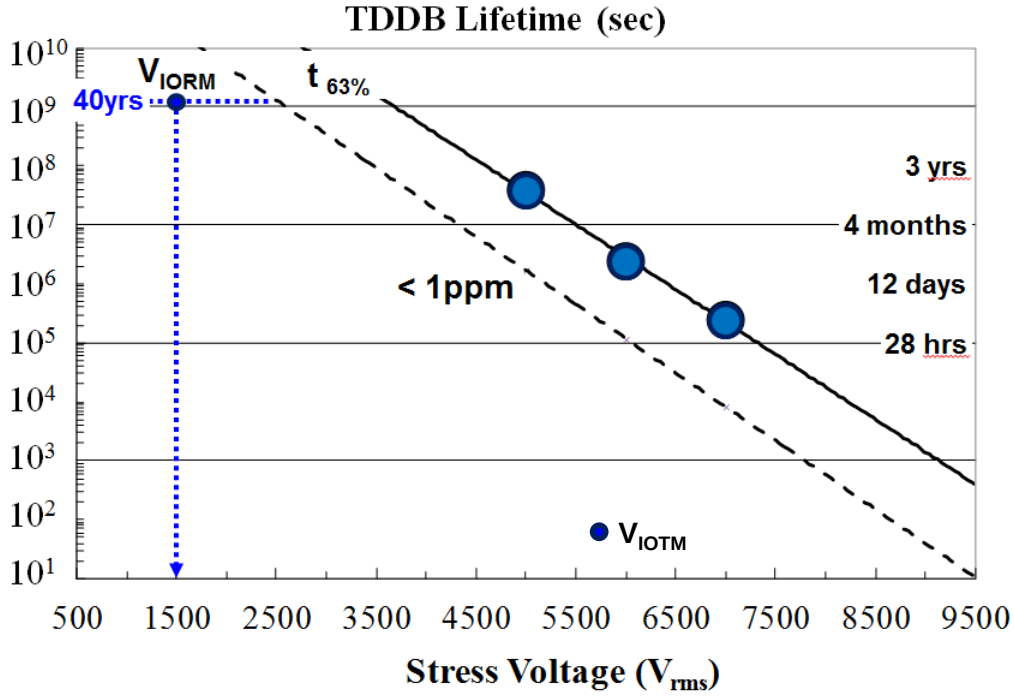
UCC2x52x, UCC2154x, UCC2351x



- Reinforced Isolation is realized by thick SiO_2 capacitors combined in series
  - Each channel uses high voltage isolation capacitors on both die
- Combined Isolation capacitor thickness is >21um
- 12.8kV surge voltage, 8kVpeak transient over-voltage, 1.5kVrms working voltage

Foundation of Quality – Qualification & Reliability

- **The main Isolation electrical lifetime test is TDDB: Qualification Test**
  - Standard methodology for determining the lifetime of a dielectric as a function of Voltage



- *TDDB is accelerated lifetime testing of the isolation barrier*
  - *Weibull statistics at each voltage*

➢ *First technology to certify to VDE 0884-11*

Foundation of Quality – SiO_2 Insulation

TI **Capacitive Isolation** uses SiO_2 as the Isolation Dielectric.

– SiO_2 advantages compared to competing HV isolative material are: **reliability** and **dielectric strength**

Insulator Materials	Dielectric Strength, 1 sec	Dielectric Strength, 40yr reliability
Air	~1 Vrms/um	
Epoxies	~20 Vrms/um	
Silica filled Mold compounds	~100 Vrms/um	
Polyimide	~300 Vrms/um	~20 Vrms/um
SiO_2	~500 Vrms/um	~100 Vrms/um

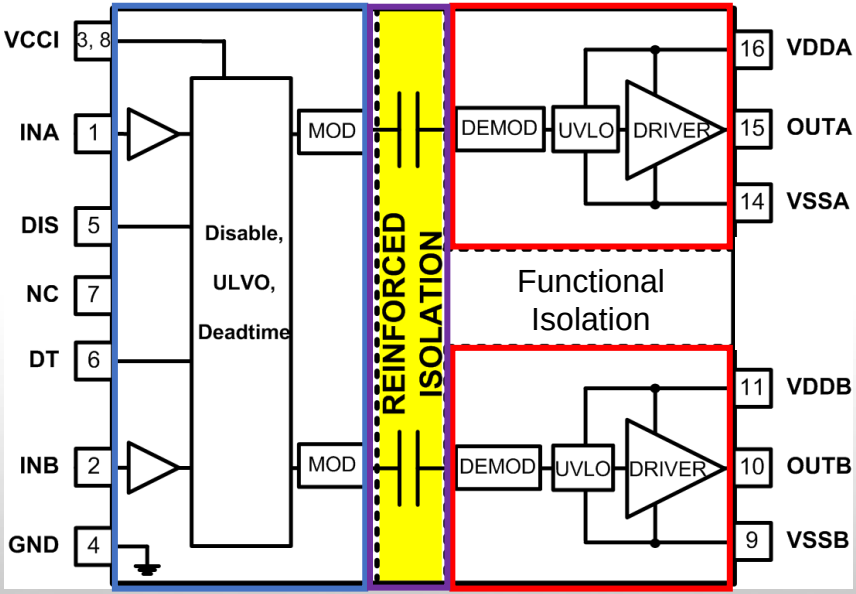
Table 1: Commonly used materials for High-Voltage isolation (SiO_2 has the highest dielectric strength and best reliability)

Dielectric Thickness (SiO_2) Fabrication Process Control & Monitor:

– **Repeatability** and **Reproducibility** – SiO_2 thickness monitored using two methods:
  - Oxide thickness sample measured in the wafer fab for each of the layers of the dielectric stack
  - Tox by capacitance measurement on test structures on every production wafer after fabrication

– Thickness is tracked on all wafers for each fabrication lot as required by UL standard

UCC21220A, UCC21540: 2-ch. Isolated Gate Driver

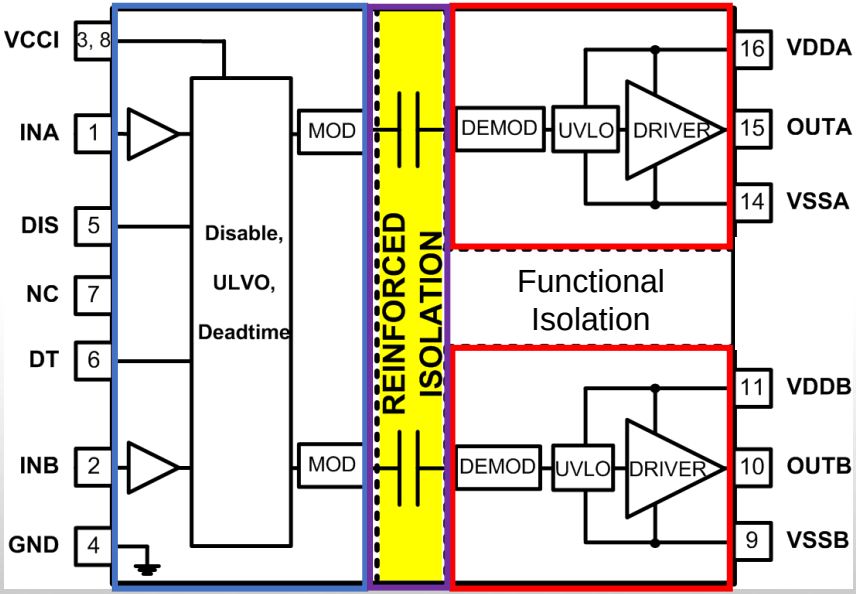


Input Die – takes inputs from µController, modulates and transmits across isolation barrier using on-off-keying

SiO2 Capacitors – provides high voltage basic or reinforced isolation, with excellent noise immunity and lifetime

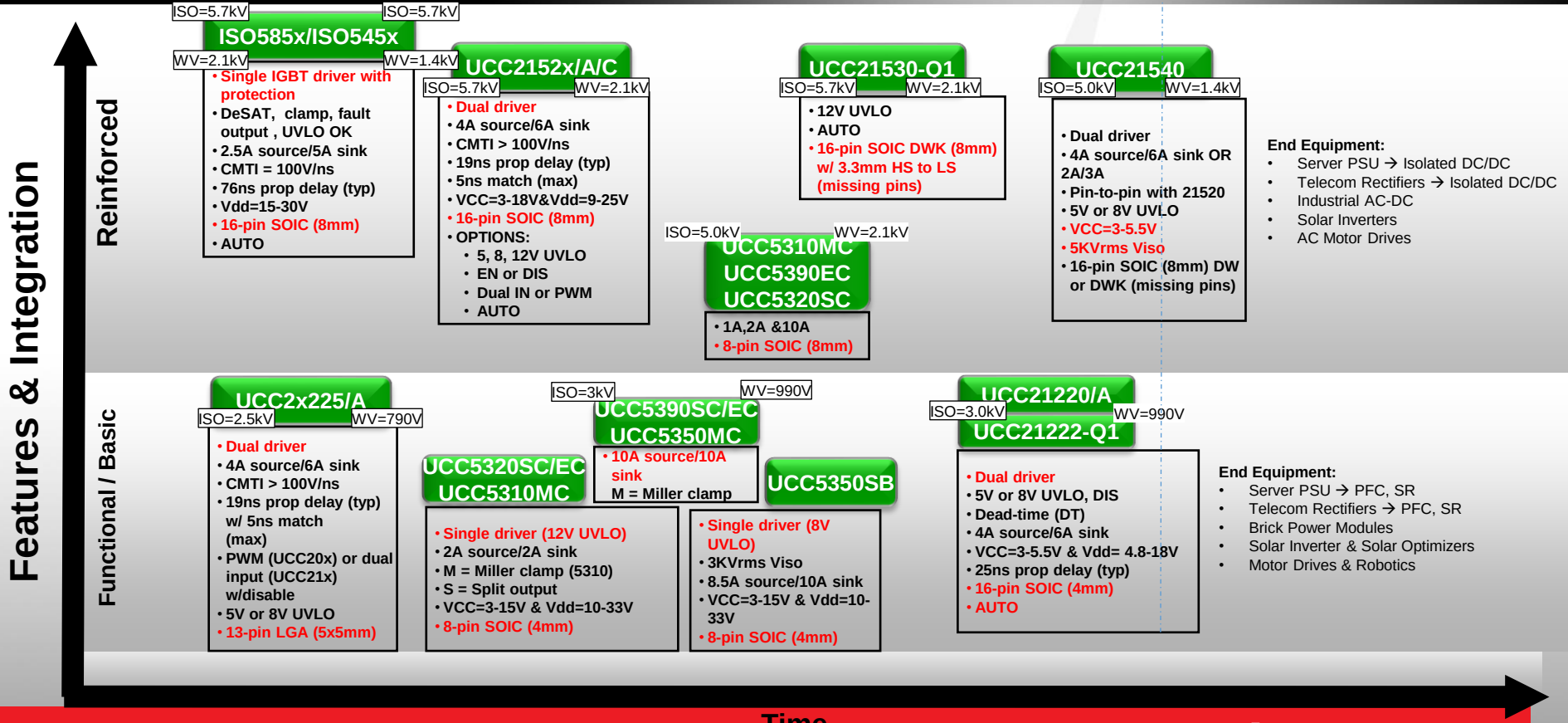
Output Die – demodulates signal and drives outputs on or off depending on logic inputs

UCC21220A, UCC21540: 2-ch. Isolated Gate Driver

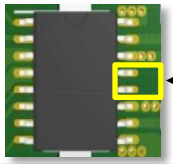
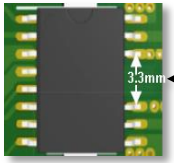


- 6A/4A sink/source
- 28ns propagation delay
- >100V/ns CMTI
- Up to 3~5V input range and 6~18V wide output voltage range
- Programmable overlap, and interlock/delay time from 0ns~5µs
- Output fail safe low with active pull down
- UVLO options: 5V, 8V
- 3.0kV, 5.7kV basic/functional and reinforced isolation
- Pin-2-pin compatible to industry standard
- UL, VDE, CQC certified

Isolated Gate Driver Portfolio



Main Differences UCC21520 & UCC21540

Parameter	UCC21520	UCC21540	Comments
VCCI/VDD AbsMax	$20V_{CCI}/30V_{DD}$	**$6V_{CCI}/20V_{DD}$**	UCC21540 – MOSFET
Output UVLO	5V, 8V, 12V	5V and 8V	
Pin 5 Functionality	DISABLE	DISABLE	UCC21540 – P2P w/ UCC21520
Driver-to-Driver Spacing	2mm	2mm & 3.3mm	3.3mm enables higher bus voltage safety standards
Propagation Delay	19ns typical	**28ns typical**	Allow accurate switching and fastest response - higher power density enabling smaller solutions
VDDA/VDDB UVLO startup delay	50µs typical	**23µs typical**	Easy synchronization between high side and low side
PCB modifications to accommodate for >600V DC Bus Voltage Applications	External coating on pins 12-13 (NC) to increase driver-to-driver working voltage  Need Conformal Coating on System PCB for HV isolation	No changes required  No coating required	UCC21540 enables: ▪ Lower cost MOSFET Solution ▪ No special coating required ▪ Higher system reliability
Automotive Grade	AEC-Q100 available	N/A	

UCC23513 Specifications

4A, 5kV$_{RMS}$, Opto-Compatible Input Gate Driver in Stretched SO-6

Overview

UCC23513 is a 4A, 5kV$_{RMS}$ opto-compatible gate driver available in stretched SO-6. Using capacitive isolation technology to simulate opto-isolation, this solution is more robust, longer-lasting, and exhibits exemplary propagation delay and Common Mode Transient Integrity specifications. With UCC23513, TI is providing customers with a pin-to-pin replacement for opto-isolated gate drivers to offer a better performing and longer-lasting solution that requires minimal effort to design in.

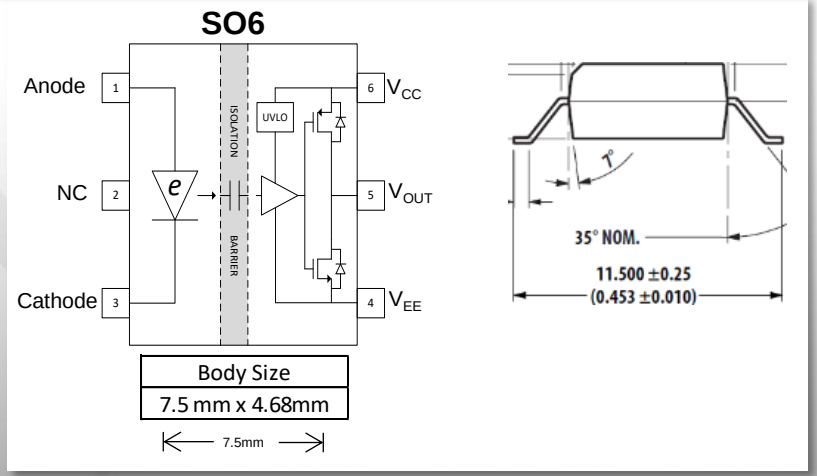
Features

- Opto-compatible input, isolated Gate driver for IGBT/MOSFET/SiCs
- SiO_2 based capacitive isolation technology
- **Pin compatible, drop-in upgrade for ACPL-W341, W346, TLP5752**
- 4A peak output drive current
- 35V max output drive (V_{CC} – V_{EE})
- SO6 (6 pin wide lead, smt), NiPdAu lead finish, material group I
- > 8.5mm Cr & Clr; 5kV$_{RMS}$ reinforced isolation
- **105ns propagation delay with 25ns part-to-part delay matching**
- **100 kV/us Common Mode Transient Integrity (CMTI)**
- 12V Under Voltage Lockout (UVLO)
- Input stage can be reverse-biased for interlock
- **Wide operating temperature range (Tj): -40°C to 150°C**

http://www.ti.com/product/UCC23513

Benefits

- **Higher common mode transient integrity**
- **Smaller propagation delay and tighter part-to-part delay matching**
- Lower pulse width distortion
- Higher reliability, resistant to temperature and aging
- No long term aging of input stage
- Very tight tolerance of cap oxide since oxide is a controlled fab process
- **Long lifetime (> 40 yrs)**
- Less variation in forward current due to tighter V_F



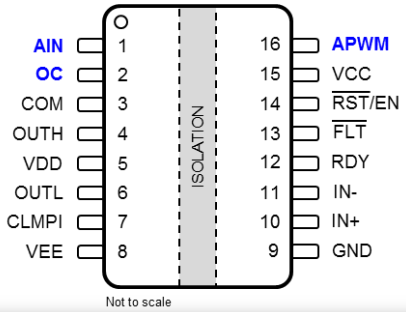
High VOLT Interactive

New Features in UCC217XX	Key System Challenge Solved …		System Benefits
	IGBT	SiC	
±10A peak drive strength (throughout drive voltage range)	>10kW systems use discrete buffers (e.g., NPN+PNP) to increase drive strength: Reliability, drive supply & cost challenges		▪ Higher System Reliability + Higher Efficiency ▪ Lower System Cost + Smaller PCB Area
>150V/ns CMTI (Min)	(Typically <50V/ns)	SiC switches fast to reduce switching loss	▪ Enhanced System Robustness ▪ Higher System Efficiency
200ns Over-Current Detection + 650ns Isolated Fault Reporting	Programmable DESAT threshold voltage	SiC has <3µs short-circuit capability	▪ Fast System Protection ▪ Enhanced System Robustness
2-Level Turn OFF (Option)	Significantly reduced V_{CE} / V_{DS} Overshoot during System Shutdown		▪ Safe System Shutdown ▪ Enhanced System Robustness ▪ Improved Switch Lifetime
Integrated Isolated Accurate Analog-to-PWM Sensor	Eliminate all discrete components used for bus voltage sensing / switch temperature sensing / sec-to-primary feedback / isolated alarm / …		▪ **Lower System Cost** ▪ **Smaller PCB Area**
VEE UVLO (Option)	Eliminate discrete circuitry for VEE monitoring (voltage sensor + isolator)		▪ Lower System Cost ▪ Smaller PCB Area
External Miller Clamp (Option)	More effective technique than internal miller clamp for high-power switch modules		▪ Enhanced System Robustness ▪ Lower System Noise (Ringing + EM)
Standard SOIC-16 DW Package	Small package size, 1mm pad pitch, pin-to-pin compatibility with better specs		▪ **Lower System Cost** ▪ **Smaller PCB Area**

High VOLT Interactive

UCC21710

: AEC-Q100



Not to scale

Fast (200ns) Over-Current Detection:

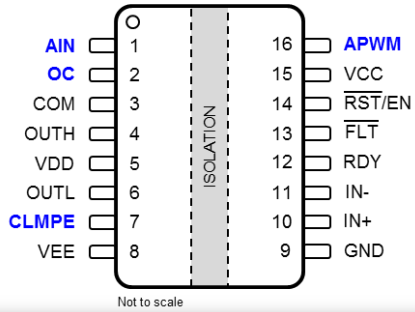
- Important for fast switch protection, especially SiC MOSFETs
- Allows for flexible DESAT threshold setting for SiC MOSFET or IGBT
- Applicable to IGBT modules with SenseFET

Internal Miller Clamp: Suited for lower power levels (<50kW) or tighter layouts (driver to switch)

Soft Turn-OFF: Preferred method for safe shutdown of SiC or IGBT switch

UCC21732 / 36

: AEC-Q100



Not to scale

Fast (200ns) Over-Current Detection:

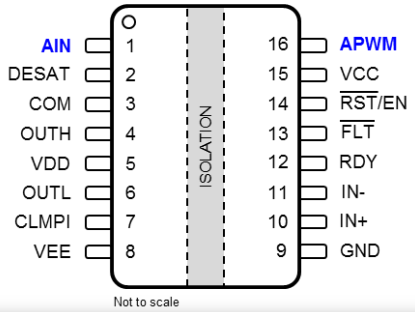
- Important for fast switch protection, especially SiC MOSFETs
- Allows for flexible DESAT threshold setting for SiC MOSFET or IGBT
- Applicable to IGBT modules with SenseFET

External Miller Clamp: Ideal for high-power IGBT/SiC modules (reduce clamp-to-gate parasitics)

2-Level Turn-OFF: Preferred for high-power modules for higher power applications

UCC21750

: AEC-Q100



Not to scale

Standard 9V DESAT:

- Exactly what typical IGBTs need (same specs as ISO58XX)
- 9V DESAT might be high for SiC MOSFETs (depends on SiC MOSFET supplier)

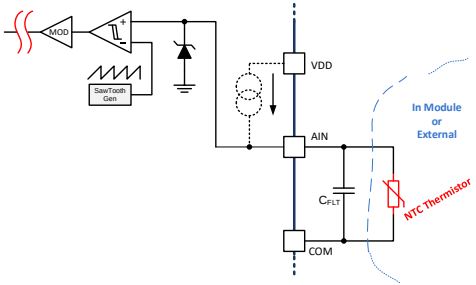
Internal Miller Clamp: Suited for lower power levels (<50kW) or tighter layouts (driver to switch)

Soft Turn-OFF: Preferred method for safe shutdown of IGBT or SiC switch

[*NOTE:* Pins in Black have same pin locations as in ISO5852S or ISO5452. Pin in **Blue** are new pin definitions.]

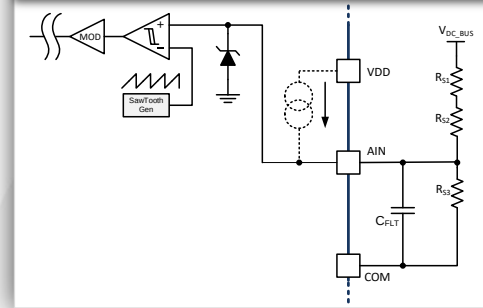
[*Disclaimer:* Specs, features & pinouts subject to change without prior notice.]

Isolated Switch Temperature Sensing: NTC/PTC



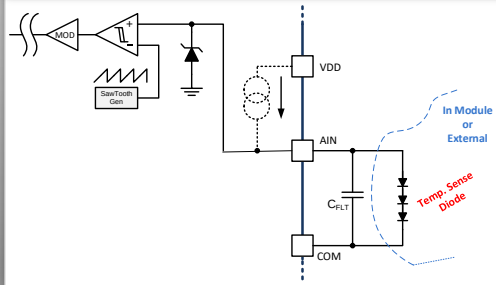
- AIN Range: 0.5V to 4.5V
- AIN Bandwidth: 50kHz
- APWM: 90% to 10%
- APWM Frequency: 400kHz
- AIN-APWM Accuracy:
  - ±1%: System-level cal.
  - ±3%: Without cal.
- I_{AIN}: 0.2mA (±3%)

Isolated Analog Signal Sensing: HV Bus / Power Supply / …



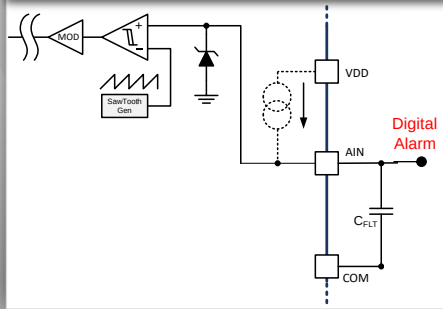
- HV Bus Sensing
- Secondary-to-Primary Bus Voltage Feedback
- Driver-side Supply Voltage Monitoring (Redundant / Additional UVLO)

Isolated Switch Temperature Sensing: Thermal Diode



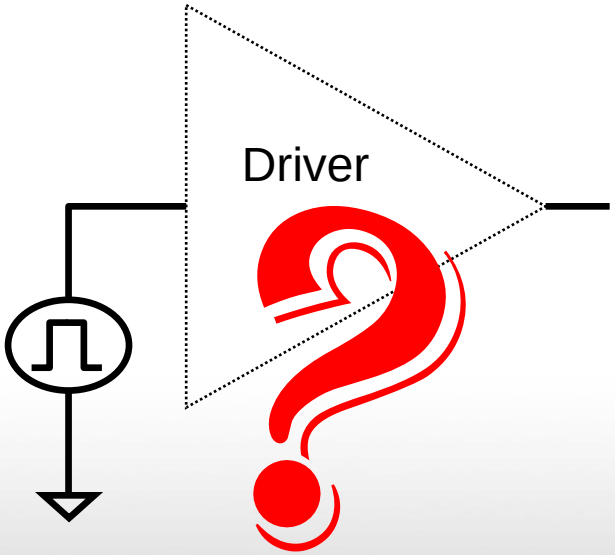
- Switch Over-temperature Detection: System Protection
- System performance optimization based on Switch Temperature Sensing
- Switch temp-cycling / lifetime monitoring

Isolated Digital Signal: Alarm / Shutdown



- Digital Alarm
- Emergency Shutdown signal

Gate Driver Design is Simple?

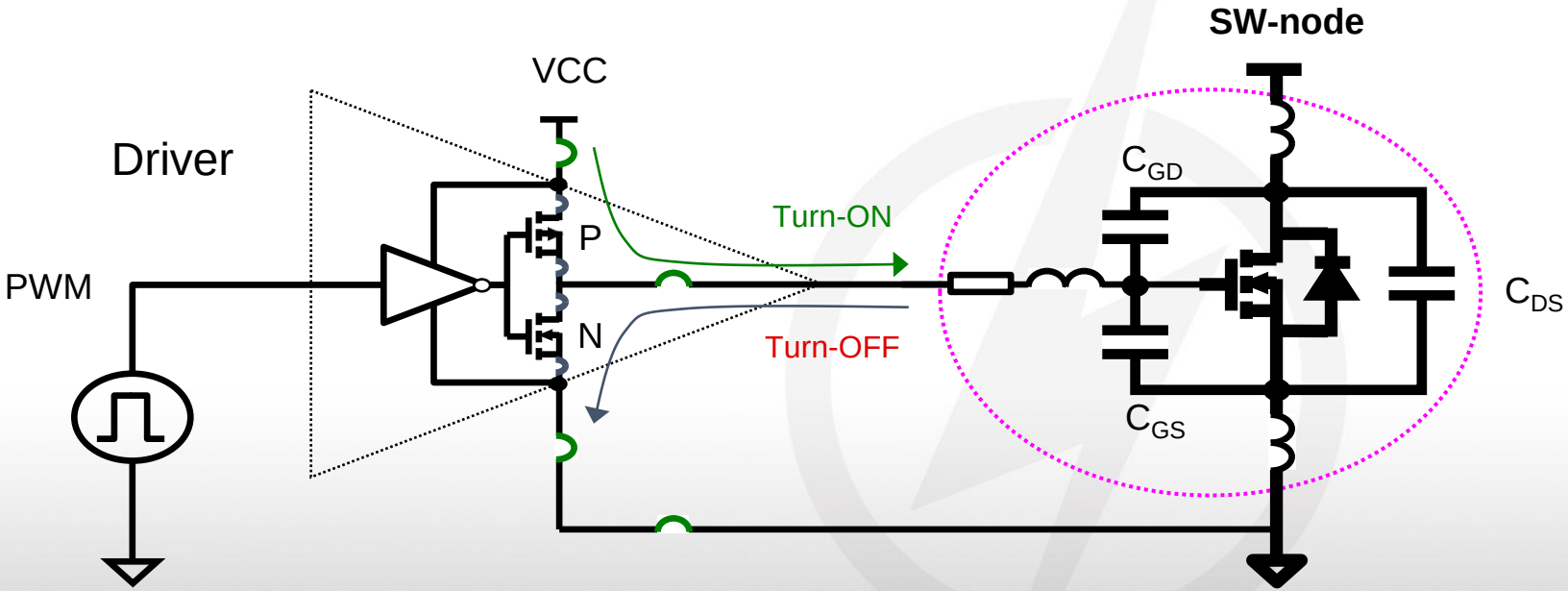


1. **Parasitics in gate driver?**
2. **Common mode transient immunity(CMTI), dv/dt and di/dt through parasitics L and C?**
3. **Gate driver soft/hard switching difference?**
4. **Strong gate driver and MOSFET nonlinear C_{oss}?**
5. **Power supply for isolated gate driver in UPS, server and Telecom system**

Gate driver deep dive

Very critical role in converter efficiency and reliability

What are the Parasitics?



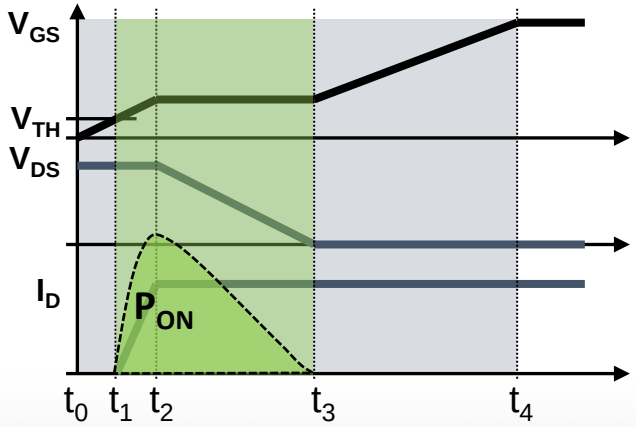
$$C_{ISS} = C_{GS} + C_{GD}$$

$$C_{RSS} = C_{GD}$$

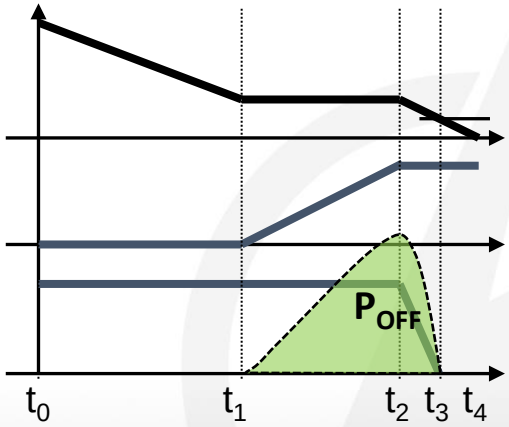
$$C_{OSS} = C_{GD} + C_{DS}$$

Turn-ON/OFF process

Turn-ON



Turn-OFF

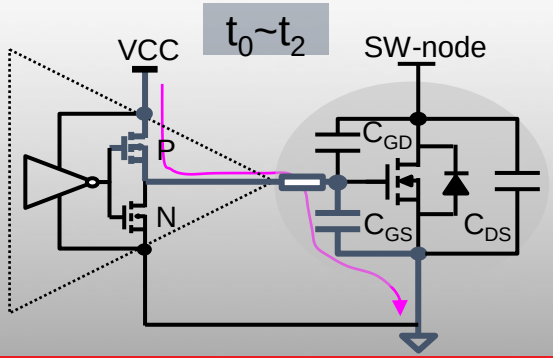


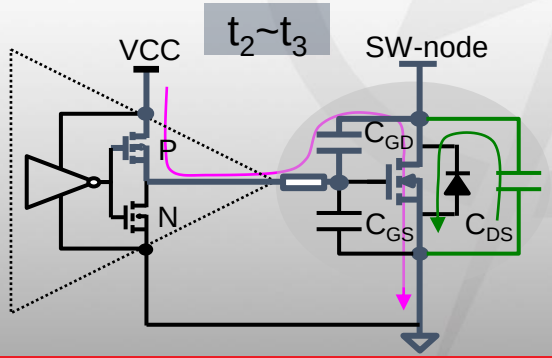
Switching on loss

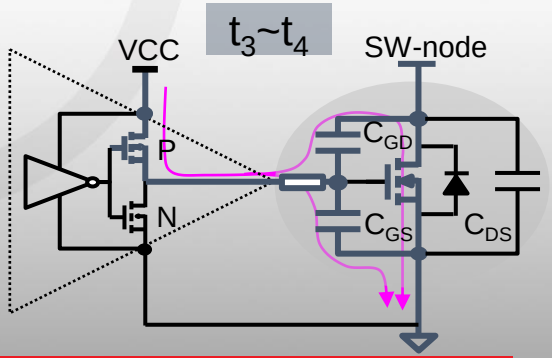
$$\int_{t_1}^{t_3} V_{DS}(t) \cdot I_D(t) dt + E_{OSS}$$

$$t_{1\sim3} \propto \frac{1}{I_{Drv}}$$

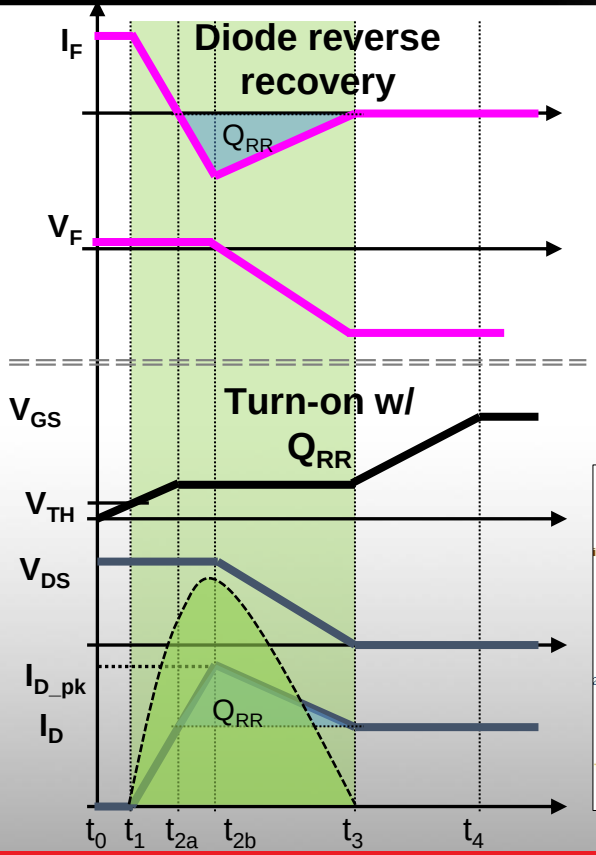
Stronger driver → lower switching loss



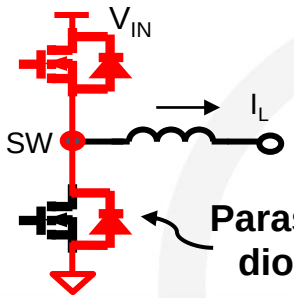


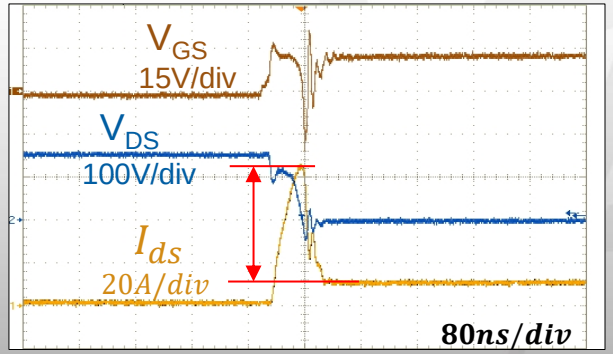


Turn-ON with Reverse Recovery

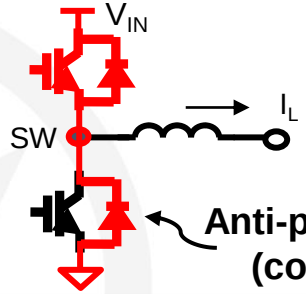


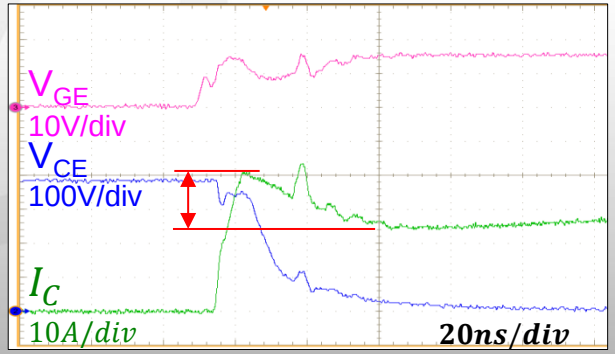
SJ-MOSFET



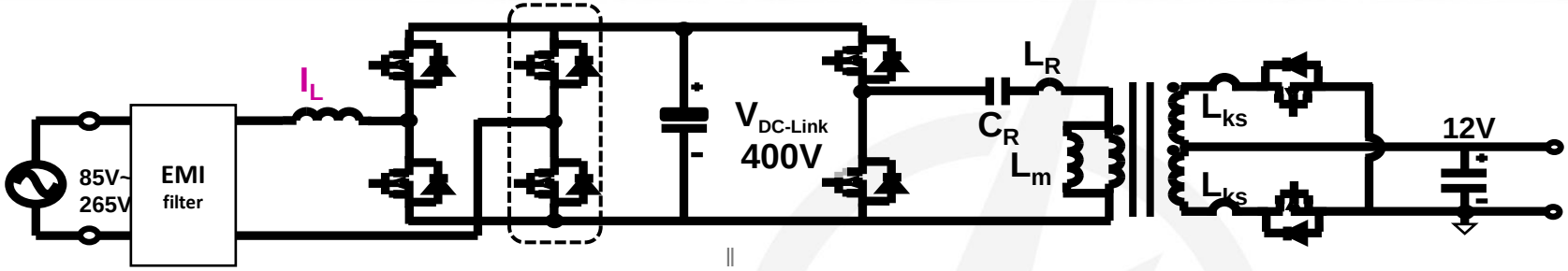


IGBT

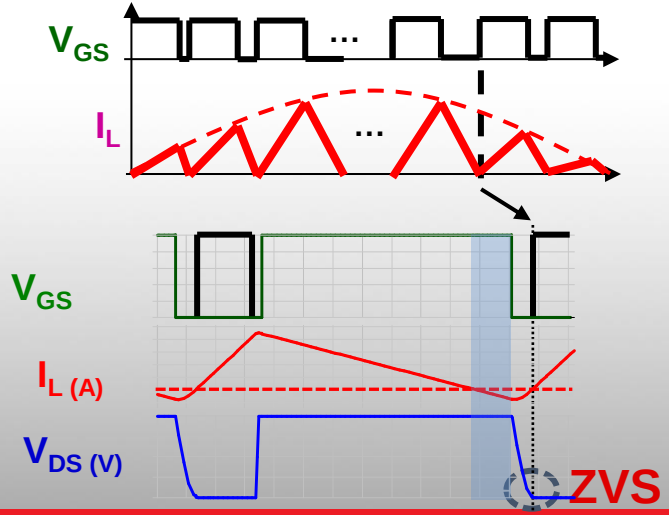




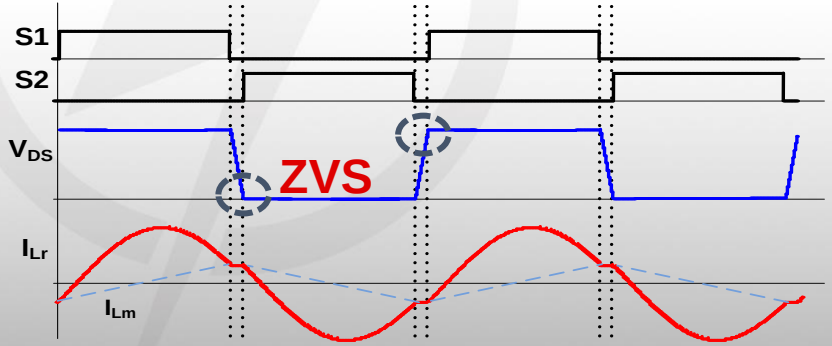
Soft Switching



CRM totem pole PFC

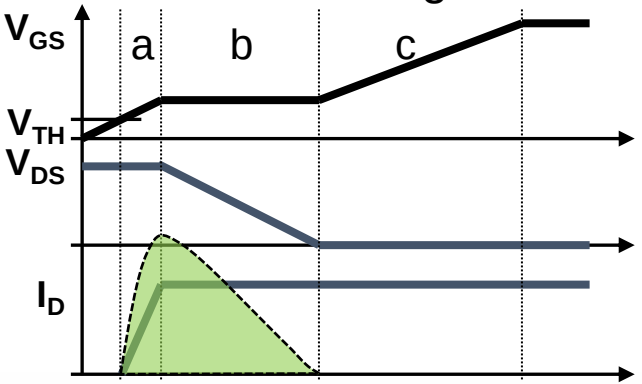


LLC converter + center-tap rectifier

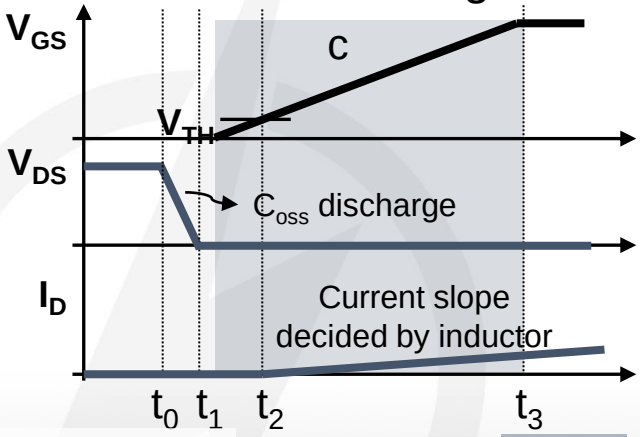


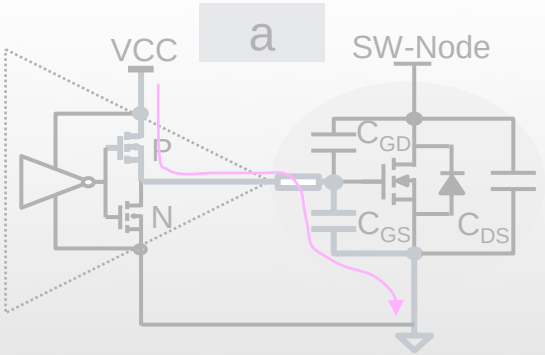
Gate Driver for Soft Switching

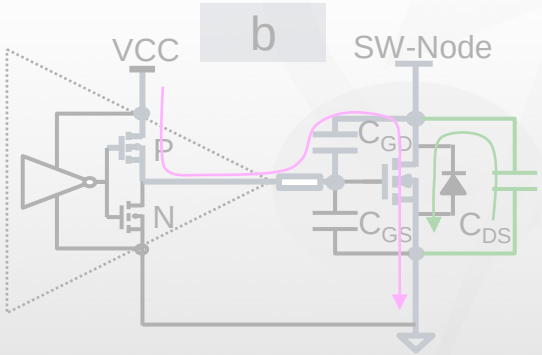
Hard-switching

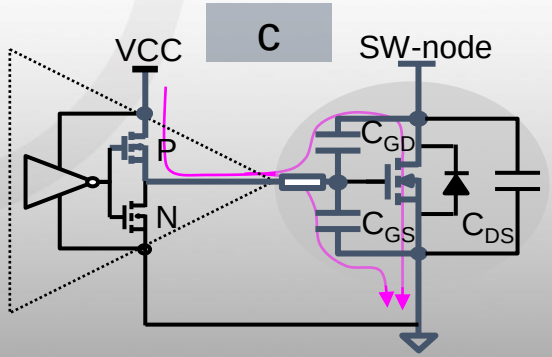


Soft-switching

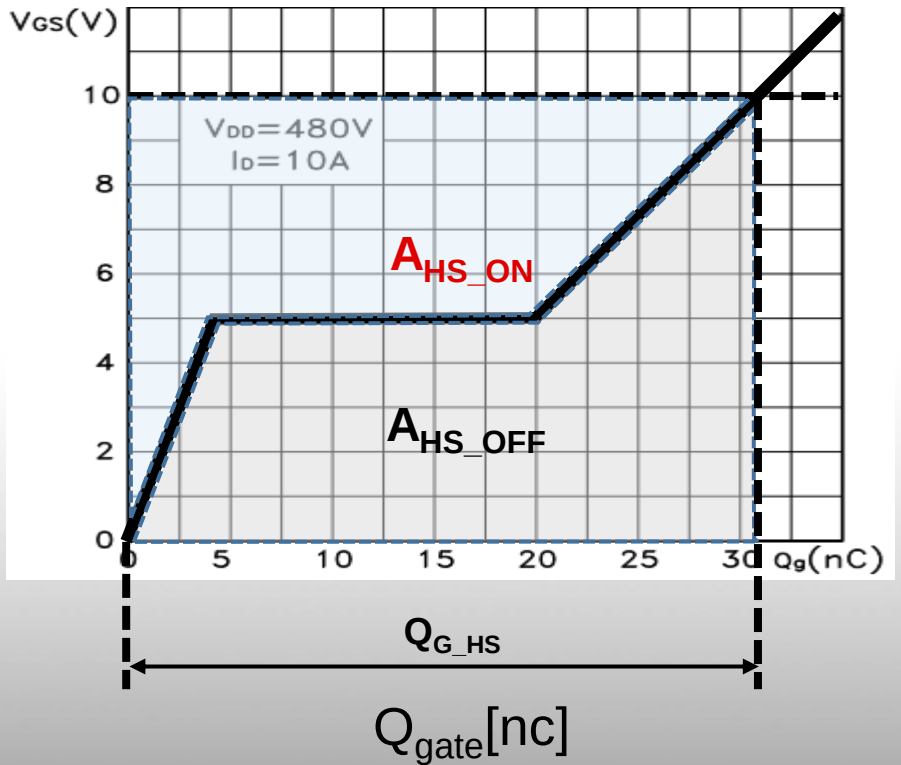




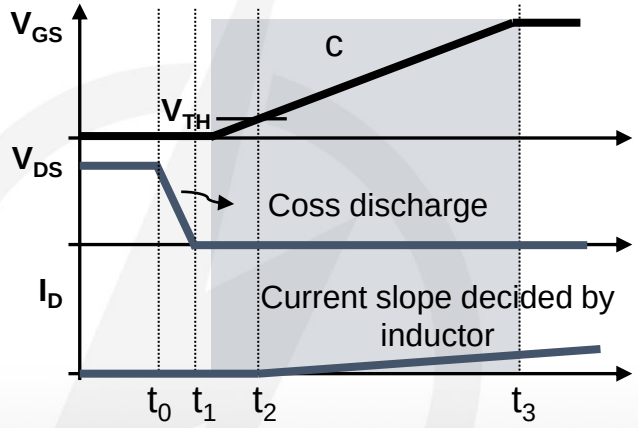




Gate Driver for Soft Switching



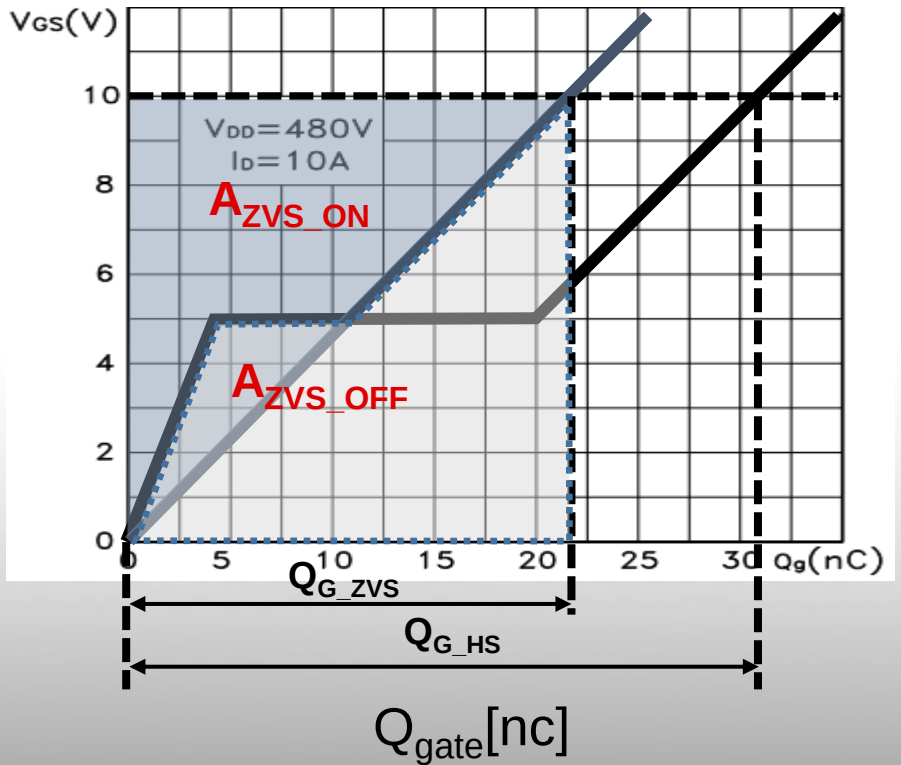
Soft-switching



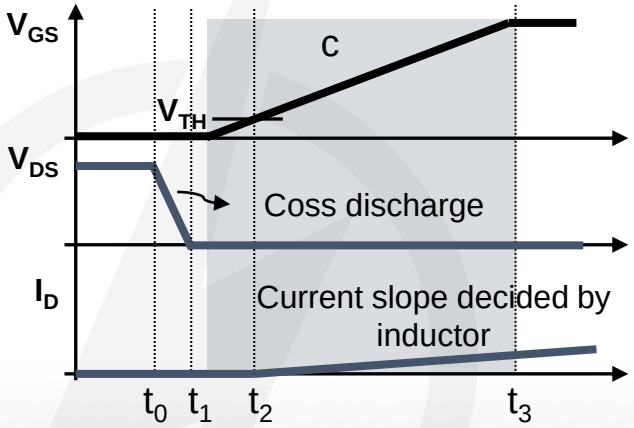
$$E_{G\_HS} = A_{HS\_ON} + A_{HS\_OFF} = V_{GS} \cdot Q_{G\_HS}$$

$$P_{GateDrv} = E_G \cdot f_{SW}$$

Gate Driver for Soft Switching



Soft-switching

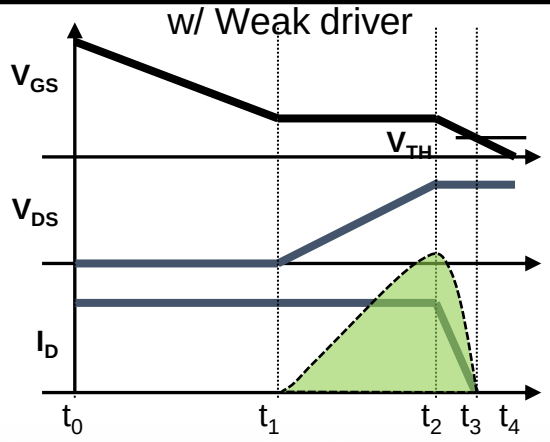


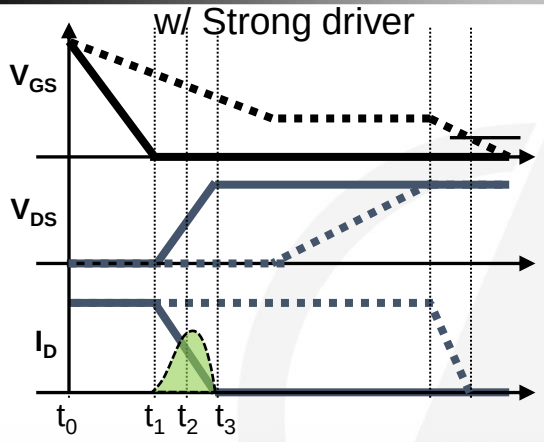
$$E_{G\_HS} = A_{HS\_ON} + A_{HS\_OFF} = V_{GS} \cdot Q_{G\_HS}$$

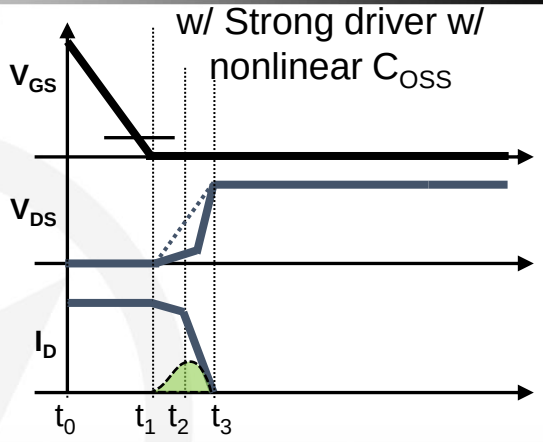
$$E_{G\_ZVS} = A_{ZVS\_ON} + A_{ZVS\_OFF} \approx V_{GS} \cdot Q_{G\_ZVS}$$

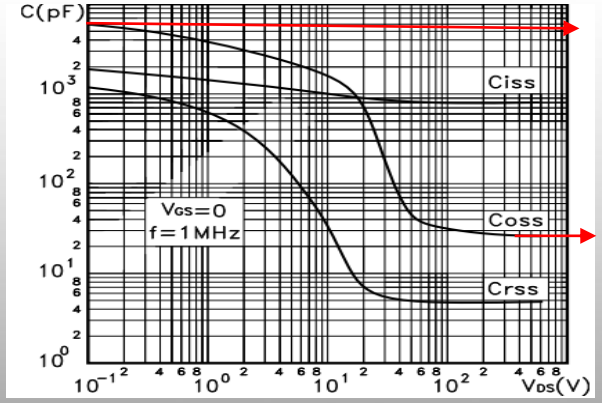
$$P_{GateDrv} = E_G \cdot f_{SW}$$

Strong Turn-OFF







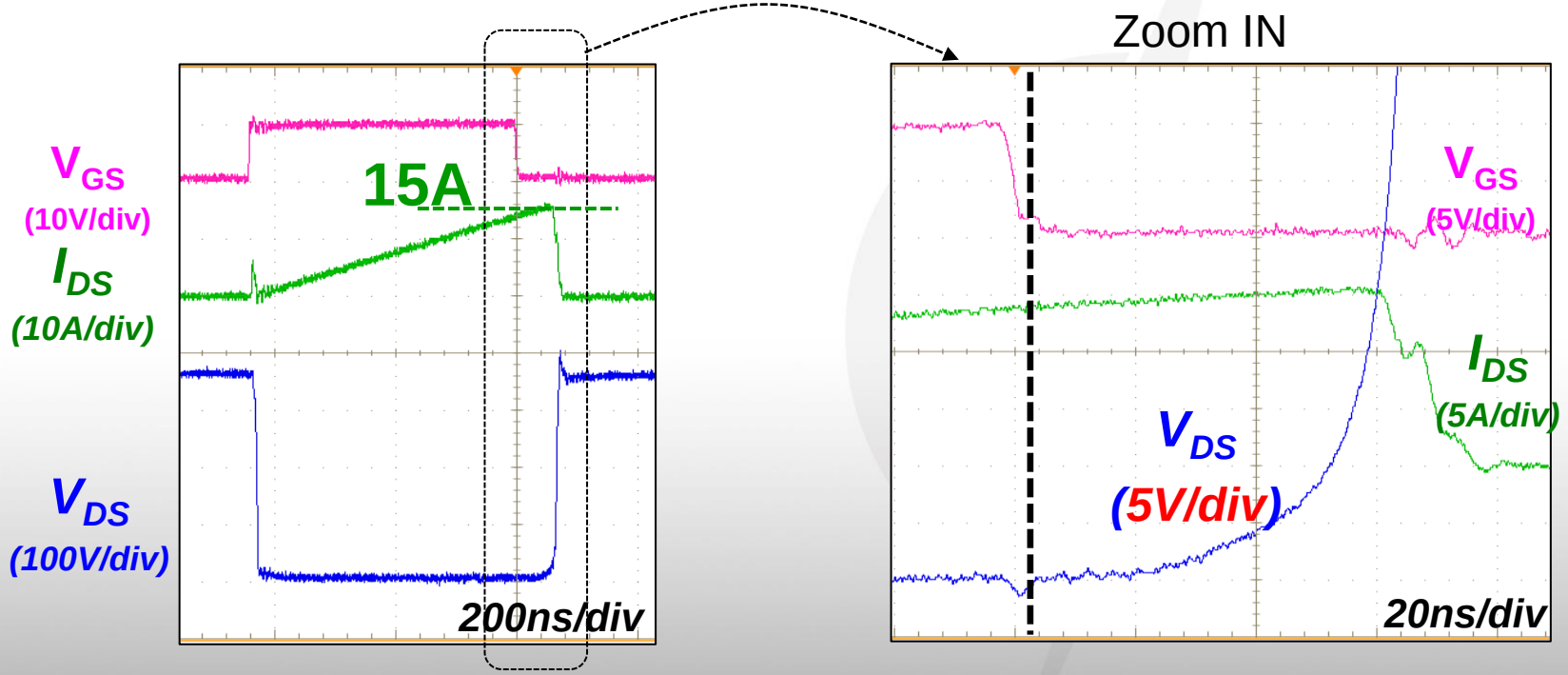


C_{OSS}(0V) =6nF

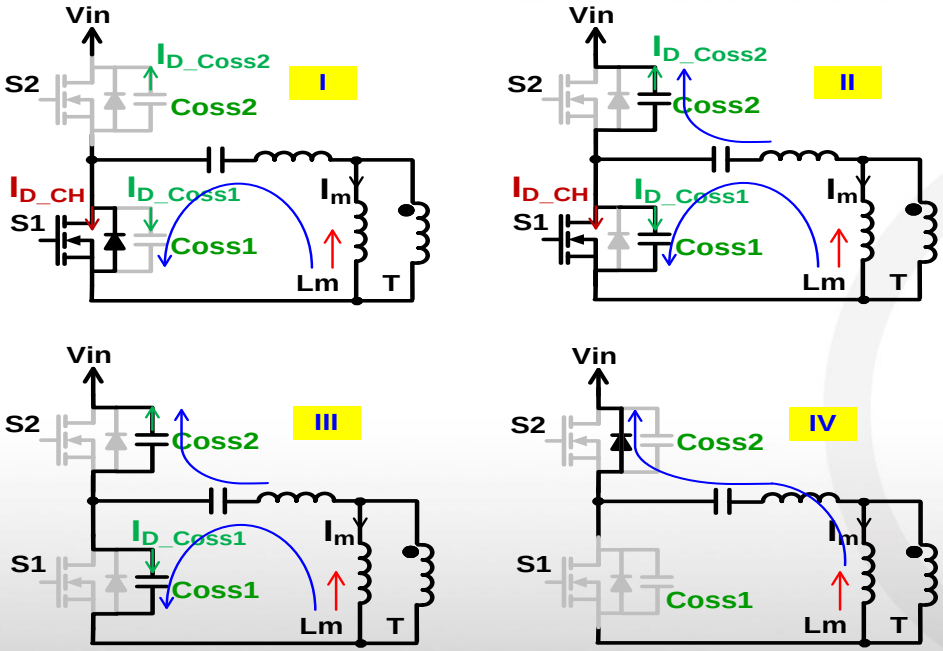
C_{OSS}(400V) <30pF

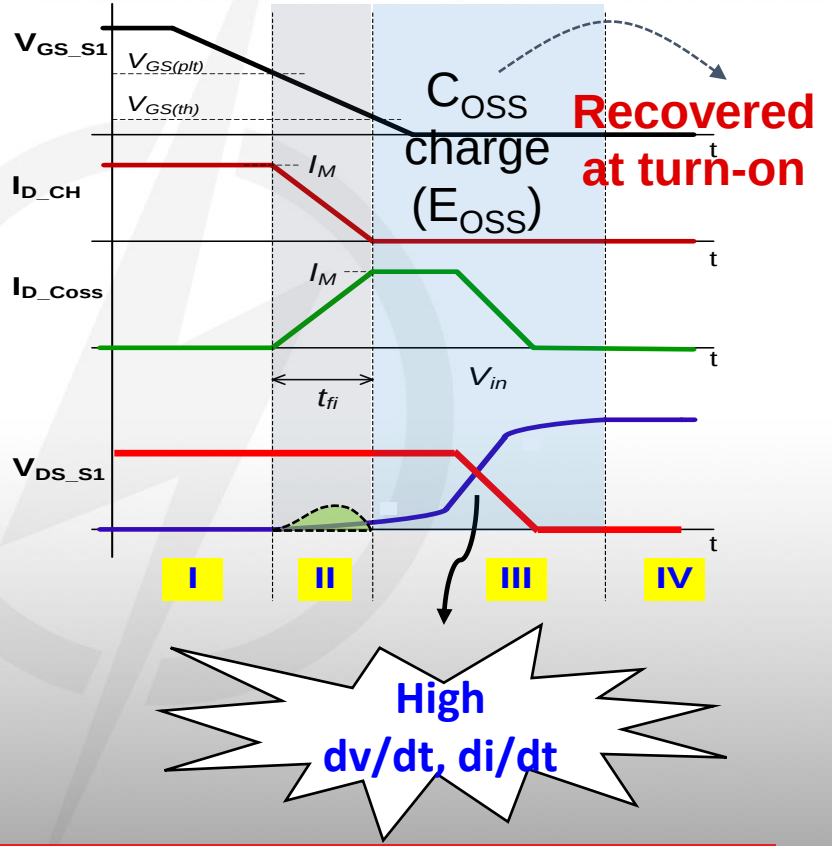
- Switching behavior is not controlled by gate current, but by C_{OSS} and load current
- Large C_{OSS} at low voltage performs as natural snubber
- Small C_{OSS} at high voltage shortens V-I overlap
- Fast dv/dt and di/dt, other bad things

Strong Turn-OFF



Strong Driver for LLC Turn-OFF

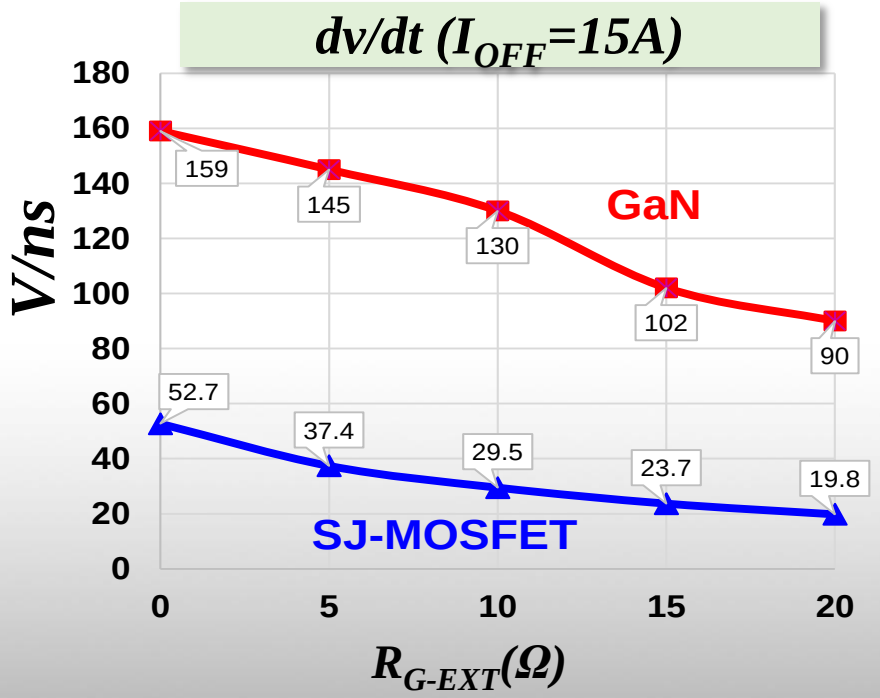


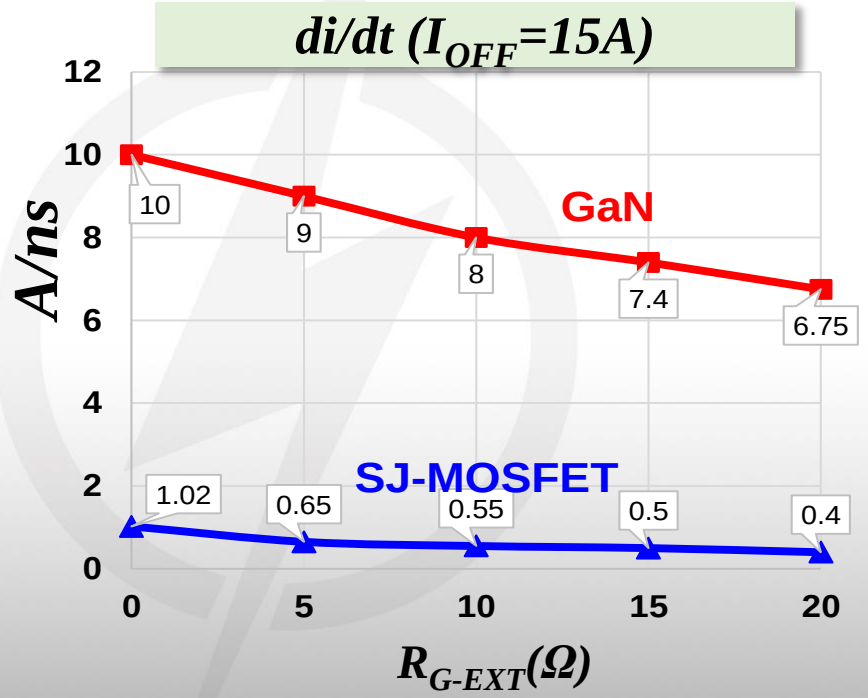


In period II, $V_{DS\_S1} << V_{DS\_S2}$; $C_{oss1} >> C_{oss2}$

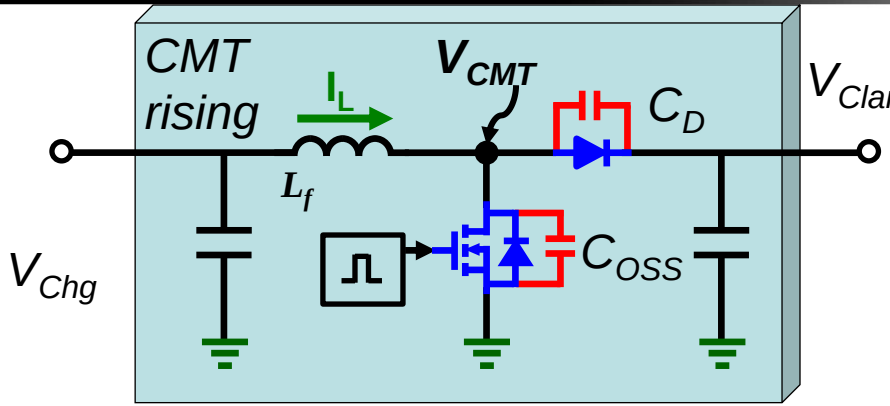
$$I_{D\_Coss} = I_{D\_Coss1} + I_{D\_Coss2} \approx I_{D\_Coss1}$$

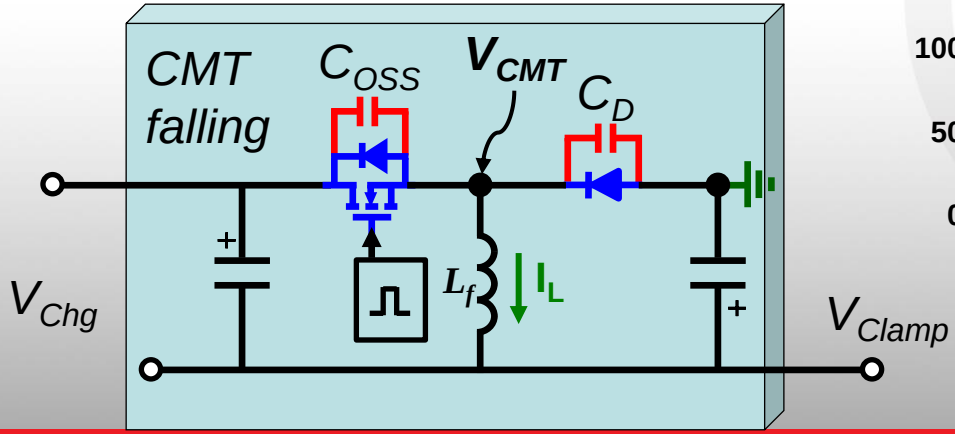
High dv/dt and di/dt: GaN vs. Si

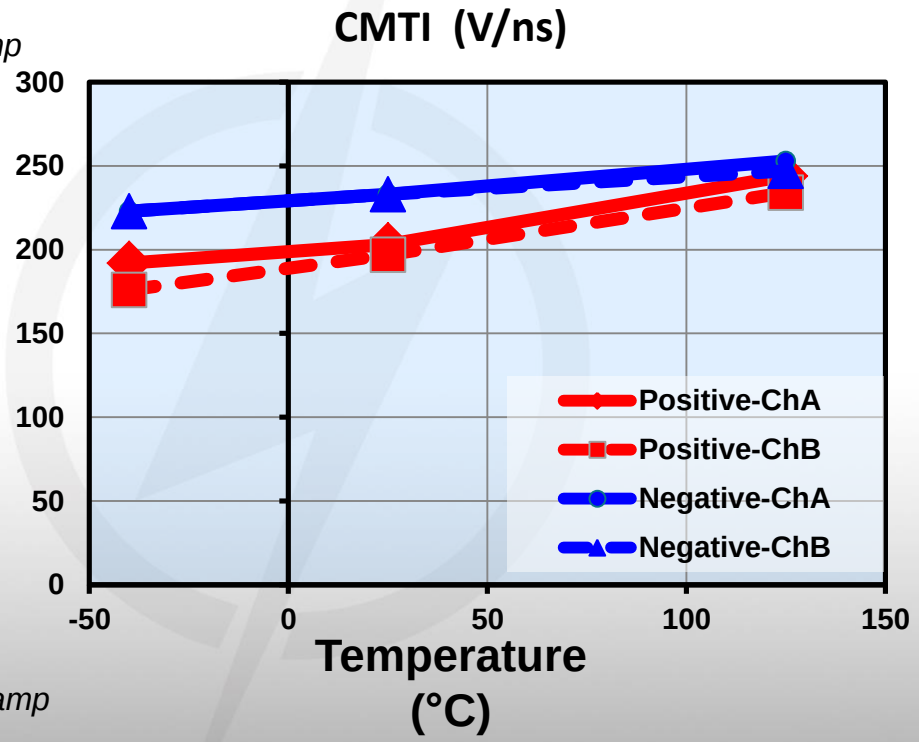




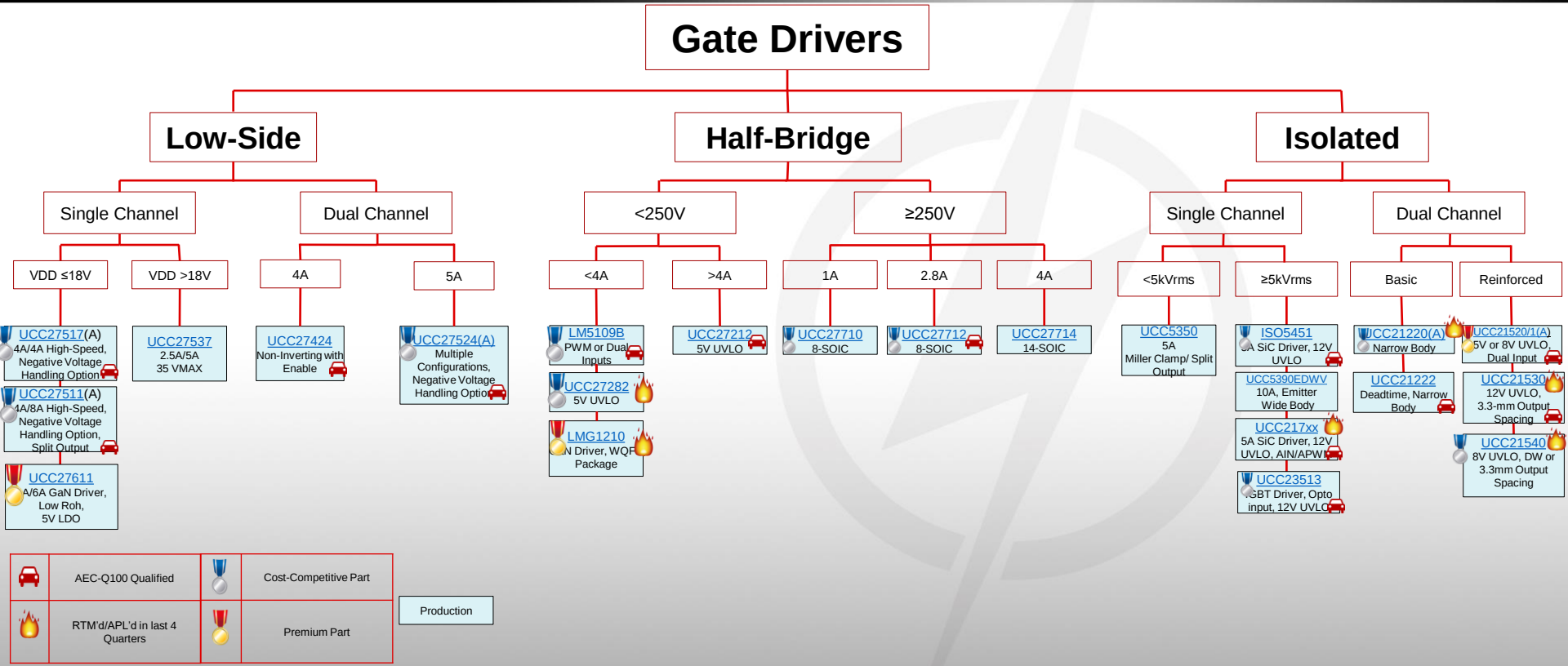
CMTI Measurement for UCC21540







Gate Driver Portfolio: Selection Tree



Summary

- Gate driver fundamentals and in-system consideration
- Low side, high- and low side, isolated gate driver
- Parasitics in gate driver?
- Gate driver soft/hard switching difference?
- Strong gate driver and MOSFET nonlinear C_{OSS}?
- Common mode transient immunity(CMTI), dV/dt and di/dt through parasitics
- Power supply for isolated gate driver in UPS, server and Telecom

Sample TI's New Isolated Gate Drivers:

- ✓ **UCC21540:** http://www.ti.com/product/UCC21540/samplebuy
- ✓ **UCC21220A:** http://www.ti.com/product/UCC21220A/samplebuy
- ✓ **UCC21710-Q1:** http://www.ti.com/product/UCC21710-Q1/samplebuy
- ✓ **UCC23513:** http://www.ti.com/product/UCC23513/samplebuy

Summary

Thank you