

# **Design Tips of OP Amplifier and TINA Simulation Tool**

## **運算放大器設計小技巧 + TINA教學**

Ting Ye

Field Application Engineer

# Agenda

- Op Amp in Over Current Protection Circuit
  - Output swing limitation
  - Input ESD steering diodes
- Improve Thermal Performance Op Amp Circuit
  - Power Dissipation Calculation
  - Thermal Impedance and Junction Temperature
  - Consider Protection Response Time, Signal Latency, Spike Signal Rise Time
- Amplifier Major Parameters in Current Sensing Application
  - High Side Current Sensing Circuit Specifications
  - Rshunt Calculation
  - Offset Voltage and Drift
  - Slew Rate and Bandwidth
  - CMRR AC
- TINA Tutorial

# Op Amp in Over Current Protection Circuit (OCP)

# Op Amp for OCP - Vout\_swing Limitation

Reference Design of Output Short-Circuit Protection for TPS61088 10A Boost Converter  
(PMP9779)

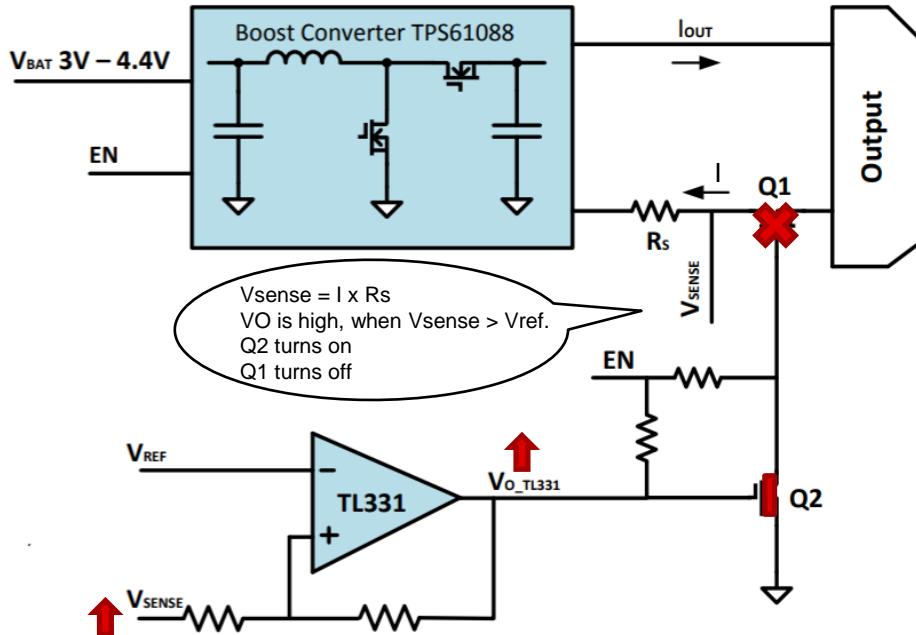


Figure 1. Block Diagram of PMP9779

- I've got a extra, not used channel of LM324 or TL074.
- Can I use it as the OCP comparator?

# Problems and Why

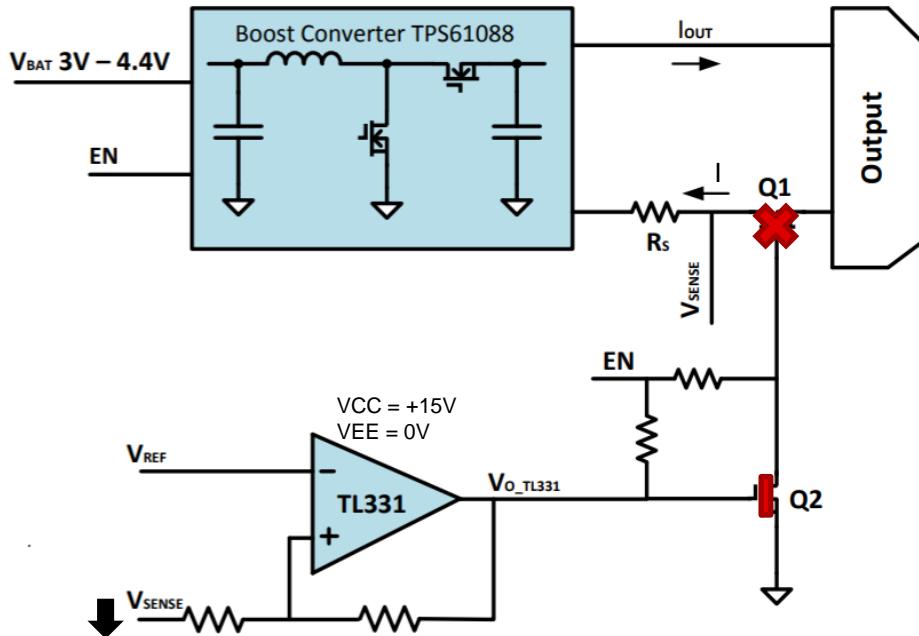


Figure 1. Block Diagram of PMP9779

- Problem:  
When set the load current within the normal operating range, the OCP circuit is **false triggered**, Q1 is off and no path for current to flow.

# Problems and Why

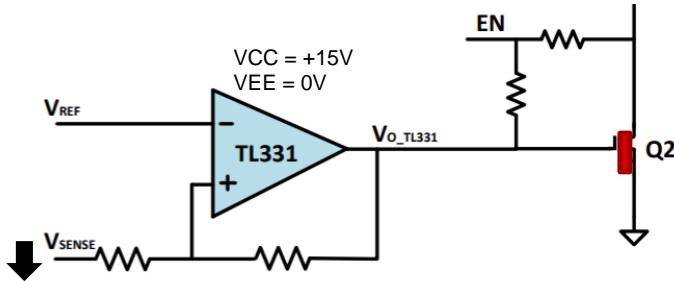


Figure 1. Block Diagram of PMP9779



[www.ti.com](http://www.ti.com)

TL071, TL071A, TL071B  
TL072, TL072A, TL072B, TL074, TL074A, TL074B, TL072M, TL074M  
SLOS080N –SEPTEMBER 1978–REVISED JULY 2017

## 6.10 Electrical Characteristics: TL071C, TL072C, TL074C

$V_{CC\pm} = \pm 15$  V (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>(1) (2)</sup>		MIN	TYP	MAX	UNIT
	$V_O = 0$	$T_A = 25^\circ C$				
$V_{IO}$ Input offset voltage	$R_S = 50 \Omega$	$T_A = Full\ range$			13	mV
			3	10		
$\alpha$ Temperature coefficient of input offset voltage	$V_O = 0$	$T_A = Full\ range$		18		$\mu V/^\circ C$
	$R_S = 50 \Omega$				10	nA
$I_{IO}$ Input offset current	$V_O = 0$	$T_A = 25^\circ C$		5	100	pA
		$T_A = Full\ range$			10	nA
$I_{IB}$ Input bias current <sup>(3)</sup>	$V_O = 0$	$T_A = 25^\circ C$		65	200	pA
		$T_A = Full\ range$			7	nA
$V_{ICR}$ Common-mode input voltage range	$T_A = 25^\circ C$		$\pm 11$	$-12$ to $15$		V
$V_{OM}$ Maximum peak output voltage swing	$R_L = 10 k\Omega$	$T_A = 25^\circ C$	$\pm 12$	$\pm 13.5$	V	
	$R_L \geq 10 k\Omega$		$\pm 12$			
	$R_L \geq 2 k\Omega$	$T_A = Full\ range$	$\pm 10$			

- Root cause:
- A. Op Amp output swing limitation. Output swing range from -40°C to +85°C with  $R_{load} \geq 2 k\text{-ohm}$  is  $VEE + 5\text{V}$  and  $VCC - 5\text{V}$ .
- B. Output swing shrinks with load current increase. In Figure 6, with  $2\text{k-ohm}$  load at  $TA = 25^\circ C$ , output swing is  $\pm 11.75\text{V}$ .  $0.6\text{k-ohm}$  load shows VOM of  $\pm 10\text{V}$ .

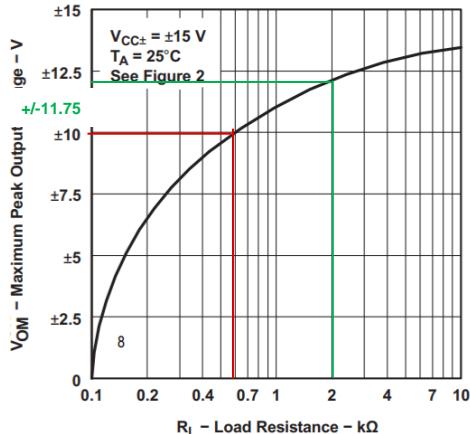
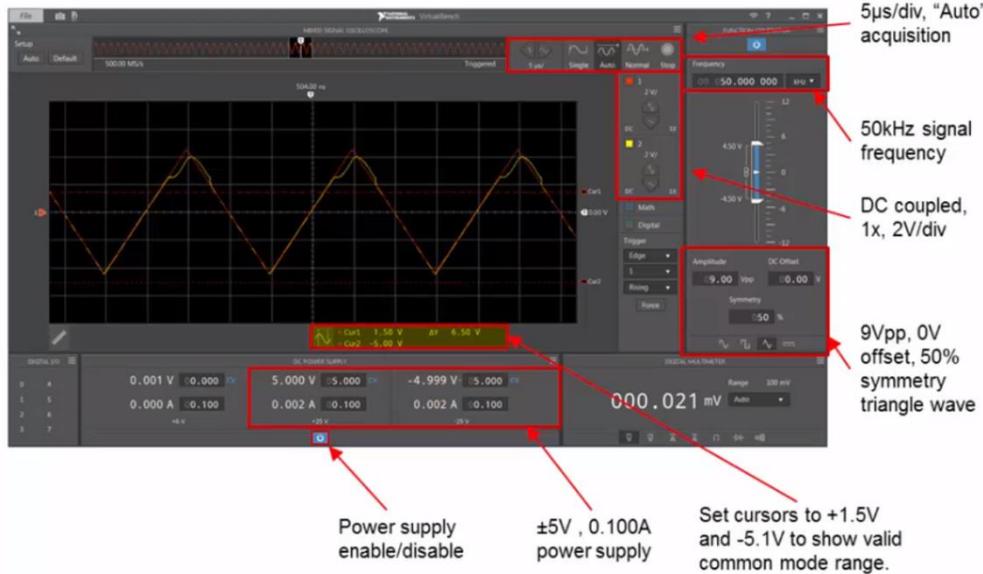


Figure 6. Maximum Peak Output Voltage vs Load Resistance

# TI Precision Labs – Op Amps: Input and Output Limitations

- <https://training.ti.com/ti-precision-labs-op-amps>

## VirtualBench Instrument Setup



13

7

# Op Amp for OCP– Input Clamping Diode

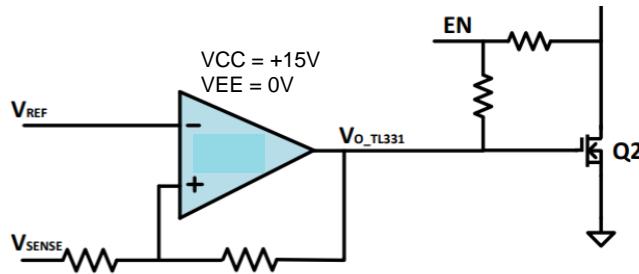


Figure 1. Block Diagram of PMP9779

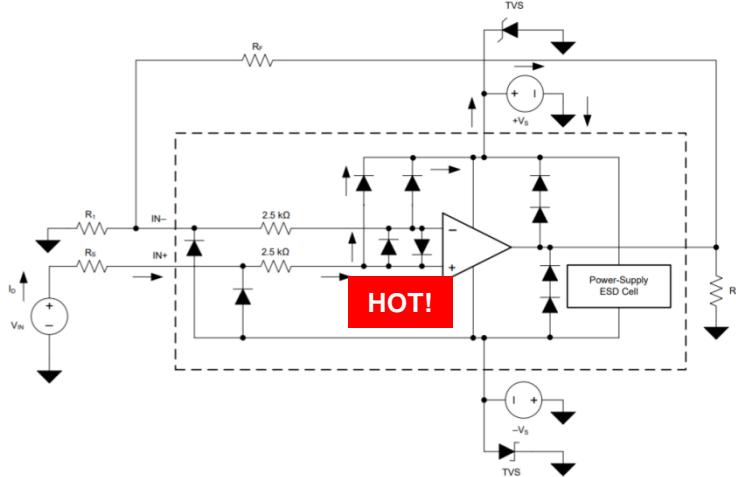
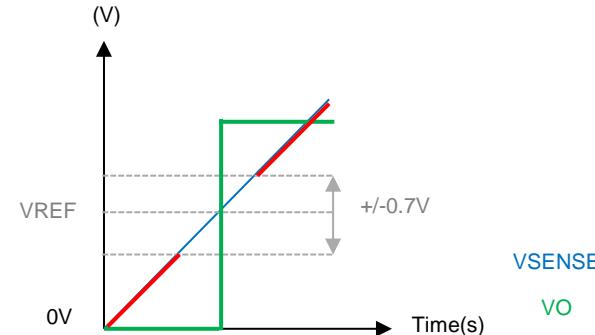


Figure 38. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

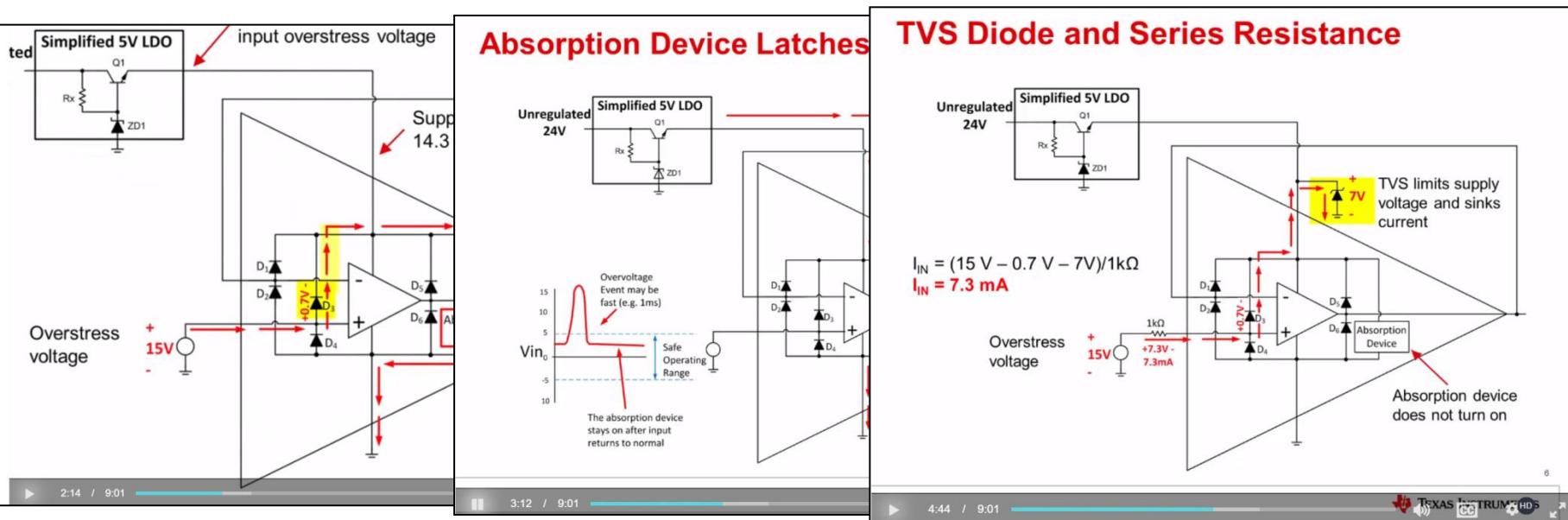
- Problems:  
Op Amp IC has high failure rate and is damaged after turning on power for a while.
- Root cause:  
Input clamping diode is conducting and could be damaged without external current limiting resistor.



8

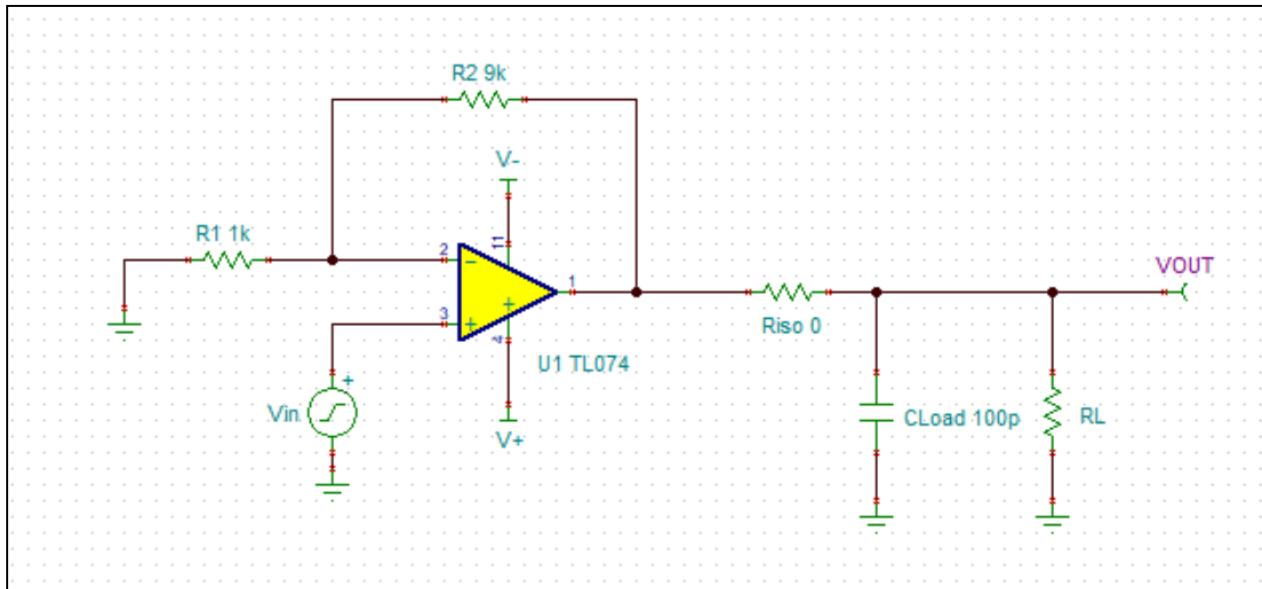
# TI Precision Labs – Op Amps: Electrical Overstress (EOS)

- <https://training.ti.com/ti-precision-labs-op-amps>



# **Improve Thermal Performance of Wide Voltage/ Dual Supply Op Amp**

# +/-15V Op Amp Gain of 10 Circuit



# Power Dissipation Calculation

## Power dissipation calculation

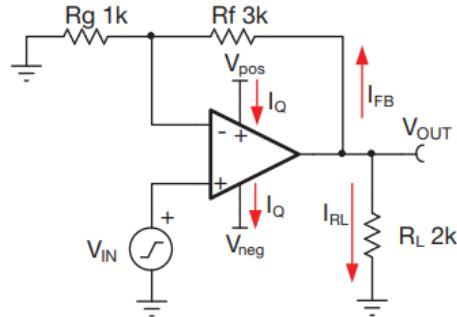


Figure 52: Current and power dissipation for non-inverting amplifier

Non-inverting amplifier power dissipation for specific  $V_{OUT}$

$$I_{RL} = \frac{V_{OUT}}{R_L} \quad (134) \text{ Current through load resistor}$$

$$I_{FB} = \frac{V_{OUT}}{R_F + R_g} \quad (135) \text{ Current through feedback network}$$

$$P_L = (|I_{RL}| + |I_{FB}|)(|V_{sup}| - |V_{OUT}|) \quad (136) \text{ Power dissipated inside op amp from load current.}$$

$V_{sup} = V_{pos}$  if the amplifier is sourcing.  
 $V_{sup} = V_{neg}$  if the amplifier is sinking.

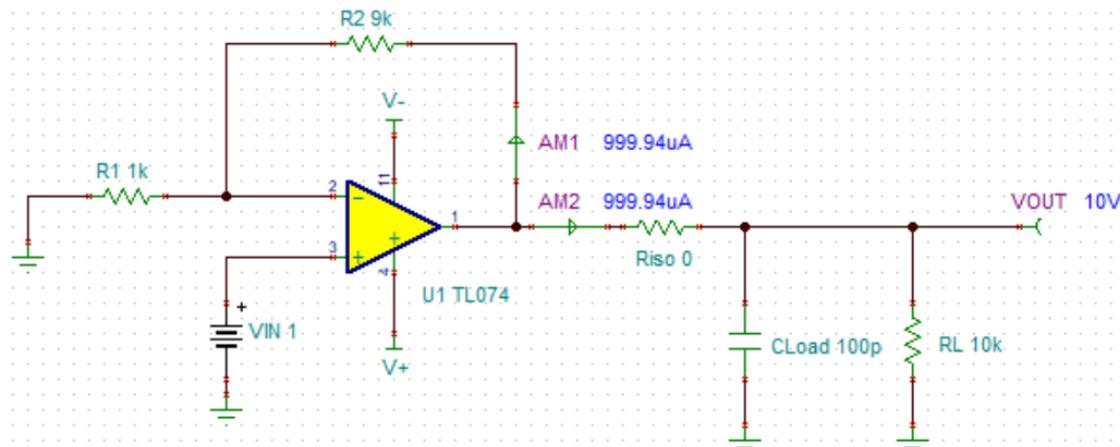
$$P_Q = (V_{pos} - V_{neg}) \cdot I_Q \quad (137) \text{ Total power from quiescent current}$$

$$P_T = P_L + P_Q \quad (138) \text{ Total power dissipated inside the op amp}$$

Non-inverting amplifier maximum power dissipation

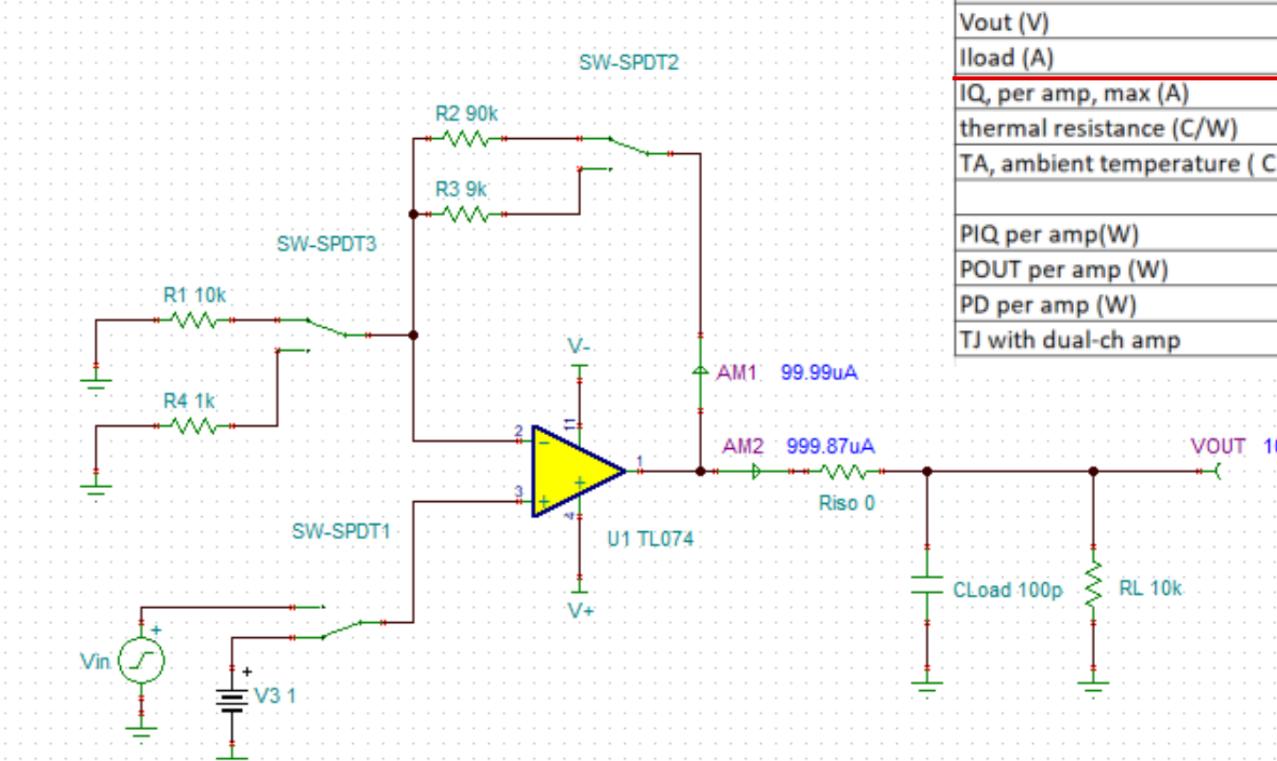
# Junction Temperature Calculation

	TL072 SOIC
V+	15
V-	-15
Vout (V)	10
Iload (A)	2.00E-03
IQ, per amp, max (A)	2.50E-03
thermal resistance (C/W)	97
TA, ambient temperature ( C )	40
PIQ per amp(W)	0.075
POUT per amp (W)	1.00E-02
PD per amp (W)	0.085
TJ with dual-ch amp	56.49



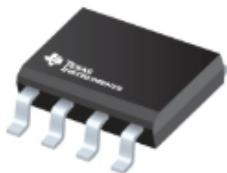
PARAMETER	TEST CONDITIONS <sup>(1) (2)</sup>		MIN	TYP	MAX	UNIT
	V <sub>O</sub> = 0; no load	T <sub>A</sub> = 25°C				
I <sub>cc</sub>	Supply current (each amplifier)	V <sub>O</sub> = 0; no load	T <sub>A</sub> = 25°C	1.4	2.5	mA

# Reduce Heat, Reduce Power, Decrease Output Current



	TL072 SOIC
V+	15
V-	-15
Vout (V)	10
Iload (A)	1.10E-03
IQ, per amp, max (A)	2.50E-03
thermal resistance (C/W)	97
TA, ambient temperature ( C )	40
PIQ per amp(W)	0.075
POUT per amp (W)	5.50E-03
PD per amp (W)	0.0805
TJ with dual-ch amp	55.617

# Reduce Heat, Reduce Power, Decrease Current Consumption



## DATASHEET

TLV930x 40-V, 1-MHz, RRO Operational Amplifiers for Cost-Sensitive Systems datasheet (Rev. A)

[View now](#)

[Download](#)

## Electrical Characteristics (continued)

For  $V_S = (V+) - (V-) = 4.5\text{ V}$  to  $40\text{ V}$  ( $\pm 2.25\text{ V}$  to  $\pm 20\text{ V}$ ) at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$ , unless otherwise noted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>OUTPUT</b>						
Voltage output swing from rail	Positive rail headroom	$V_S = 40\text{ V}$ , $R_L = \text{no load}$	3			mV
		$V_S = 40\text{ V}$ , $R_L = 10\text{ k}\Omega$	50	75		
		$V_S = 40\text{ V}$ , $R_L = 2\text{ k}\Omega$	250	350		
	Negative rail headroom	$V_S = 4.5\text{ V}$ , $R_L = \text{no load}$	1			
		$V_S = 4.5\text{ V}$ , $R_L = 10\text{ k}\Omega$	20	30		
		$V_S = 4.5\text{ V}$ , $R_L = 2\text{ k}\Omega$	40	75		
$I_{SC}$	Short-circuit current			$\pm 60$		mA
$C_{LOAD}$	Capacitive load drive			See <i>Typical Characteristics</i>		
$Z_o$	Open-loop output impedance $f = 1\text{ MHz}$ , $I_O = 0\text{ A}$			600		$\Omega$
<b>POWER SUPPLY</b>						
$I_Q$	Quiescent current per amplifier	$I_Q = 0\text{ A}$		150	175	$\mu\text{A}$
			$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$		175	

	SOIC
V+	15
V-	-15
Vout (V)	10
Iload (A)	1.10E-03
IQ, per amp, max (A)	1.75E-04
thermal resistance (C/W)	97
TA, ambient temperature ( C )	40
PIQ per amp(W)	0.00525
POUT per amp (W)	5.50E-03
PD per amp (W)	0.01075
TJ with dual-ch amp	42.0855

# What else needs to be considered? SR, BW, Spike Signal Capture

TL07x Circuit	
SR = 2 x pi x F x Vout	
F	1.00E+04 Hz
Vout	20 V
SR	1.256 V/us
Topology	Non-inverting
R1	1.00E+04 ohm
R2	9.00E+04 ohm
Noise Gain	10
TL07x Unity Gain Bandwidth	3.00E+06 Hz
Bandwidth	0.3 MHz
0.35 = TR x BW	
BW	0.3 MHz
Signal Rise Time (able to capture)	1.16666667 us
TL07x 13V/us	
TLV930x 3V/us	
TLV930x Unity Gain Bandwidth	1.00E+06 Hz
Bandwidth	0.1 MHz
BW	0.1 MHz
Signal Rise Time (able to capture)	3.5 us

# Op Amp Selection Tips

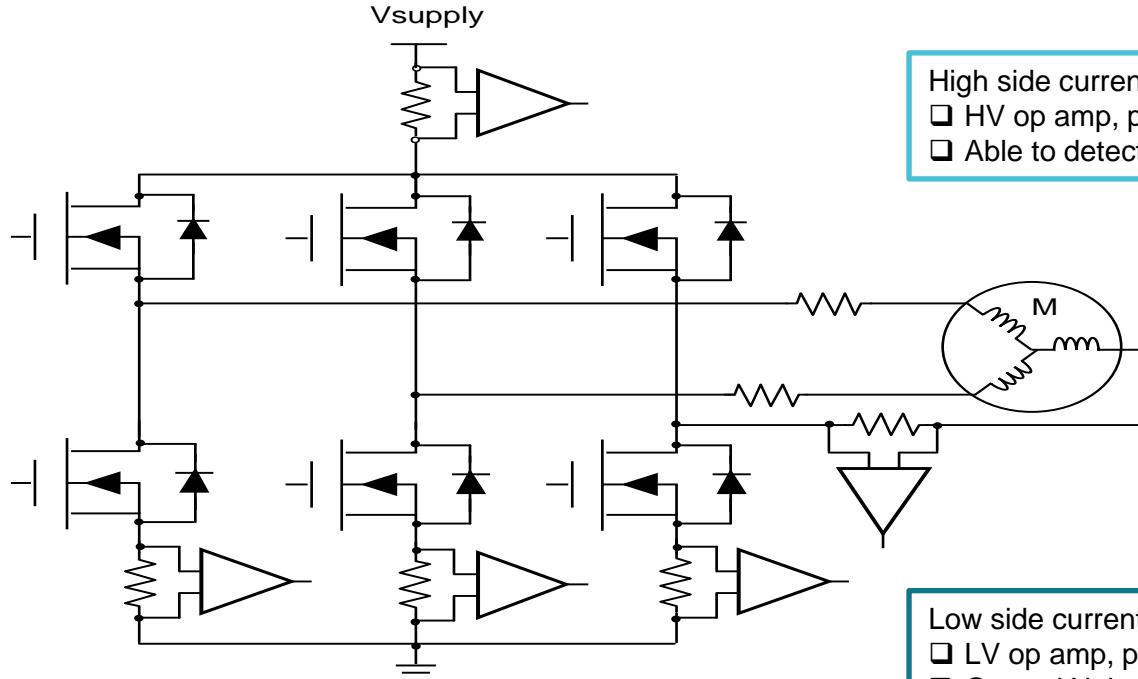
- Considering circuit function and important specs of it:
- Process sine wave/ care synchronization => Small signal latency => GBW
- Use as OCP/ OVP protection function => Large signal response time => Slew Rate
- Light load current monitoring/precision current sensing

Accuracy: Offset, drift, PSRR, CMRR, noise, potential external noise etc.

- AC-coupling cap may be required; differential cap may degrade performance since forming low impedance path for interference
- Surrounding circuits are noisy => EMIRR may help to suppress high frequency noise hence improving accuracy
- Power sources are from DC-DC with switching noise => High PSRR and wide bandwidth may be needed

# High Side Current Sensing Considerations

# High Side and Low Side Current Sensing



High side current sensing:

- ❑ HV op amp, potential higher cost
- ❑ Able to detect load short circuit/leakage

Low side current sensing:

- ❑ LV op amp, potential lower cost
- ❑ Ground Noise, Inaccuracy at light load
- ❑ Not able to detect load short circuit/leakage

# High Side Current Sensing Example

# High Side Current Sensing Circuit Specifications

## Design Goals

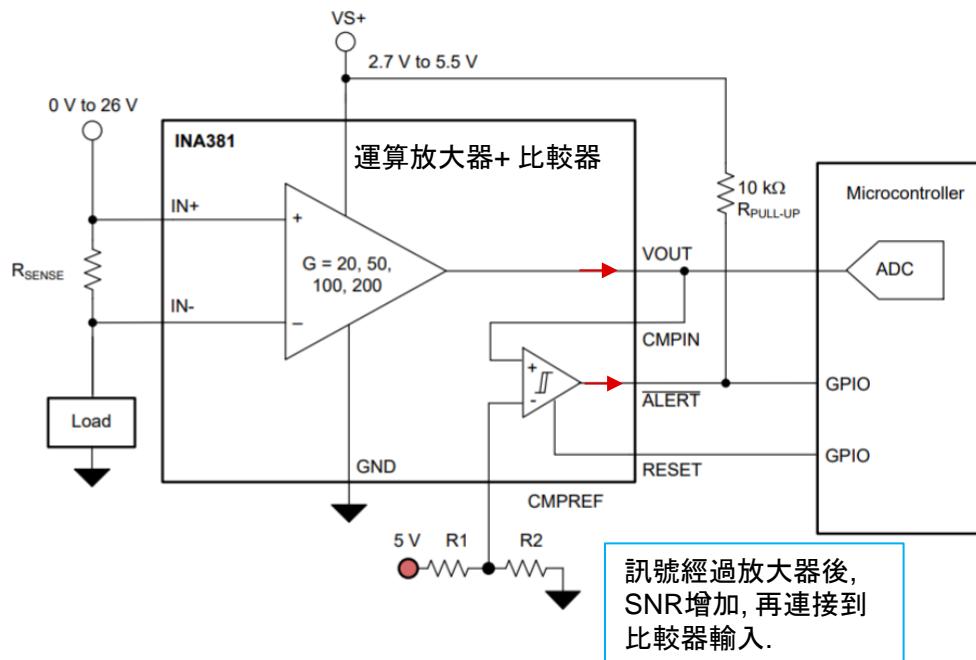
Input		Overcurrent Conditions		Output		Supply	
$I_{load\ Min}$	$I_{load\ Max}$	$I_{OC\_TH}$	$I_{Release\_TH}$	$V_{out\_OC}$	$V_{out\_release}$	$V_S$	$V_{REF}$
1.5A	40A	35A	32A	2.8V	2.61V	3.3V	2.8V

Light Load Accuracy  
@1.5A +/-10%

OCP response time  
10us

Input signal max frequency sine  
10kHz

# INA381 Current Shut Monitor Overview



## 1 Features

- Common-Mode Input Range: -0.2 V to 26 V
- High Accuracy Amplifier:
  - Offset Voltage,  $V_{CM} = 12 \text{ V}$ : 500  $\mu\text{V}$  (Maximum)
  - Offset Voltage,  $V_{CM} = 0 \text{ V}$ : 150  $\mu\text{V}$  (Maximum)
  - Offset Voltage Drift:  $1 \mu\text{V}/^\circ\text{C}$  (Maximum)
  - Gain Error: 1% (Maximum)
  - Gain Error Drift: 20 ppm/ $^\circ\text{C}$  (Maximum)
- Available Amplifier Gains:
  - INA381A1: 20 V/V
  - INA381A2: 50 V/V
  - INA381A3: 100 V/V
  - INA381A4: 200 V/V
- Comparator Specifications:
  - Hysteresis: 50 mV
  - Response Time: 500 ns
  - Alert Threshold Set Through External Reference Voltage
- Open-Drain Comparator Output With Latching Mode
- Package: WSON-8 (2 mm × 2 mm)

350	kHz
210	kHz
150	kHz
105	kHz

# System Specs and INA381 Parameter Rshunt Calculation

Input		Overcurrent Conditions		Output		Supply	
I <sub>load</sub> Min	I <sub>load</sub> Max	I <sub>OC_TH</sub>	I <sub>Release_TH</sub>	V <sub>out_OC</sub>	V <sub>out_release</sub>	V <sub>S</sub>	V <sub>REF</sub>
1.5A	40A	35A	32A	2.8V	2.61V	3.3V	2.8V

Rshunt Calculation: Highest SNR

$$V_{out\_max} = I_{max} \times R_{shunt} \times Gain$$

$$R_{shunt} = \frac{V_{out\_max}}{gain \times I_{max}} = \frac{V_S - 0.02V}{gain \times I_{max}} = \frac{3.3V - 0.02V}{20V/V \times 40A} = 0.0041\Omega \quad R_{max}$$

$$R_{standard \ shunt} = 4m\Omega \text{ (standard 1% value)}$$

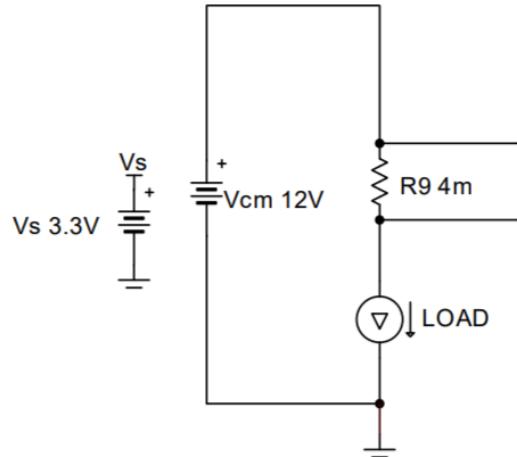
Considering power loss:

$$12V \times 40A = 480W$$

$$480W \times 0.1\% = 0.48W$$

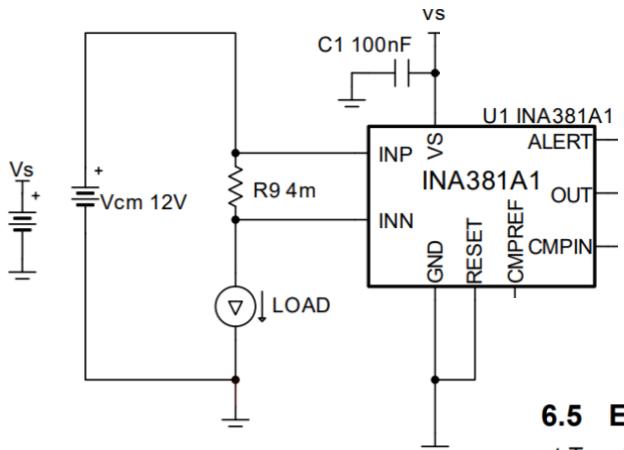
$$0.48W = I^2R$$

$$R = 0.48/1600 = 0.3m\text{-ohm}$$



# System Specs and INA381 Parameter Offset Voltage and Drift

Input		Overcurrent Conditions		Output		Supply	
I <sub>load</sub> Min	I <sub>load</sub> Max	I <sub>OC_TH</sub>	I <sub>Release_TH</sub>	V <sub>out_OC</sub>	V <sub>out_release</sub>	V <sub>S</sub>	V <sub>REF</sub>
1.5A	40A	35A	32A	2.8V	2.61V	3.3V	2.8V



Light Load Accuracy @ 1.5A +/-10%:

$$V_{sense} = I_{min} \times R_{sense}$$

$$V_{sense} = 1.5A \times 4m\text{-ohm}$$

$$V_{sense} = 6mV$$

$$\begin{aligned} \text{Allowable Error} &= 6m\text{-ohm} \times +/-10\% \\ &= +/-600\mu V \end{aligned}$$

Drift calculation

Max ambient temperature 45C

Vos\_Drift

$$= 1\mu V/C \times (\Delta T)$$

$$= 1\mu V/C \times (45-25)$$

$$= 20\mu V$$

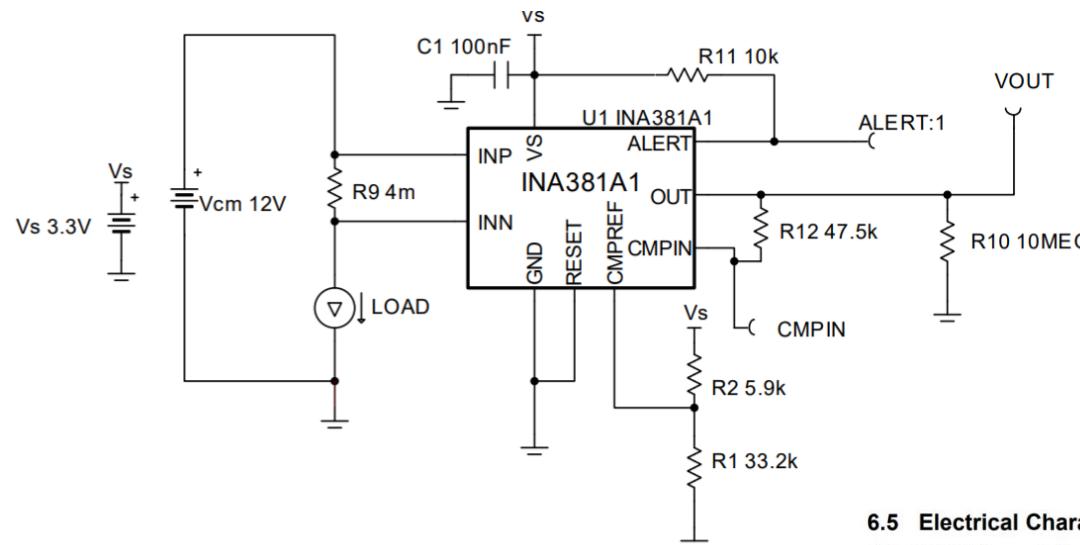
## 6.5 Electrical Characteristics

at  $T_A = 25^\circ C$ ,  $V_{SENSE} = V_{IN+} - V_{IN-} = 10 \text{ mV}$ ,  $V_S = 5 \text{ V}$ ,  $V_{IN+} = 12 \text{ V}$ , and  $CMPREF = 2 \text{ V}$ , (unless otherwise noted.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>INPUT</b>					
$V_{CM}$	Common-mode input voltage range	-0.2	26	26	V
CMRR	Common-mode rejection ratio, RTI	84	100	100	dB
$V_{os}$	Offset voltage, RTI <sup>(1)</sup>	$\pm 100$	$\pm 500$	$\pm 500$	$\mu V$
		$\pm 25$	$\pm 150$	$\pm 150$	$\mu V$
$dV_{os}/dT$	Offset voltage drift, RTI <sup>(1)</sup>	0.1	1	1	$\mu V/\text{C}$

# System Specs and INA381 Parameter Slew Rate and Bandwidth

Input		Overcurrent Conditions		Output		Supply	
I <sub>load</sub> Min	I <sub>load</sub> Max	I <sub>OC_TH</sub>	I <sub>Release_TH</sub>	V <sub>out_OC</sub>	V <sub>out_release</sub>	V <sub>S</sub>	V <sub>REF</sub>
1.5A	40A	35A	32A	2.8V	2.61V	3.3V	2.8V



Slew Rate Requirement:

$$V_{out\_35A} = I_{OC\_TH} \times R_{standard \ shunt} \times \text{gain}$$

$$= 35A \times 4m\Omega \times 20V/V = 2.8V$$

OCP response time  
10us

Slew Rate  
= Vout\_max/ time  
= 2.8V/ 10us  
= 0.28V/us

Fin max  
10kHz

## 6.5 Electrical Characteristics

at T<sub>A</sub> = 25°C, V<sub>SENSE</sub> = V<sub>IN+</sub> - V<sub>IN-</sub> = 10 mV, V<sub>S</sub> = 5 V, V<sub>IN+</sub> = 12 V, and CMPREF = 2 V, (unless otherwise noted.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>FREQUENCY RESPONSE</b>					
BW	Bandwidth	INA381A1	350		kHz
		INA381A2	210		kHz
		INA381A3	150		kHz
		INA381A4	105		kHz
SR	Slew rate		2		V/μs

# High Side Current Sensing Circuit Specifications

## Design Goals

Input		Overcurrent Conditions		Output		Supply	
I <sub>load</sub> Min	I <sub>load</sub> Max	I <sub>OC_TH</sub>	I <sub>Release_TH</sub>	V <sub>out_OC</sub>	V <sub>out_release</sub>	V <sub>S</sub>	V <sub>REF</sub>
1.5A	40A	35A	32A	2.8V	2.61V	3.3V	2.8V

Light Load Accuracy  
@1.5A +/-10%

Allowable Error :  
 $4\text{m-}\Omega \times 1.5\text{A} \times$   
+/-10% = +/-600uV

0.25m- $\Omega$  x 1.5A x  
+/-10% = +/-37.5uV

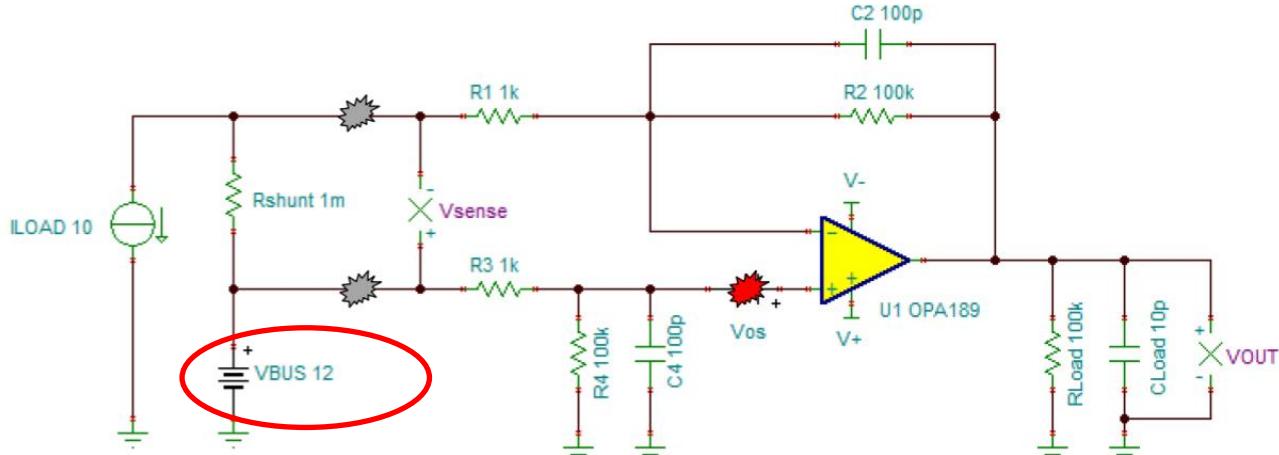
OCP response time  
10us

Slew Rate  
= V<sub>out\_max</sub> / time  
= 2.8V / 10us  
= 0.28V/us

Input Signal max frequency sine  
10kHz

Slew Rate (SR)  
Full power Bandwidth  
 $SR = 2 \times \pi \times F \times V_{pp}$   
 $SR = 2 \times 3.14 \times 10\text{kHz} \times 2.8$   
 $SR = 0.176\text{V/us}$

# Current Sensing Error Sources



Shunt Resistor  
Tolerance

Trace  
Resistance

Op Amp Input Offset  
Voltage(Vos) Correlated:

- Vos at Room Temperature 25C
- Vos\_Drift
- Vos\_CMRR\_DC
- Vos\_CMRR\_AC
- vos\_PSRR\_DC
- Vos\_PSRR\_AC
- Bias Current

Noise

- Extrinsic Noise
- Intrinsic Noise

24

27

# VCM 12V Ripple and FFT



~7.3mV ~4.1mV  
50kHz 100kHz

~4.1mV  
280kHz

~4.1mV ~0.13mV  
460kHz 570kHz  
~4.1mV  
520kHz

~0.13mV ~4.1mV ~13mV  
860kHz 920kHz 970kHz

12V supply  
AC coupling mode



TEXAS INSTRUMENTS

# System Specs and INA381 Parameter CMRR AC



INA381

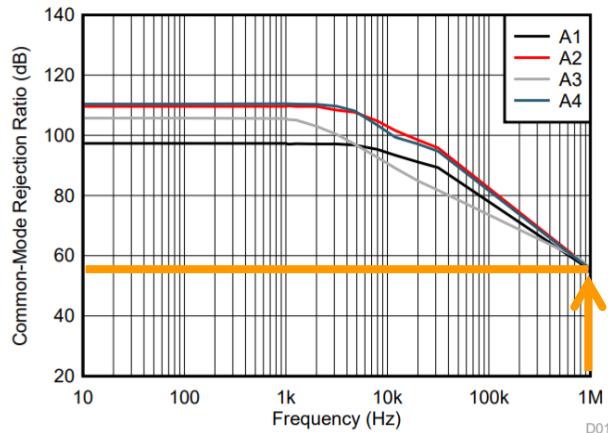
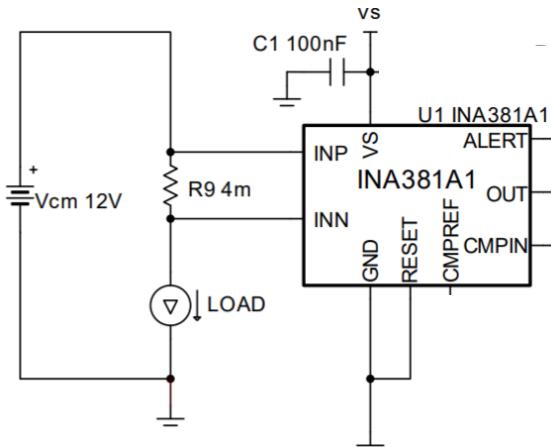
www.ti.com

SBOS848A –DECEMBER 2017–REVISED APRIL 2018

## 6.5 Electrical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_{SENSE} = V_{IN+} - V_{IN-} = 10 \text{ mV}$ ,  $V_S = 5 \text{ V}$ ,  $V_{IN+} = 12 \text{ V}$ , and  $CMPREF = 2 \text{ V}$ , (unless otherwise noted.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>INPUT</b>					
$V_{CM}$	Common-mode input voltage range	-0.2	26	26	V
CMRR	Common-mode rejection ratio, RTI $V_{IN+} = 0 \text{ V}$ to $26 \text{ V}$ , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	84	100	100	dB



- A1 CMRR is ~55dB@1MHz at 25-C.
- It has 1.78mV/V attenuation capability to the common mode noise.
- $V_{OS\_CMRR\_AC} = 13\text{mV} \times 1.78\text{mV} = 23.14\mu\text{V}$

# To see more circuit detail analysis:

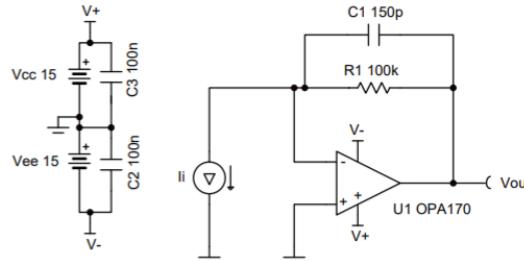
## *Transimpedance amplifier circuit*

### Design Goals

Input		Output		BW	Supply	
$I_{\text{Min}}$	$I_{\text{Max}}$	$V_{\text{oMin}}$	$V_{\text{oMax}}$	$f_p$	$V_{\text{cc}}$	$V_{\text{ee}}$
0A	50 $\mu$ A	0V	5V	10kHz	15V	-15V

### Design Description

The transimpedance op amp circuit configuration converts an input current source into an output voltage. The current to voltage gain is based on the feedback resistance. The circuit is able to maintain a constant voltage bias across the input source as the input current changes which benefits many sensors.

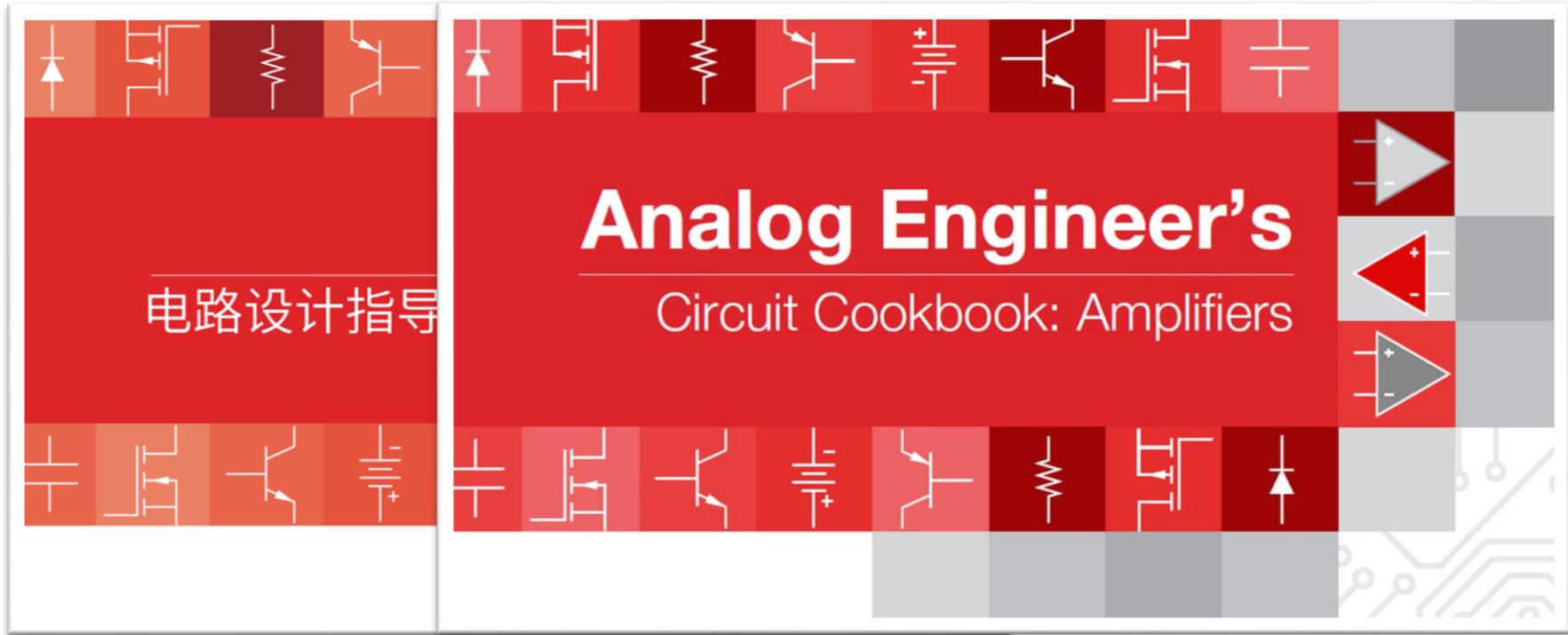


Copyright © 2018, Texas Instruments Incorporated

### Design Notes

1. Use a JFET or CMOS input op amp with low bias current to reduce DC errors.
2. A bias voltage can be added to the non-inverting input to set the output voltage for 0-A input currents.
3. Operate within the linear output voltage swing (see  $A_{\text{cl}}$  specification) to minimize non-linearity errors.

# 類比工程師 電路設計指導手冊



<https://www.ti.com/seclit/sl/zhcy082a/zhcy082a.pdf>

<https://www.ti.com/seclit/sl/slyy137a/slyy137a.pdf>

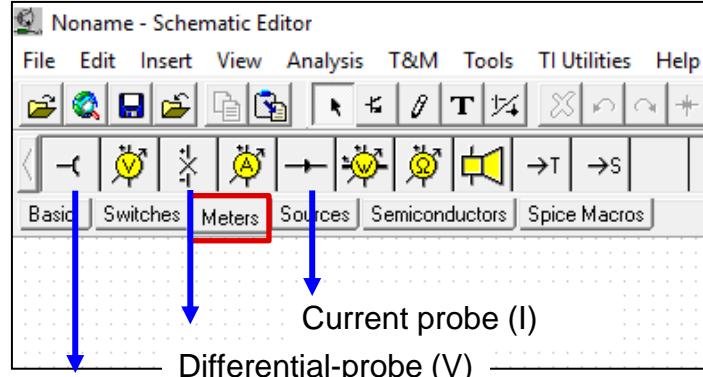
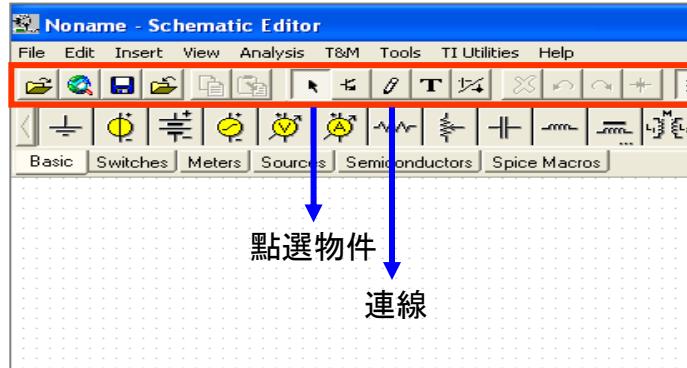
# Introduction to TINA-TI Simulations

## OPA189 Circuit

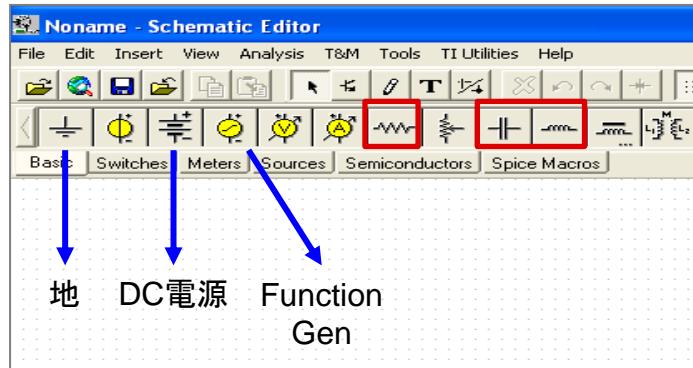


TEXAS INSTRUMENTS

# TINA-TI Editor/Tool Bar



Single-ended probe (V)



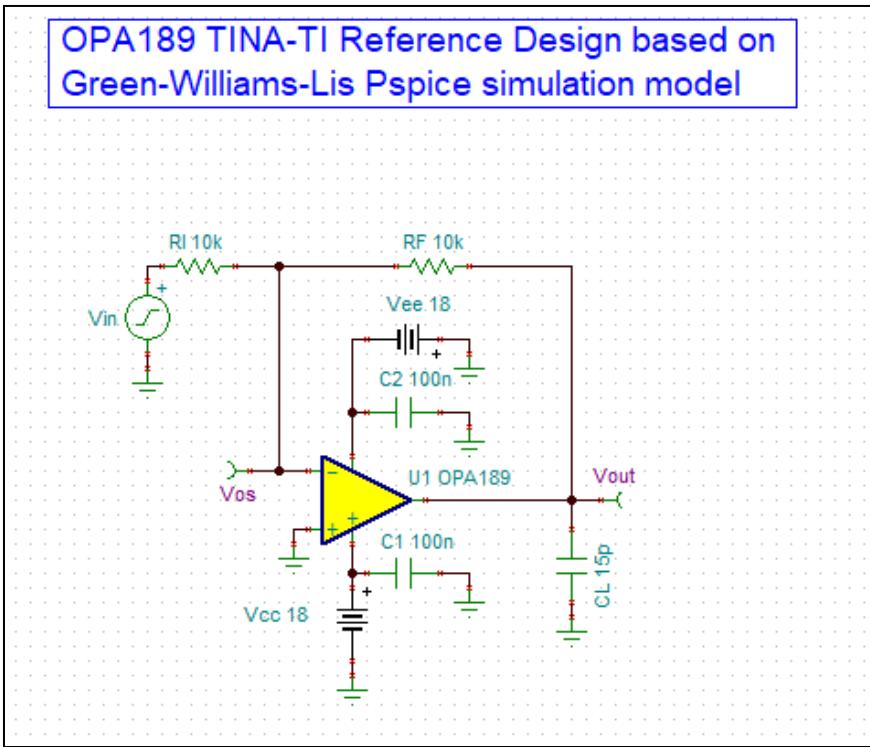
# DC, Transient, and AC Simulation

# Performing Analysis with TINA-TI

Case Study: OPA189 Circuit from TINA Reference Design

- Running DC Analysis
- Running AC Analysis
- Running Transient Analysis

# Simulate OPA189 with a 1 uF load



# TINA Model 模擬參數

OPA189(ACTIVE)

14MHz, MUX-friendly, low-noise, zero-drift, RRO, CMOS precision operational amplifier

In English ▾ Alert me



## DATASHEET

OPAx189 Precision, Lowest-Noise 36-V, Zero-Drift, 14-MHz MUX-Friendly, Rail-to-Rail Output, Operational Amplifiers datasheet (Rev. E)

[View now](#) [Download](#)

Description & parametrics

Technical documents

Design & development

Order now

Quality & packaging

Supp

[Models](#) | [Design kits & evaluation modules](#) | [TI Designs & reference designs](#) | [Software](#) | [Development tools](#) | [TI design](#)

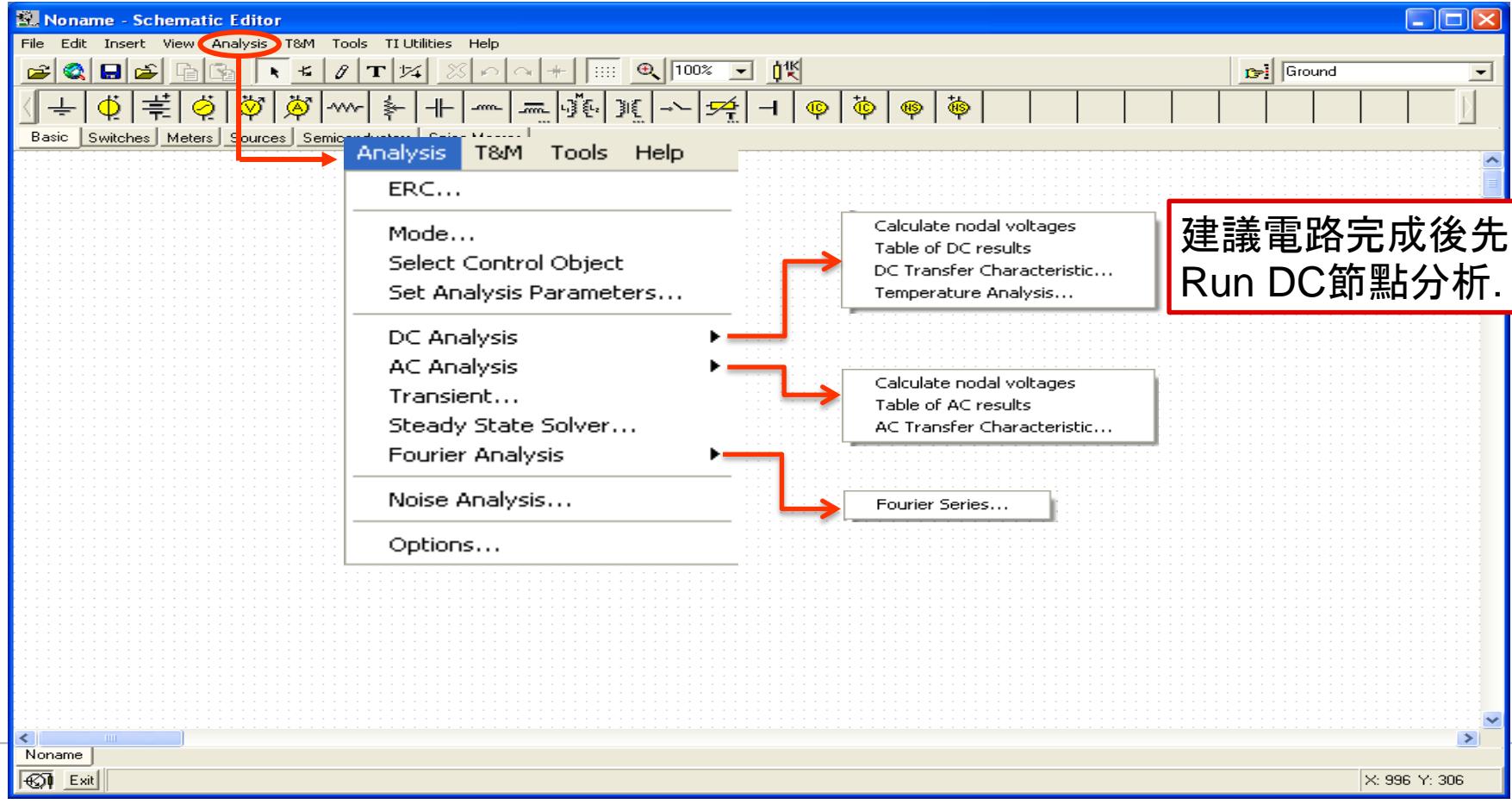
## Models (3)

Title	Category	Type	Date
<a href="#">OPA189 PSpice Model (Rev. C)</a>	PSpice Model	ZIP	27 Feb 2019
<a href="#">OPA189 TINA-TI Reference Design (Rev. C)</a>	TINA-TI Reference Design	TSC	27 Feb 2019
<a href="#">OPA189 TINA-TI Spice Model (Rev. D)</a>	TINA-TI Spice Model	ZIP	27 Feb 2019

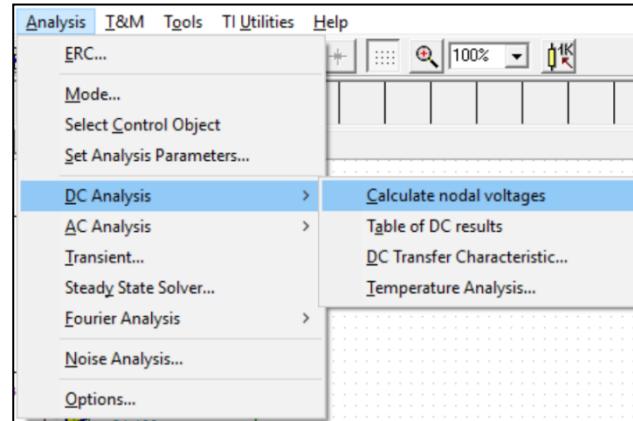
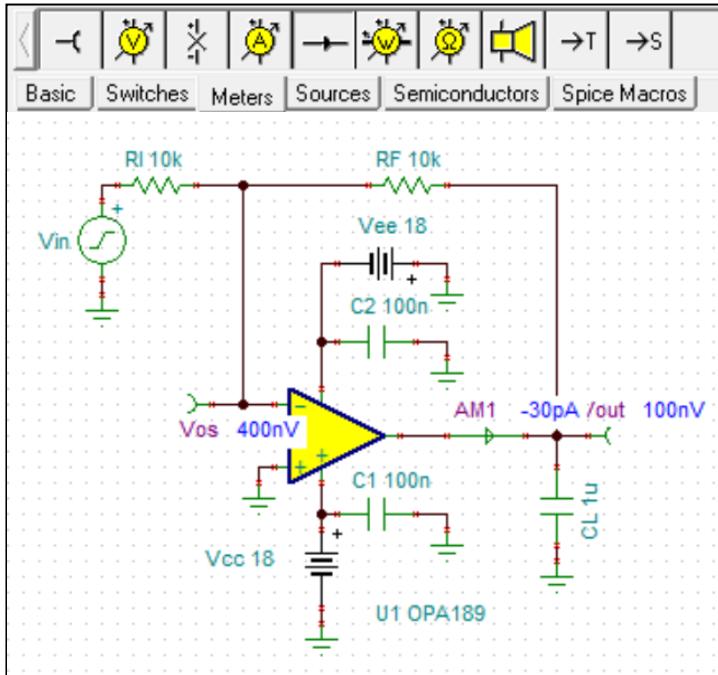
\*\*\*\*\*  
\*  
\*\* Released by: Online Design Tools, Texas Instruments Inc.  
\* Part: OPA189  
\* Date: 04FEB2019  
\* Model Type: Generic (suitable for all analysis types)  
\* EVM Order Number: N/A  
\* EVM Users Guide: N/A  
\* Datasheet: SBOS830D DECEMBER 2017 REVISED DECEMBER 2018  
\* Created with Green-Williams-Lis Op Amp Macro-model Architecture  
\*  
\* Model Version: Final 1.0  
\*\*\*\*\*  
OPEN-LOOP GAIN AND PHASE VS. FREQUENCY WITH RL, CL EFFECTS (Aol)  
UNITY GAIN BANDWIDTH (GBW)  
INPUT COMMON-MODE REJECTION RATIO VS. FREQUENCY (CMRR)  
POWER SUPPLY REJECTION RATIO VS. FREQUENCY (PSRR)  
DIFFERENTIAL INPUT IMPEDANCE (Zid)  
COMMON-MODE INPUT IMPEDANCE (Zic)  
OPEN-LOOP OUTPUT IMPEDANCE VS. FREQUENCY (Zo)  
OUTPUT CURRENT THROUGH THE SUPPLY (Iout)  
INPUT VOLTAGE NOISE DENSITY VS. FREQUENCY (en)  
INPUT CURRENT NOISE DENSITY VS. FREQUENCY (in)  
OUTPUT VOLTAGE SWING vs. OUTPUT CURRENT (Vo)  
SHORT-CIRCUIT OUTPUT CURRENT (Isc)  
QUIESCENT CURRENT (Iq)  
SETTLING TIME VS. CAPACITIVE LOAD (ts)  
SLEW RATE (SR)  
SMALL SIGNAL OVERSHOOT VS. CAPACITIVE LOAD  
LARGE SIGNAL RESPONSE  
OVERLOAD RECOVERY TIME (tor)  
INPUT BIAS CURRENT (Ib)  
INPUT OFFSET CURRENT (Ios)  
INPUT OFFSET VOLTAGE (Vos)  
INPUT OFFSET VOLTAGE VS. TEMPERATURE (Vos Drift)  
INPUT COMMON-MODE VOLTAGE RANGE (Vcm)  
INPUT OFFSET VOLTAGE VS. INPUT COMMON-MODE VOLTAGE (Vos vs. Vcm)  
INPUT/OUTPUT ESD CELLS (ESDin, ESDout)  
\*\*\*\*\*



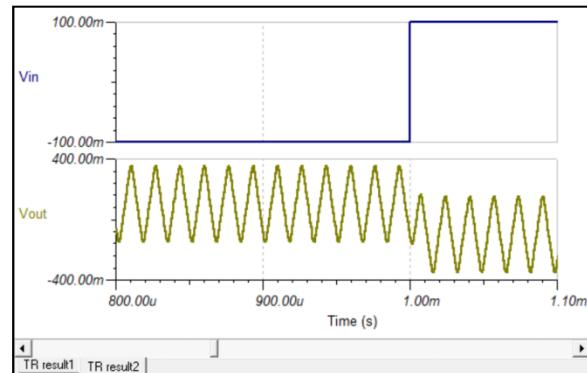
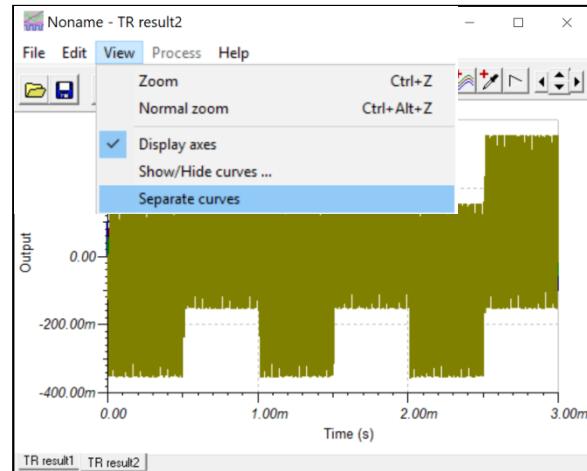
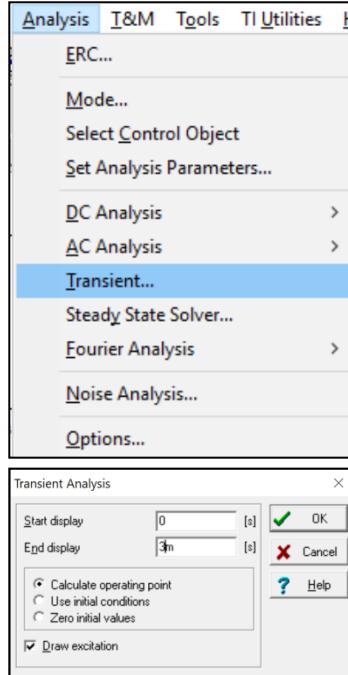
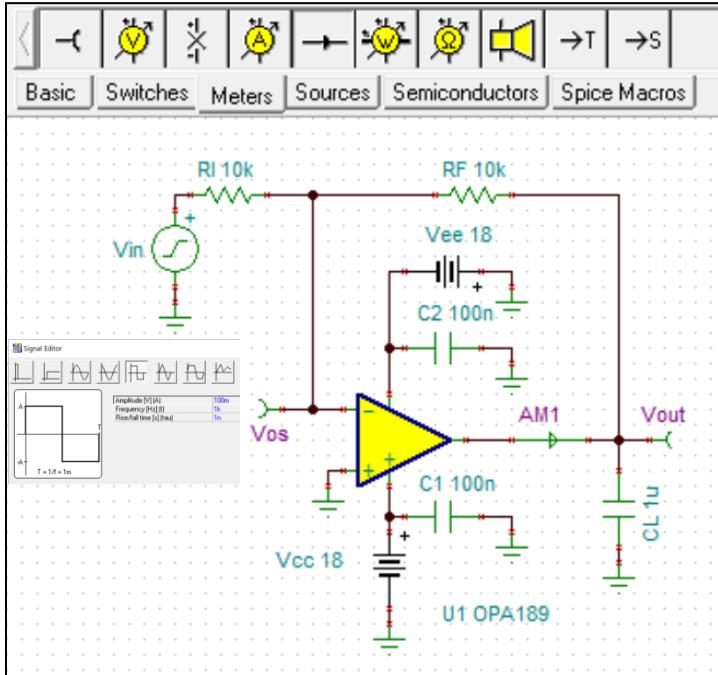
# TINA-TI Schematic Editor Tour



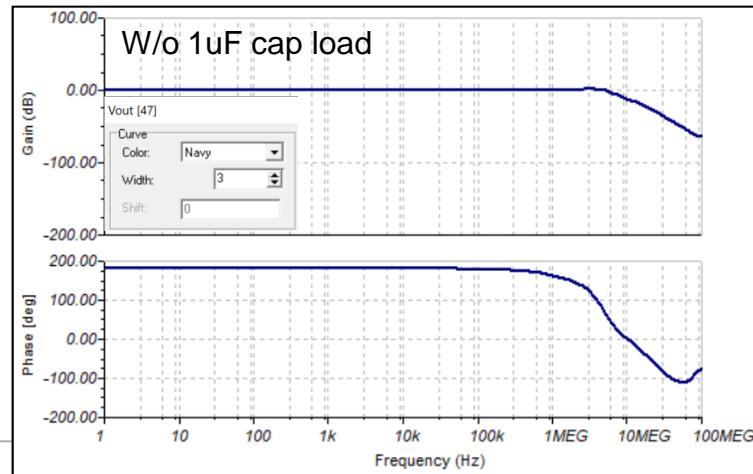
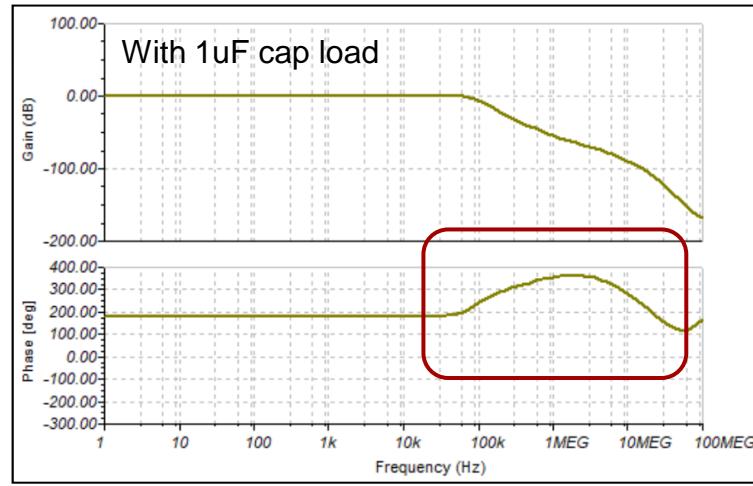
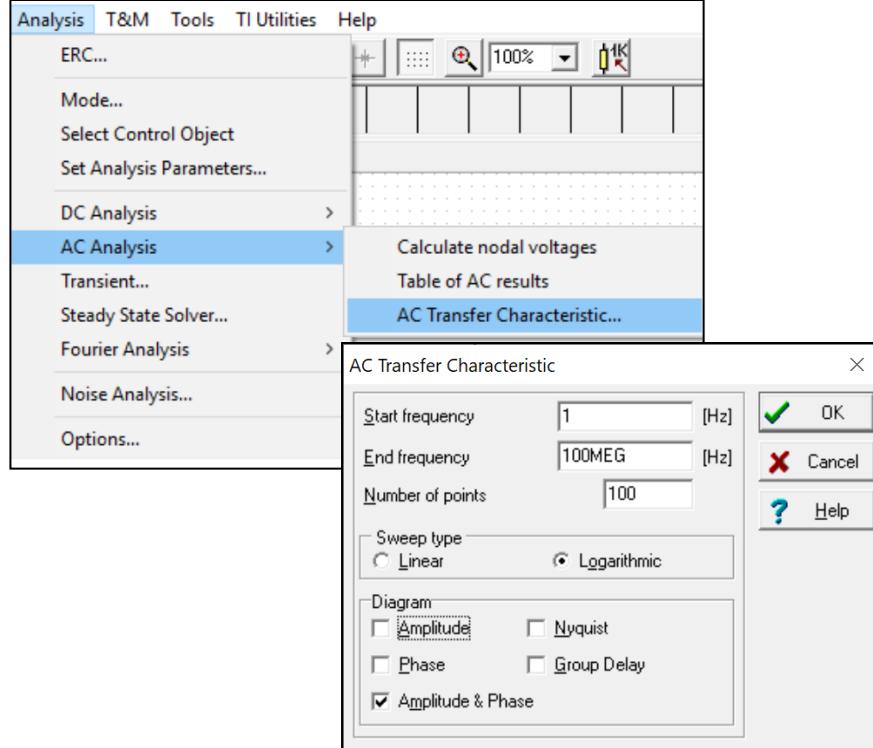
# DC Nodal Analysis



# Transient Analysis

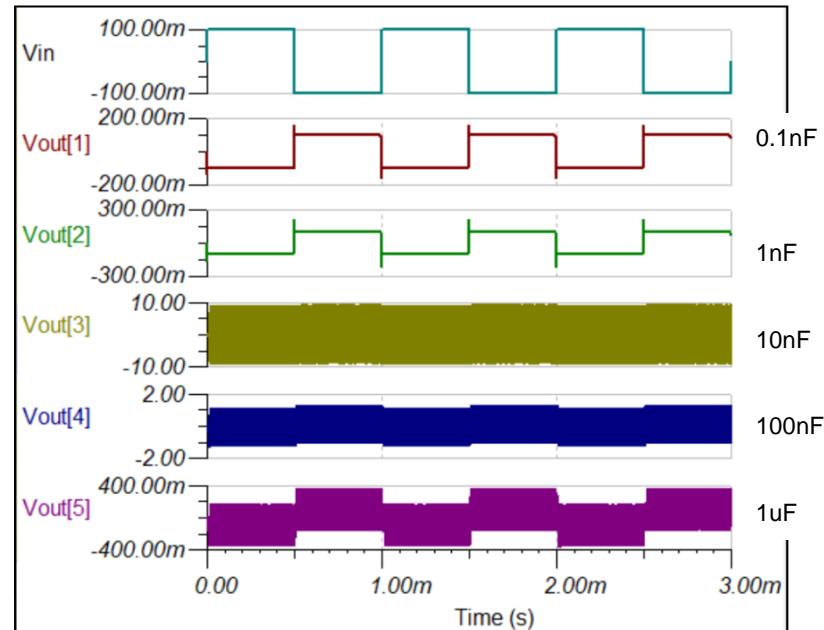
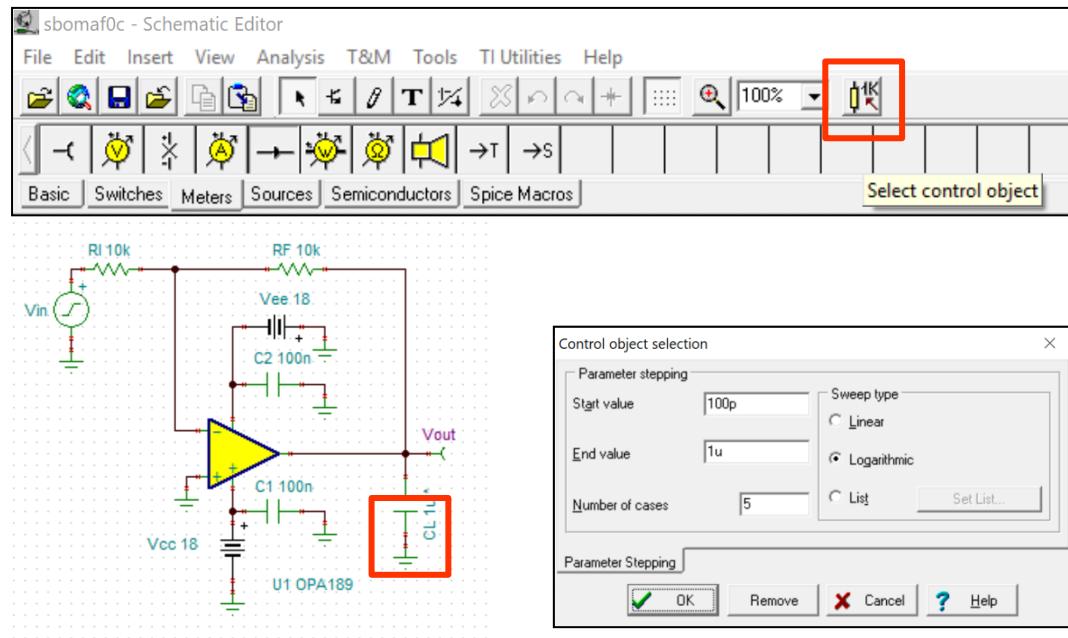


# AC Analysis

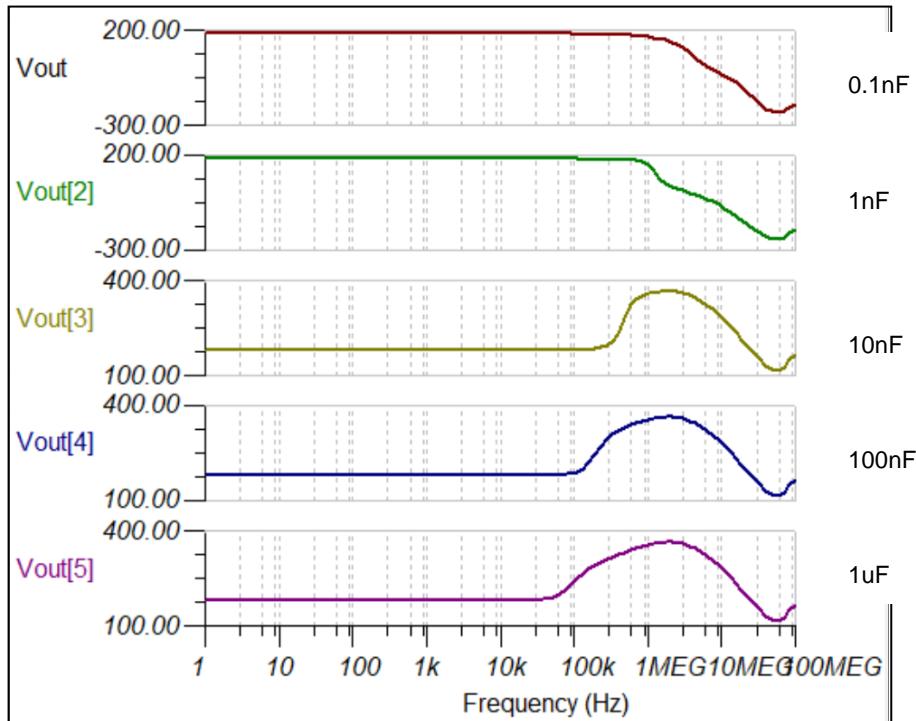
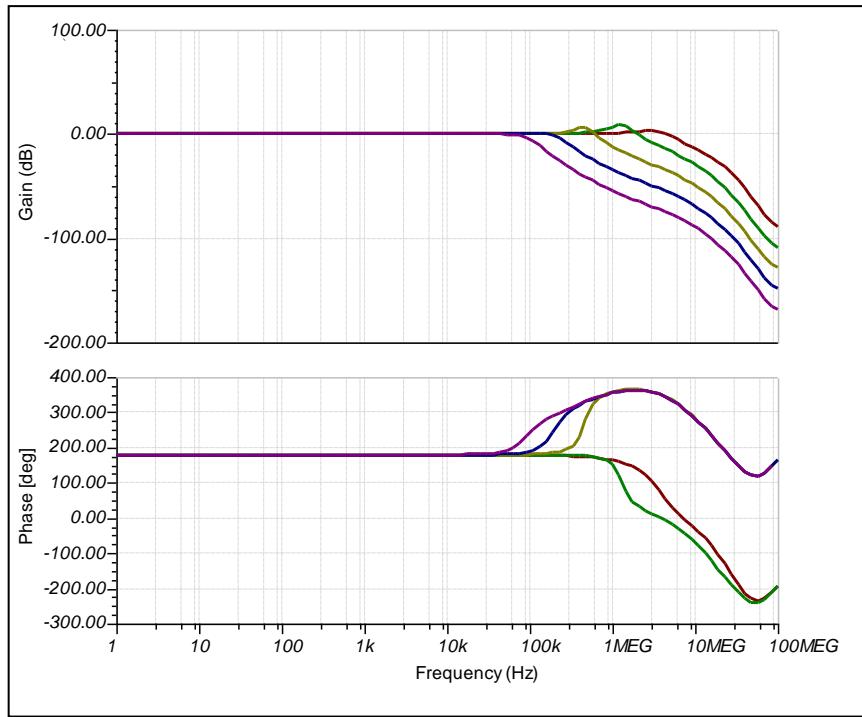


# Parameter-stepping

# Parameter-stepping – Transient Analysis



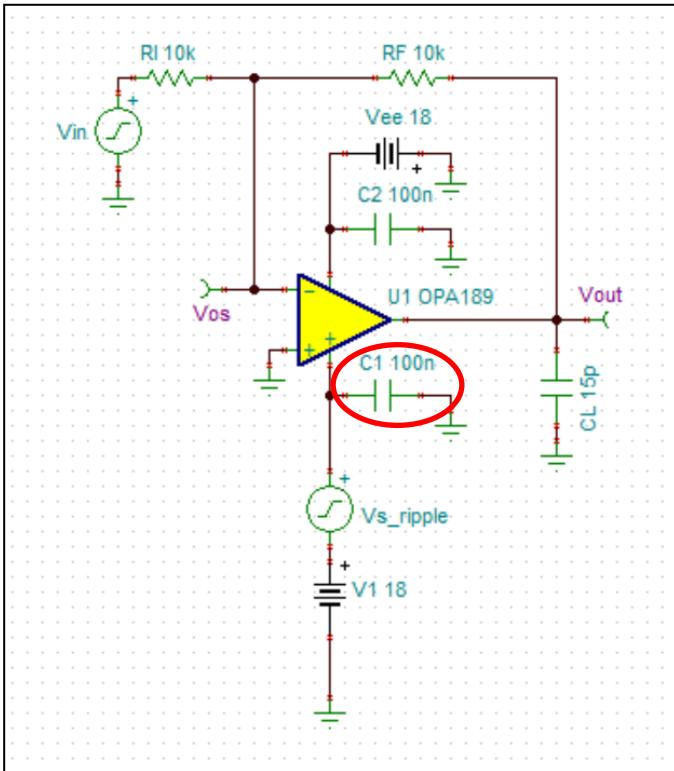
# Parameter-stepping – AC Analysis



# TINA Tips



# Supply Noise and Decoupling Cap



PSRR at high frequency:  
assume  $10mVpp$  ripple:  
 $40dB \Rightarrow 10mV/V \Rightarrow 0.1mV$  ( $V_{os\_PSRR}$ )  
 $20dB \Rightarrow 100mV/V = 1mV$   
 $10dB \Rightarrow 316mV/V \Rightarrow 3.16mV$

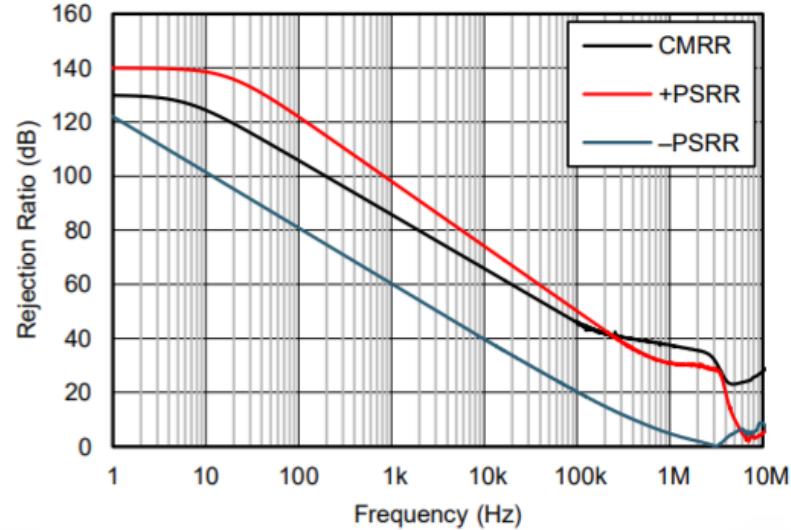


Figure 14. CMRR and PSRR vs Frequency

# Put Real Capacitor in TINA

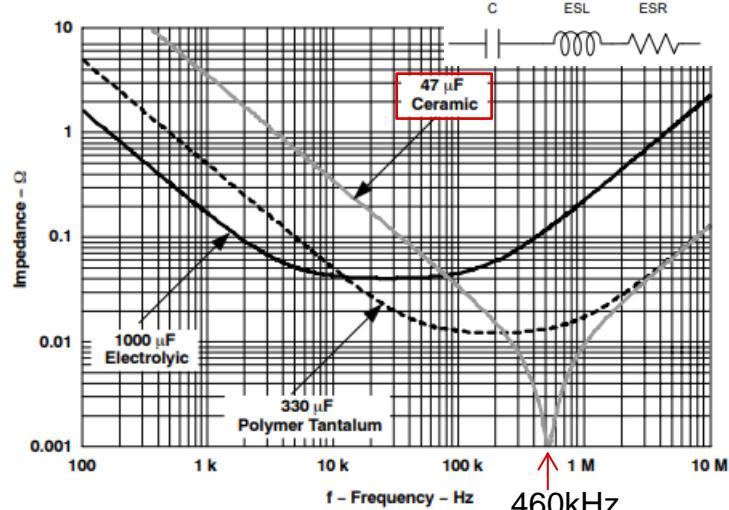
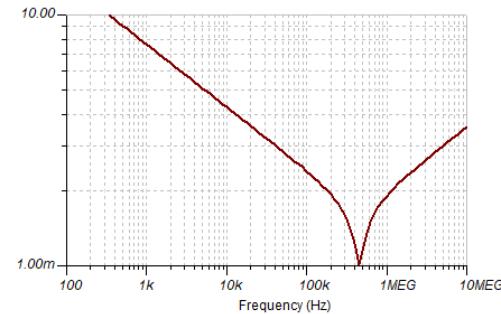
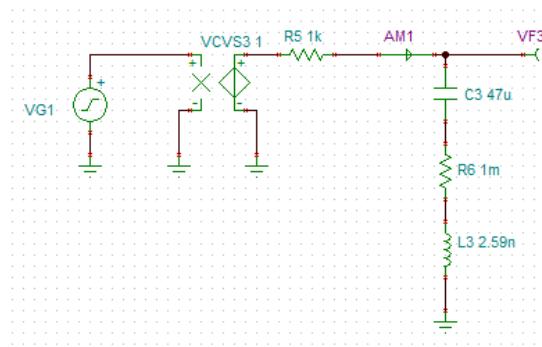


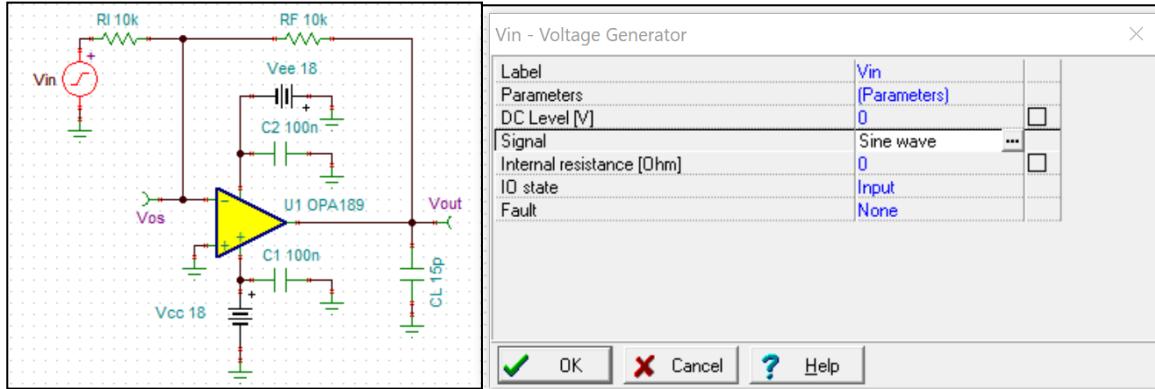
Figure 4. Capacitor Impedance Characteristics

$f = 1/(2 \times \pi \times \sqrt{LC})$	
$L = 1/(2 \times \pi \times f \times C)$	
$f$	4.60E+05 Hz
$C$	4.70E-05 F
$L$	2.549571 nH



C Simulation 2.TSC

# Function Generator



# Error – Irregular Circuit

The screenshot shows a complex electronic circuit being analyzed in TINA software. The circuit includes two operational amplifiers (U1 OPA192 and U2 OPA192), various resistors (R1 to R8), capacitors (C1 to C3), and voltage sources (VG1, VG2, V1, V2, V3). A Texas Instruments Z1 IN2004 diode is also present. On the right side of the interface, an 'Error' dialog box is open, displaying the message "Irregular circuit." with "OK" and "Help" buttons. Below the dialog, status messages say "Current of component: V1" and "Current of component: V2". In the foreground, a help window titled "TINA Help" is open, showing search results for "Irregular circuit". The results explain that this error occurs when TINA cannot solve the circuit equations due to contradictions in the circuit topology. It provides a simple example involving a shorted voltage source or an open current source.

**TINA Help**

Index | Search |  
Type in the keyword to find:  
About  
AC Analysis  
AC Table  
AC Transfer  
Add new X axis  
Add new Y axis  
Advanced VHDL / MCU Options

**Irregular circuit**

This error message means that TINA could not solve the circuit equations, probably due to a irregular (contradictory) feature of the circuit.

A simple example of a irregular circuit is a circuit containing a shorted voltage source or an open current source. These circuits have a topology that contradicts the definition of the parts, resulting in unsolvable equations (system of linear equations with a zero determinant).

# Error – Convergence Problem

The screenshot shows a circuit simulation environment with three main windows:

- Schematic Editor:** Displays a complex circuit diagram for an operational amplifier (OPA192) configured as a sin/cos converter. The circuit includes various resistors (R1 to R17, R21 to R24), capacitors (C1 to C7), and a THS4551\_GWL op-amp. A red box highlights a warning message: "Convergence problem. Check the analysis parameters!"
- Analysis Parameters:** A dialog box showing the current analysis settings. Key parameters include:
  - TR max. iteration number [-] (20)
  - TR max. abs. voltage incr. [V] (200m)
  - TR max. abs. current incr. [A] (20m)
  - TR max. relative increment [%] (1.0E+30)
  - TR maximum value relative error [%] (1m)
  - TR LTE voltage-based/charge-based (Yes)
  - TR truncation error factor [-] (7)
  - TR iteration control factor [-] (500m)
  - TR charge tolerance (10f)
  - TR maximum time step [s] (10G)
  - TR minimum time step [s] (1.0E-30)
  - TR excitation subdivisions [-] (10)
  - TR time intrv. subdivisions [-] (100)
  - Abs. error of optimization [-] (1n)
  - Rel. error of optimization [%] (1u)
  - Semiconductor capacitors enabled (Yes)
  - Shunt conductance [S] (0)
  - Shunt capacitance [F] (0)
  - Max. no. of saved TR points [-] (1000000)
  - Wave processing quality (1-4) (1)
  - Audio latency [s] (500m)
- Plot Window:** Shows a graph of multiple waveforms over time, with a progress bar indicating the calculation is at 67% completion.

# TINA-TI Training Videos

Right-Click the desired line and select *Open Hyperlink*.

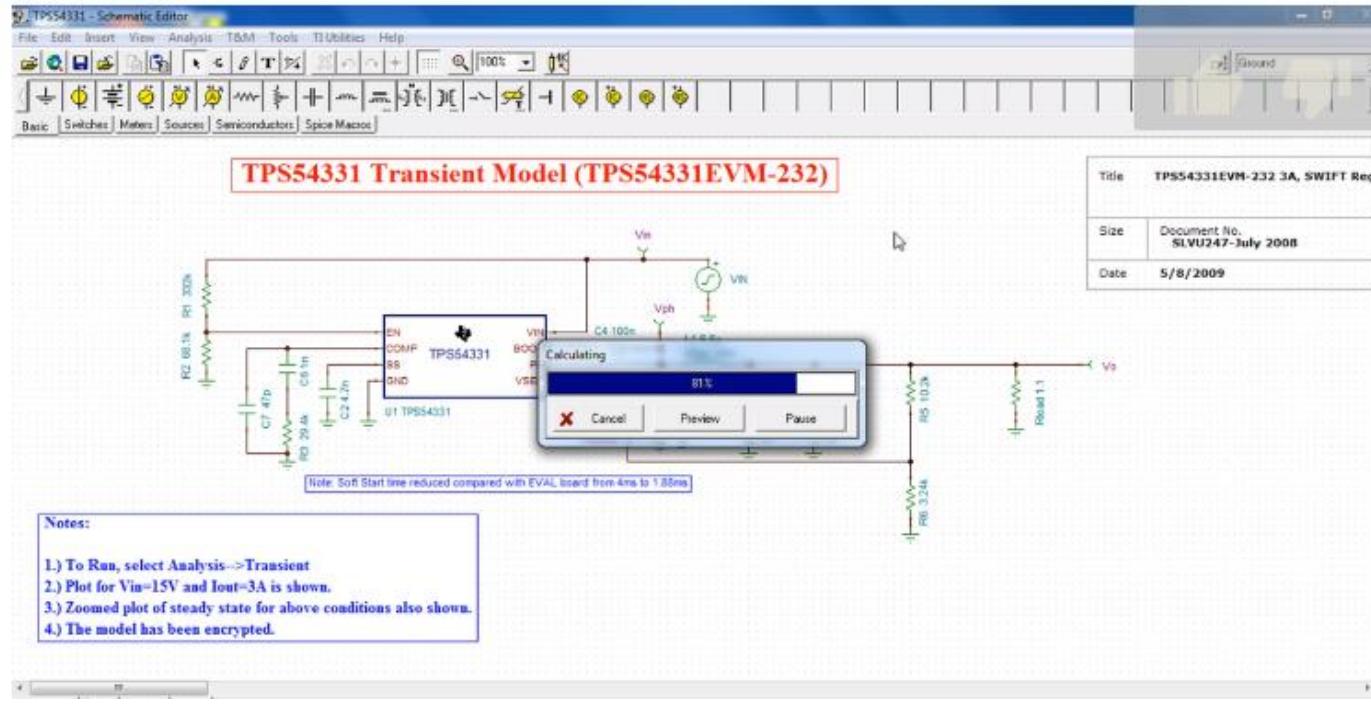
- [Introduction to TINA-TI](#)
- [Using the TINA-TI simulator – ERC and Analysis types](#)
- [Configuring Sources in TINA-TI simulator](#)
- [TINA-TI Waveform Viewer, Part 1](#)
- [TINA-TI Waveform Viewer, Part 2](#)
- [Sweeping parameters in TINA-TI simulator](#)
- [Noise, Fourier analysis and Signal Chain content in TINA-TI](#)
- [Power product simulation in TINA-TI simulator](#)
- [Importing SPICE models into TINA-TI](#)
- [Tips and Tricks for TINA-TI simulator](#)
- [How to use the Controlled Source Wizard in the TINA-TI simulator](#)
- [Using WEBENCH® simulation export to create files for TINA-TI simulator](#)
- <https://training.ti.com/tina-ti-video-training-series>

# TI Training & Videos

- Tips and Tricks for TINA-TI simulator

## 1.10 Tips and Tricks for TINA-TI(TM) simulator

Email



# Summary

- Op Amp in Over Current Protection Circuit
  - Output swing limitation
  - Input ESD steering diodes
- Improve Thermal Performance Op Amp Circuit
  - Power Dissipation Calculation
  - Thermal Impedance and Junction Temperature
  - Consider Protection Response Time, Signal Latency, Spike Signal Rise Time
- Amplifier Major Parameters in Current Sensing Application
  - High Side Current Sensing Circuit Specifications
  - Rshunt Calculation
  - Offset Voltage and Drift
  - Slew Rate and Bandwidth
  - CMRR AC
- TINA Tutorial

**Thank you.**