

# PLL Building Blocks Part 2

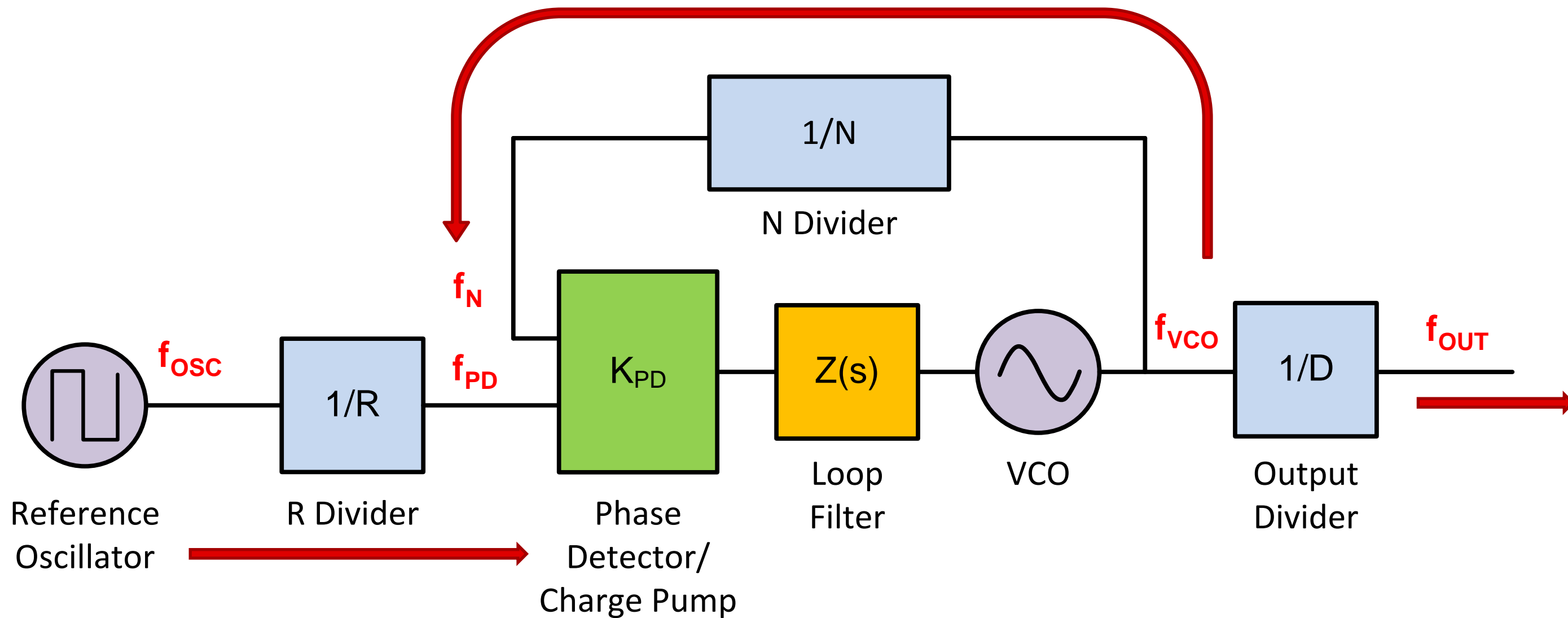
TI Precision Labs – Clocks and Timing

Presented by Dean Banerjee

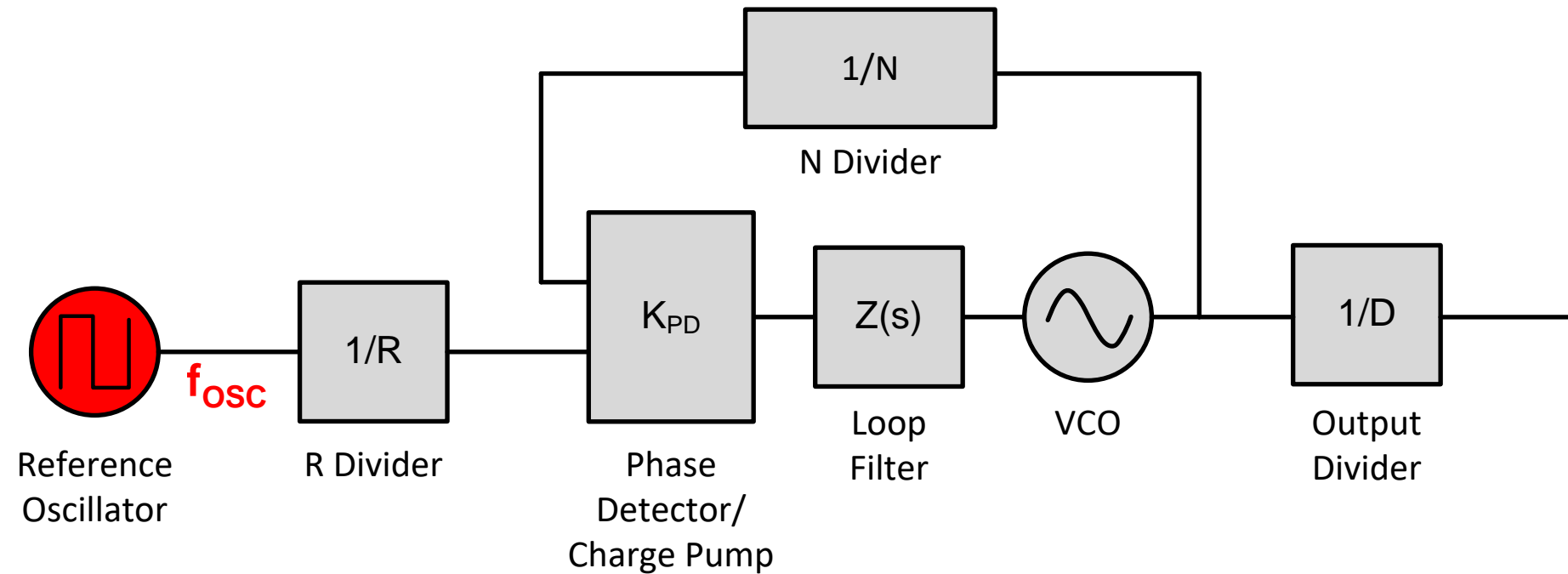
Prepared by Liam Keese



# Phase lock loop (PLL) overview

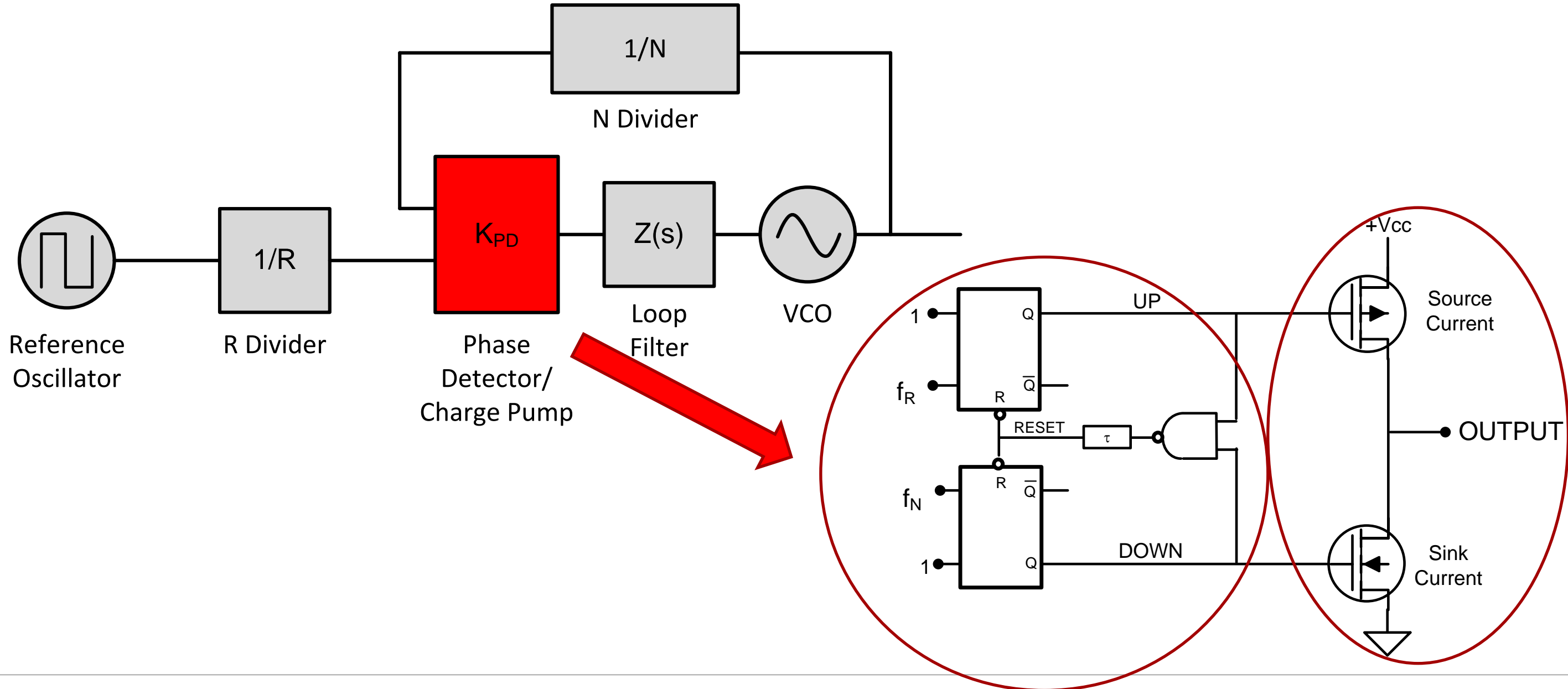


# Input sources



- Crystal oscillator (XO)
- Temperature compensated crystal oscillator (TCXO),
- Oven controlled crystal oscillator (OCXO),
- Clock output from another device

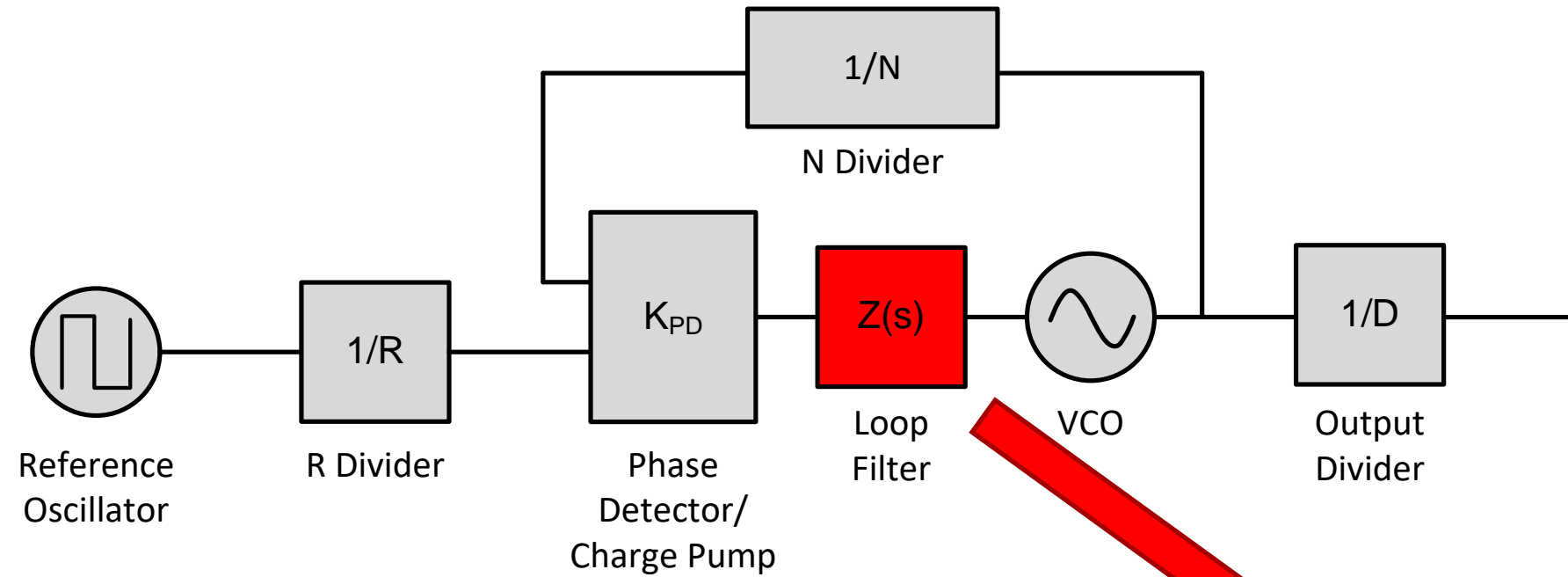
# Phase frequency detector/charge pump



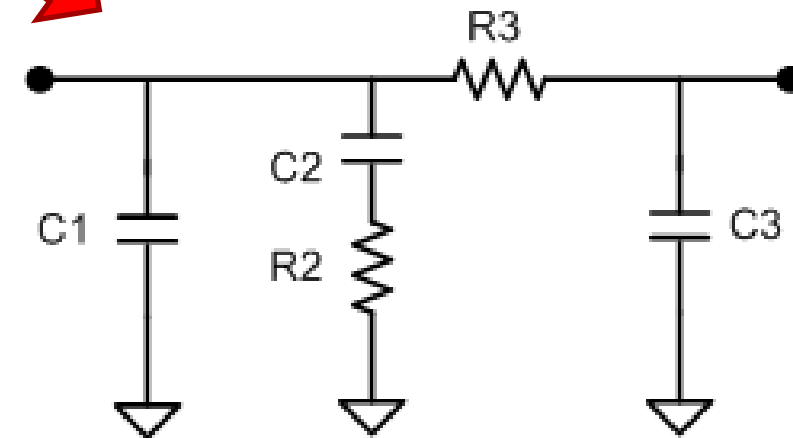
# Phase detector/charge pump operation

- High Impedance (tri-state) if output frequency/phase is correct (within tolerances)
- Sources Current if output frequency/phase is too low
- Sinks Current if output frequency/phase is too high

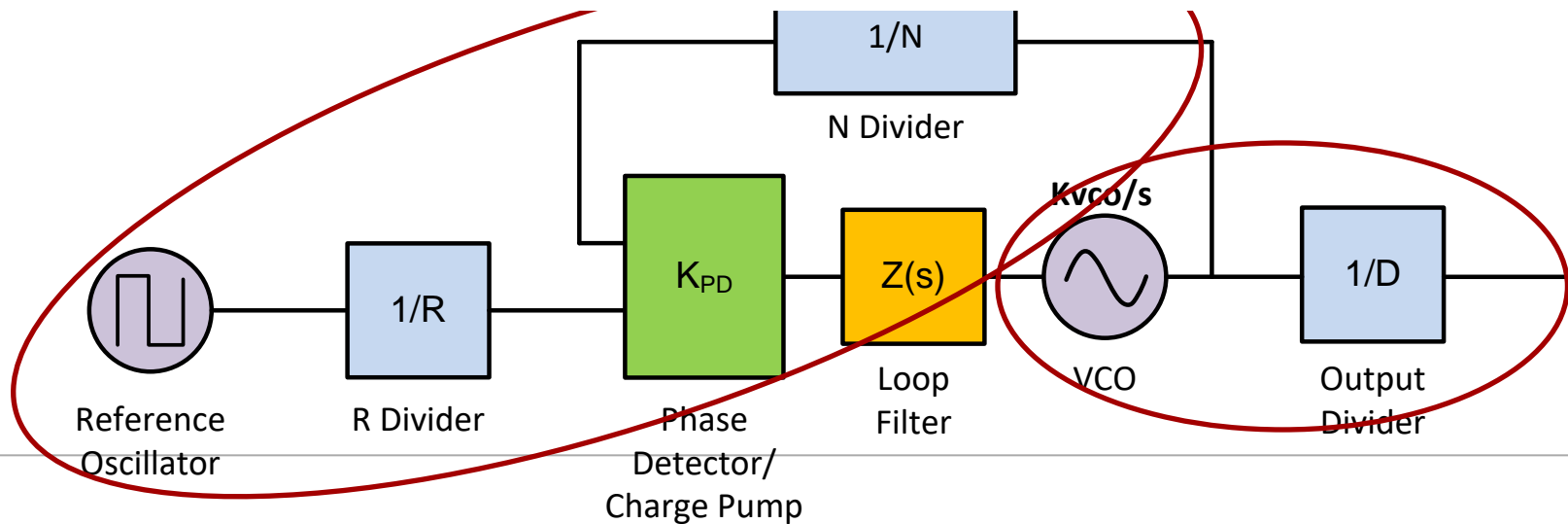
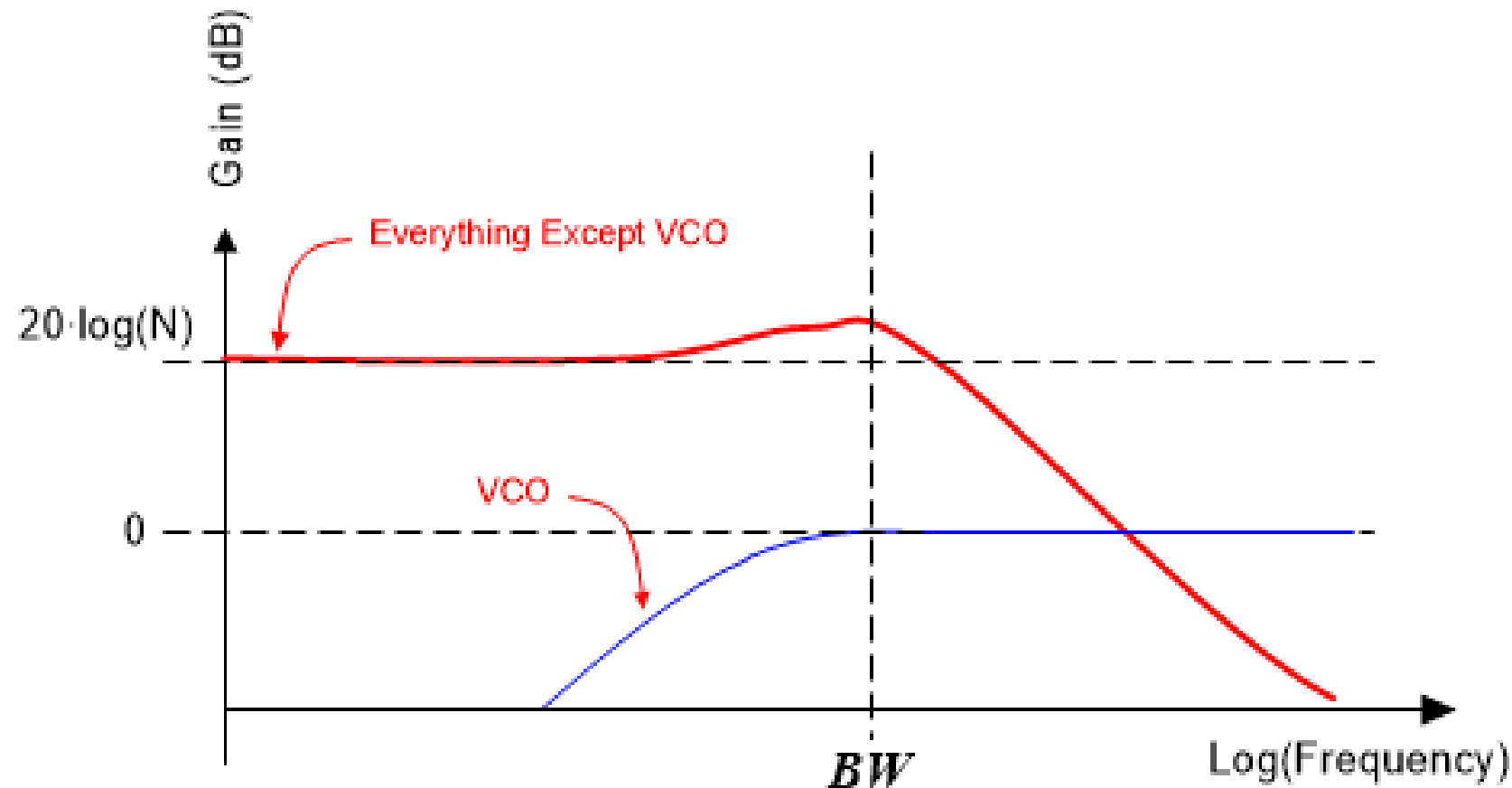
# Loop filter



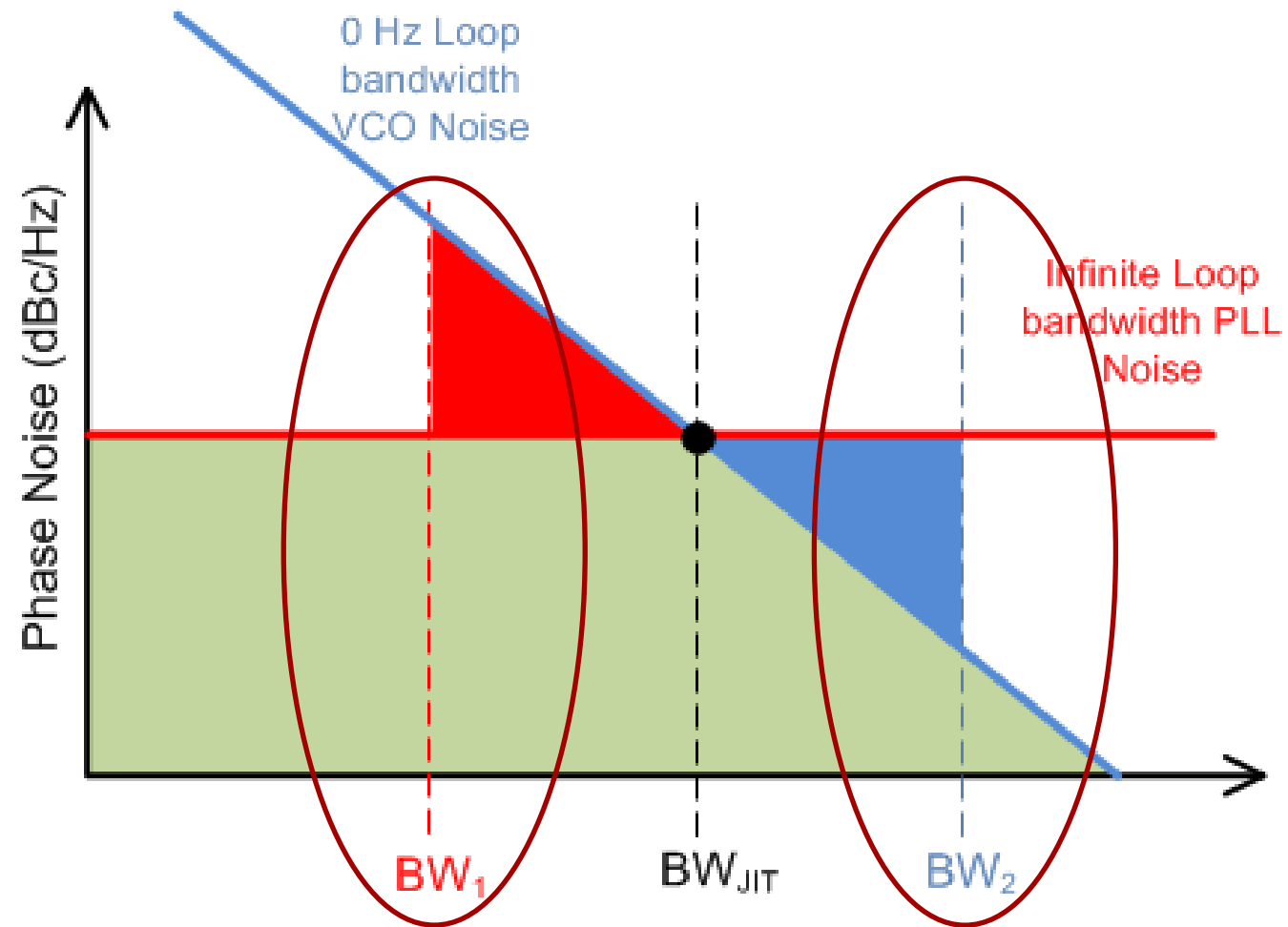
- The loop filter is a low pass filter
  - Has a dramatic effect on performance



# Brief overview of loop dynamics



# Choosing loop bandwidth



- Choose optimal jitter loop bandwidth to be  $BW_{JIT}$  to minimize area under the curve



# Choosing loop bandwidth

Design Goal	Bandwidth
Minimize Jitter	$BW = BW_{JIT}$
Minimize Phase Noise at offset $< BW_{JIT}$	$BW > BW_{JIT}$
Minimize Phase Noise at offset $> BW_{JIT}$	$BW < BW_{JIT}$
Minimize Lock Time	$BW > BW_{JIT}$
Minimize Spurs	$BW < BW_{JIT}$

To find more technical resources and search products, visit [ti.com/clocks](https://ti.com/clocks)

# Short Quiz

## 1. True or False:

The reference input frequency is provided by VCO.

# Short Quiz

## 1. True or False:

The reference input frequency is typically fixed frequency and provided by a stable reference source such as crystal oscillator.

# Short Quiz

## 2. Choose one:

The phase detector will

- (a) Sink and source current to the loop filter
- (b) Sample the phase error between the R and N counter
- (c) Provide the output frequency

# Short Quiz

## 2. Choose one:

The phase detector will

- (a) Sink and source current to the loop filter
- (b) Sample the phase error between the R and N counter
- (c) Provide the output frequency

# Short Quiz

## 3. True or False:

Choose loop bandwidth to be the point where VCO noise is equal to PLL noise to minimize jitter.

# Short Quiz

## 3. True or False:

Choose loop bandwidth to be the point where VCO noise is equal to PLL noise to minimize jitter.



# Short Quiz

## 4. Choose all that apply:

When choosing a loop bandwidth, which of these tradeoff are correct?

- a) To reduce lock time, increase the loop bandwidth
- b) To reduce spurious noise, increase the loop bandwidth
- c) To reduce phase noise at larger frequency offsets, reduce the loop bandwidth

# Short Quiz

## 4. Choose all that apply:

When choosing a loop bandwidth, which of these tradeoffs are correct?

- a) To reduce lock time, increase the loop bandwidth
- b) To reduce spurious noise, increase the loop bandwidth
- c) To reduce phase noise at larger frequency offsets, reduce the loop bandwidth



© Copyright 2019 Texas Instruments Incorporated. All rights reserved.

This material is provided strictly “as-is,” for informational purposes only, and without any warranty.  
Use of this material is subject to TI’s **Terms of Use**, viewable at [TI.com](https://www.ti.com)