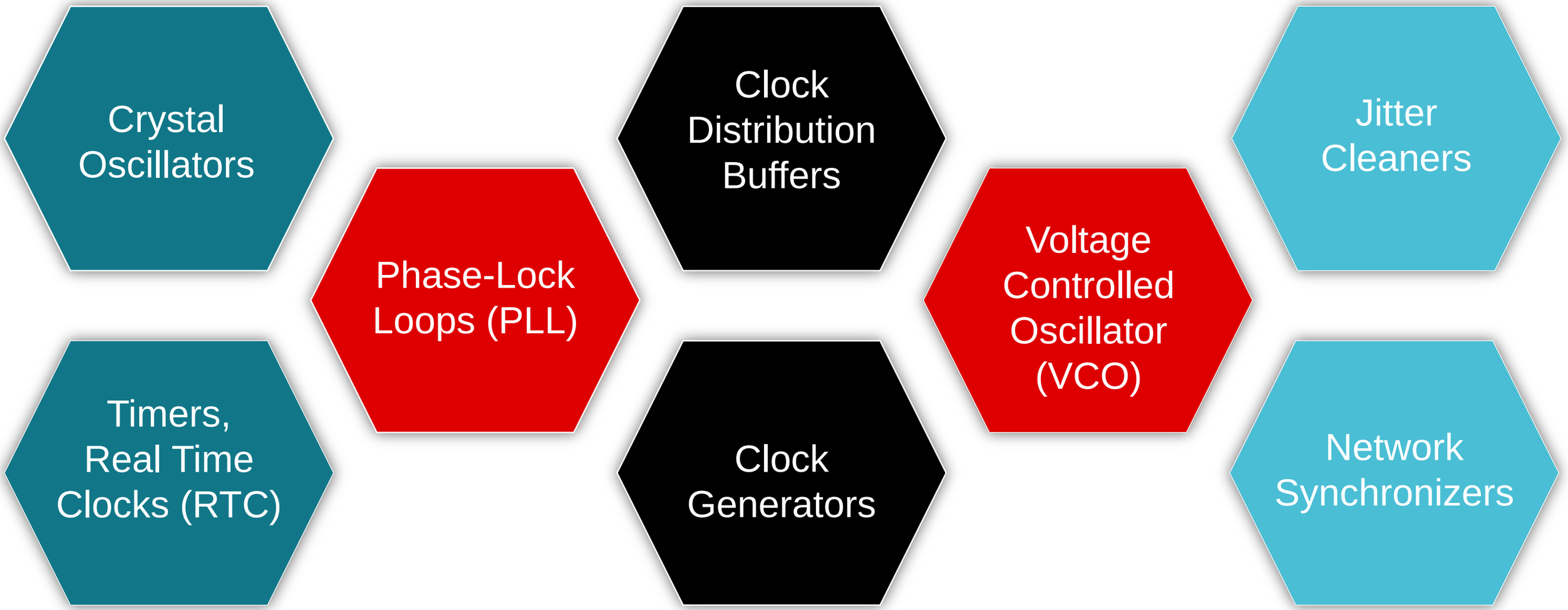
Overview of Clock and Timing Systems

TI Precision Labs – Clocks and Timing

Presented and Prepared by Liam Keese

Clock and timing product functions



Introduction to Clocks

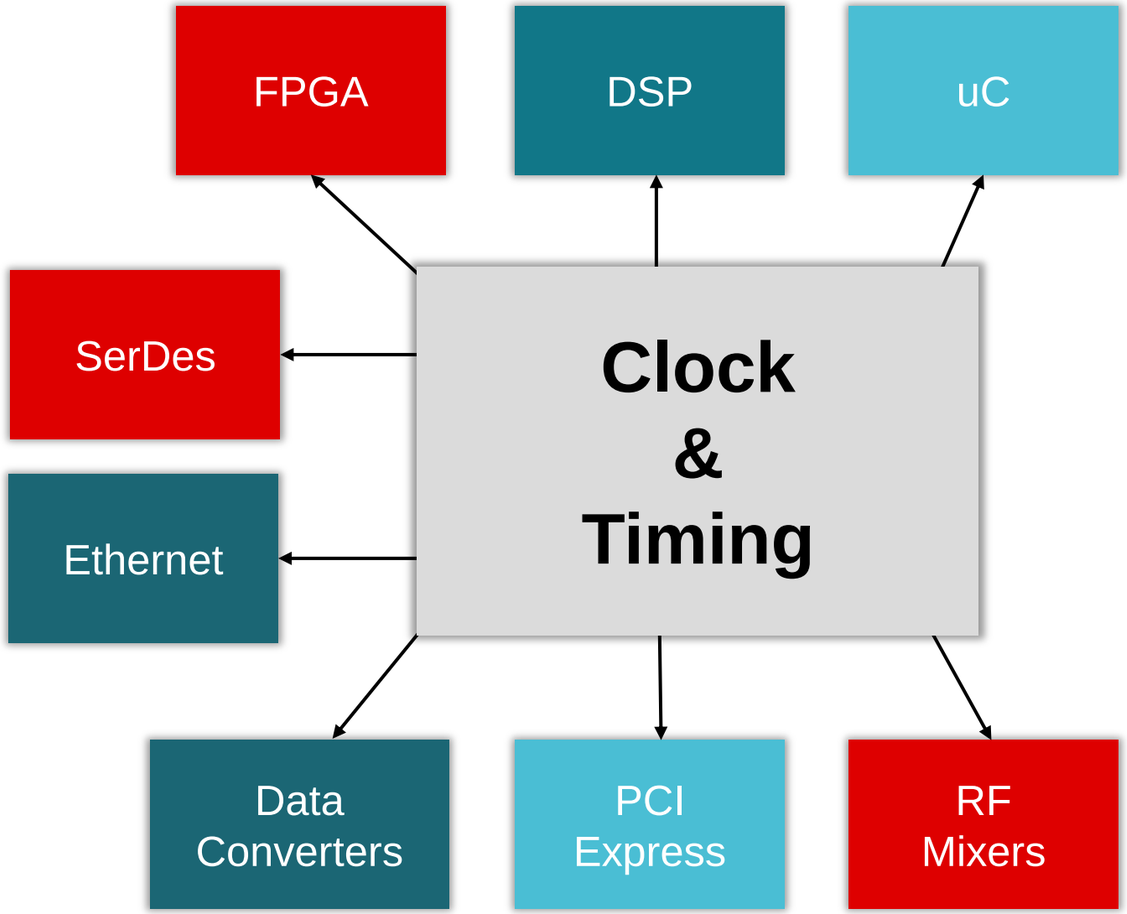
What are clocks?

- Clocks provide the “pulse” in electronics.

Why do I need a clock?

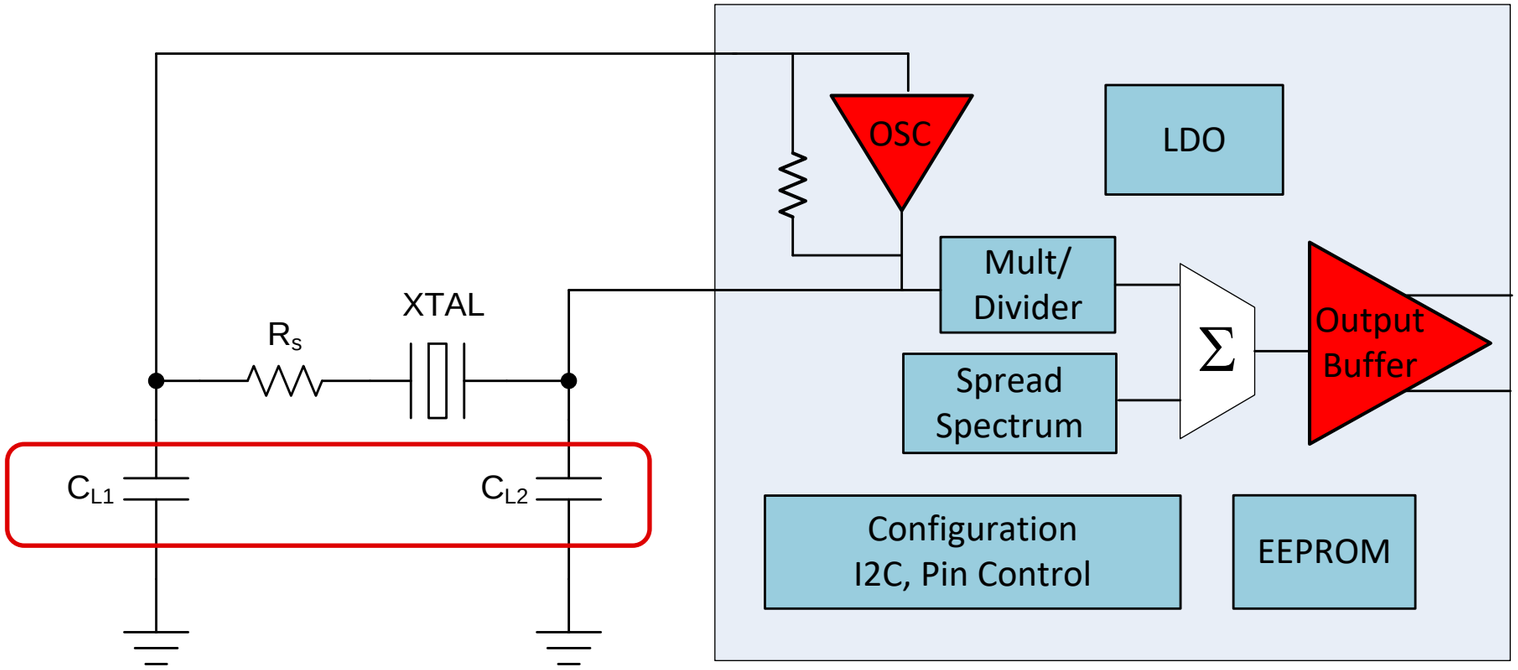
- Clocks allow data transmission in a synchronized manner

- Clocks also multiply/divide a source to fan out a specific frequency or frequencies



Crystal Oscillators

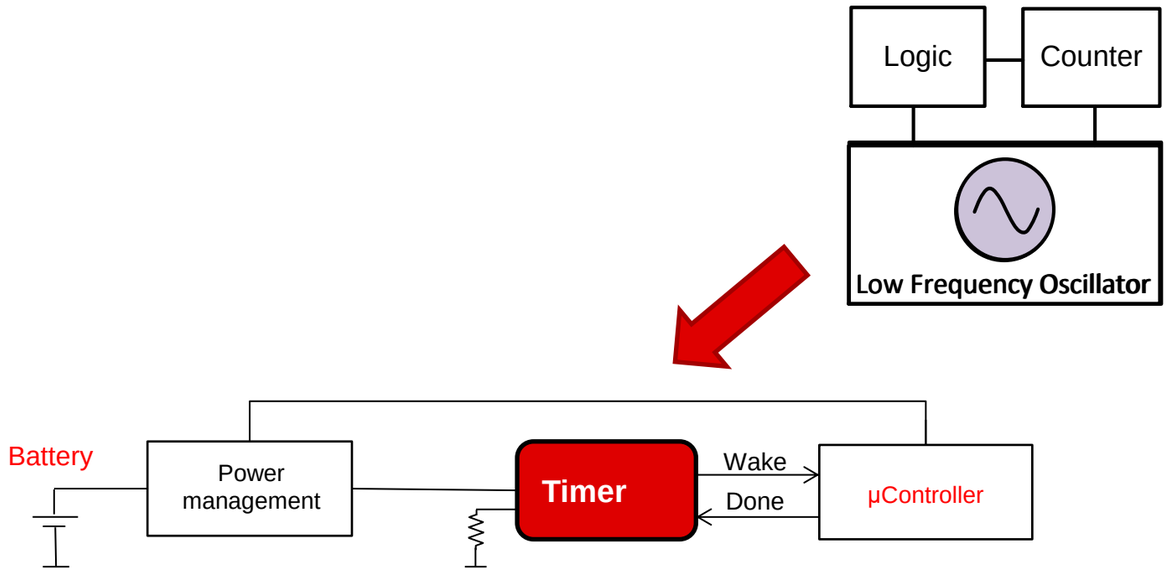
- Frequency, PPM accuracy
- Jitter / phase noise
- XO, TCXO, OCXO, VCXO, VCTCXO



Single Ended
Or
Differential

Real time clocks (RTC) and timers

- RTC in almost any electronic device or system which needs to track time accurately
  - Very low power, low frequency oscillator
  - Frees up system for time critical processing
- Timers wake up the system controller after a predetermined sleep period
  - Internal oscillator and counter
  - Greatly reduces overall system sleep current to < 100 nA



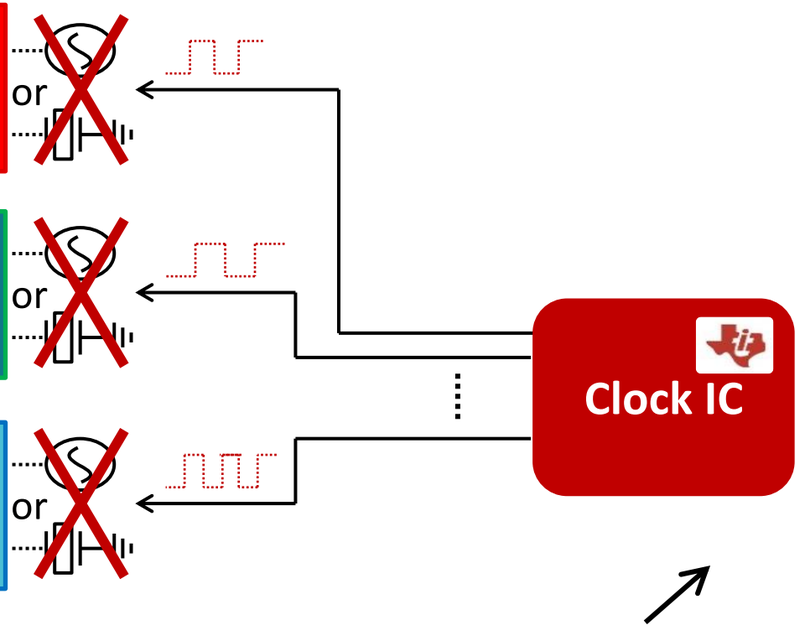
Replacing Crystals and Oscillators

If your system has….

Processors
(FPGA, DSP, ASIC, ARM/MIPS-based processor, etc.)

I/O
(USB controller, backplane SERDES, etc.)

Connectivity
(Switch ASIC, Ethernet MAC/PHY, WiFi, 3G/LTE modem, etc.)

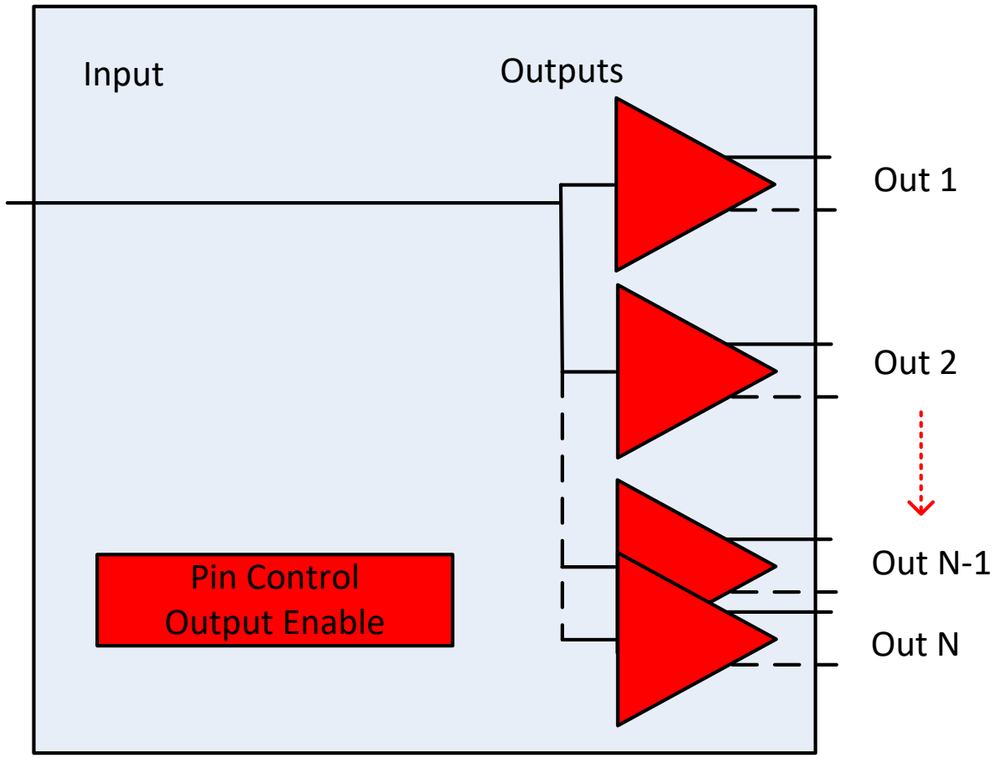


… there are certainly multiple crystals or low frequency oscillators used

…that can be replaced by a clock IC at lower BOM & better reliability

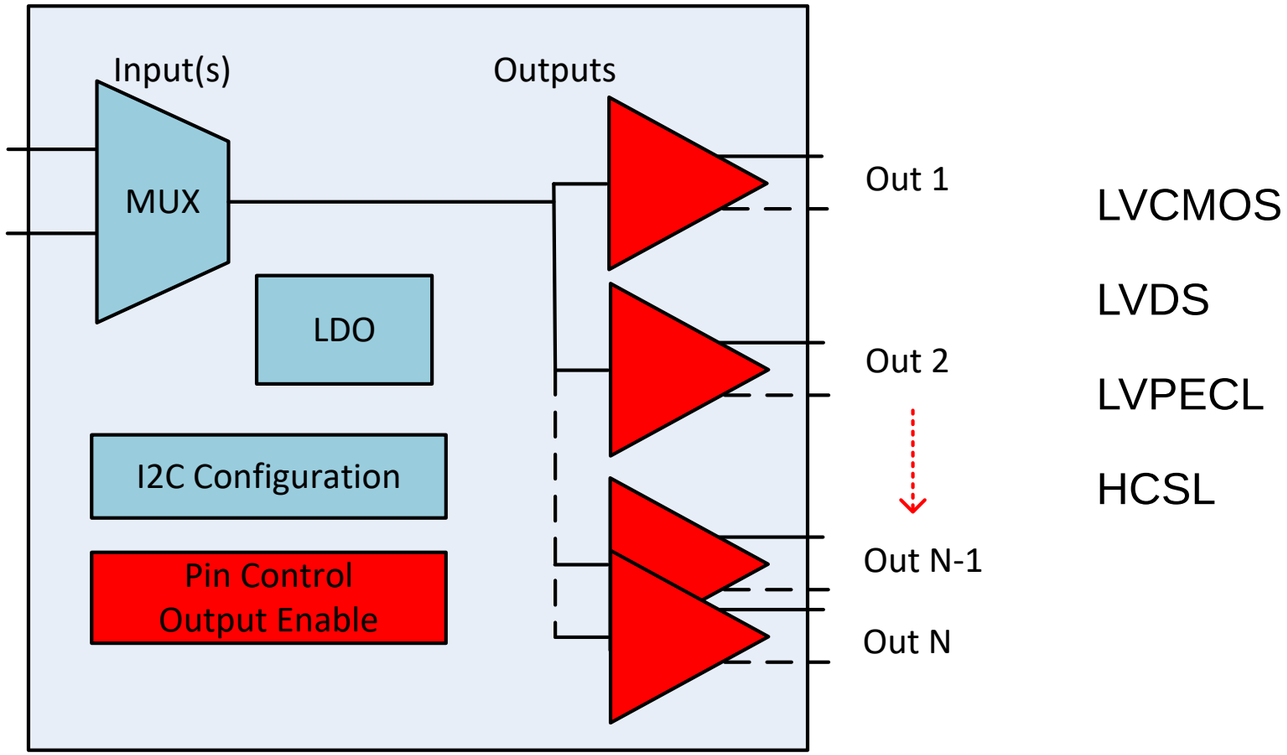
Clock Buffers

- Very low additive jitter
- Low solution cost
- Low output-to-output skew

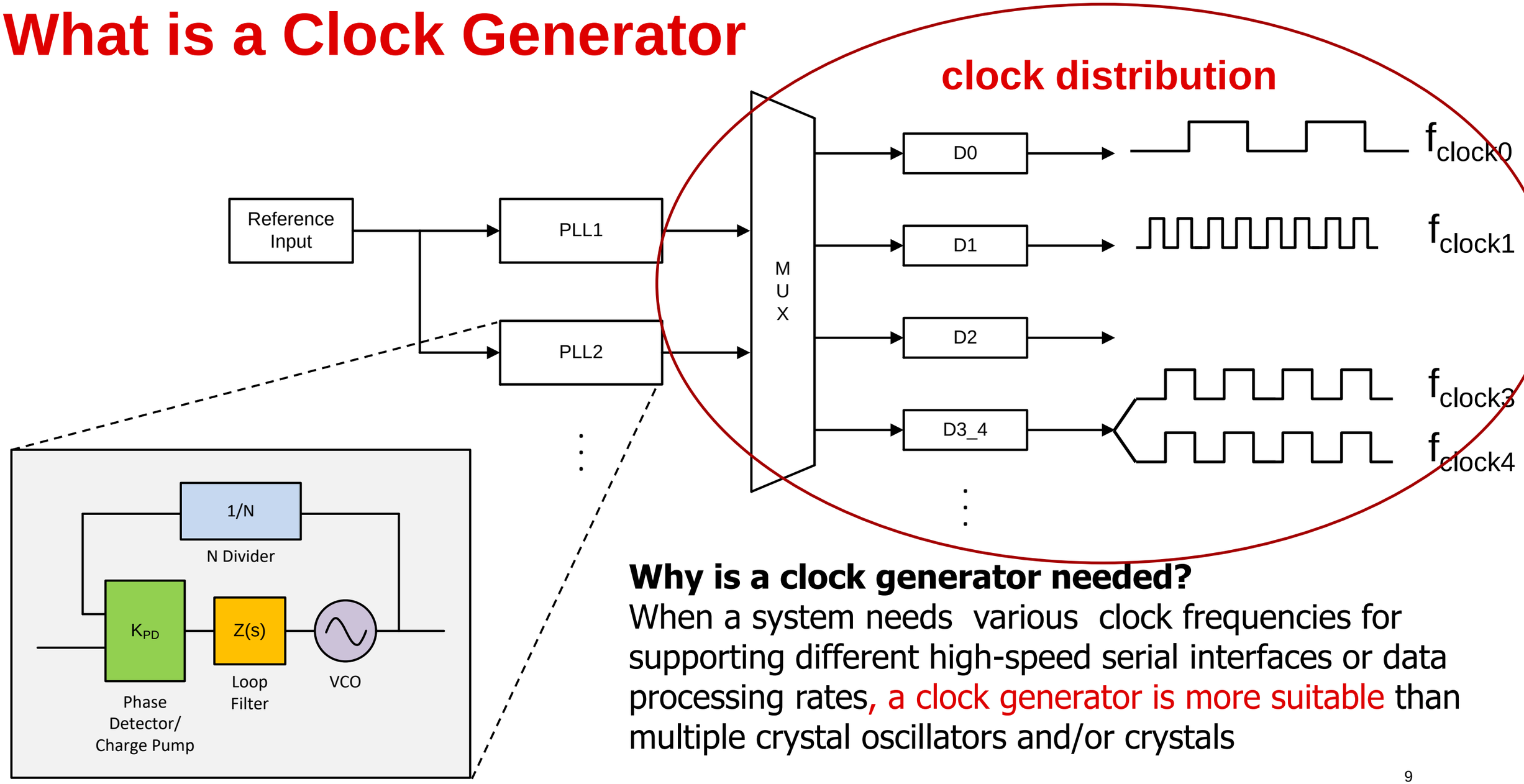


Clock Buffers

- Very low additive jitter
- Low propagation delay and variation
- Low output-to-output skew



What is a Clock Generator

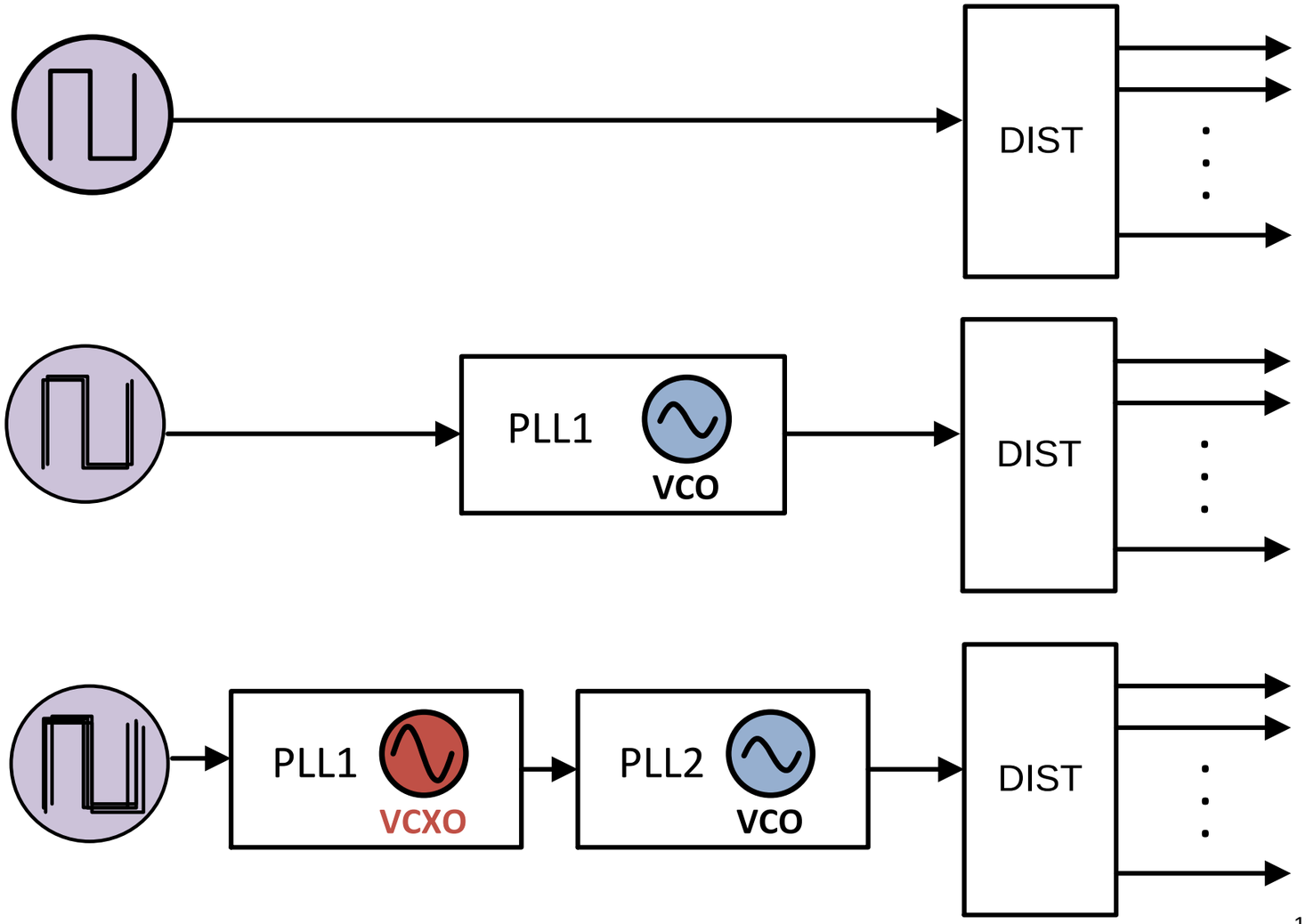


Why is a clock generator needed?

When a system needs various clock frequencies for supporting different high-speed serial interfaces or data processing rates, a clock generator is more suitable than multiple crystal oscillators and/or crystals

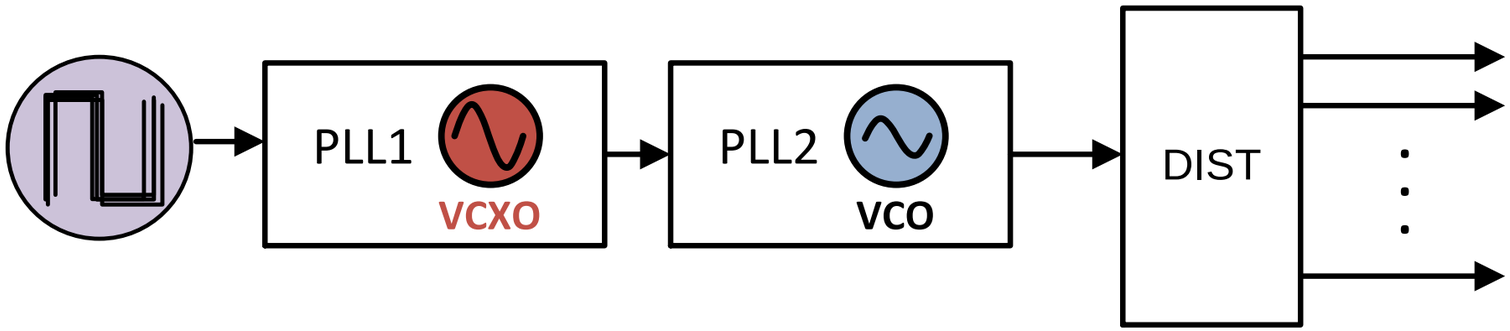
Analog PLL clock architectures: Dual and single loop with external VCOs

- Clock Distribution
  - No jitter cleaning lowest power consumption
- Single Loop
  - Good jitter cleaning, lower power consumption
- Dual Loop (Jitter Cleaner)
  - Best jitter cleaning
  - PLL1 narrow loop bandwidth
  - PLL2 wide loop bandwidth



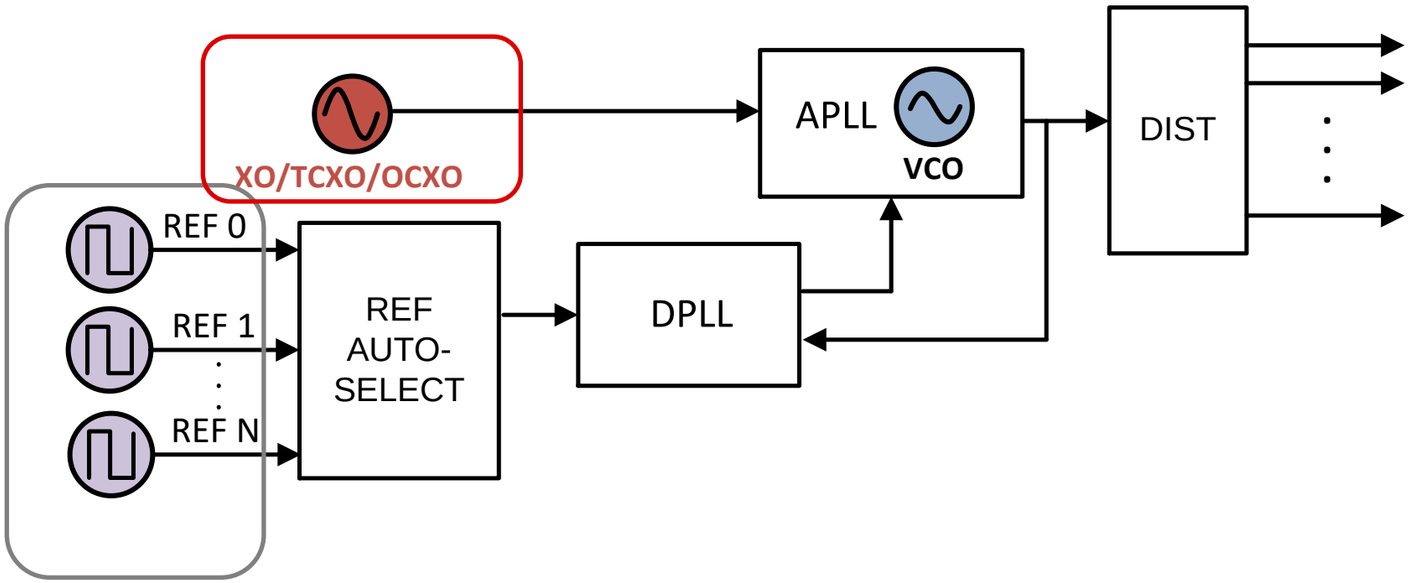
When to use Dual/Cascaded Loop

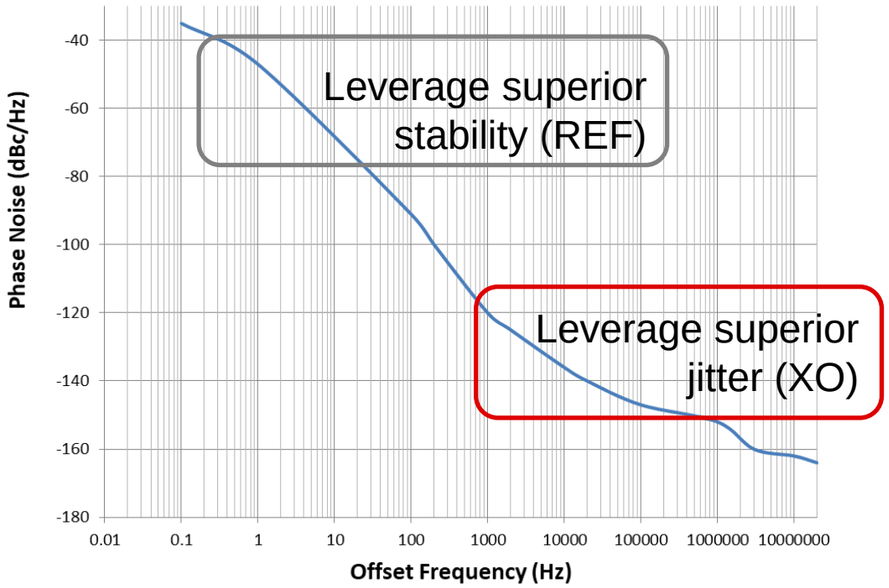
- Noisy reference input, jitter cleaning is required
- When input frequency is low, or does not relate well with output frequency
- Synchronization required between multiple frequency domains



When to use a Network Synchronizer

- Highly stable clocks needed at all times irrespective of whether reference input is present or not
  - Multiple and redundant input references need to be monitored and switched between, based on qualification, in a “hitless” manner
- System time and frequency must be guaranteed accurate at all times
  - Adjustable timing and synchronization required between multiple frequency domains





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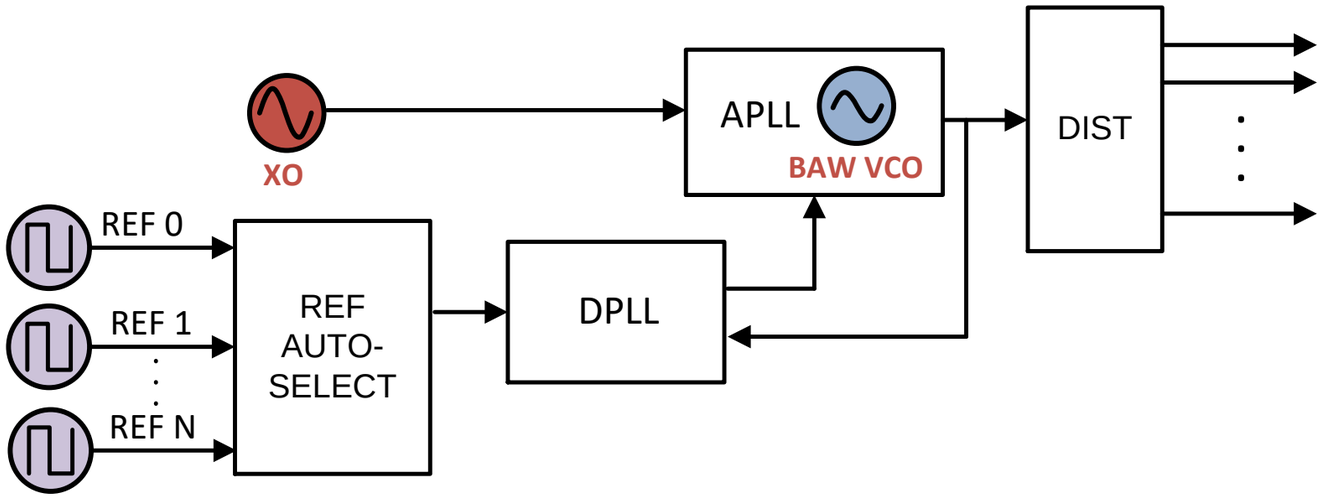

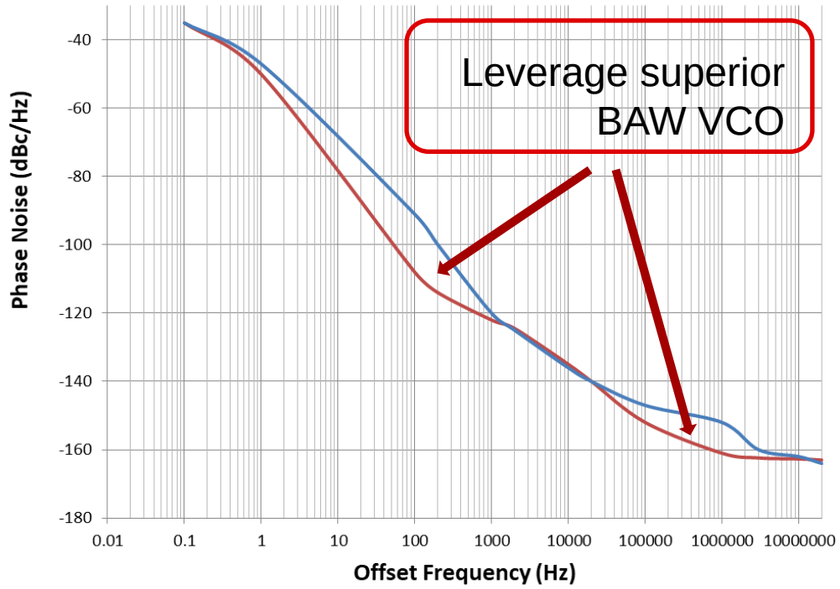

To find more technical resources and search products, visit ti.com/clocks

Quiz

- True or false: A crystal oscillator is required for each system frequency domain
- True or false: A clock distribution network may consist of multiplexers, dividers, delay networks and multiple output buffers
- True or false: Skew is a measure of the frequency difference between clock buffer outputs
- True or false: A dual loop PLL architecture is used for a noisy reference input to provide a jitter cleaning function and then multiply up a clean reference
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