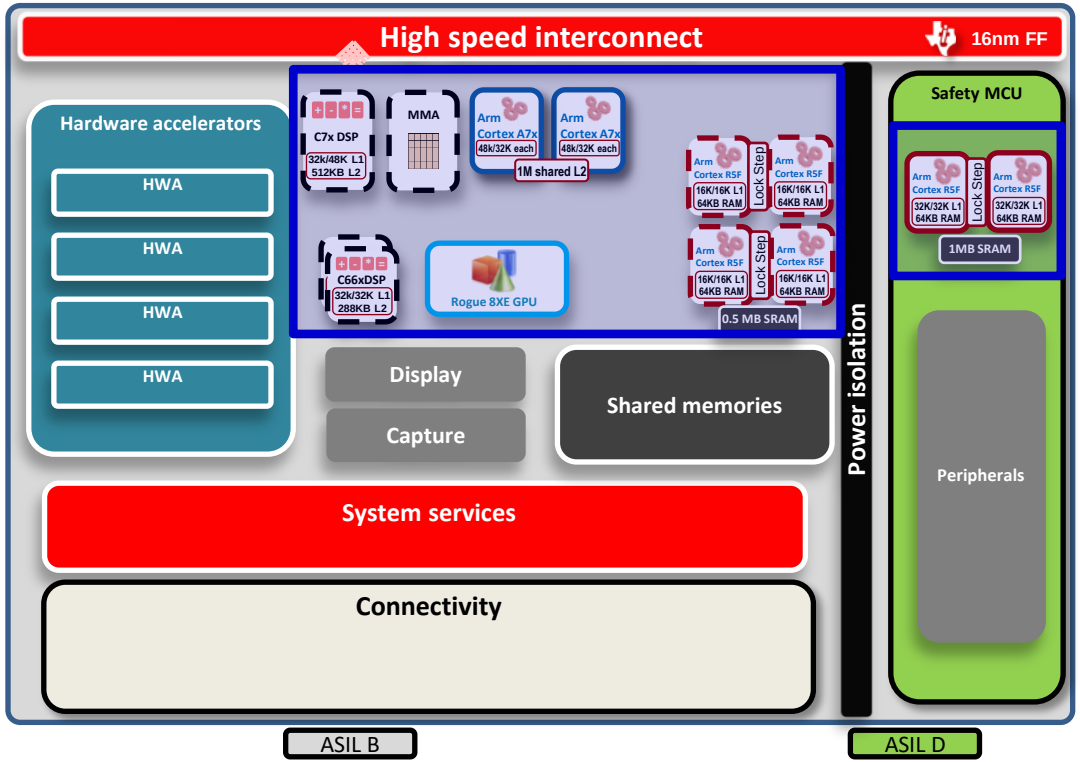
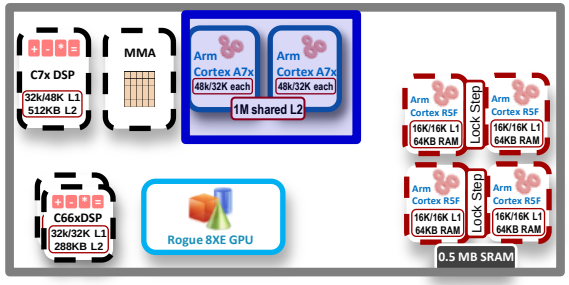
Jacinto™ 7 processors: heterogenous processing cores

Heterogeneous processing cores

- Key features and benefits
- **Heterogeneous processing cores**
- Application-specific hardware accelerators
- Device management architecture
- Memory architecture and data movement
- Safety and isolation features
- Virtualization features
- Security features
- Power management features
- Network connectivity
- Flash and storage
- Serial connectivity

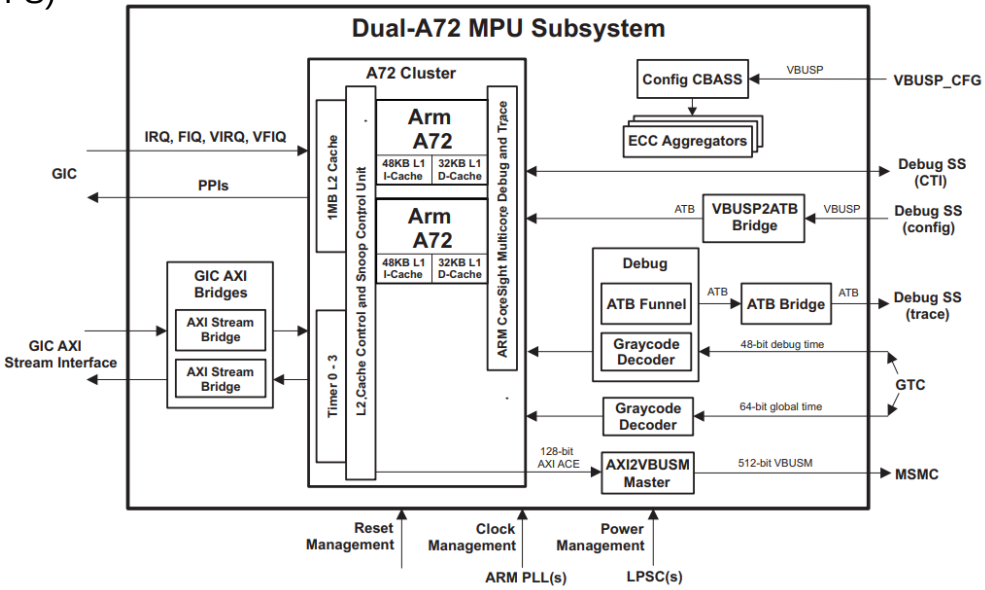


Heterogeneous processing cores



Arm® Cortex®-A72 MPU (up to 2 GHz):

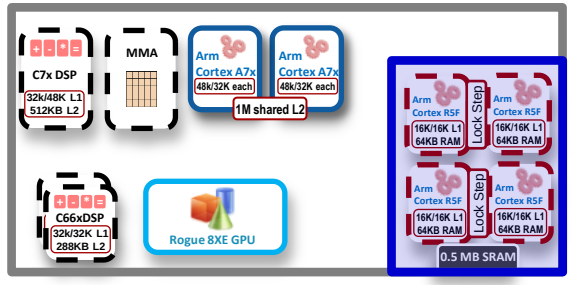
- Armv8-A 64-bit architecture
- SIMD and floating-point extensions
- Organized as dual-core MP2 cluster
- Dedicated cluster PLL for dynamic frequency switching (DFS)
- Memory system:
  - 48kB/32kB L1 instruction and data caches per CPU
  - 1MB L2 shared cache per cluster
  - ECC on L1/L2 data parity on L1 instruction
  - Memory Management Unit (MMU)
  - Access to L3 with IO and CPU cache coherency
- Arm GIC-500 (Generic Interrupt Controller): GICv3
- CPU cache coherency
- Arm CoreSight debug and trace

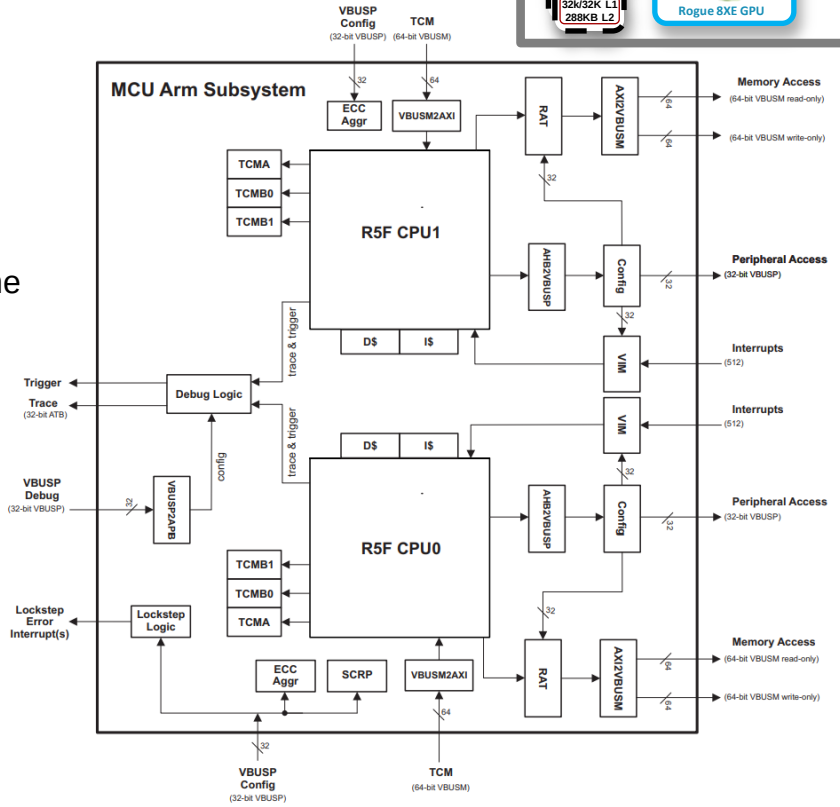


Heterogeneous processing cores

Arm® Cortex®-R5F MCU (up to 1 GHz):

- Arm®v7-R architecture with full-precision vector floating point (VFPv3)
- Organized as dual-core clusters:
  - 2x clusters in main domain
  - 1x cluster in Safety MCU domain (as shown)
- Configurable as split or lock-step mode
- Memory system:
  - 16kB/16kB L1 instruction (I$) and data (D$) cache
  - 64KB tightly-coupled memory RAM
  - All memories are ECC protected
  - Access to L3 with IO coherency
  - 16-region Memory Protection Unit (MPU)
- Vector Interrupt Manager (VIM)
- Region Address Translator (RAT) extending to 48b
- Execute-in-place (XIP) support from Flash with in-line ECC and authentication



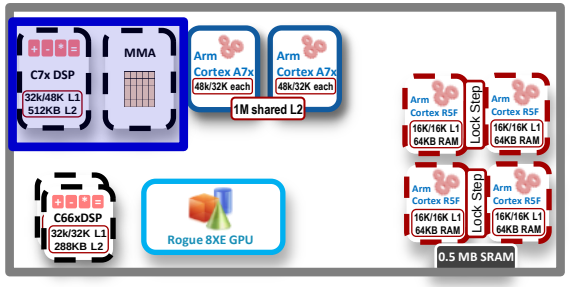


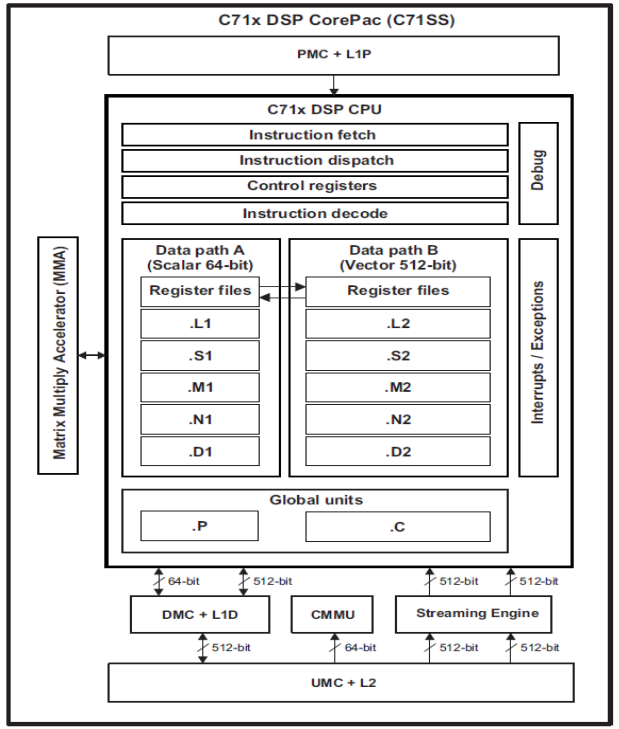
Heterogeneous processing cores

C71x DSP (up to 1 GHz):

- Next-generation, TI-true 64b DSP core:
  - 512b SIMD processing
  - Dual-data path CPU
    - 64-bit scalar + 512-bit vector
  - Vision processing enhancements
  - OpenVX support for computer vision processing
- Matrix Multiply Accelerator (MMA) for deep learning
- Memory system:
  - 32kB L1 program cache
  - 48kB L1 data cache or RAM
  - 512kB L2 unified cache or RAM
  - Access to L3 with IO and CPU cache coherency
  - CorePac Memory Management Unit (CMMU)
    - ARM®v8-A compliant
- Multi-dimensional Streaming Engine (SE) provides high-speed synchronous access to L3 memory

Assuming 1 GHz as clock for frequency for C6x, C7x and MMA,				
		C6x	C7x	MMA
GMAC	Fixed 8-bit	32	144	4096
	Fixed 16-bit	32	144	1024
GOPS	Fixed 8-bit	96	496	8192
	Fixed 16-bit	80	392	2048
GFLOPS	Float	16	88	NA

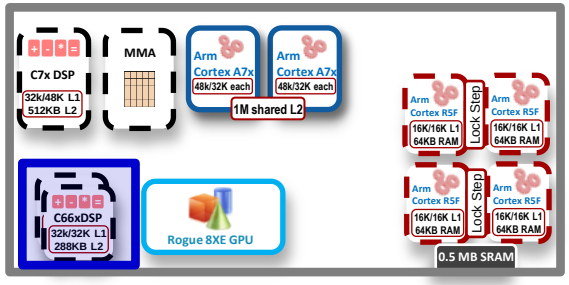


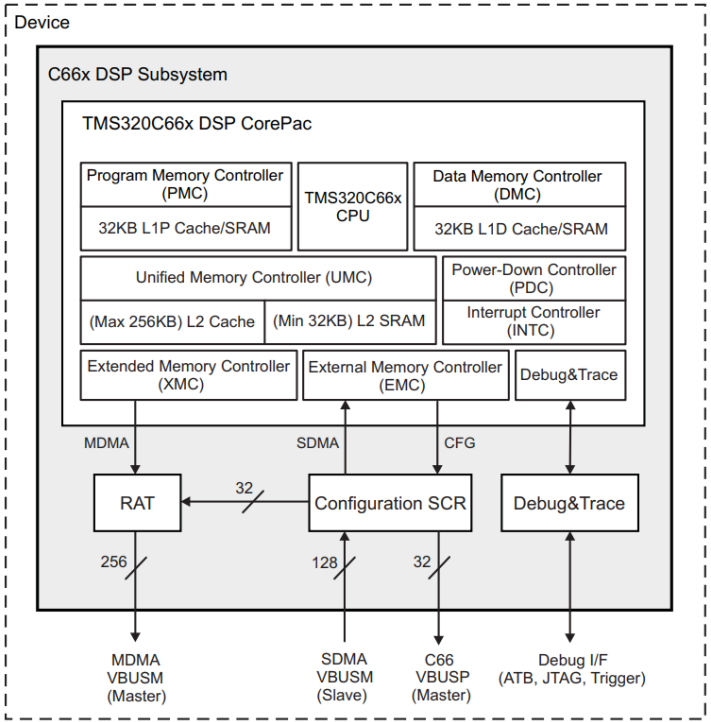


Heterogeneous processing cores

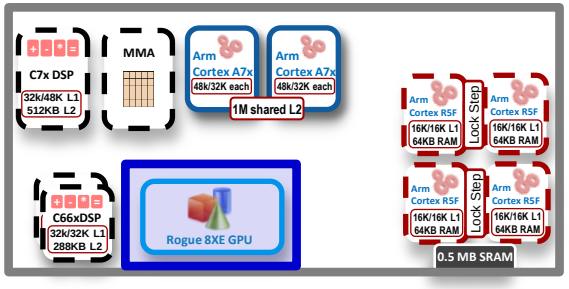
C66x DSP (up to 1.3 GHz):

- 2x TI-standard TMS320C66x DSP cores
- Maximum reuse of optimized code from previous-generation TI SoC
- Fixed and floating-point support (C64x + C67x ISA)
- SIMD / highly-parallel vector processing
  - 8x instructions per cycle, up to 128b vectors
- Memories:
  - 32kB L1 program cache or RAM
  - 32kB L1 data cache or RAM
  - 288kB L2 unified cache (up to 256KB) or RAM
  - Error detection for all L1 and L2 program and data memories
  - Error correction for all L1 and L2 data memories
- Region Address Translator (RAT) up to 48b
  - Access to full device memory map





Heterogeneous processing cores



GE8430 GPU:

- PowerVR 8XE GE8430 graphics processing unit from Imagination Technologies
- Processing up to 96 GFLOPS and 6 GPixel/second
- 3-dimensional and 2-dimensional graphics processing unit supporting OpenGL ES
- Frame Buffer Compression (FBC) and Decompression (FBDC)
- Memory Management Unit (MMU) for virtualization memory space
- Hardware virtualization and security
  - Support of priority task pre-emption at fine granularity
- Unified Shading Clusters (USC):
  - Multi-threaded rendering with vertex shader, pixel shader and compute shader
  - Tiled-Based Deferred Rendering (TBDR)
- High-quality image anti-aliasing

For more information

- For more training on Jacinto 7 processors: http://training.ti.com/jacinto7
- Download Processor SDK Automotive for Jacinto 7 processors: http://www.ti.com/tool/PROCESSOR-SDK-DRA8X-TDA4X
- Order TDA4VM Jacinto Automotive processors for ADAS & autonomous vehicles: http://www.ti.com/product/TDA4VM
- Order the TDA4VMx evaluation module: http://www.ti.com/tool/TDA4VMXEVM
- Order DRA829V Jacinto Automotive processors for gateway & vehicle compute: http://www.ti.com/product/DRA829V
- Order the DRA829Vx evaluation module: http://www.ti.com/tool/DRA829VXEVM
- For questions regarding topics covered in this training, visit the processors support forum at the TI E2E Community website: https://e2e.ti.com