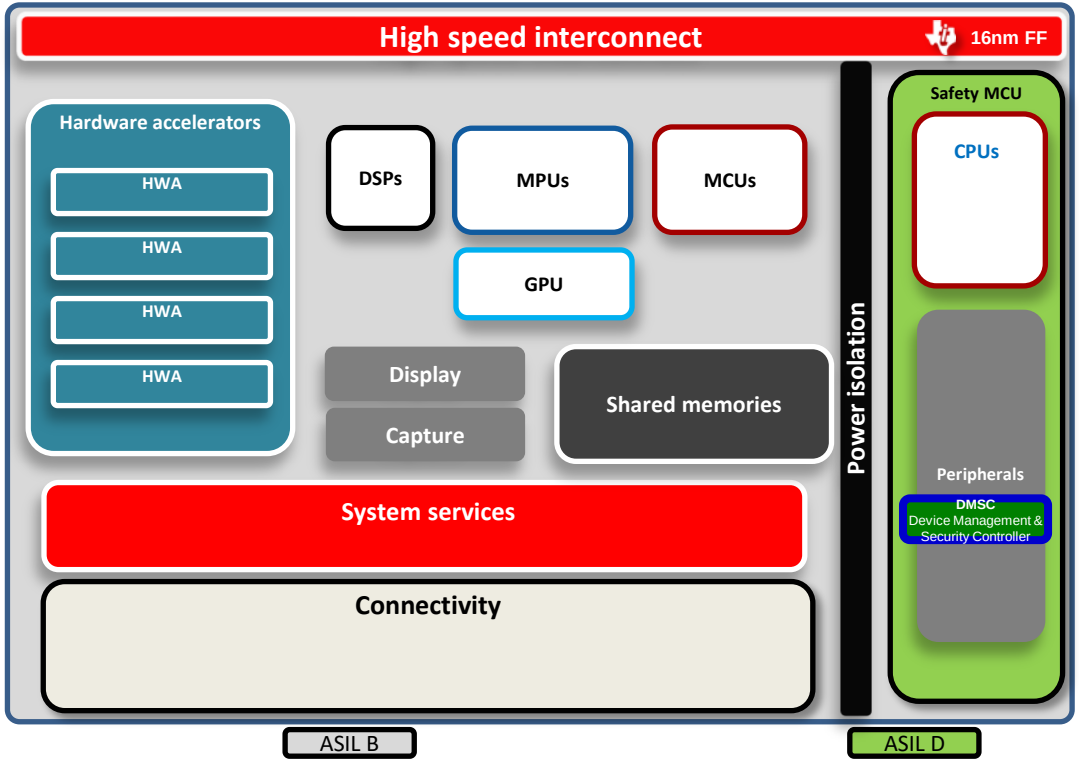
Jacinto™ 7 processors: device management

Device management architecture

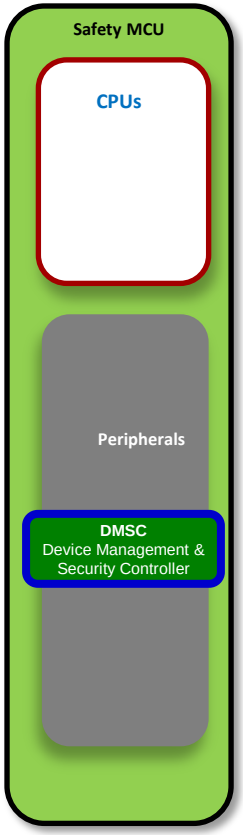
- Key features and benefits
- Heterogeneous processing cores
- Application-specific hardware accelerators
- **Device management architecture**
- Memory architecture and data movement
- Safety and isolation features
- Virtualization features
- Security features
- Power management features
- Network connectivity
- Flash and storage
- Serial connectivity



Device management architecture

Device Management and Security Controller (DMSC):

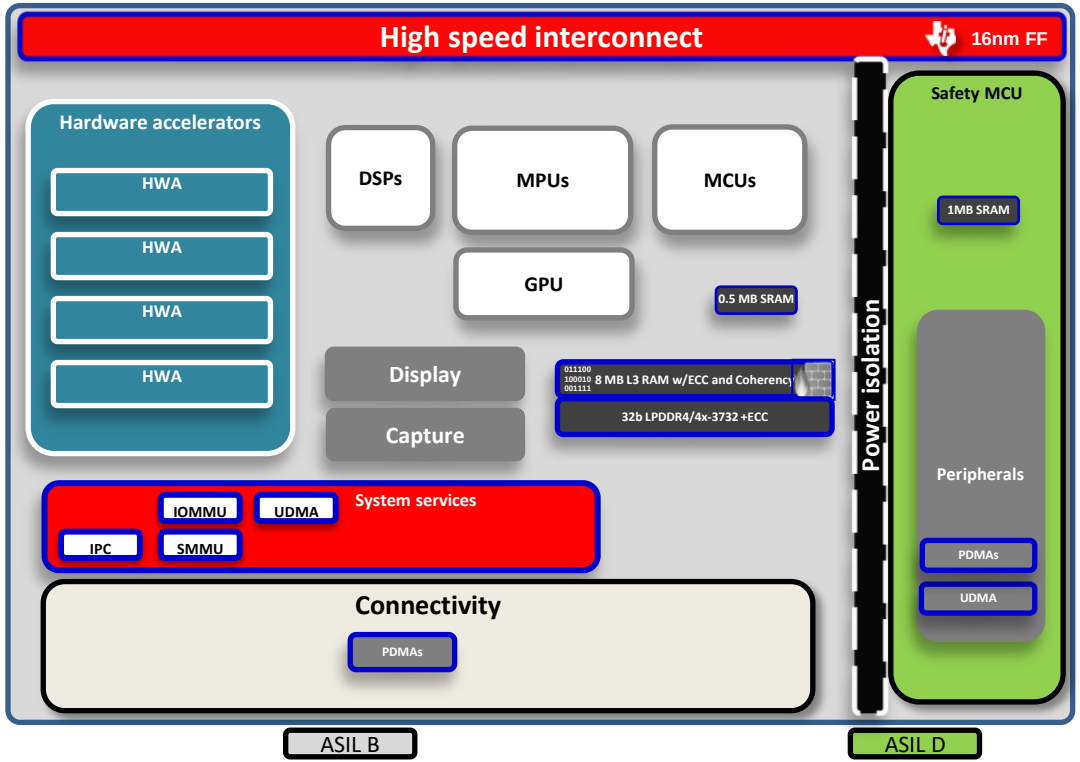
- Closed Arm® Cortex®-M3 subsystem running TI firmware
- *Abstracts key device management functions from other cores:*
  - Power management:
    - Clock and PLL control
    - Power domain control
    - Power mode and wakeup control
  - Device management:
    - Boot configuration
    - Quality of Service (QoS) configuration
    - Interrupt and event allocations
    - DMA configuration and channel allocations
  - Security management:
    - Firewall control
    - Boot security
    - Runtime security
    - Manage secure resources (cryptography)
- Secure messaging hardware for any allowed core to request services



Jacinto™ 7 processors: memory architecture & data movement

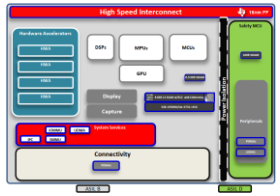
Memory architecture and data movement

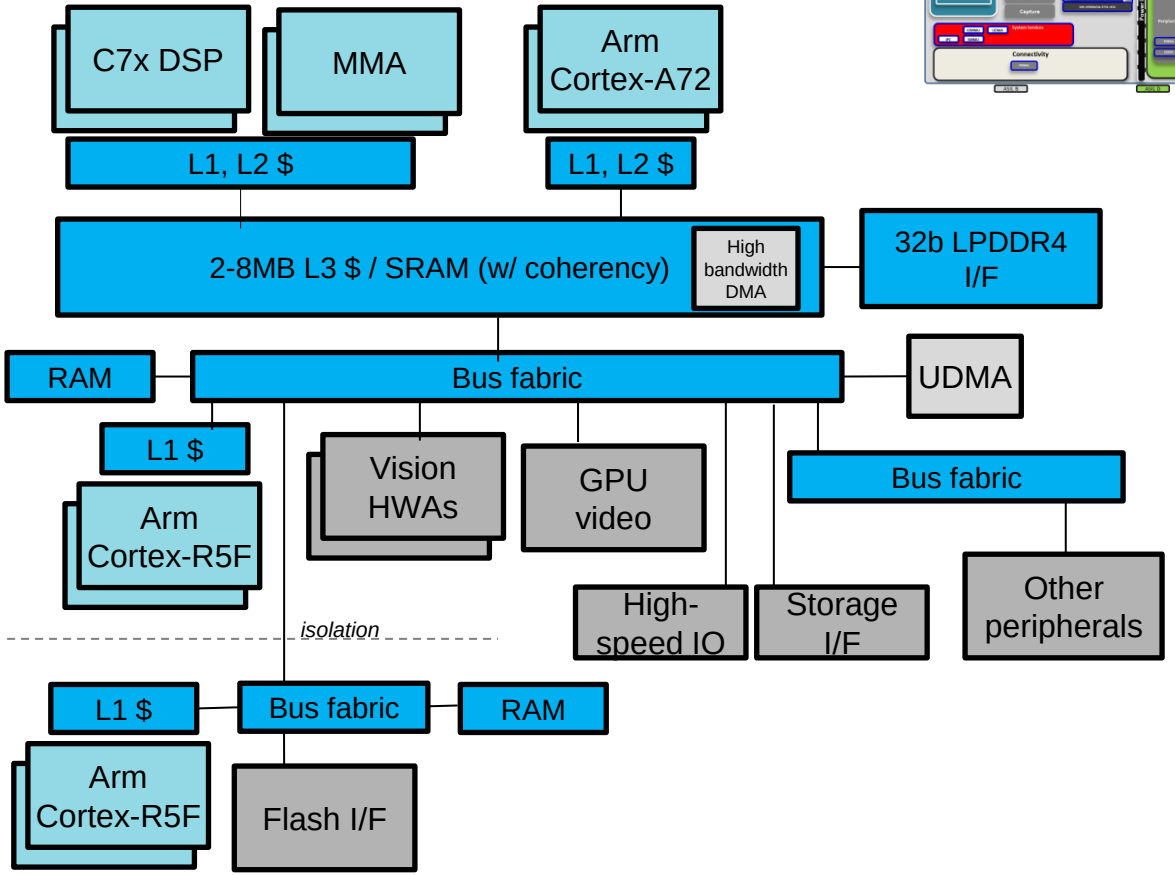
- Key features and benefits
- Heterogeneous processing cores
- Application-specific hardware accelerators
- Device management architecture
- **Memory architecture and data movement**
- Safety and isolation features
- Virtualization features
- Security features
- Power management features
- Network connectivity
- Flash and storage
- Serial connectivity



Memory architecture and data movement

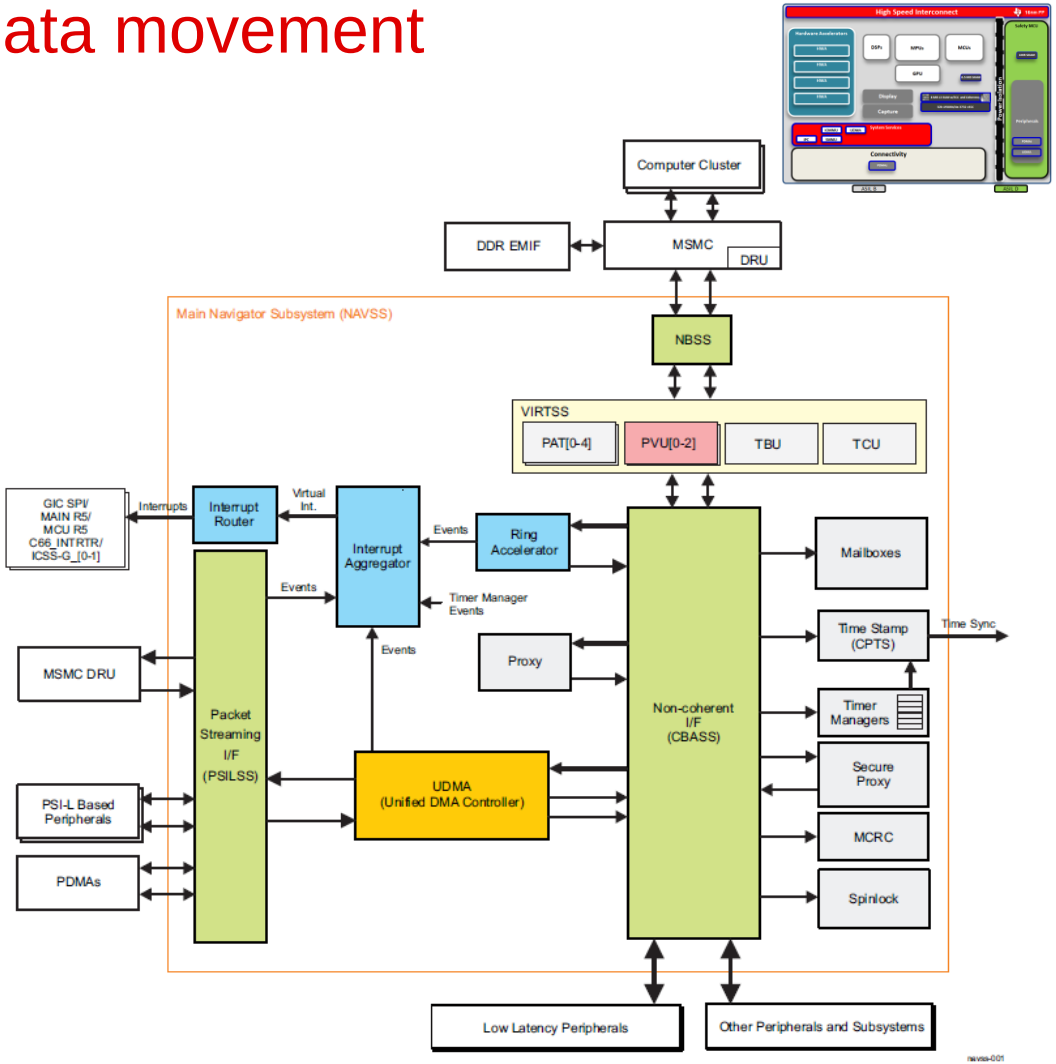
- Optimized memory architecture:
  - 3-level hierarchical memory
  - Multi-Core Shared Memory Controller (MSMC)
    - Provides 2-8 MB of shared L3 SRAM/cache
    - CPU cache coherency for direct connected masters
    - IO coherency for allocated L3 data
  - High-speed LPDDR4/4x interface
    - In-line ECC with context cache
- Efficient SoC bus fabric:
  - High-bandwidth, non-blocking internal bus infrastructure for real-time traffic
  - Multi-channel DMA engines
  - Optimized paths to most relevant memory interfaces per core
- Quality-of-service features
  - MSMC credit based real-time paths
  - DMSC controlled route balancing
  - Priority arbitration and re-ordering





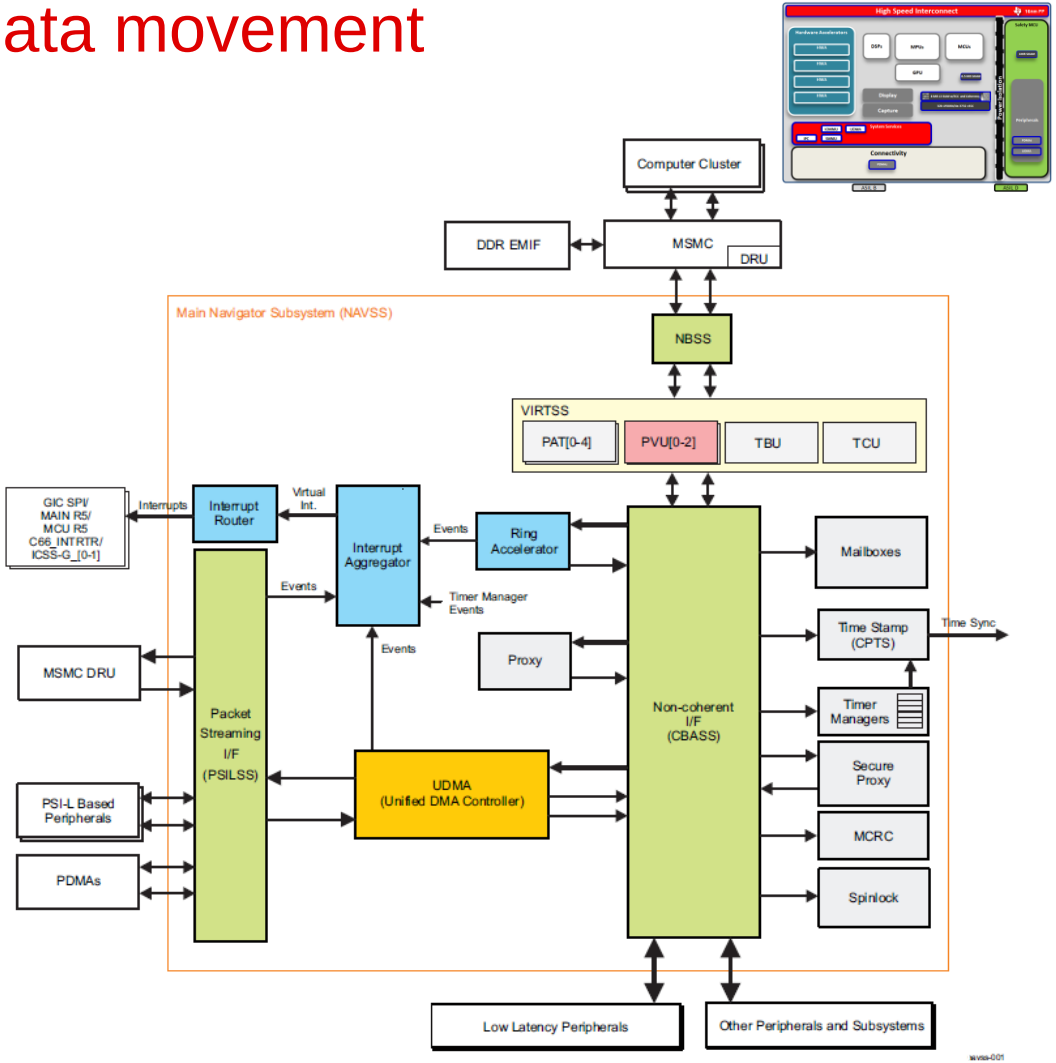
Memory architecture and data movement

- **Data Routing Unit (DRU):** Embedded DMA in MSMC for high-bandwidth C71x/MMA data paging
- **IO masters w/ direct DMA:** DSS, encoder, decoder, etc.
- **Navigator Sub-System (NAVSS):**
  - Collection of data-movement components
- **NAVSS: Unified DMA controller (UDMA)+**
  - DMA engine for block copy and data peripheral support
  - Standard parallel data slave peripherals via TI Common Bus Architecture Sub-System fabric (CBASS)
  - Channel control for some direct IO masters (VPAC, DMPAC)
  - Channel control for Packet Streaming Interface Link (PSIL) peripherals (Ethernet switch, CSI-2 camera interface, PDMA)
- **NAVSS: Peripheral DMA (PDMA):**
  - Distributed local-buffered DMA close to IO Peripherals
  - Transparent to software, program channels on UDMA
- **NAVSS: MCRC**
  - Safety block copy DMA for CRC checking
- **NAVSS: Ring Accelerator (RA):** DMA queue management providing abstracted software view to hardware DMA queues
- **NAVSS: Proxy:** Allows efficient access to RA queues with optional virtualization



Memory architecture and data movement

- **NAVSS: Virtualization IP subsystem (VIRTSS):**
  - All uDMA/IO masters can optionally route via VIRTSS
    - Per channel selection for uDMA
    - Per master via QOS registers
    - Per channel for virtualized peripherals
  - PAT, PVU, sMMU (TBU/TCU)
- **NAVSS: North Bridge Subsystem (NBSS)**
- **NAVSS: Event management:** Interrupt and event routers and aggregators
- **NAVSS: IPC (Inter-processor communication):**
  - Secure Proxy/RA (a.k.a "secProxy"): secure messaging between masters & DMSC
  - Mailbox: Legacy mailboxes with doorbells/interrupts
  - Spinlock: Legacy spinlock for real-time OS /software
- **NAVSS: Time management:**
  - Common Platform Time Stamp (CPTS) timestamping of events from various peripheral sources (e.g PCIe)
  - Timer manager: Enables scheduling / pacing of DMA to prevent excessive blocking



For more information

- For more training on Jacinto 7 processors: http://training.ti.com/jacinto7
- Download Processor SDK Automotive for Jacinto 7 processors: http://www.ti.com/tool/PROCESSOR-SDK-DRA8X-TDA4X
- Order TDA4VM Jacinto Automotive processors for ADAS & autonomous vehicles: http://www.ti.com/product/TDA4VM
- Order the TDA4VMx evaluation module: http://www.ti.com/tool/TDA4VMXEVM
- Order DRA829V Jacinto Automotive processors for gateway & vehicle compute: http://www.ti.com/product/DRA829V
- Order the DRA829Vx evaluation module: http://www.ti.com/tool/DRA829VXEVM
- For questions regarding topics covered in this training, visit the processors support forum at the TI E2E Community website: https://e2e.ti.com