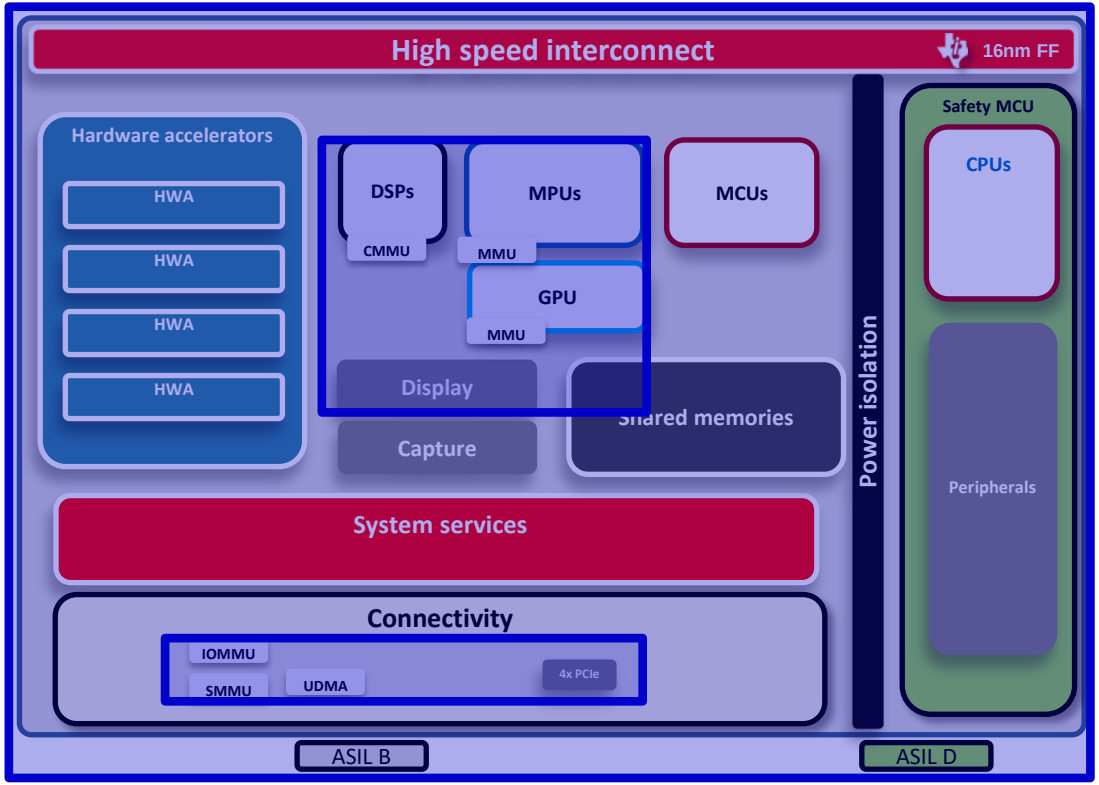
# Jacinto™ 7 processors: virtualization

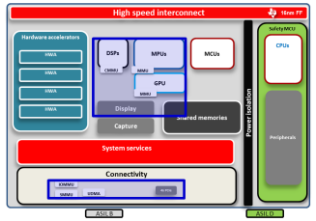
# Virtualization features

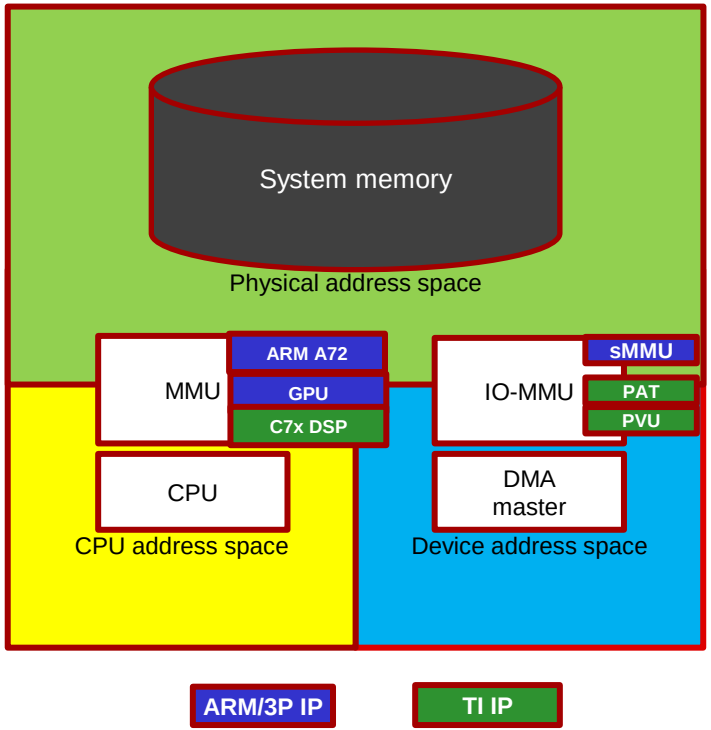
- Key features and benefits
- Heterogeneous processing cores
- Application-specific hardware accelerators
- Device management architecture
- Memory architecture and data movement
- Safety and isolation features
- **Virtualization features**
- Security features
- Power management features
- Network connectivity
- Flash and storage
- Serial connectivity



# Virtualization features

- Memory Management Unit (MMU)
  - CPU 2-stage MMUs: A72, C71x, GPU (PVU as 2nd stage)
- IO-MMU
  - System MMU (sMMU):
    - Standard ARMv3 SMMU 2-stage system MMU
    - Support for PCIe Single-Root I/O Virtualization (SRIOV)
  - TI IO-MMU – Peripheral Virtualization Unit (PVU):
    - Deterministic address translation for real-time data (e.g. DSS)
    - Channelized Translation Lookaside Buffer (TLB); SW-triggered Flexible page size
- Page-based Address Translator (PAT):
  - Fine-grain, real-time address translation (4/16/64KB or 1MB)
  - Supports deterministic scatter-gather /defragmentation (e.g. display)
  - Address-mapped translation space
- Peripheral support:
  - DSS virtualized ownership of pipe and overlay management
  - GPU virtual resource manager
  - ARM generic interrupt controller (GIC-500)



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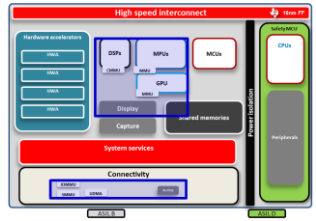


GIC

A72

R5F

R5F

C7x+ MMA

8 virtual GPUs

GPU

4 independent display pipelines

DSS

Up to 64 flows

Ethernet

Virtualized endpoints

PCIe

Rest of peripherals

MMU

MMU

MMU

Credentials mapping

PVU + PAT

sMMU

Address translation + resource isolation

Firewalls – per channel basis

Memory

Peripheral configuration

DMA configuration

# Jacinto™ 7 processors: security management

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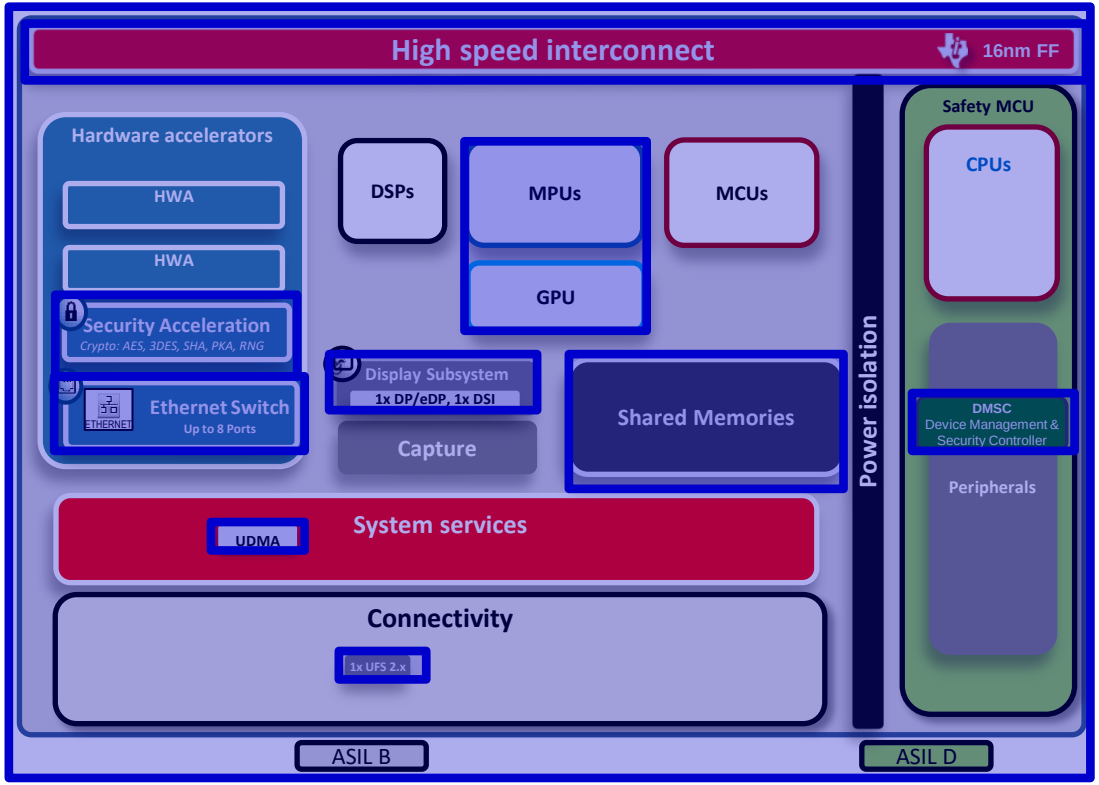
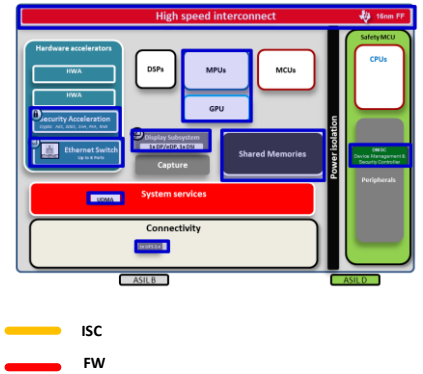
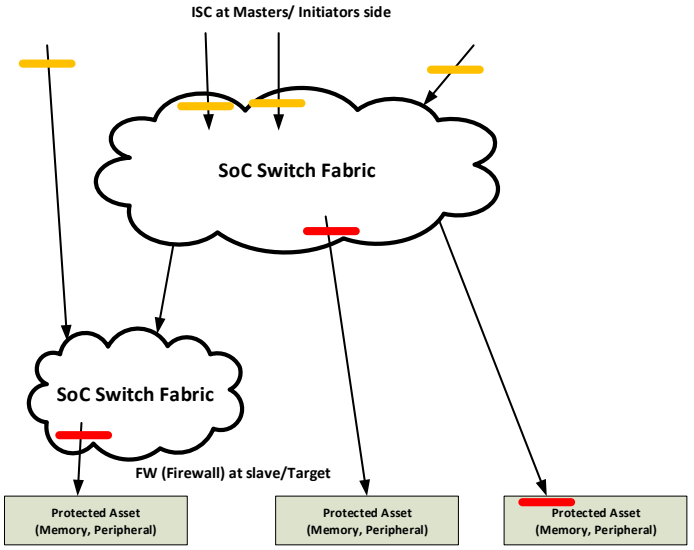


# Security management features

- Secure boot and runtime security support
- Customer-securable device via One-Time-Programmable (OTP) ROM
- DMSC (Arm Cortex-M3) security manager:
  - Sandbox concept for base root of trust
  - Secure messaging for all requests to DMSC
- Endpoint protection:
  - Initiator-Side Security Control (ISC)
  - Firewalls: Peripheral, Channelized, Memory
- Central hardware cryptography:
  - Multiple algorithms implemented in hardware
    - SHA2, AES, etc.
  - DMA flows route-able to or from crypto engines
  - Permissions controlled by DMSC
- IP/peripheral features
  - Cryptography required by standards (EDP, UFS, etc.)
  - GPU/decoder/DSS/Ethernet secure features
- Arm TrustZone



# Jacinto™ 7 processors: power management

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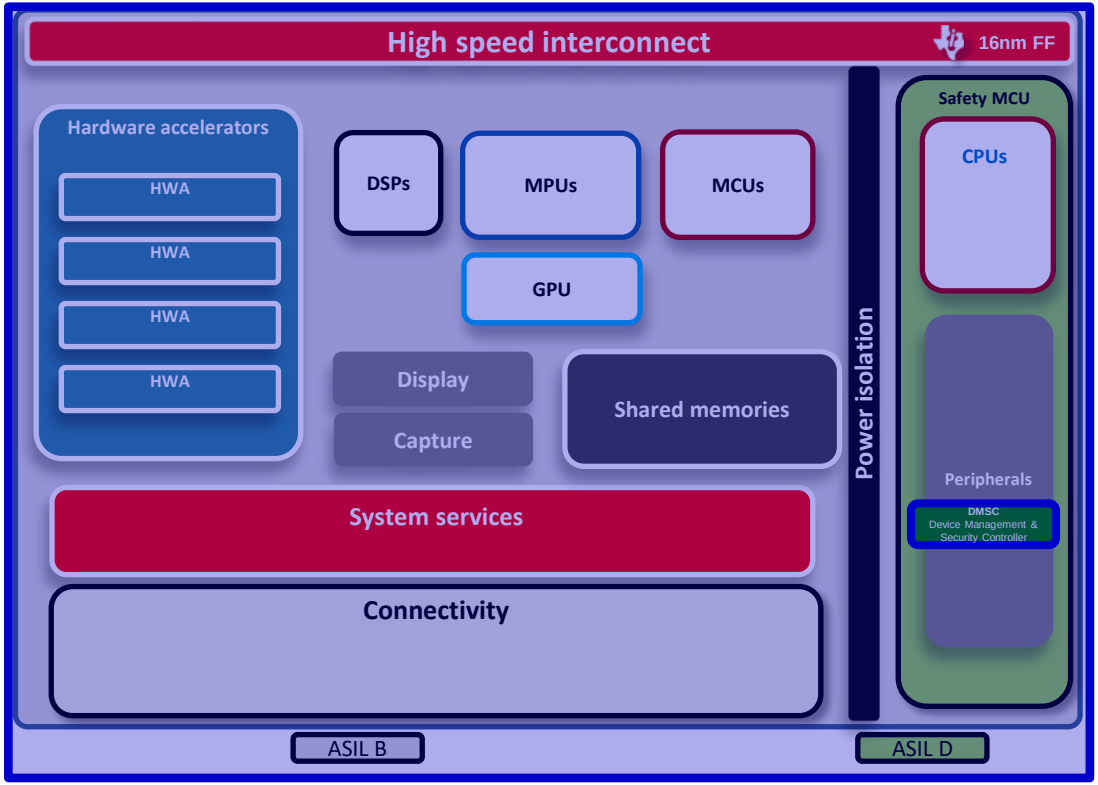
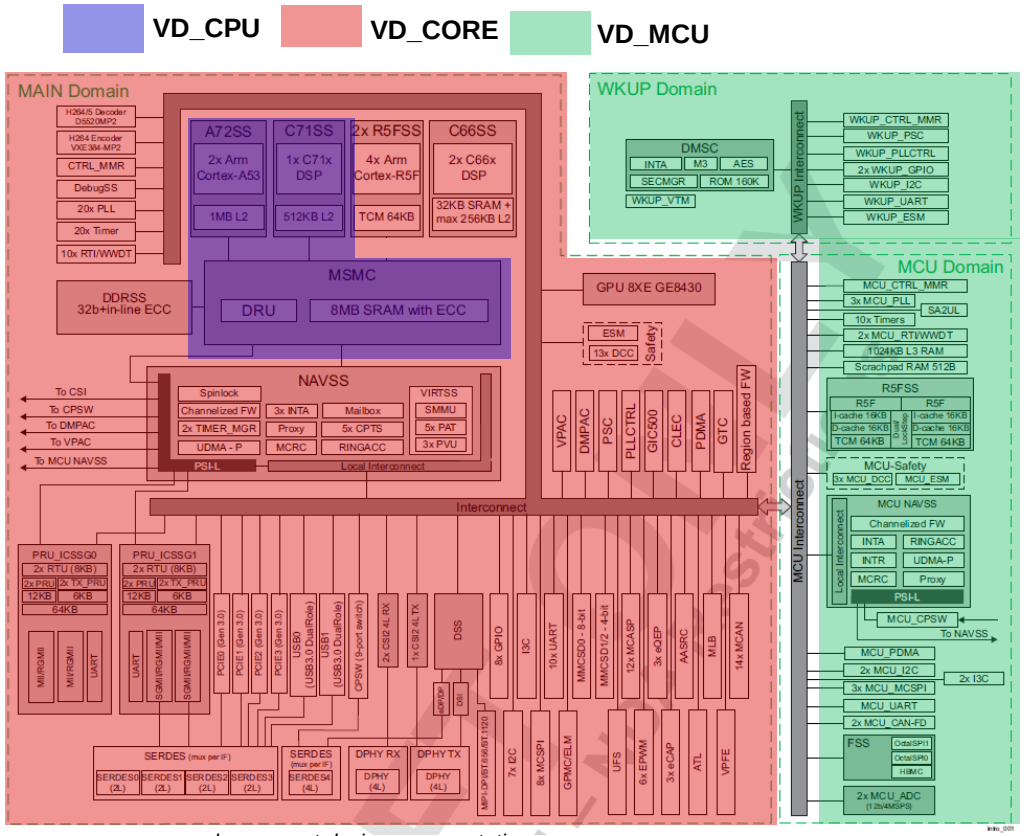


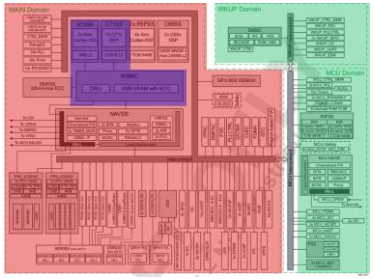
# Power management features

- Voltage domains (AVS, power modes):
  - Adaptive voltage scaling for main CPUs
  - Shut off Main during MCU-only mode
- Power domains:
  - Internally-switched domains on major core/IP
- Clocking control:
  - Multiple PLL for fine-grain clock control
  - Dynamic Frequency Scaling (DFS)
  - Clock gating (SW and automatic)
- Power management IP:
  - Wake-up (WKUP) domain
  - Power-OK (POK) voltage detectors
  - Power glitch detectors (PGD)
  - Temperature sensors (per major domain)
  - Thermal diode




*example superset device representation*

# Power management features



high

Total power

low

Power modes:

- ***ACTIVE**: All rails on, cores/peripherals active
- **Standby:** Arm CPU WFI (wait for interrupt) mode, system idled
- **Core power domain OFF:** All main power domains OFF, MCU on
- **Deep sleep:** All main power domains OFF, MCU Arm Cortex-R5 CPU off
- ***MCU-only:** Main voltage domain OFF, MCU on
- **Suspend2RAM:** All rails off except DDR IO, DDR in self-refresh mode

** NOTE: Can boot directly into MCU-only or ACTIVE mode*

# For more information

- For more training on Jacinto 7 processors: http://training.ti.com/jacinto7
- Download Processor SDK Automotive for Jacinto 7 processors: http://www.ti.com/tool/PROCESSOR-SDK-DRA8X-TDA4X
- Order TDA4VM Jacinto Automotive processors for ADAS & autonomous vehicles: http://www.ti.com/product/TDA4VM
- Order the TDA4VMx evaluation module: http://www.ti.com/tool/TDA4VMXEVM
- Order DRA829V Jacinto Automotive processors for gateway & vehicle compute: http://www.ti.com/product/DRA829V
- Order the DRA829Vx evaluation module: http://www.ti.com/tool/DRA829VXEVM
- For questions regarding topics covered in this training, visit the processors support forum at the TI E2E Community website: https://e2e.ti.com