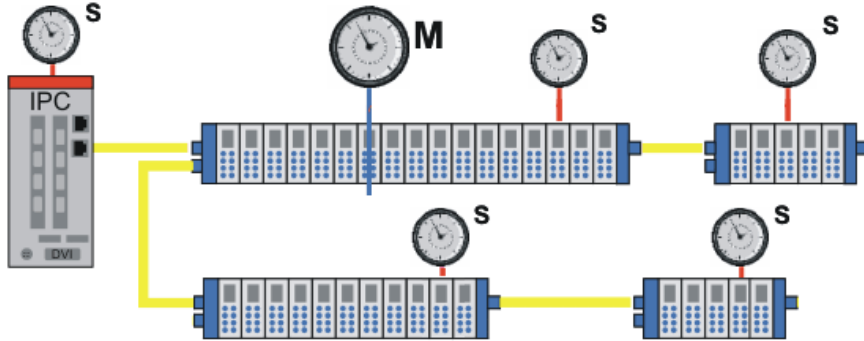


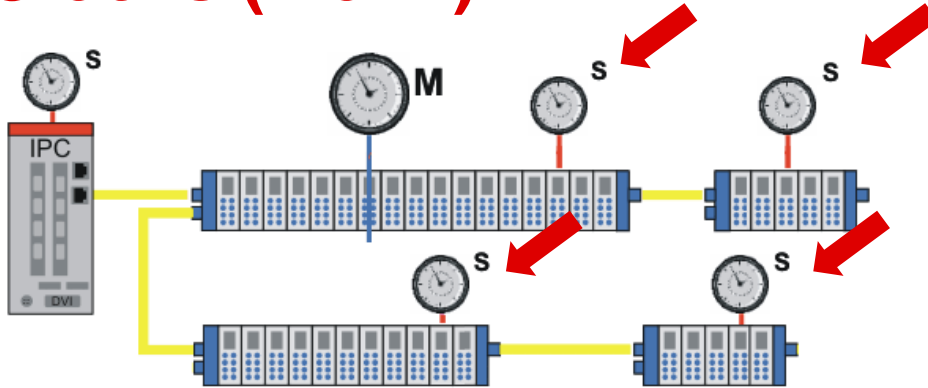
EtherCAT Feature: Distributed Clocks

Distributed Clocks (1 of 2)



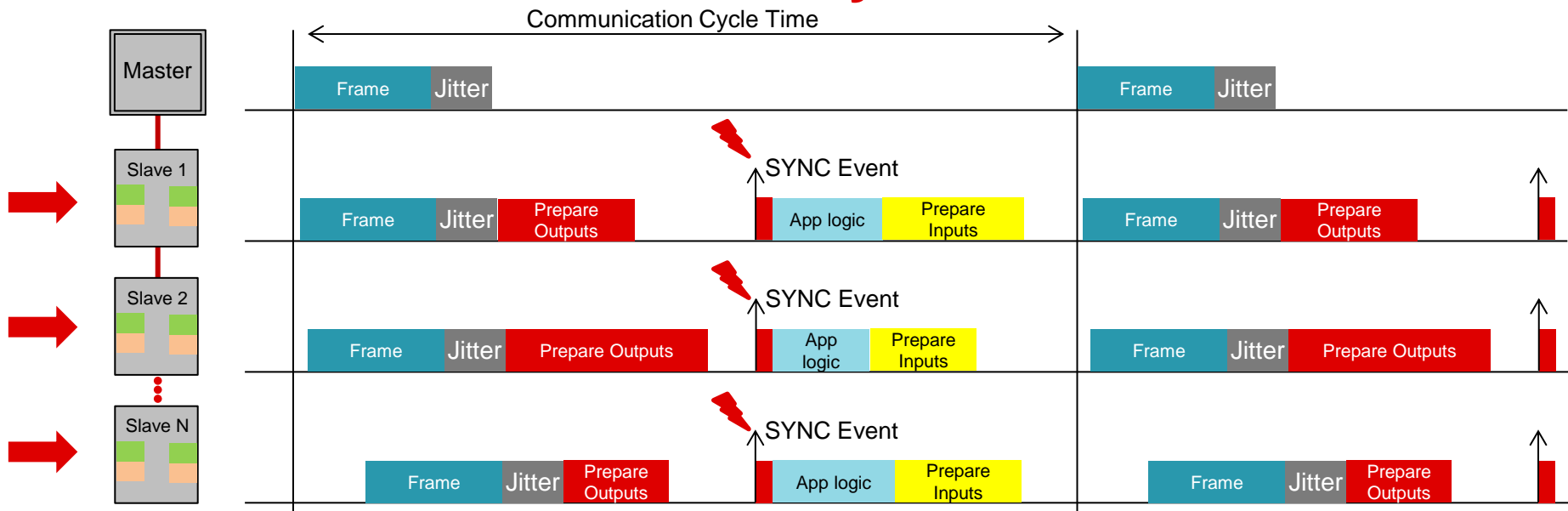
- Distributed Clocks (DC) enables all EtherCAT devices (master and slaves) on the network to share the same EtherCAT system time (Nanosecond resolution)
- EtherCAT master maintains the reference clock which is typically the first ESC in network with DC capability

Distributed Clocks (2 of 2)



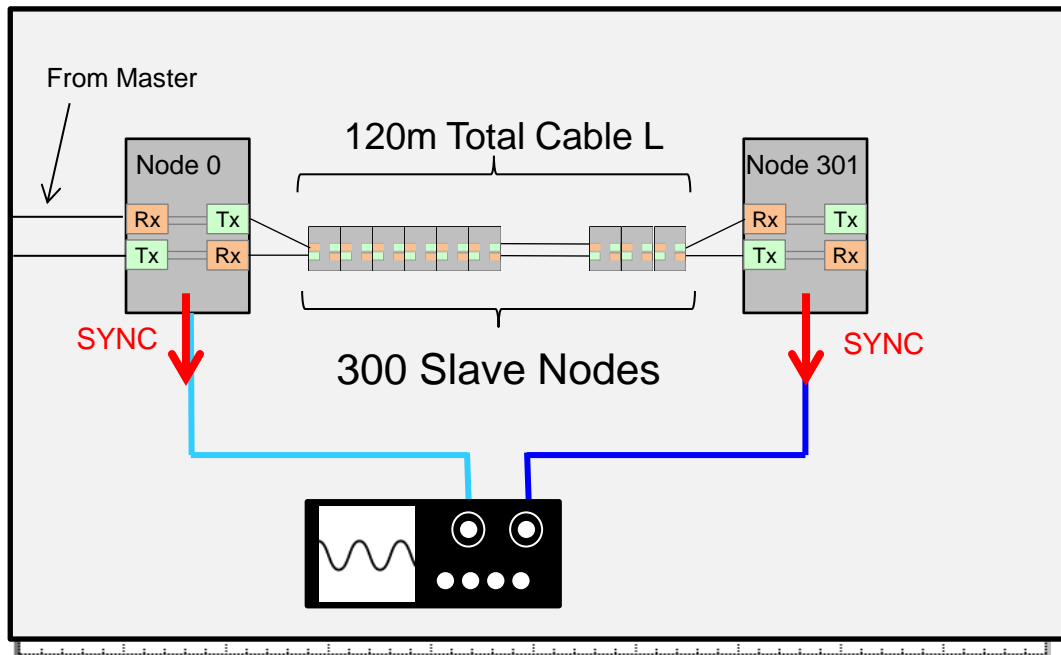
- The master queries the slaves to determine the drift of the local clock for each ESC with regards to the reference clock and programs the adjustment in each respective ESC. Master continues to adjust reference clock on each ESC.
- SYNC Events – Generated to a synchronized EtherCAT system time
 - Can be used to trigger system events such as interrupts or synchronize peripherals such as PWMs, ECAPs, etc
- Latch Events – Generated to capture time stamps for external signals
 - Can capture time stamps from sources such as pin, NMI, GPTRIPOUTx, PWMXBAROUT, etc

Distributed Clocks – Slave Synchronization



- With DC enabled, all the DC-enabled slaves on the network synchronize to the SYNC event
- Regardless of the frame delay, jitter, or required preparation, the SYNC event occurs at the same time across the network to execute the slave app logic

Distributed Clocks – Synchronization Delay



Clock Synchronization Process

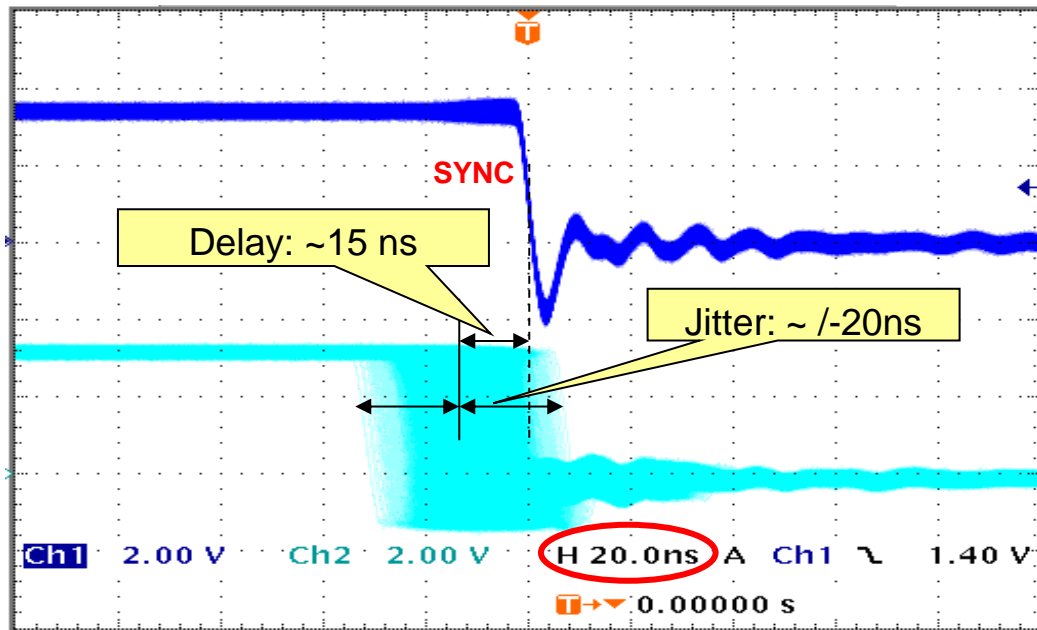
- Master sends clock sync packages
- Slave provides local clock to Master
- Master calculates **offset** between reference and slave clocks
- Slave adds **offset** to local clock (same system time)
- Master **sends repeating clock sync packages** for drift compensation

RESULT:

Clocks are synchronized,
with jitter and delay $\ll 100\text{ns}$

Note: The ESC IP requires a source clock frequency accuracy of 25PPM

Distributed Clocks – Synchronization Delay



Clock Synchronization Process

- Master sends clock sync packages
- Slave provides local clock to Master
- Master calculates **offset** between reference and slave clocks
- Slave adds **offset** to local clock (same system time)
- Master **sends repeating clock sync packages** for drift compensation

RESULT:

Clocks are synchronized,
with jitter and delay << 100ns

Note: The ESC IP requires a source clock frequency accuracy of 25PPM

More Information on EtherCAT



www.ethercat.org