Design 3: PCB Layout Guidelines for Motor Drivers

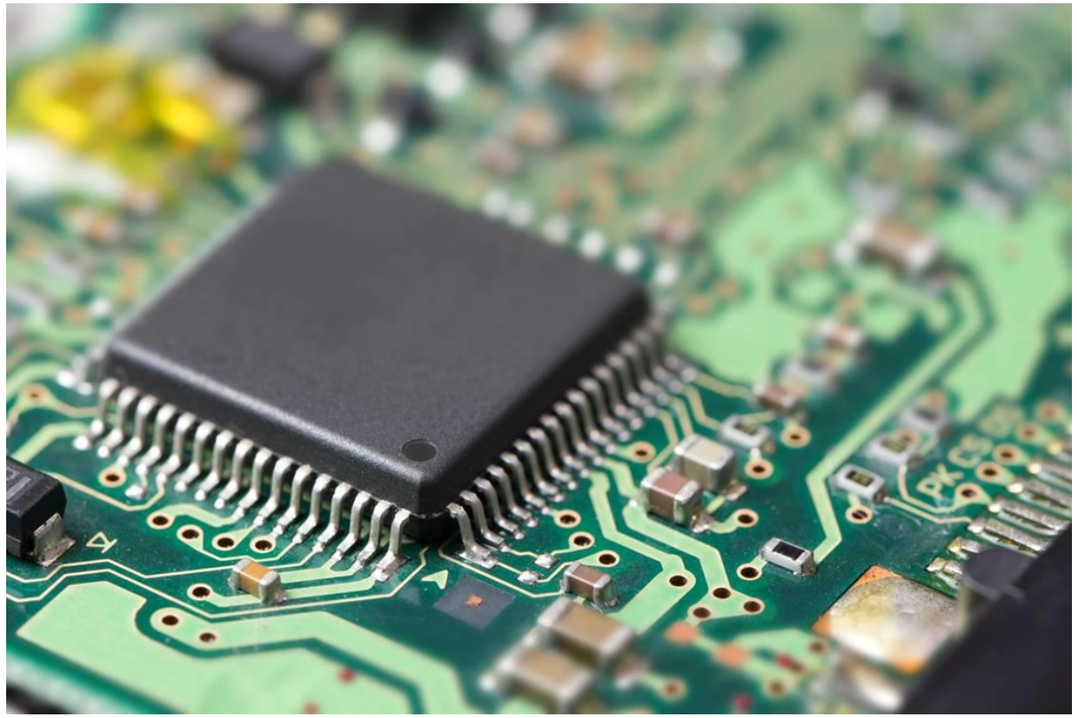
TI Precision Labs – Motor Drivers

Presented and prepared by Pablo Armet

Table of contents

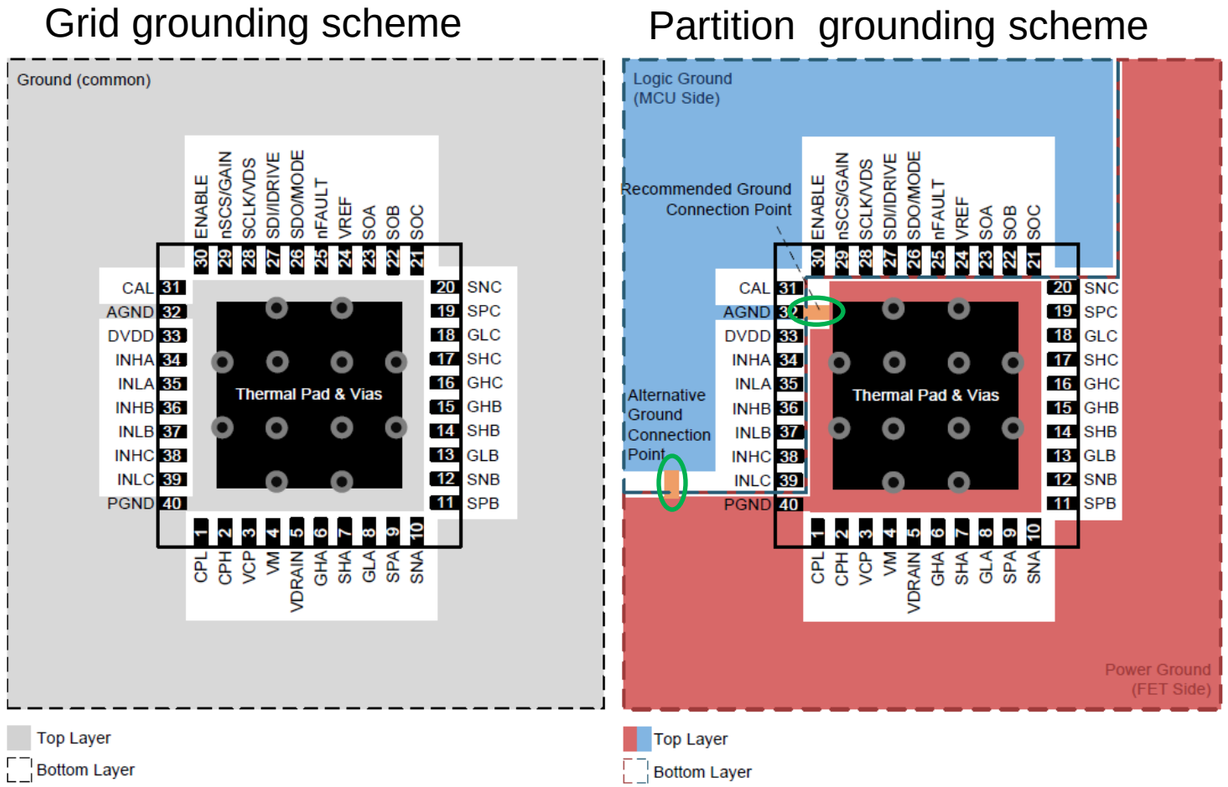
Importance of good PCB layout in motor drivers

- Bad PCB layout can cause issues such as:
  - Poor thermal performance
  - Capacitive and inductive coupling
  - Common and differential noise
  - Increased EMI noise



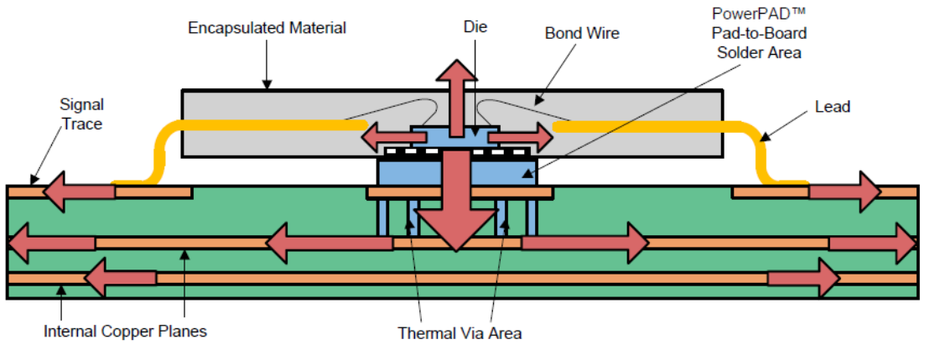
Grounding optimization

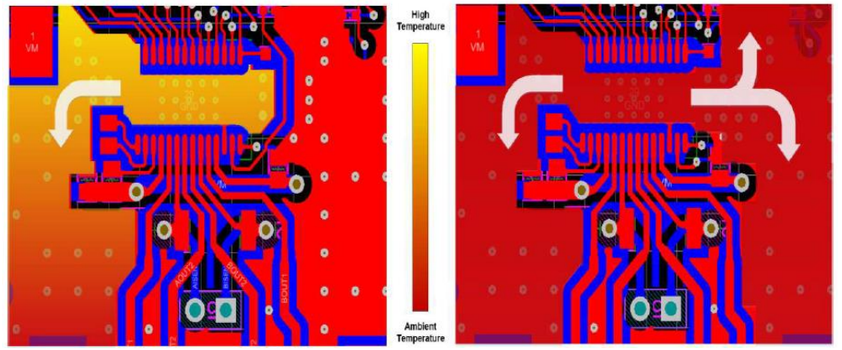
- Common grounding schemes:
  - Partition
  - Grid
- General grounding techniques:
  - Have a continuous ground plane
  - Maximize the amount of GND copper on the PCB
  - Minimize ground plane discontinuity



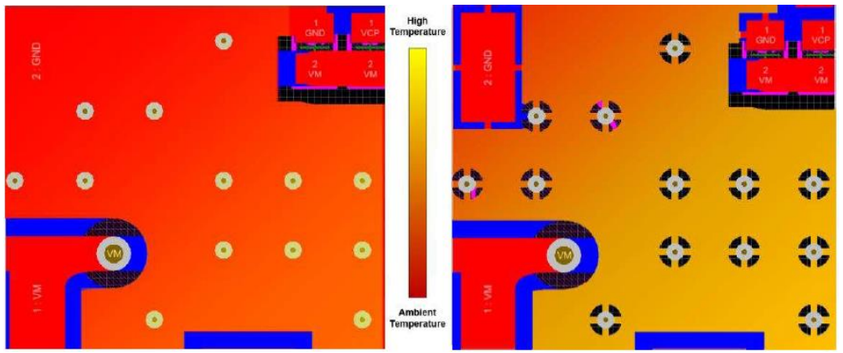
Improving thermal performance

- Heat dissipation paths:
  - Most of the heat is dissipated to the PCB
  - Some of the heat is dissipated to the open-air environment
- General thermal improving layout techniques:
  - Continuous top-layer pours from thermal pad to ground planes
  - Use 1.5-oz or 2-oz copper thickness
  - Use direct-connect thermal vias
  - Use 8 mil by 20 mil thermal via size
  - Group thermal vias into arrays





Discontinuous pour Continuous pour

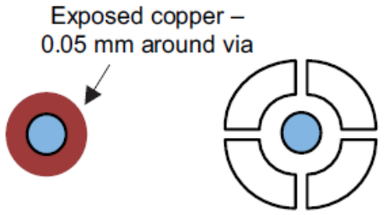


Direct-connect vias Thermal relief vias

Vias

- General via layout and placement techniques:
  - Use vias with solid exposed copper
  - Choose the appropriate via size and quantity for the appropriate current capacity needs
  - Place multi-vias or “via stitching” to power and ground planes when needed to route to another layer.
  - Don’t place vias too close to each other

1



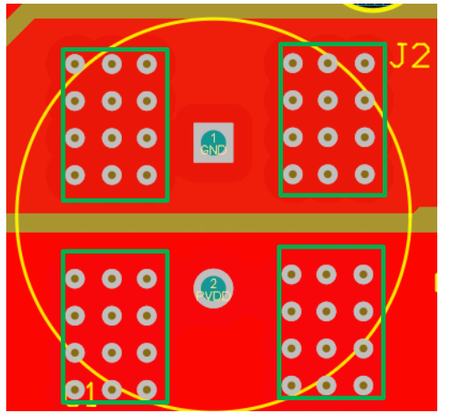
Solid Via
Recommended

Web or Spoke Via
NOT Recommended

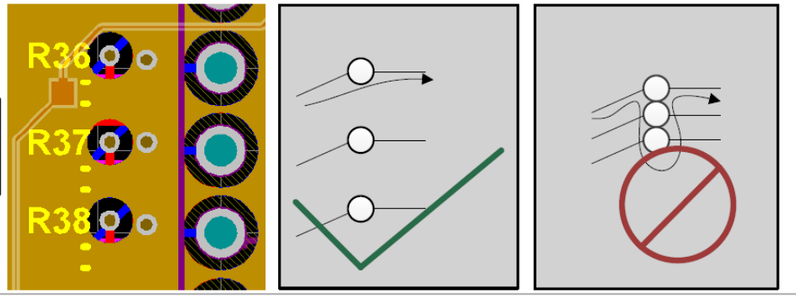
2

Via Diameter	Current Capacity
6 mil	0.2 A
8 mil	0.55 A
10 mil	0.81 A
12 mil	0.84 A
16 mil	1.1 A

3

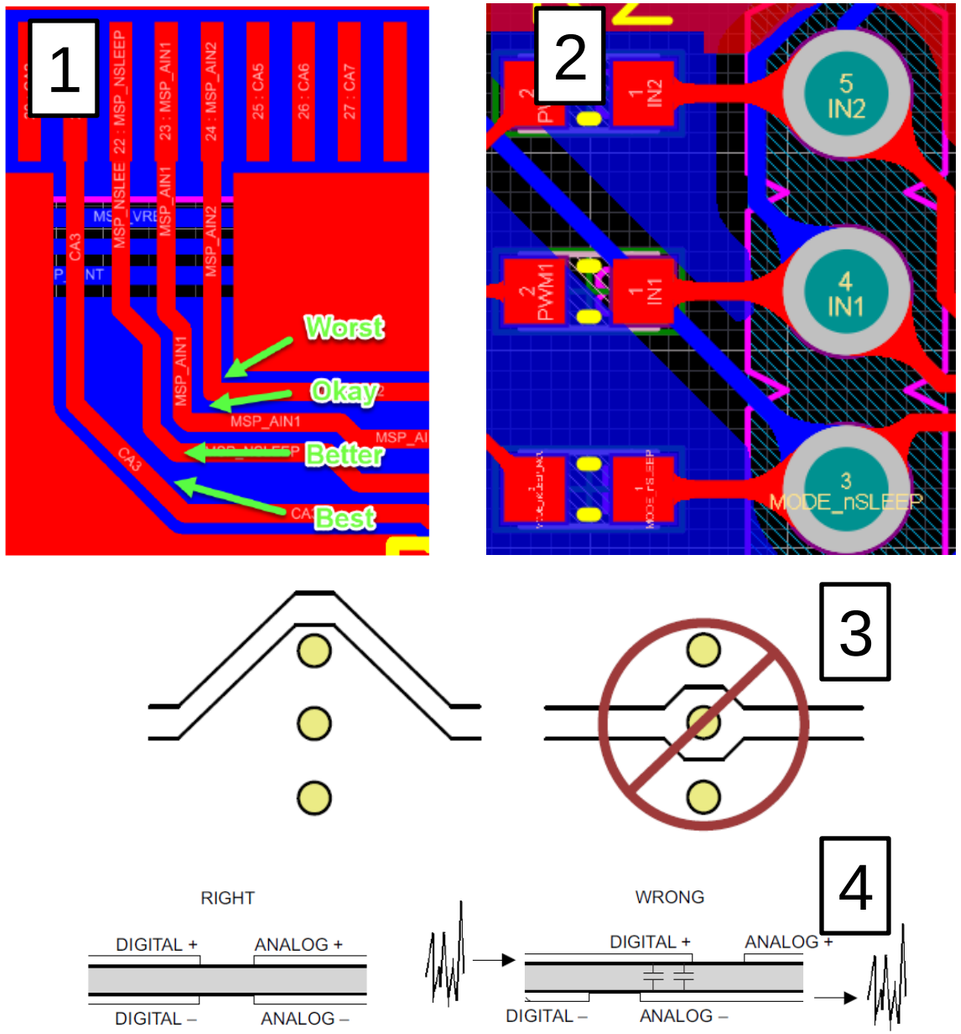


4



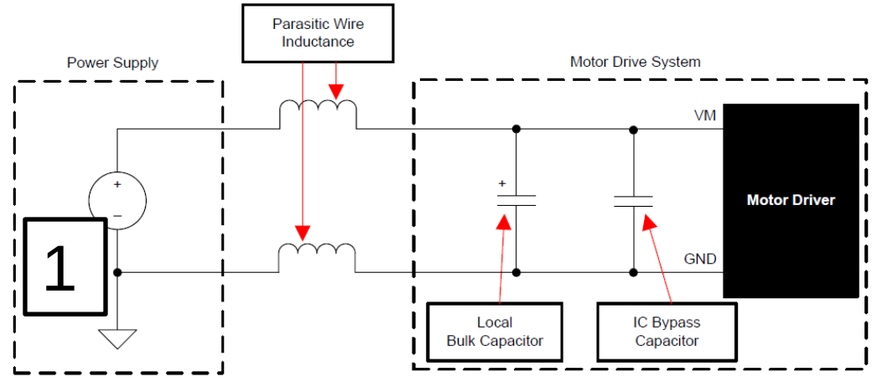
General routing techniques

- Make gate drive traces as wide and short in length as possible
- For gate drivers, route the high-side gate and the switch node trace as close as possible
- Do NOT use right-angle traces
- Use the “teardrop” technique when transitioning from a vias to pads
- Route traces in parallel pairs when routing around an object
- Have separate grounding for analog and digital parts of the circuit



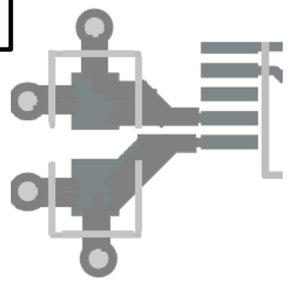
Bulk and bypass capacitor placement

- Place all bulks capacitors near the power entry point of the board
- Place charge pump or bootstrap capacitors as close to the driver as possible
- Place local bypass capacitor on the same layer as the driver and as close to the driver as possible
- Avoid placing vias between the bypass capacitor and the driver
- Use small ceramic capacitors on the power stage to attenuate high frequency current transients
- Place filtering capacitors near the sensing pins of a device with integrated current sense amplifier
- Place capacitors near the voltage regulator output pin for devices with integrated voltage regulators

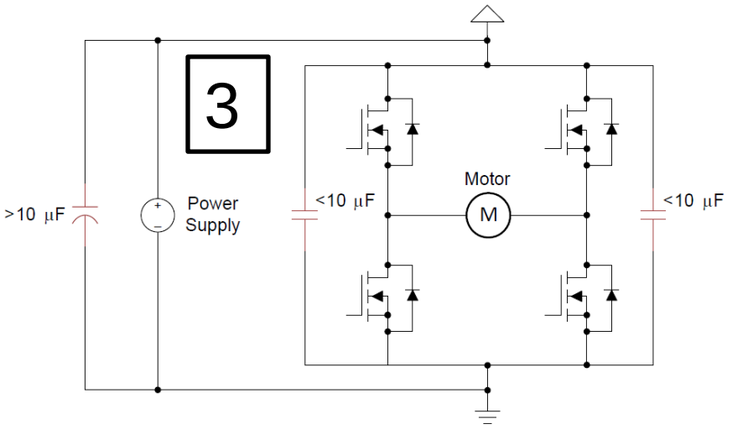


Poor Bypassing

2



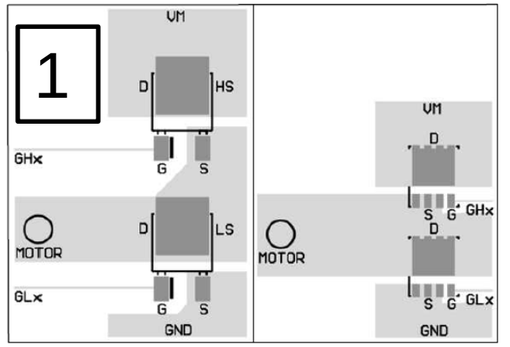
Good Bypassing



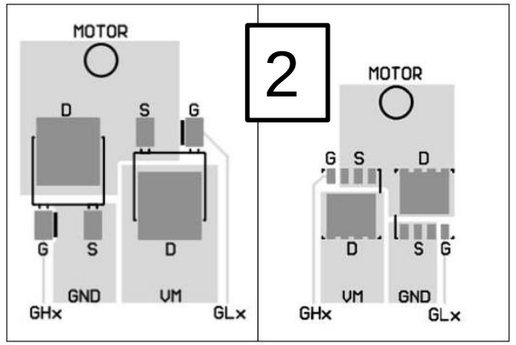
Power stage routing and MOSFET placement

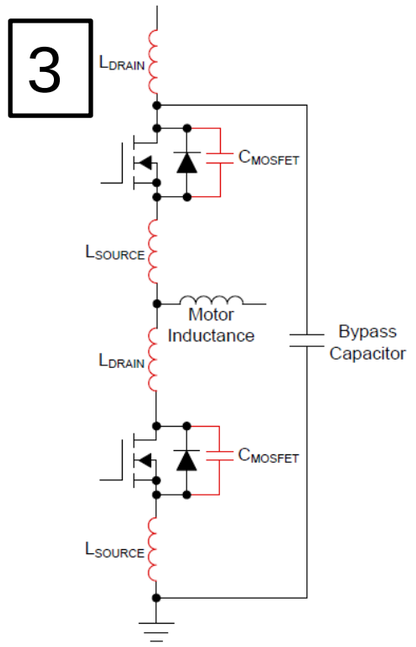
- The MOSFETs should be placed such that the high current loops are minimized
- Minimize the parasitics in the power stage to reduce switch-node ringing oscillations
- Minimize switch-node ringing by external measures such as reducing slew rates or including external snubbers
- Optimize layout for reducing the high current loop path

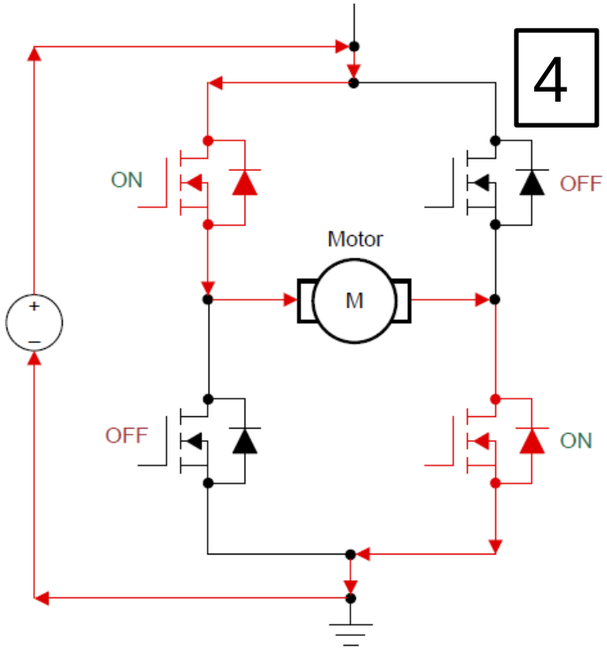
Half-bridge stack configuration



Half-bridge side-by-side configuration







To find more motor driver technical resources and search products, visit ti.com/motordrivers

Resouces

- [1] “Best Practices for Board Layout of Motor Drivers”, ti.com
- [2] “Understanding Smart Gate Drive”, ti.com