TI POWER

Cell balancing considerations for industrial and automotive applications

Battery Management Deep Dive Training

October 2020

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Cell imbalance and its impacts?

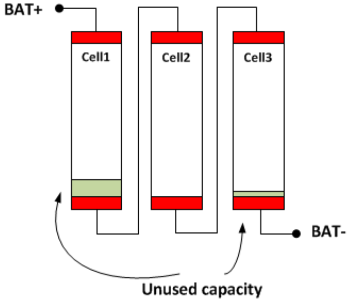
- **What is cell imbalance?**
  - In a multiple cell (in series) battery pack, the cells are mismatched in voltage, especially toward fully charged and fully discharged

- **What are the impacts of the cell imbalance?**
  - Reduction in runtime
    - Premature charge (or early discharge) termination
  - Degrading cycle life of the battery pack
    - Cell stress from cycling above/below voltage limits

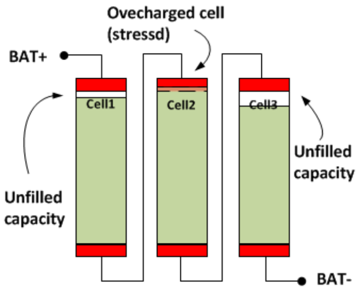
- **How can cell balance help?**
  - Balancing allows cells to reach 100% capacity around the same time, maximizing the runtime and avoid overcharging to stress on the “weaker” cells to maximize cell life

Cell imbalance and its impacts?

- Reduction in runtime

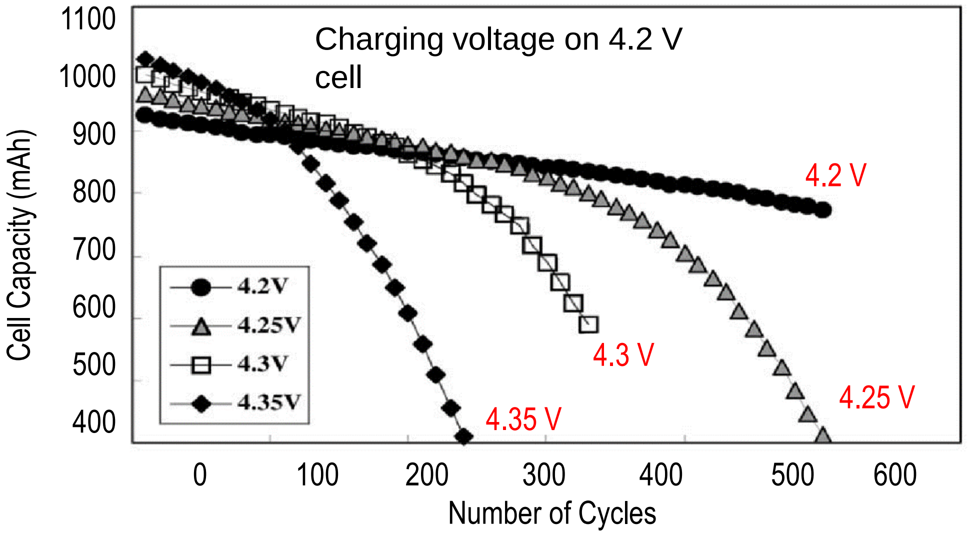


During discharge



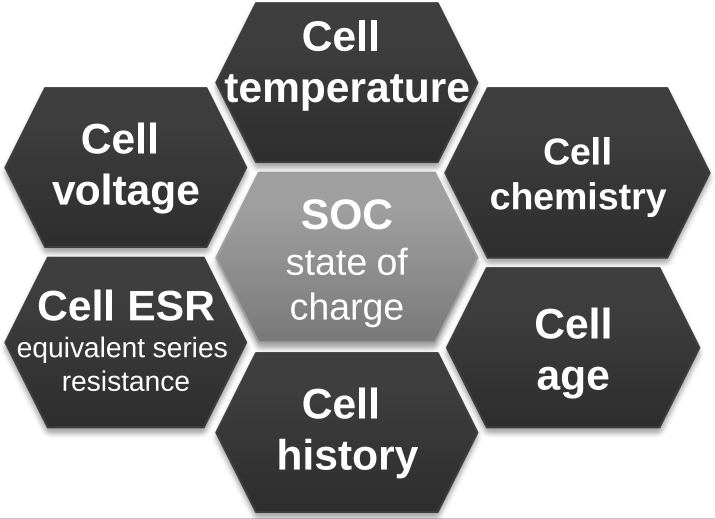
During charge

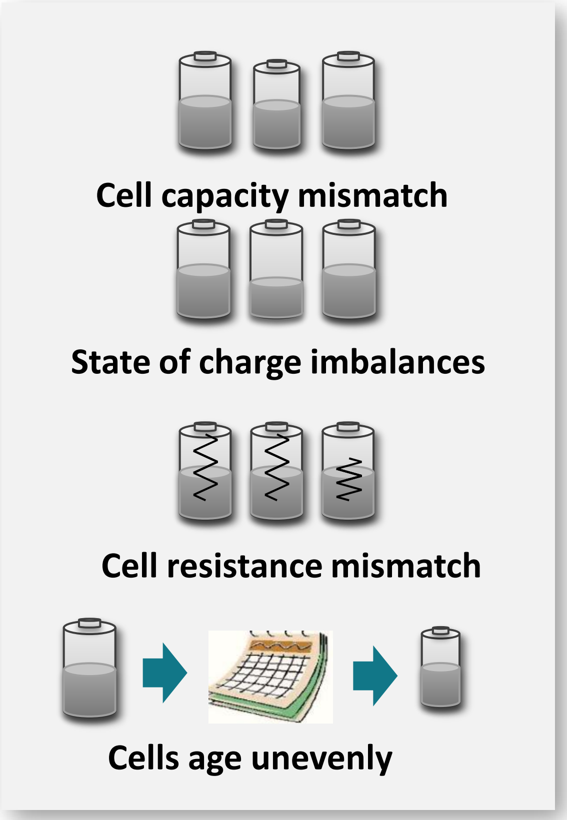
- Degrading cycle life of the battery pack



Cell mismatches

- Cells will have production & grading tolerances
- Cells in series will develop voltage mismatch in use over time
- Mismatches will result in state of charge differences and be observed as voltage





But I use high quality cells…

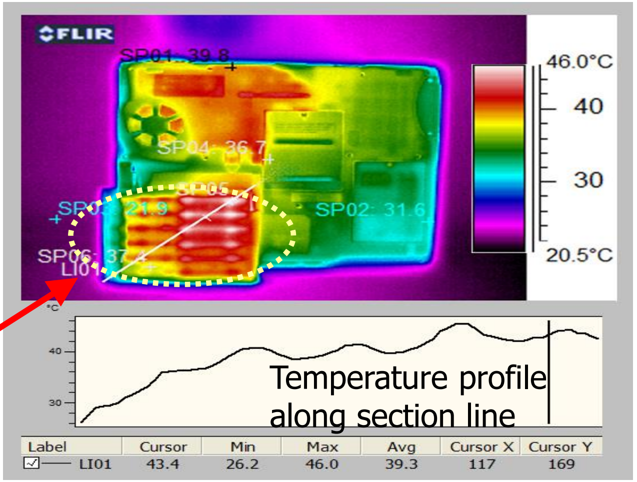
- **High quality cells when new**
  - Closely matched capacity
  - Similar cell impedance

- **There are no perfectly matched cells – over time, voltage delta may show due to**
  - Capacity difference
  - SOC (state of charge) difference
  - Impedance difference

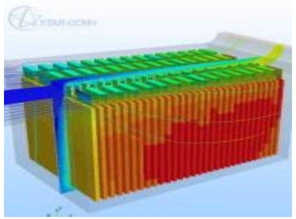
- **Aging rate delta (leads to further impedance differences) can be caused by**
  - Temperature variation across the pack
  - Different stress exposed onto the “weaker” cells during charge and discharge

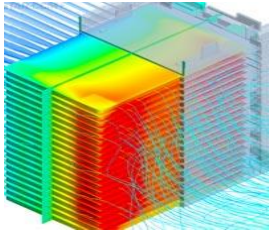
Temperature variation inducing imbalance

- Space-limited design causes local heat imbalance
- Cell degradation accelerated
- Leads to cell imbalance
- System thermal design may reduce imbalance



>10ºC variation between cells





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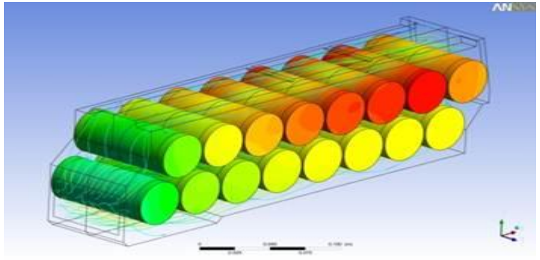

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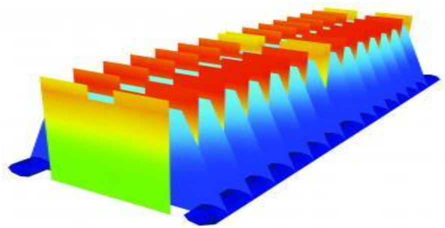
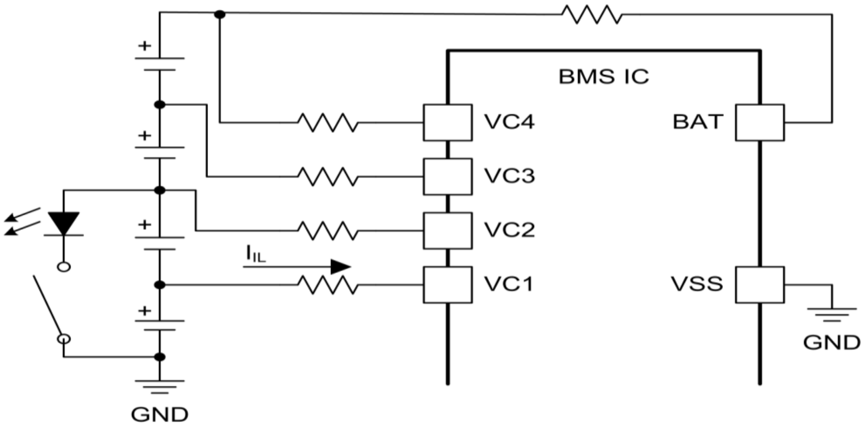


www. ThermoAnalytics.com

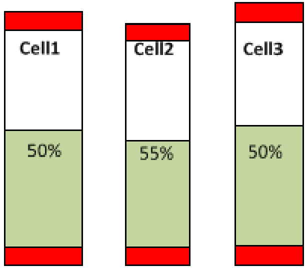
Electronics

- Typically want load to come from complete stack
- Cell monitoring pins may induce imbalance
  - 1µA input or leakage:
    - 1 µA x 24 hrs/day x 365 days/year
    - 8760 µAh/year
    - (8.76 mAh/year)/2000 mAh → 0.44%/year
- Systems with asymmetrical load will need balancing to keep up with load

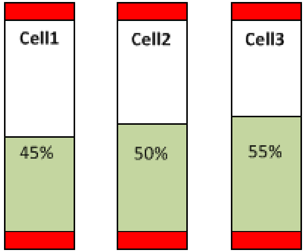


What is imbalance among the cells?

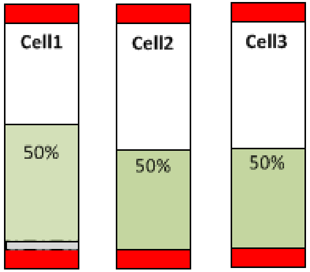
- **Capacity imbalance**
  - Different chemical capacity – with same amount of charge going into the cells, the smaller capacity cell will have higher SOC
  - Over time, the smaller capacity cell will reach OV and UV earlier than the others and be more stressed compared to the others



- **SOC imbalance**
  - Same capacity, but different SOC results in different voltages
  - Over time, the higher SOC cell will reach OV/UV earlier than the others



- **Impedance imbalance**
  - Cell may have the same SOC, but the IR drop (during discharge) or IR increase (during charge) causes the voltage delta among the cells
  - Cell with higher impedance have higher IR and trigger OV/UV prematurely
- All 3 factors above can lead to cell voltage imbalance
- Cell balancing can only balance out the SOC variation



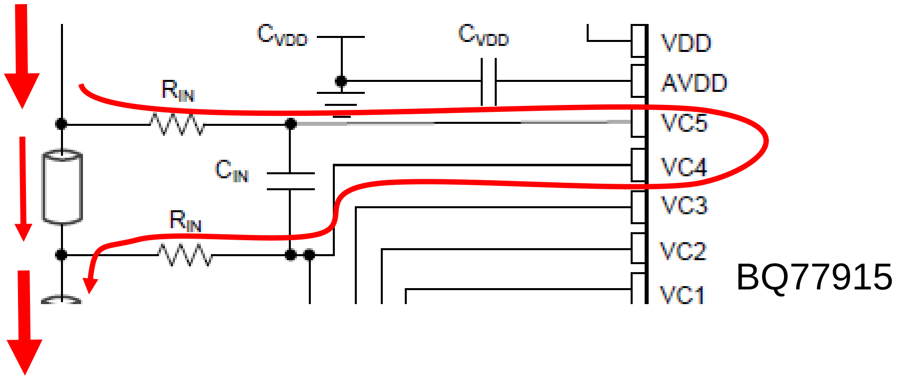
Cell balancing

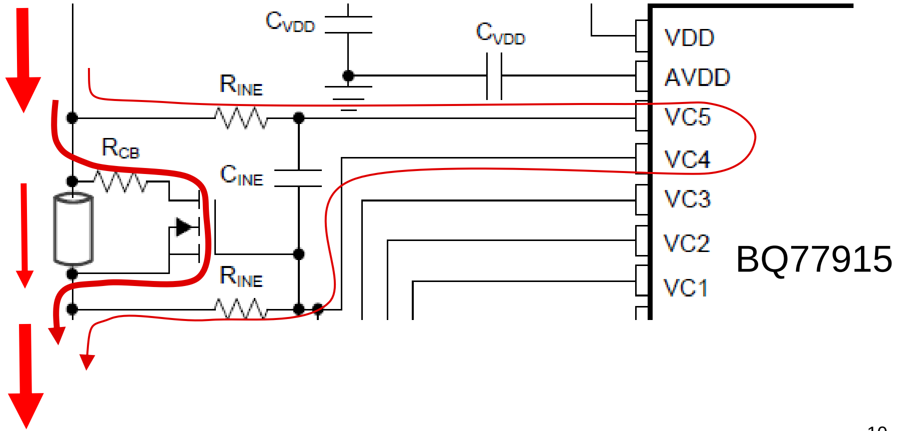
- **Algorithm to identify the cell that needs to be balanced**
  - Voltage based balancing
    - Monitor individual cell voltage and make balancing decision based on cell voltage delta
  - SOC based balancing
    - Track SOC on individual cell and make balancing decision based on SOC delta

- **The method of moving the charge among cells**
  - Passive balancing
    - Bleeding off charge of the “stronger” cell to allow “weaker” cell to catch up (e.g., during charge) or
    - Bleeding off charge of the “stronger” cell to meet the “weaker” cell level (e.g., during relax)
  - Active balancing
    - Transfer charge from “stronger” cell to “weaker” cell

BQ77915 cell balancing mechanism

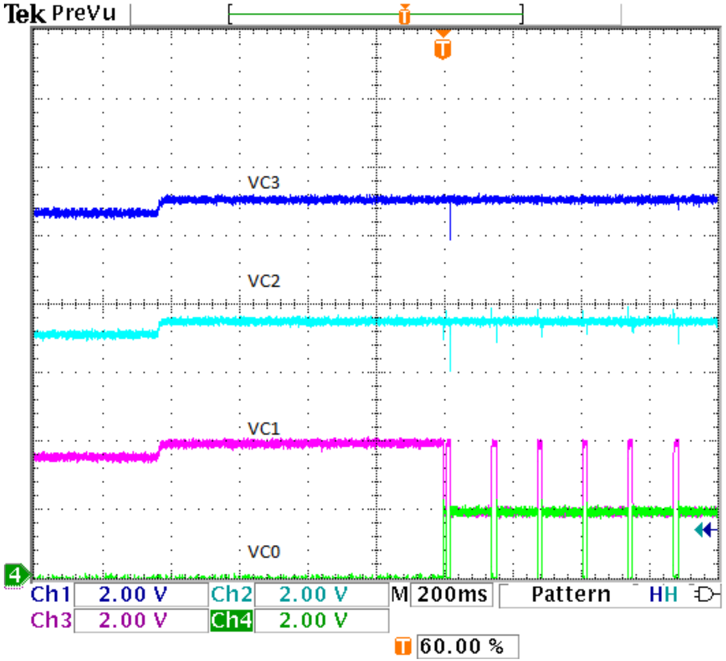
- Passive balancing
  - Lossy
    - Power dissipated in resistors
    - Done during charge
  - Internal current set by input filter resistors
  - External balancing possible
- Voltage balancing
- Enable signal available



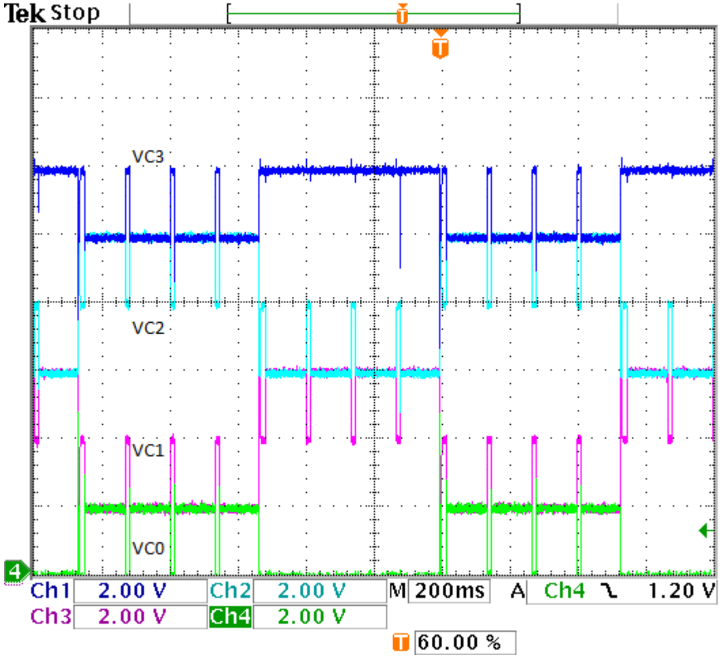


BQ77915 cell balancing

- Duty cycles to measure cells
- Interleaves balancing to avoid adjacent cells



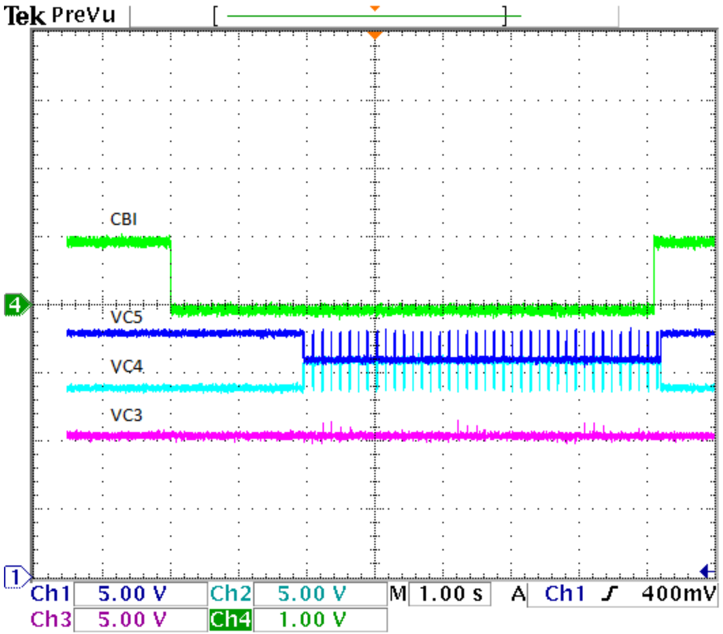
Cell 1 balances



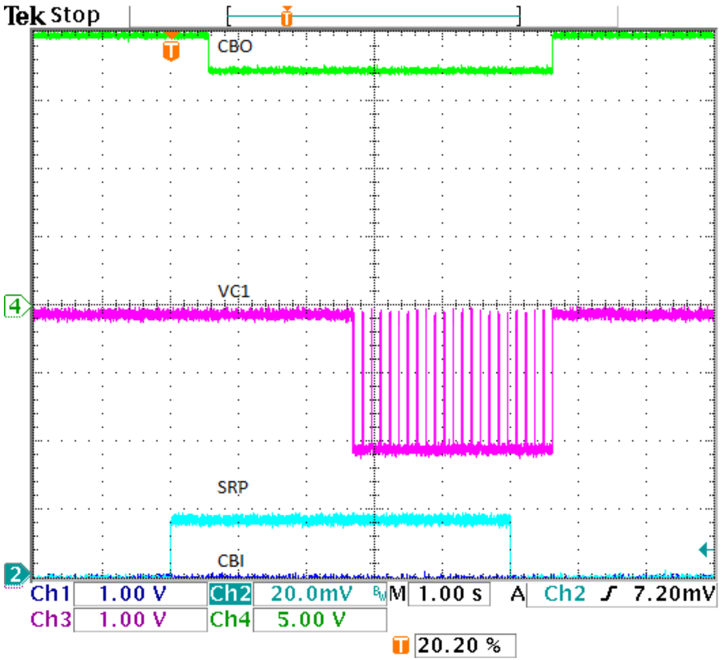
Cells 1, 2, & 3 balance

BQ77915 cell balance enable

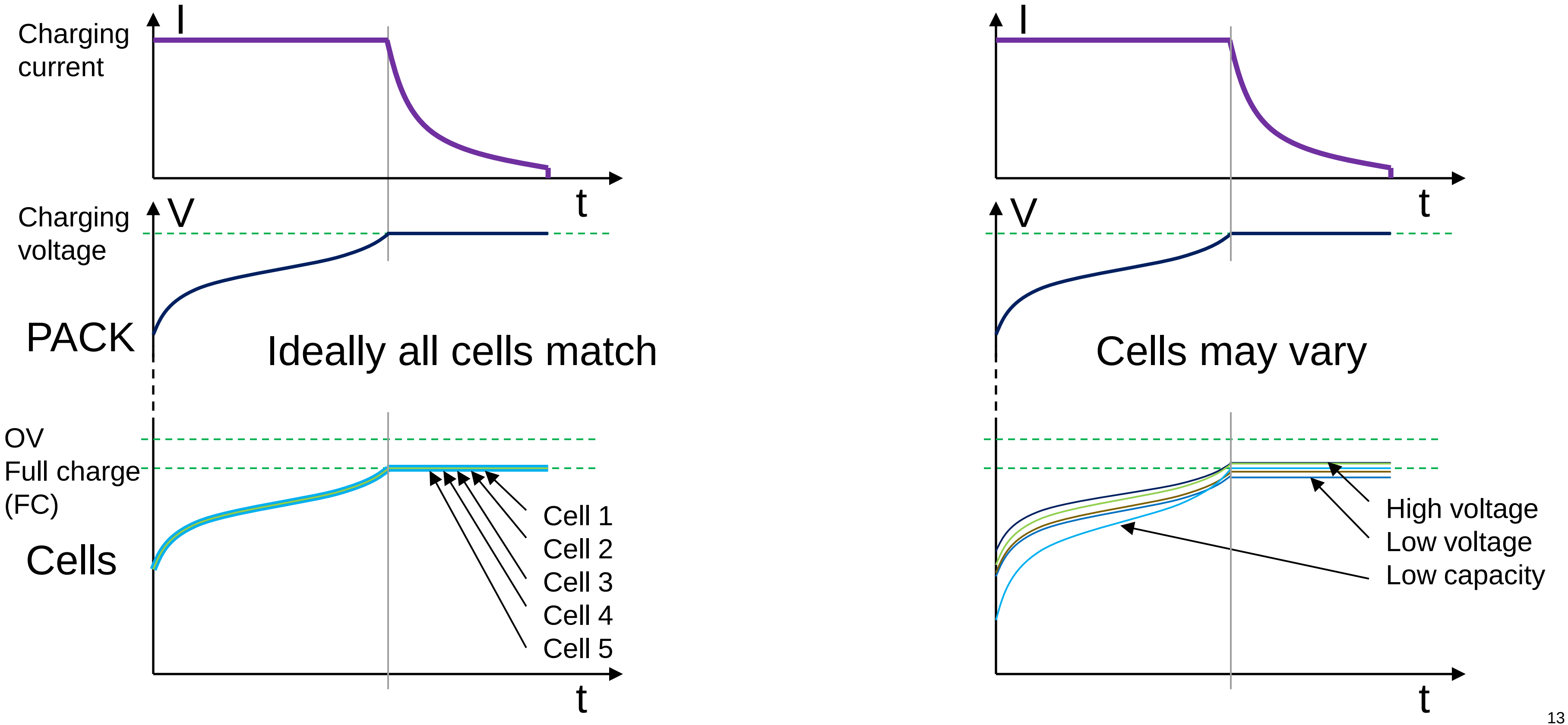
- Enabled through CBI pull down
  - Primarily for configuration and stacking



- Requires current
  - No balance when idle or discharge

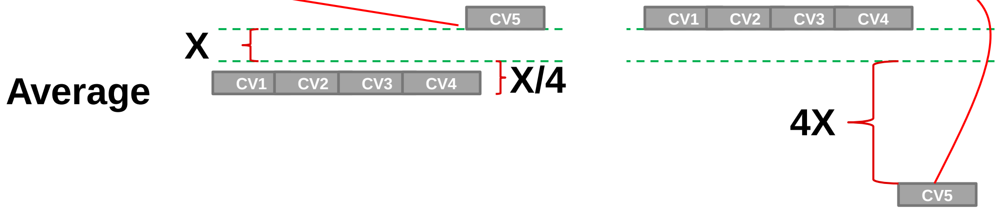


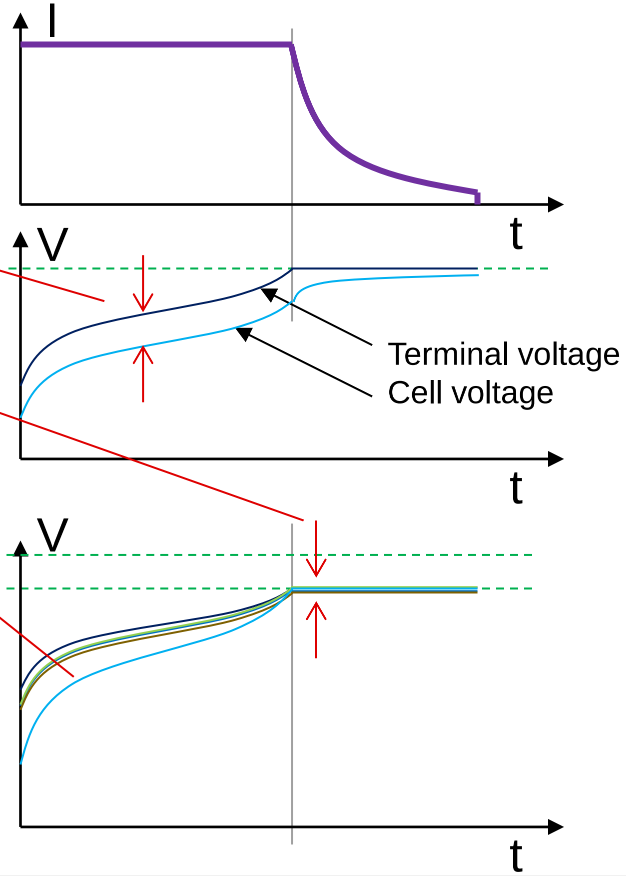
Charging series cells



Voltage cell balancing challenges

- IR drop
  - May balance wrong cell
- Balancing matched cells
  - If they are the same, don't need it
- Capacity difference
  - Large voltage difference at low voltage
- Voltage excursion to a fixed threshold
  - 1 cell high gives small voltage difference
  - 1 cell low gives large voltage difference

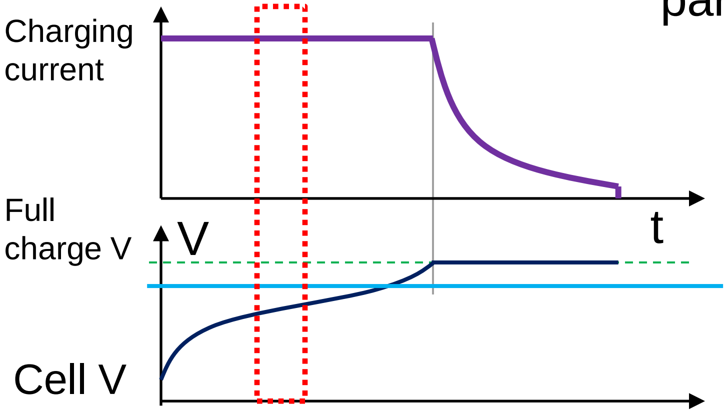


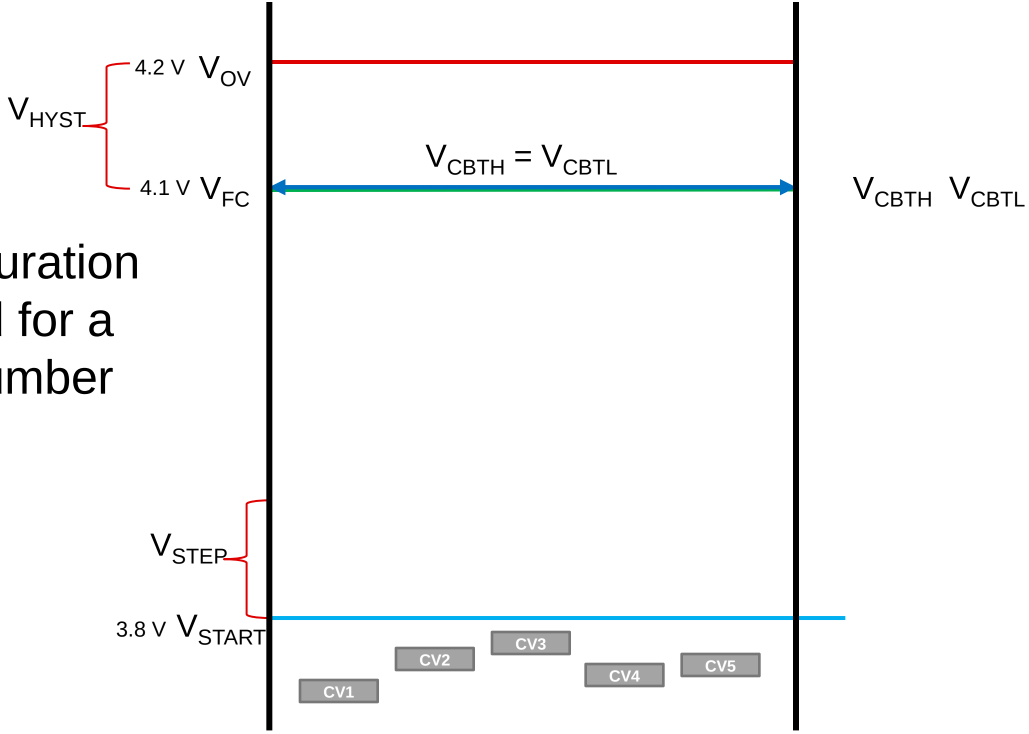


BQ77915 balance algorithm – Below balance

- V_{START} voltage threshold
  - No balance until above threshold
  - Thresholds are parked
  - 3.8 or 3.5 V options
- V_{HYST} and V_{STEP} options
  - 50 to 200 mV, 50 mV steps

Configuration is fixed for a part number

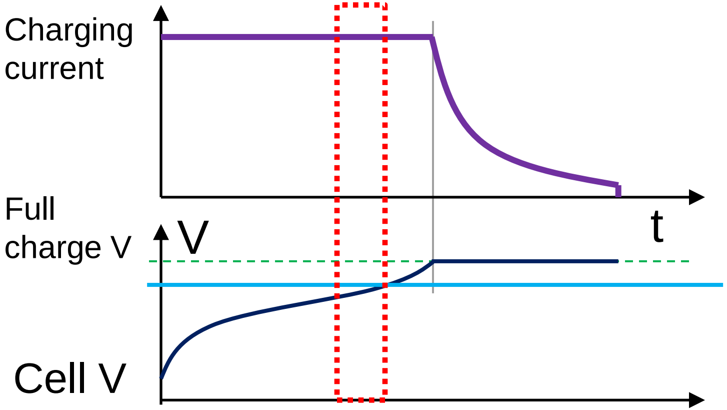


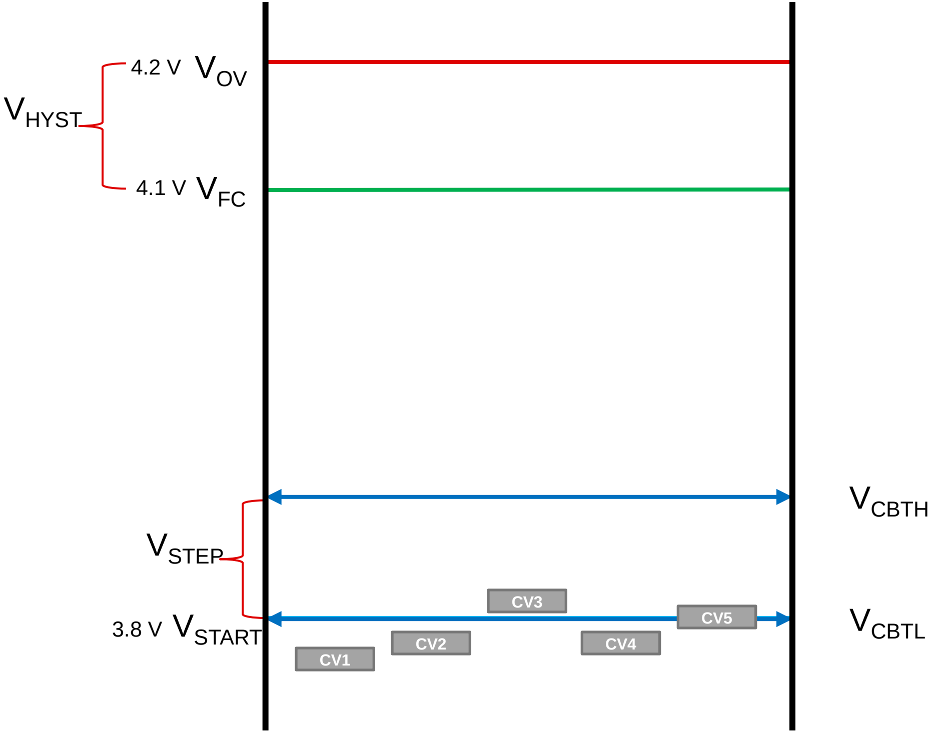


Texas Instruments

Balance start region

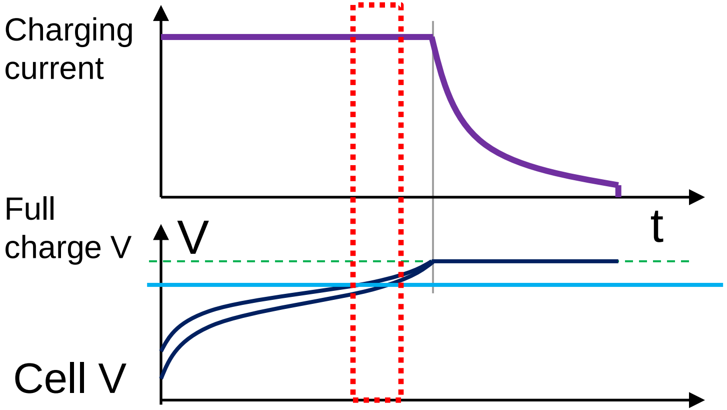
- Cell(s) cross the V_{START} threshold
  - Thresholds are set:
    - V_{CBTL} at V_{START}
    - V_{CBTH} at V_{STEP} above

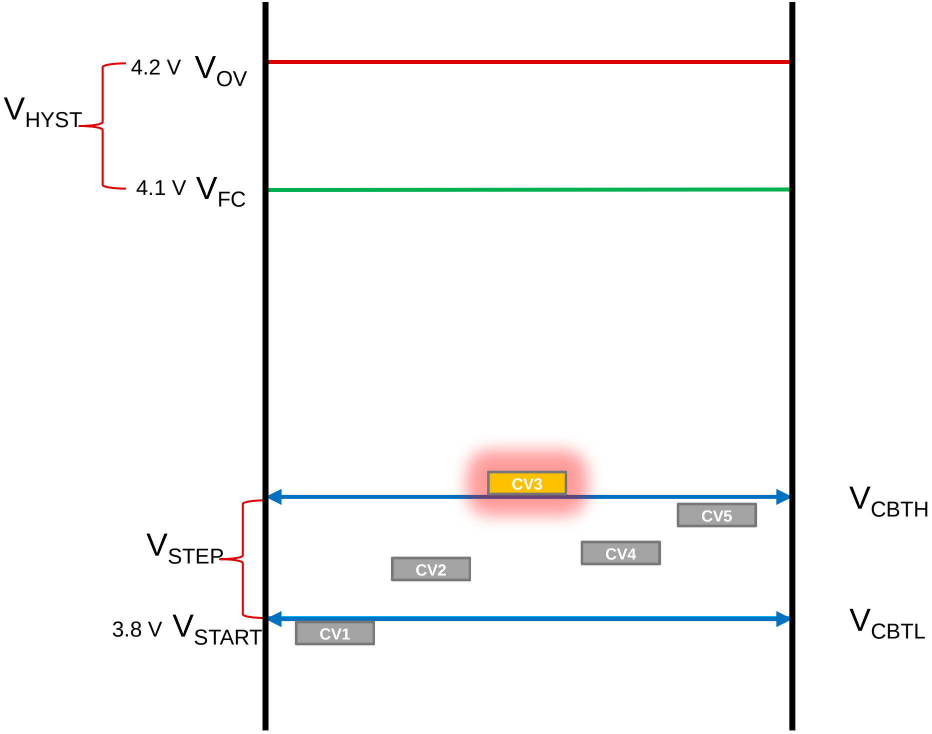




Balance with voltage separation

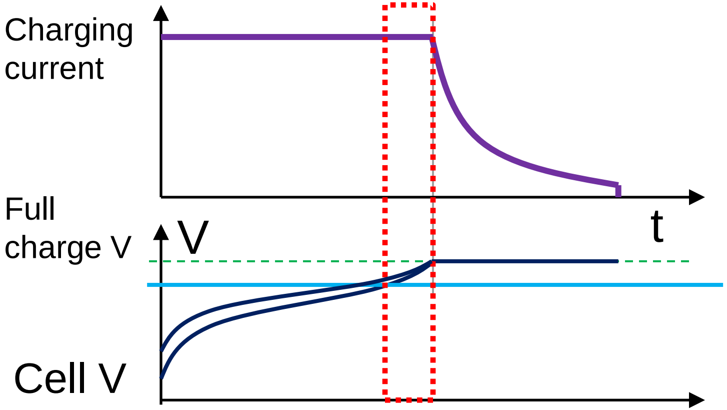
- Cell voltages are widely separated
  - Cell(s) above V_{CBTH}
  - Cell(s) below V_{CBTL}
- Cells above V_{CBTH} balance if:
  - Charge current is present
  - No faults are present

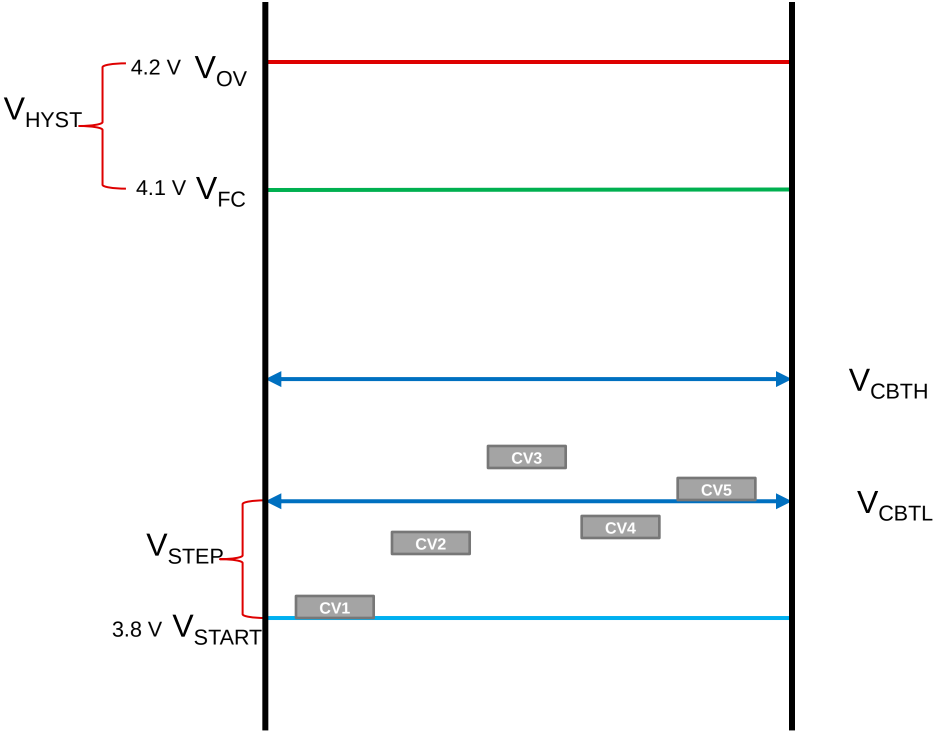




Balance window increment

- When cells are above V_{CBTL}, both thresholds increment by V_{STEP}
  - Balancing may stop

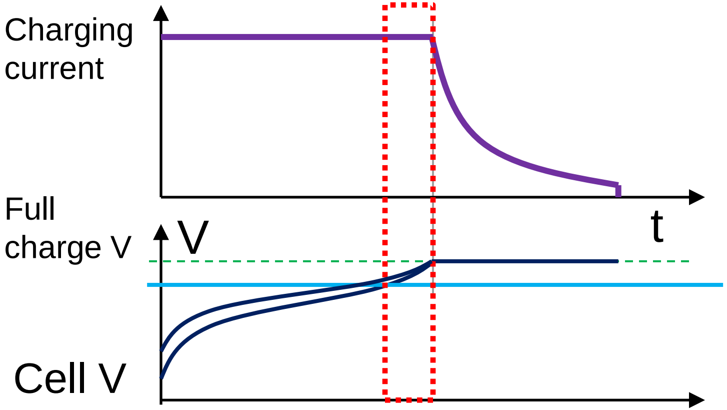


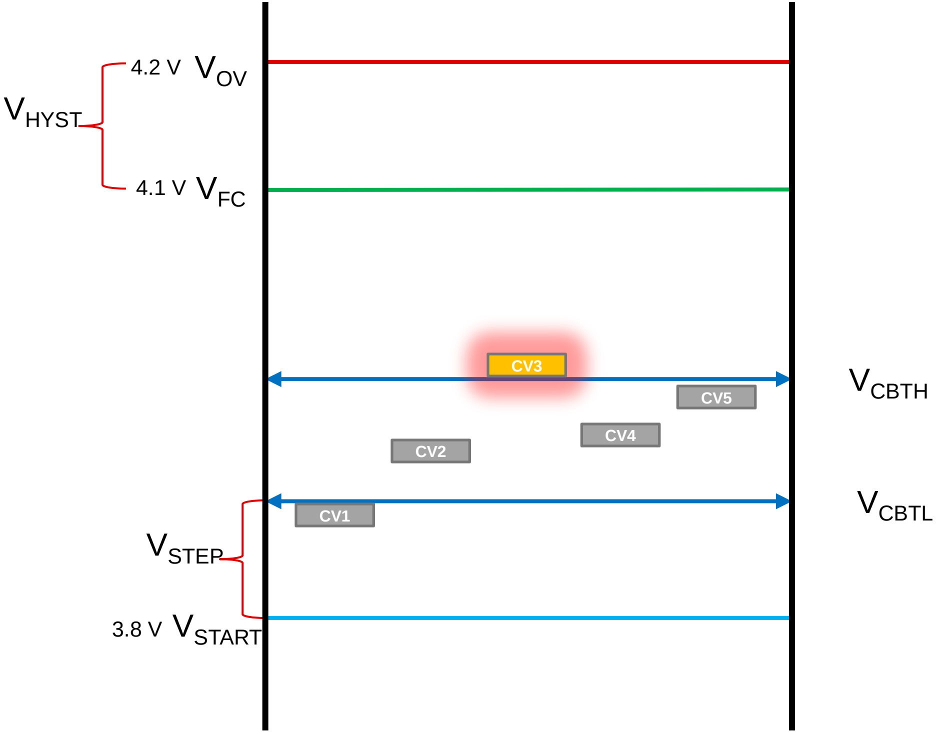


Texas Instruments

Balance resume

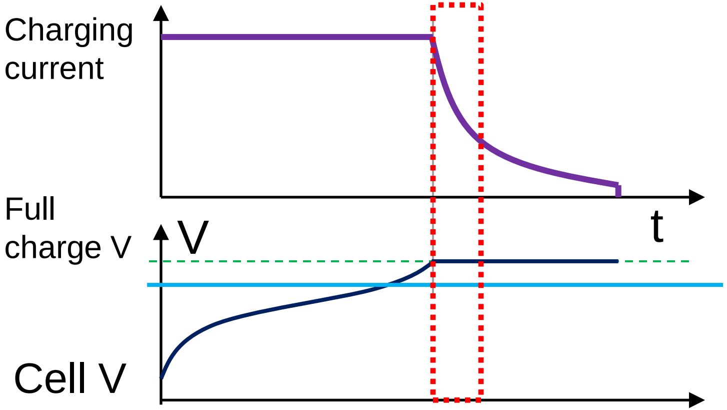
- Balancing resumes if cell voltage separation persists
  - Cell(s) above V_{CBTH}
  - Cell(s) below V_{CBTL}
  - Charge current is present
  - No faults are present

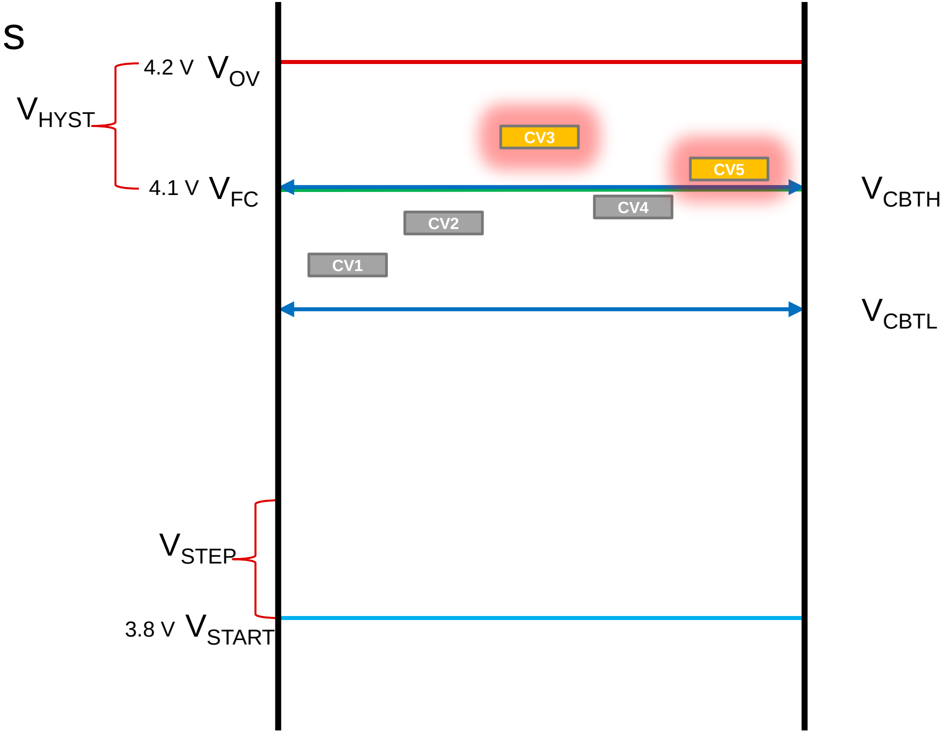




Balance at V_{FC}, full charge

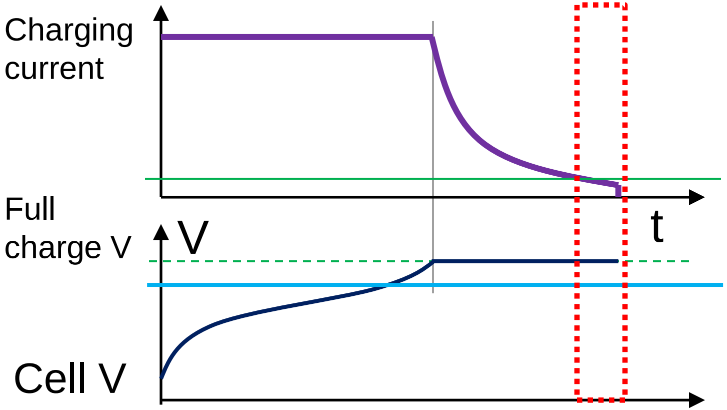
- When V_{CBTH} advances to V_{FC}, all cells above V_{FC} balance
  - Cell(s) can be above V_{CBTL}
  - Charge current is present
  - No faults are present

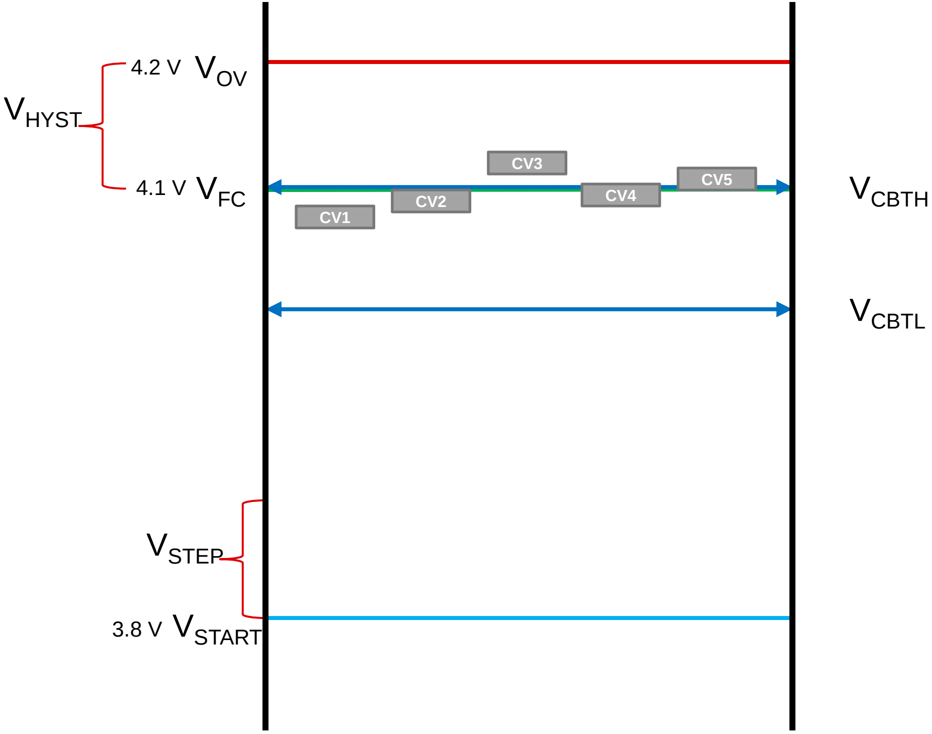




Balance stop

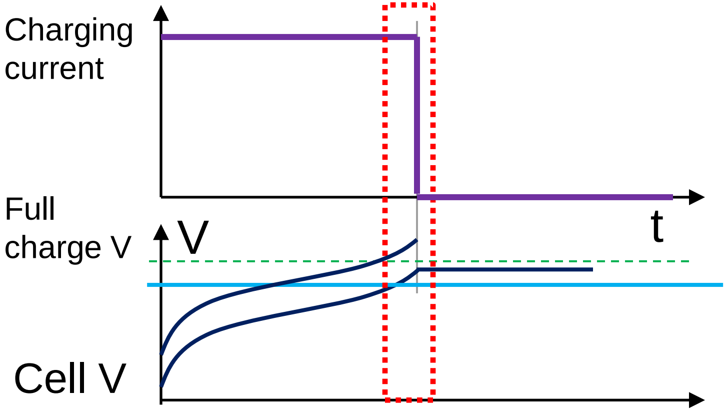
- When current falls below state comparator hysteresis, balance will stop
  - Level will depend on sense resistor

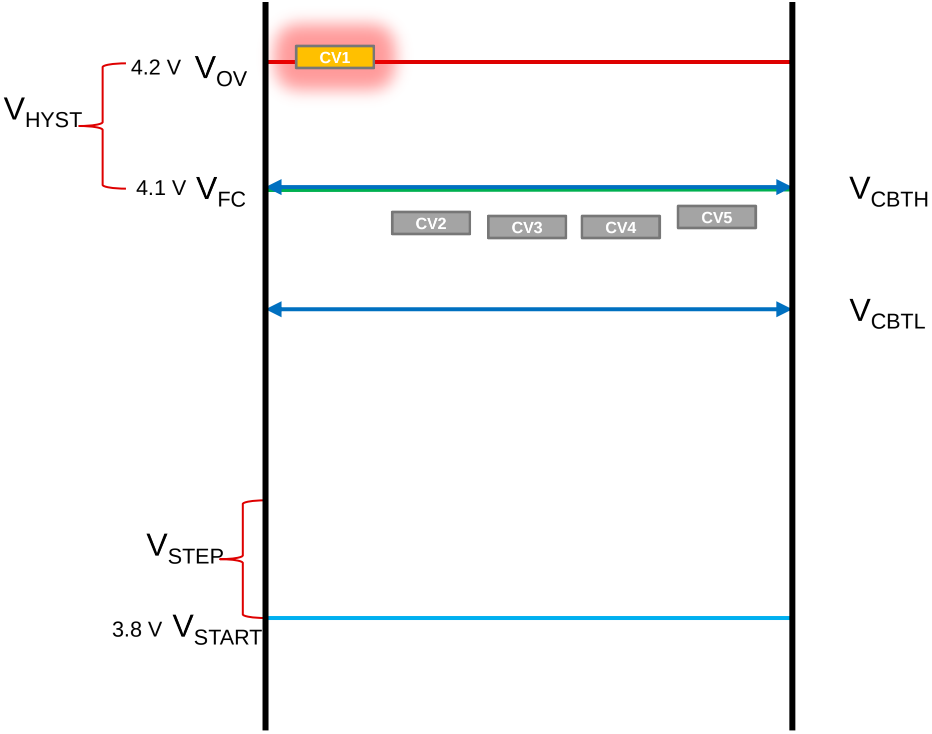




Balance in OV

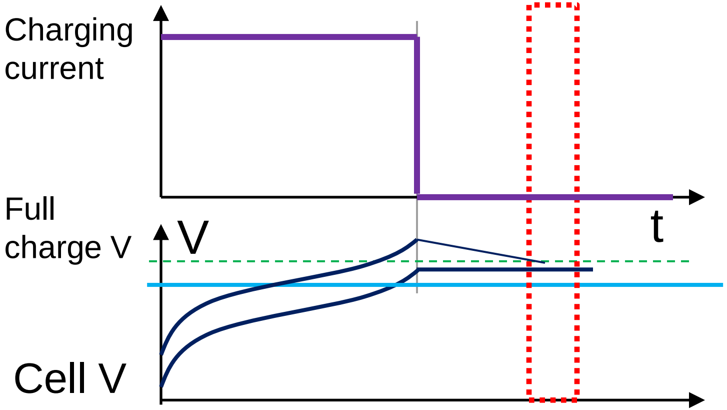
- If a cell reaches V_{OV}
  - CHG FET off from OV
    - Current stops
  - Other balancing stops because of fault
  - The OV cell balances if CBI is enabled

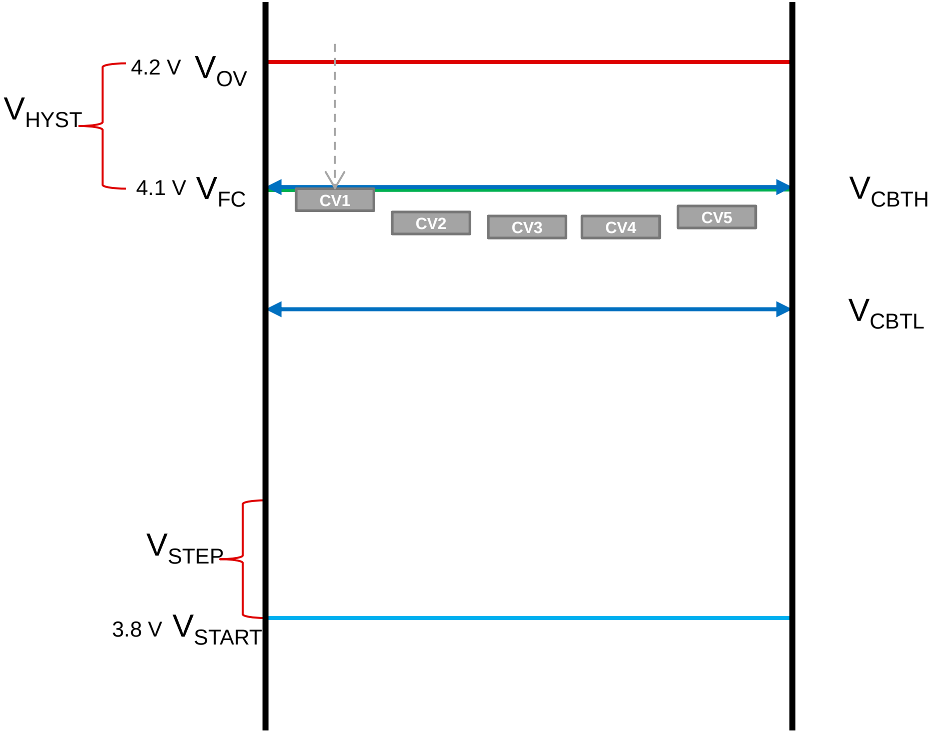




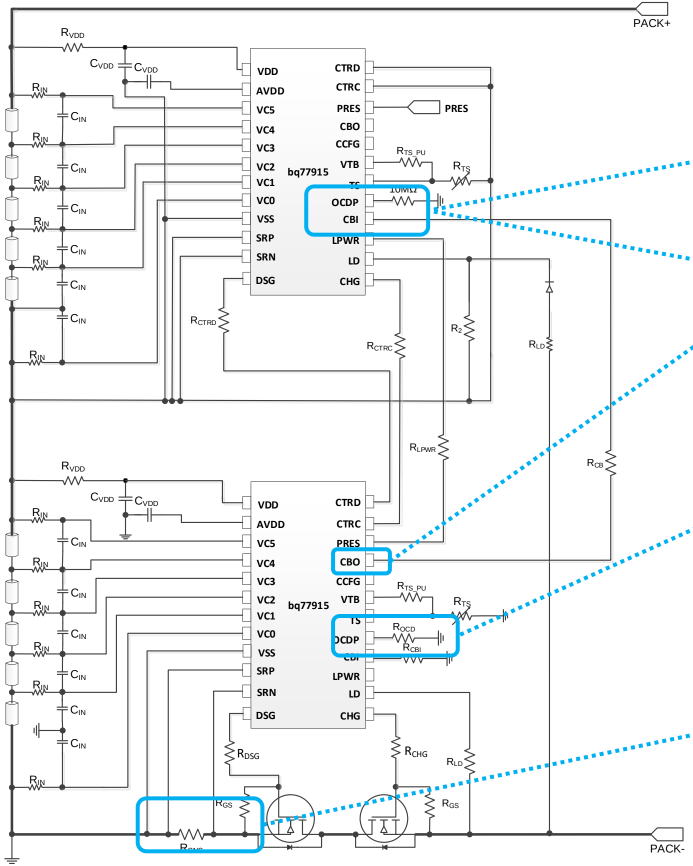
Balance in OV stop

- The OV cell balances until
  - Voltage is reduced to below V_{FC} (or OV hysteresis)
  - CBI is disabled
  - Hibernation





BQ77915: Cell balancing during stacking



OCDP with a 10M resistor indicates device is a top device

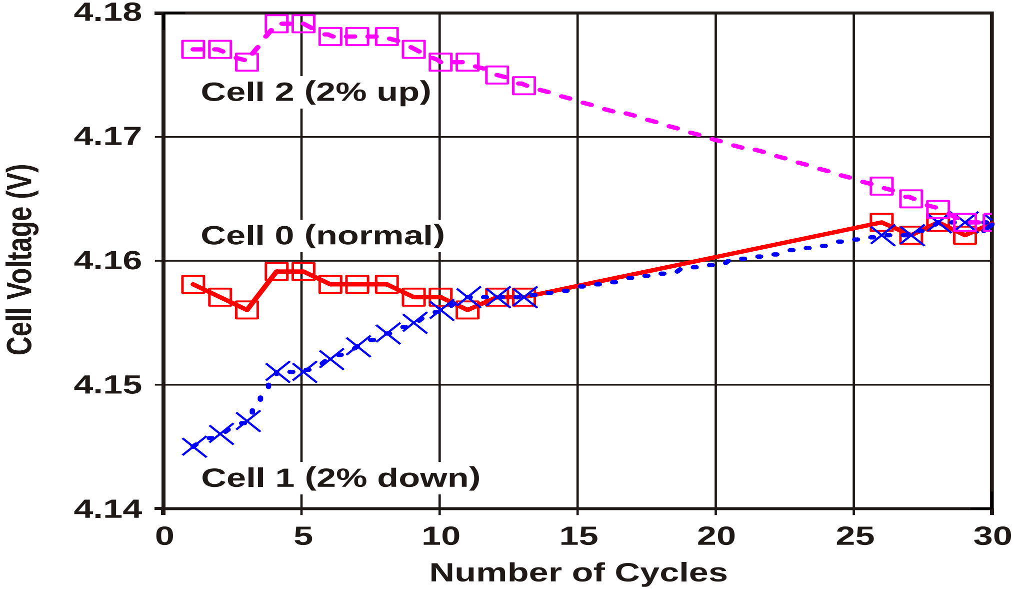
CBI from upper device communicates CB enabled / disabled

OCDP must be <500k OR leave floating to indicate device is at bottom of stack

State comparator will monitor Rsense to indicate when charging is occurring where then cell balancing can occur

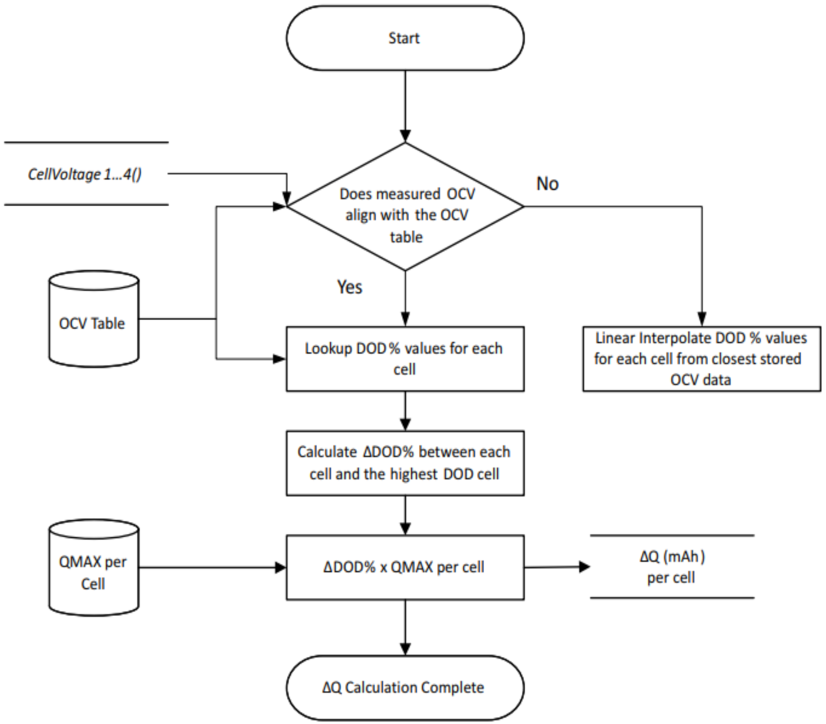
SOC and capacity-based balancing

- Impedance Track™ devices calculate the <u>delta charge</u> required to reach 100% for each cell
- Balance is achieved by controlling the balancing time
- Slow
- Example: BQ40Z80 / BQ40Z50



SOC based balancing example using BQ40Z80

- Battery gauges can balance based on state of charge (SOC) instead of voltage
- The BQ40Z80 takes the opportunity to calculate the charge difference between cells each time a rest voltage reading is taken
- Cell balancing will activate during charge, but can be configured to run during a relax state or even during sleep
- Multiple cells can be balanced simultaneously if internal balancing is used or one cell at a time if external FETs are used for higher balancing currents



Flexible balancing using battery monitors

- Battery monitor devices like the BQ769x0 or the BQ769x2 allow flexible balancing by leaving the balancing algorithm to the user's host processor

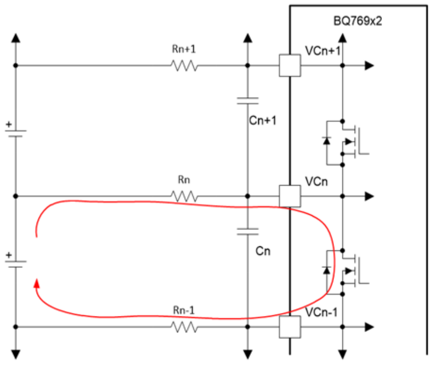
- This allows the system designer the choice of voltage-based or SOC-based balancing and when to balance (idle, charging, discharging)

- The BQ769x2 family which includes the BQ76942 (10S) and BQ76952 (16S) also offers the option to run its own balancing algorithm in stand-alone mode

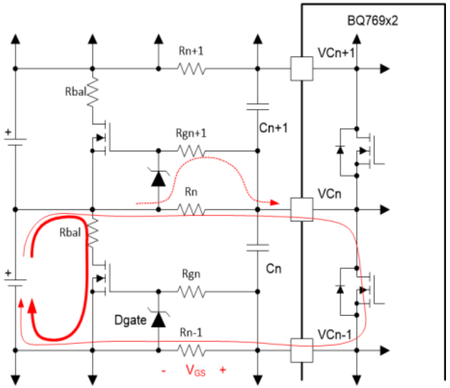
Cell balancing using BQ769x2

- Internal balancing supported through integrated switches with $R_{DS(ON)}$ = 25 Ω (typ), 40 Ω (max)
- Internal balancing current with 20 Ω series cell resistances before duty-cycling = 4.2 V / (20+20+25) = 64 mA
- Cell balancing timing will be optimized, to avoid blocking all balancing while any cell voltage measurement is underway
- Allows external cell balancing using NFETs, PFETs or BJTs
- Autonomous cell balancing based on voltage imbalance can be enabled, with settings configured in OTP to control algorithm

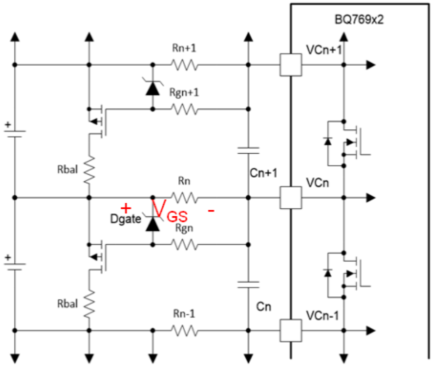
Internal CB



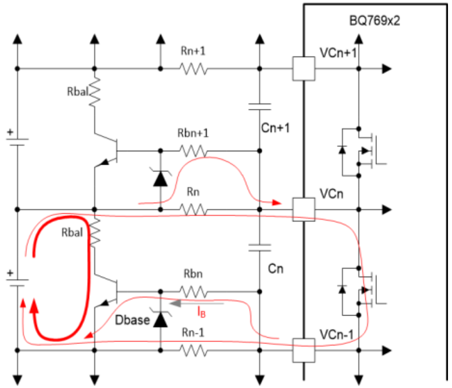
External CB w/ NFET



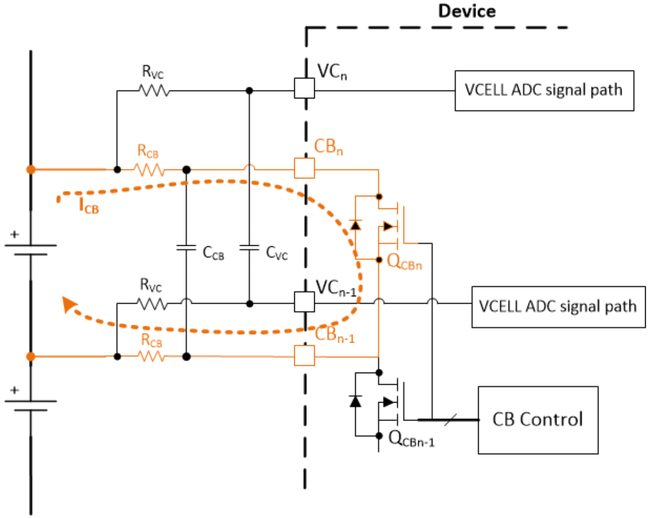
External CB w/ PFET



External CB w/ NPN

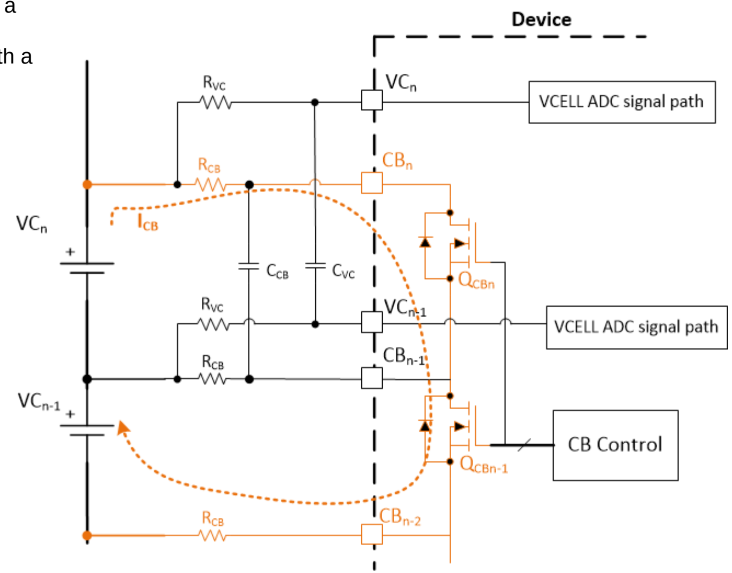


Cell balancing current for automotive monitor and balancer BQ7961x-Q1



External resistors set the cell balancing current

The BQ7961x-Q1 integrates a MOSFET for each cell to enable passive balancing with a minimum of external components

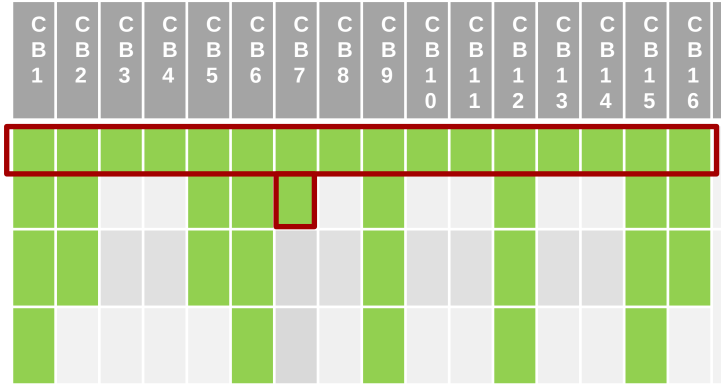


$$I_{CB} = \frac{V_{CELL}}{(2 \times RCB) + R_{DS(ON)(QCB)}}$$

$$I_{CB} = \frac{Sum\ of\ two\ VCELL}{(2 \times RCB) + R_{DS(ON)(QCBn)} + R_{DS(ON)(QCBn-1)}}$$

Cell balancing control

	Auto CB control **The cell balancing algorithm is fully configurable and runs autonomously once enabled**	**Manual CB control**
Control	Always duty cycle between odd and even	Only turn on the channels that are enabled
Stop conditions	Timers (up to 10 hr) AND cell voltage threshold	Timers (up to 10 hr) AND cell voltage threshold
Thermal pause	Yes	Yes



Valid or invalid setting	**Manual CB control**
Invalid setting	Total enabled channels > OR > 2 consecutive channels are enabled
Valid	Ok, device turns on the enabled channels

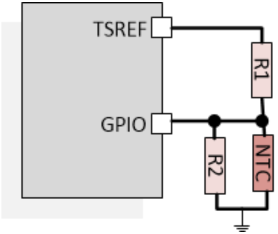
- **Auto CB control** can support all the configuration list above

CB thermal pause

CB TWARN

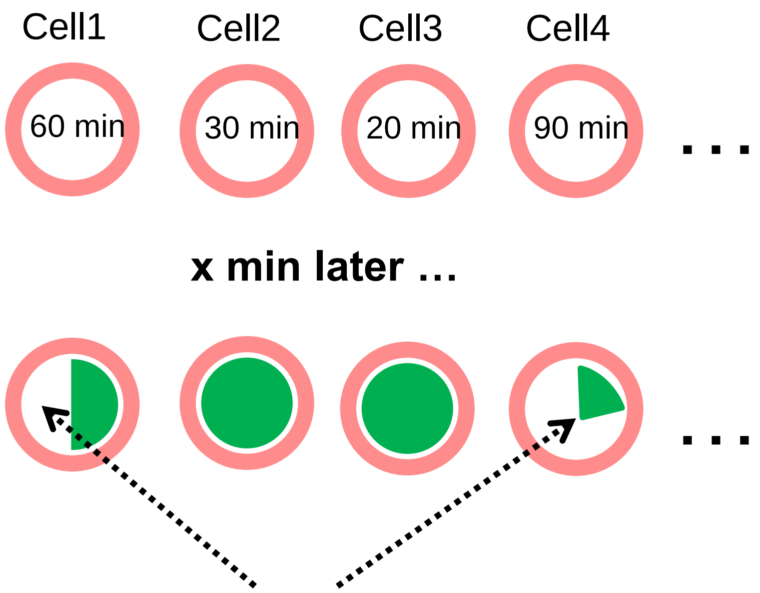
- Monitor through internal die temperature
- Pause CB if die temp > 105ºC
- Recover with 10ºC hysteresis
- Always on

Thermistor OTCB



- Monitor through external thermistor
- Pause CB if thermistor measurement > OTCB threshold (programmable)
- Resume CB with COOLOFF hysteresis (programmable)
- Register bit enable

CB remaining timers



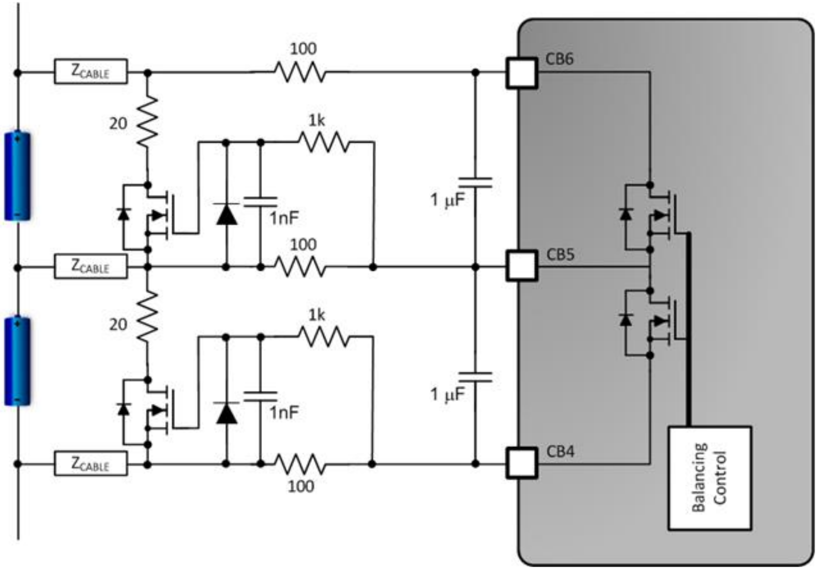
MCU can read out the remaining balancing time

Better balancing time tracking, better capacity estimation

- Each cell can set with a different balancing time
- CB thermal pause function
  - Good for hardware thermal control
  - But system may lose track of the total balancing time for SOC calculation
- CB remaining timers
  - Keep track of the remaining balancing time on each cell
  - MCU can read this information anytime (only valid if CB is running)

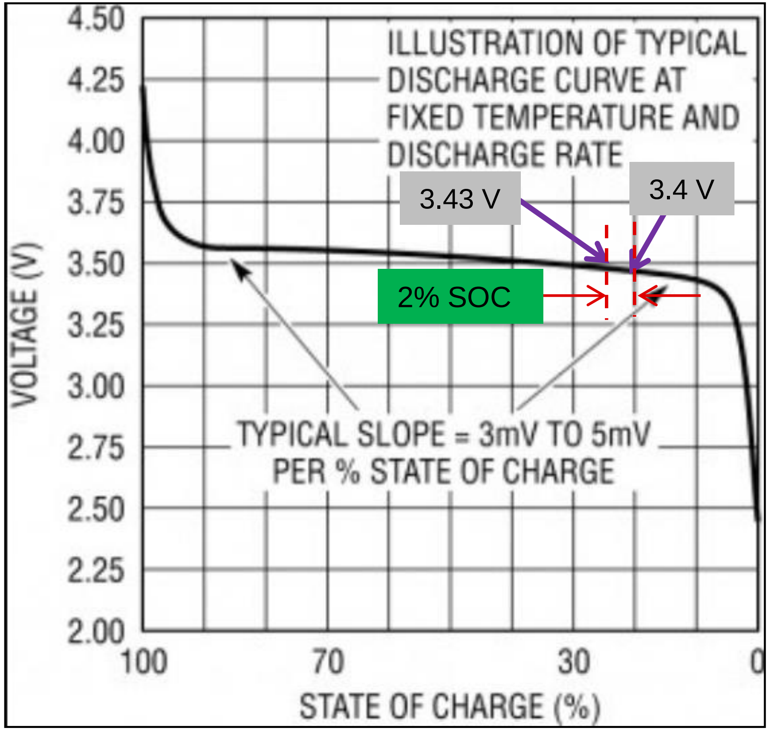
External cell balancing

- For applications that require more balancing current, the BQ79606-Q1 supports external FETs
- Power dissipation of the FET is a function of discharge current selected and the resistance value of FET at that worst-case condition, usually at hot temperature



Example of cell balancing

- A car battery can have up to a 15 Ah cell that needs to balance from 3.43 V to 3.4 V
- This corresponds to 2% of SOC
- This means 300 mAh need to be burned out in cell balancing
- With 150 mA, it requires 2 hours
- With BQ79606, both timer and voltage comparator can be set to monitor the cell balancing sequence:
  - The CB comparator monitors the cell voltage until it reaches 3.4 V and stops the cell balancing
  - AND monitor the timer until it reaches 2 hours
  - The cell balancing will complete to whatever finishes first (timer OR voltage)
  - The µC does not have to fully monitor or pull the ADC. The BQ79606 takes care of the monitoring process.



Example of R_{CB} calculation

Assume desired cell Balancing Current is 240 mA at 80℃ with 4.2 cell voltage.

1. Calculation for Cell Balancing Resistor

$V_{BAT} = 4.2V$ → Voltage of Battery

$I_{CB} = 240\ mA$ → Desired Cell Balancing Current

$R_{DS(ON)} = 5\ \Omega$ → Maximum Resistance of Internal FET at 80℃

$$R_{CB} = \frac{1}{2} \times \left(\frac{4.2\ V}{240\ mA} - 5\ \Omega\right)$$

$$R_{CB} = 6.25\ \Omega$$

2. Calculation for Power rating for R_{CB} at worst case

$V_{BAT} = 4.2V$ → Voltage of Battery

$R_{CB} = 6.25\ \Omega$ → Cell Balancing Resistor

$R_{DS(ON)} = 1.25\ \Omega$ → Minimum Resistance of Internal FET at Cold Ambient

$$I_{CB} = \frac{V_{Cell}}{2 \times R_{CB} + R_{DS(on)}}$$

$$I_{CB} = \frac{4.2\ V}{2 \times 6.25\ \Omega + 1.25\ \Omega}$$

$$I_{CB} = 305\ mA$$

$$R_{CB}\ \text{Power rating} = V_{BAT} \times I_{CB}$$

$$R_{CB}\ \text{Power rating} = 305\ mA \times 4.2V$$

$$R_{CB}\ \text{Power rating} = 0.58\ \text{W}$$

Conclusion

- Cells are not perfectly matched: capacity, SOC, impedance imbalance
- Over time imbalanced cells lead to reduction in runtime and battery lifetime
- Cell balancing, when implemented correctly, can avoid over stressing the imbalanced cell and maximizes battery capacity
- Combination of internal/external balancing using voltage/SOC based algorithm should be selected based on the application needs

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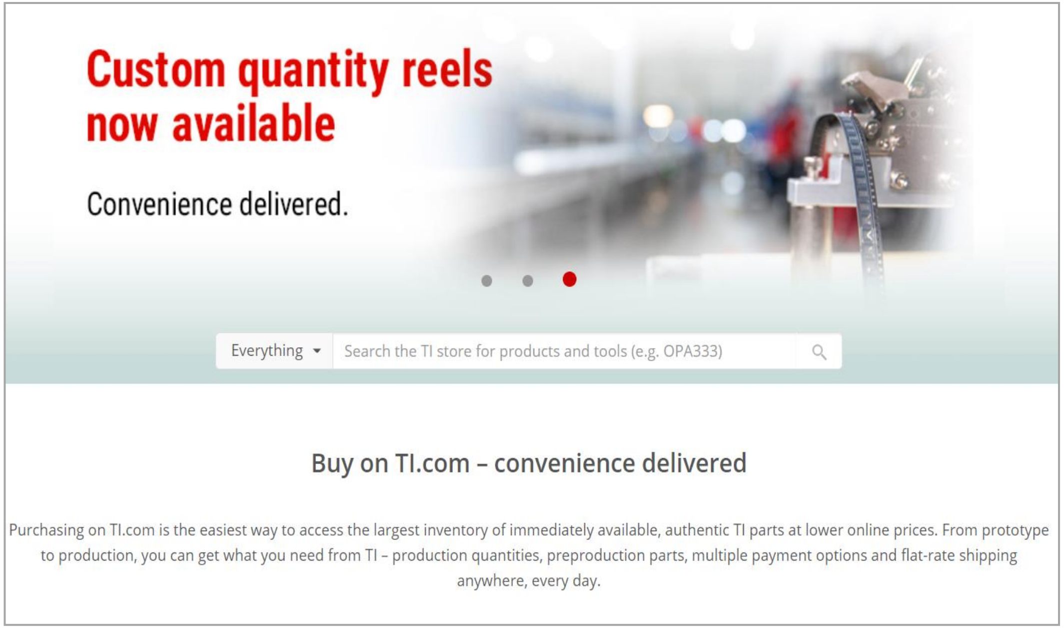

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