Clock Tree Design

TI Precision Labs – Clocks and Timing

Presented by Dean Banerjee

Prepared by Vibhu Vanjari

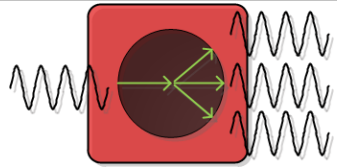
Overview

- Types of clocking devices
- Examples of common clock trees
- System-level constraints
- Output clock requirements
- Input considerations

Types of clocking devices

Oscillators

“I don’t have a clock but I need one”



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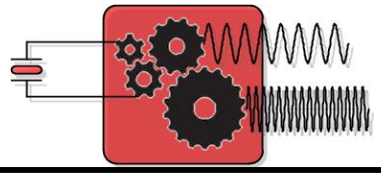

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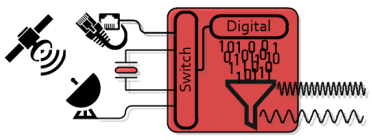

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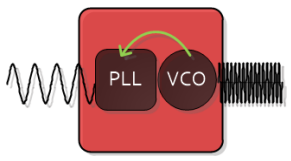

RF Synths & RF Distribution

“what do you have above 5GHz?”

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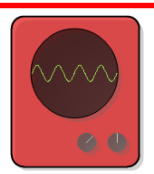

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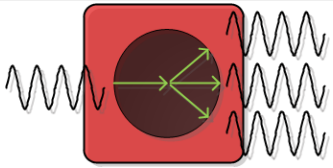

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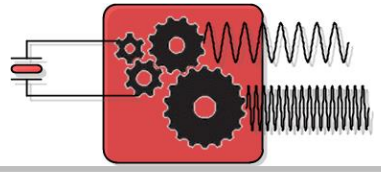

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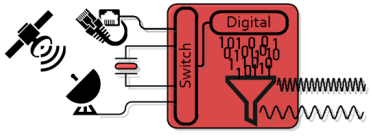

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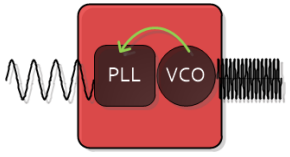

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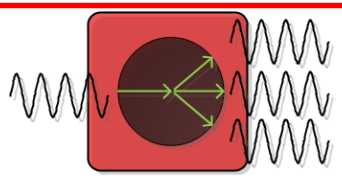

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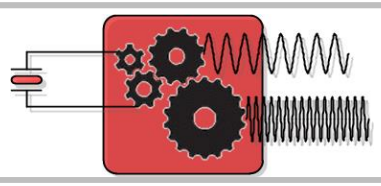

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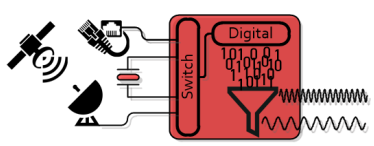

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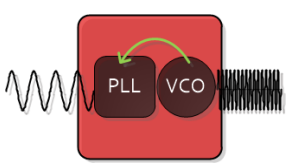

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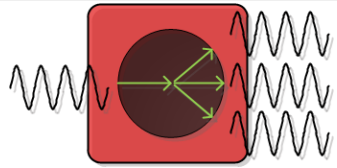

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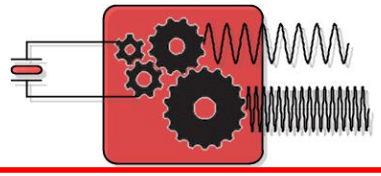

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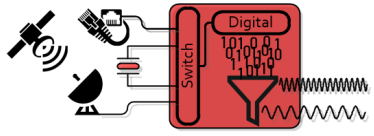

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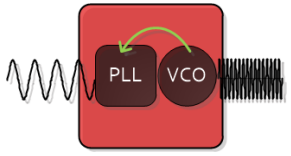

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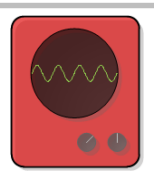

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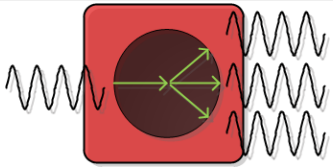

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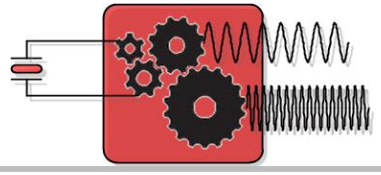

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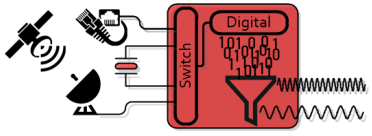

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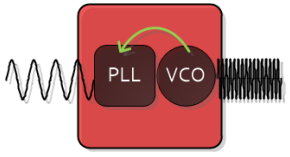

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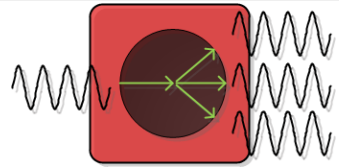

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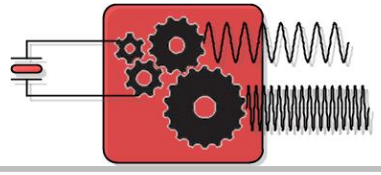

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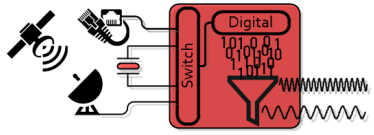

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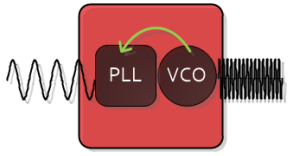

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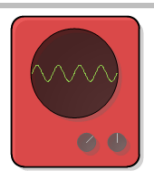

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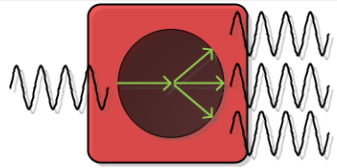

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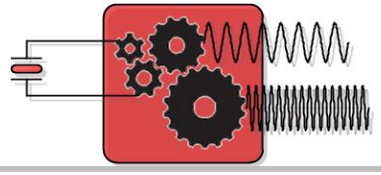

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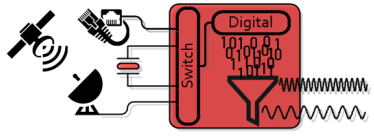

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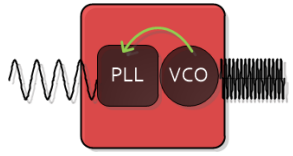

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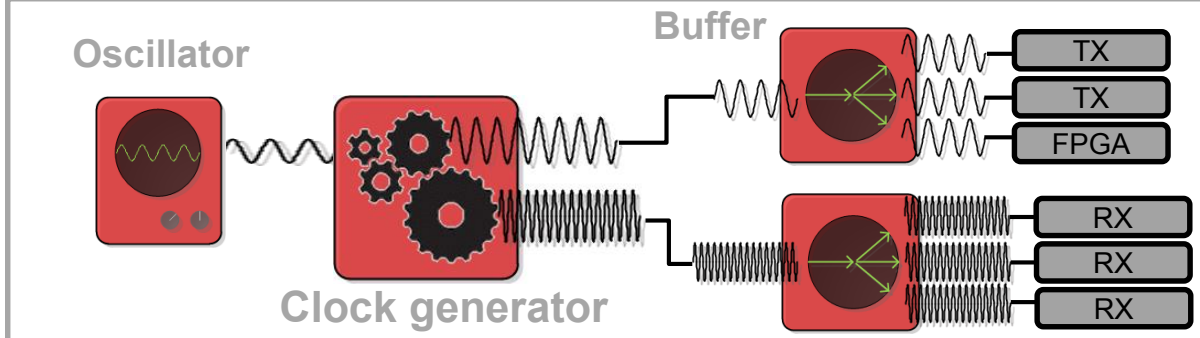
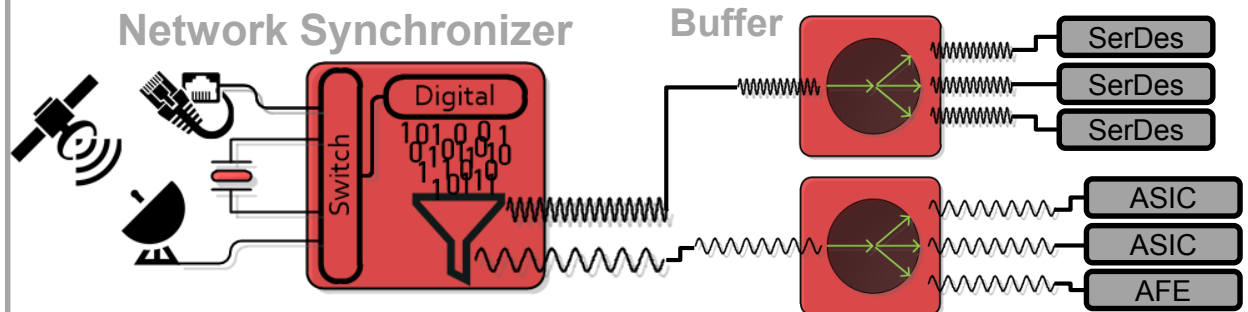
Examples of common clock trees



Clock Generator Based

Commonly used in:
Ultrasound
Pro audio/video



Network Synch Based

Commonly used in:
Wireless communication
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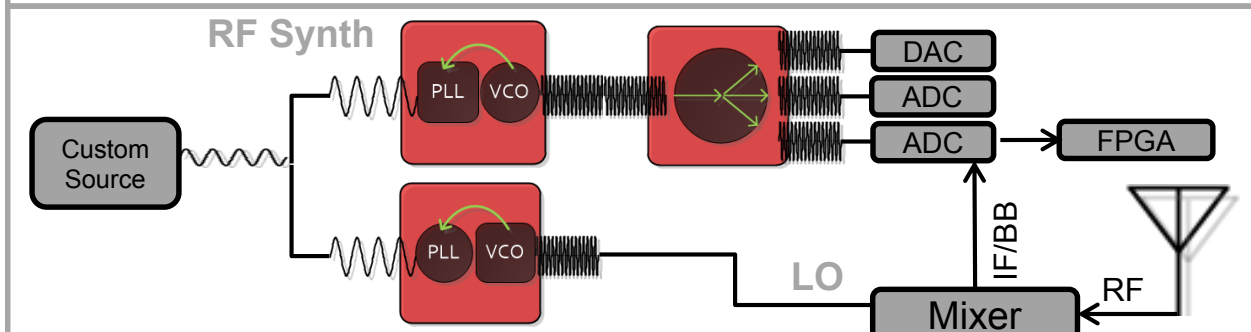

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Wireless backhaul
Point-to-point radios

Texas Instruments

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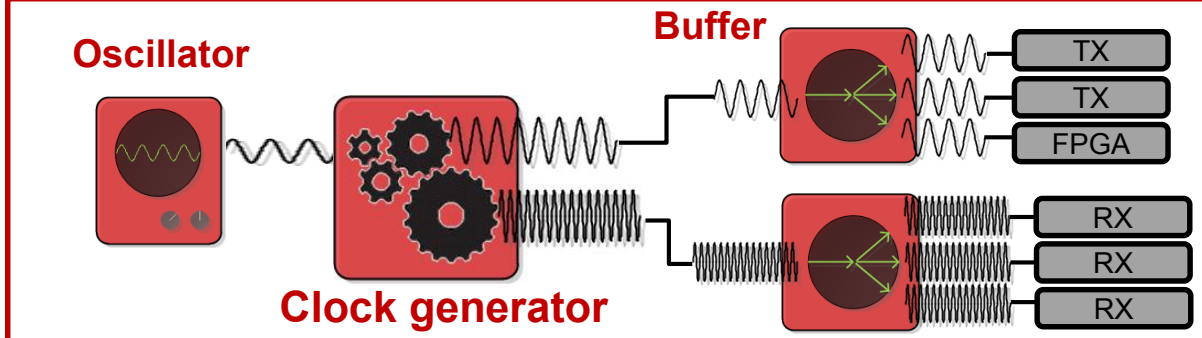

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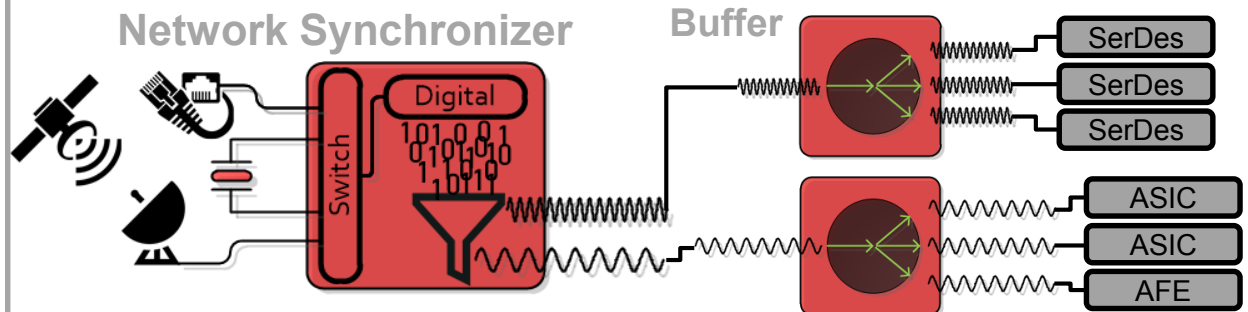

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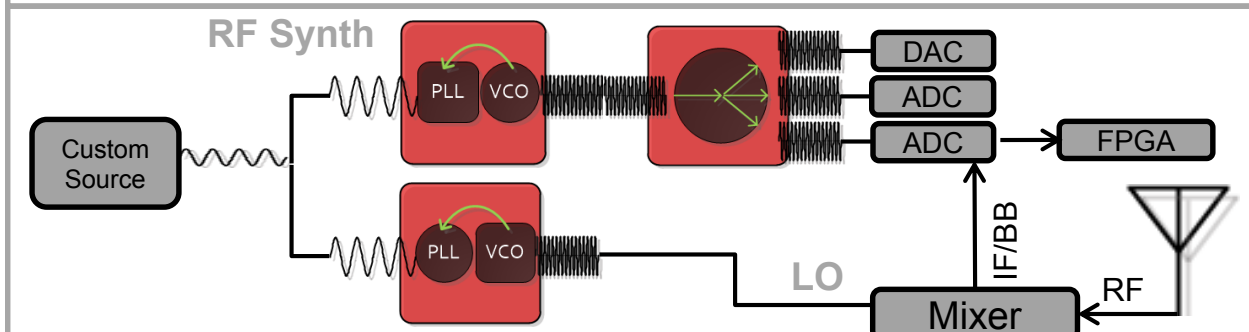

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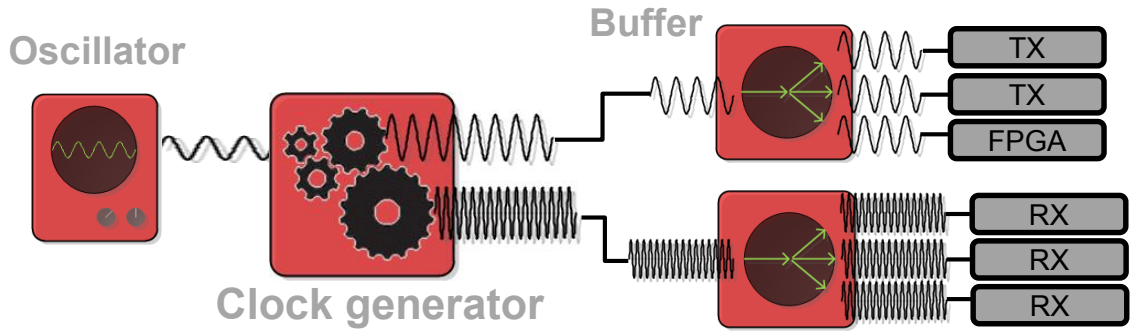

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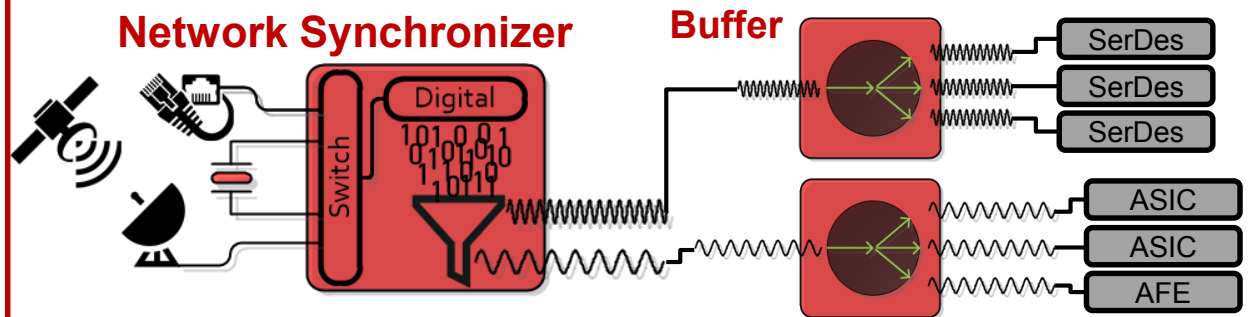

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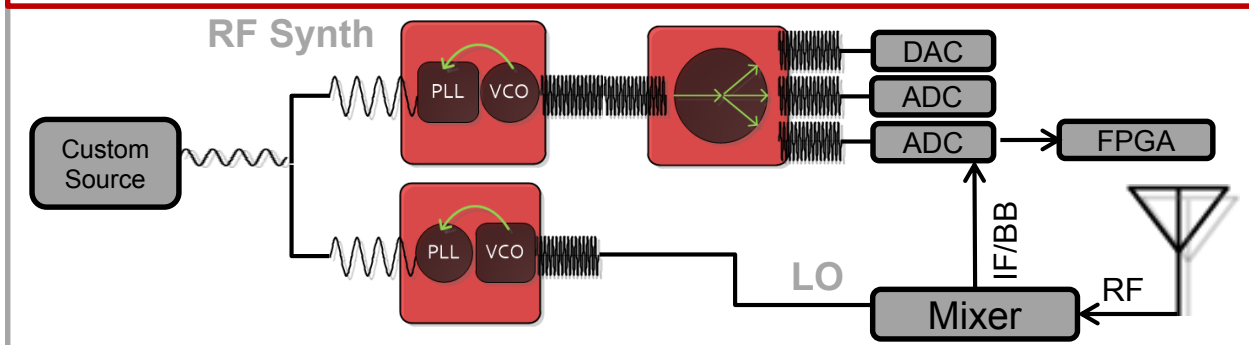

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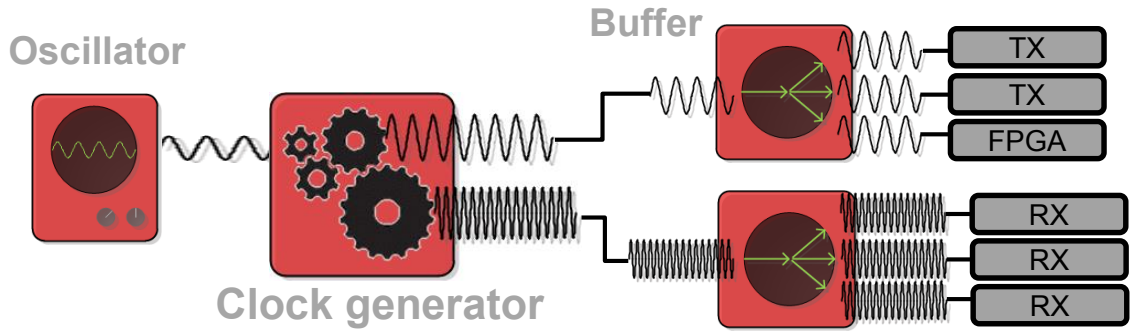

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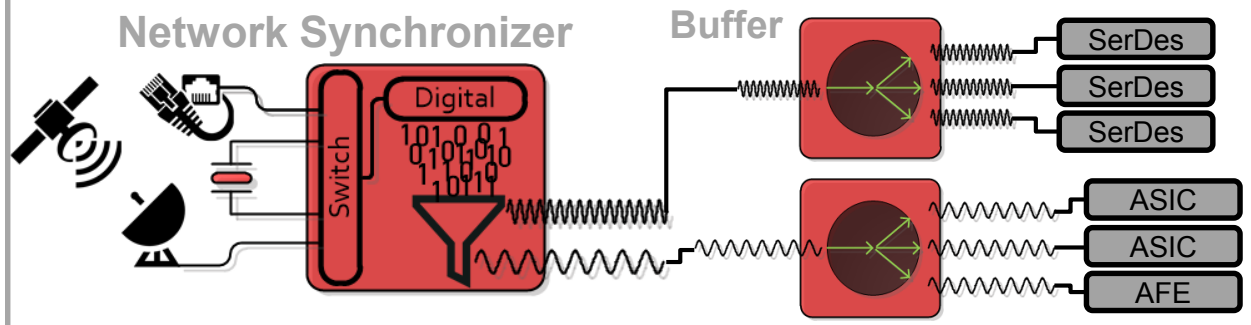

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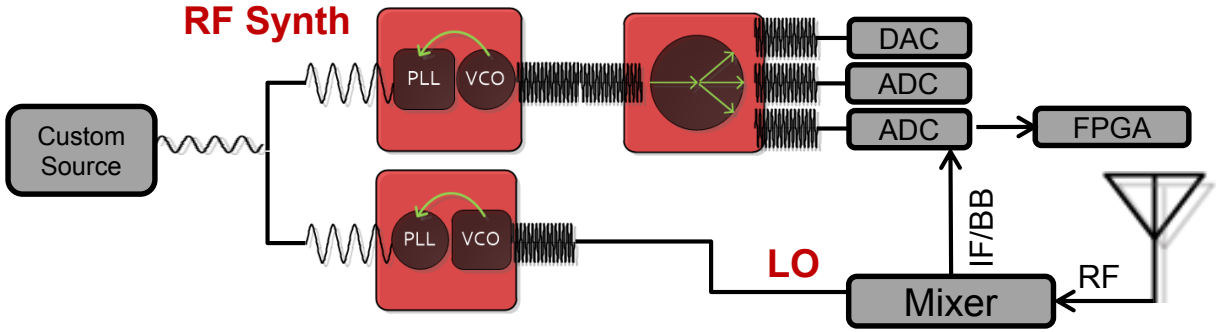

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- Price
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			MIN	NOM	MAX	UNIT
V_{DD}	Device supply voltage		1.7	1.8	1.9	V
V_O	Output Yx supply voltage, Vddout	CDCE937	2.3		3.6	V
		CDCEL937	1.7		1.9	

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
I_{DD}	Supply current (see Figure 1)	All outputs off, $f_{(CLK)}$ = 27 MHz, $f_{(VCO)}$ = 135 MHz	All PLLS on		29		mA
			Per PLL		9		
I_{DDOUT}	Output supply current (see Figure 2 and Figure 3)	No load, all outputs on, f_{OUT} = 27 MHz	CDCE937, V_{DDOUT} = 3.3 V		3.1		mA
			CDCEL937, V_{DDOUT} = 1.8 V		1.5		
$I_{DD(PD)}$	Power-down current	Every circuit powered down except SDA/SCL, f_{IN} = 0 MHz, V_{DD} = 1.9 V			50		µA

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I_{DD}	Supply current (see Figure 1)	All outputs off, $f_{(CLK)}$ = 27 MHz, $f_{(VCO)}$ = 135 MHz	All PLLS on		29		mA
			Per PLL		9		
I_{DDOUT}	Output supply current (see Figure 2 and Figure 3)	No load, all outputs on, f_{OUT} = 27 MHz	CDCE937, V_{DDOUT} = 3.3 V		3.1		mA
			CDCEL937, V_{DDOUT} = 1.8 V		1.5		
$I_{DD(PD)}$	Power-down current	Every circuit powered down except SDA/SCL, f_{IN} = 0 MHz, V_{DD} = 1.9 V			50		µA

System-level constraints

- Power consumption
- Price
- Area
- High reliability
- Free-running vs synchronous

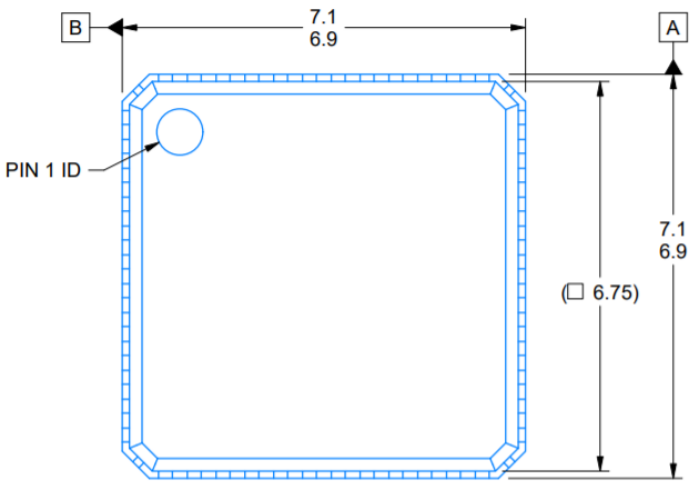
Compare the price of the devices selected.

Compare	Part Number Filter by part number	Function	Number of outputs	Output type	Output frequency (Max) (MHz)	Input type	Core supply voltage (V)	Output supply voltage (V)	Operating temperature range (C)	Package size: mm2:W x L (PKG)	Approx. price (USD)
☐	CDCEL937 - Programmable 3-PLL VCXO clock synthesizer with 1.8-V LVCMOS outputs	Clock synthesizer	7	LVCMOS	230	XTAL, LVCMOS	1.8	1.8	-40 to 85	42 mm2: 6.4 x 6.5 (TSSOP | 20	$1.883 | 1ku
☐	CDCEL913 - Programmable 1-PLL VCXO clock synthesizer with 1.8-V LVCMOS outputs	Clock synthesizer	3	LVCMOS	230	XTAL, LVCMOS	1.8	1.8	-40 to 85	32 mm2: 6.4 x 5 (TSSOP | 14)	$1.408 | 1ku
☐	CDCEL925 - Programmable 2-PLL VCXO clock synthesizer with 1.8-V LVCMOS outputs	Clock synthesizer	5	LVCMOS	230	XTAL, LVCMOS	1.8	1.8	-40 to 85	22 mm2: 4.4 x 5 (TSSOP | 16)	$1.584 | 1ku
☐	CDCEL949 - Programmable 4-PLL VCXO clock synthesizer with 1.8-V LVCMOS outputs	Clock synthesizer	9	LVCMOS	230	XTAL	1.8	1.8	-40 to 85	34 mm2: 4.4 x 7.8 (TSSOP | 24	$2.068 | 1ku
☐	CDCE937 - Programmable 3-PLL VCXO clock synthesizer with 2.5-V or 3.3-V LVCMOS outputs	Clock synthesizer	7	LVCMOS	230	XTAL, LVCMOS	1.8	2.5, 3.3	-40 to 85	42 mm2: 6.4 x 6.5 (TSSOP | 20	$1.883 | 1ku

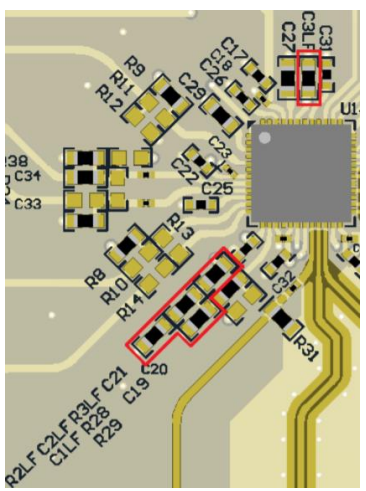
System-level constraints

- Power consumption
- Price
- Area
- High reliability
- Free-running vs synchronous

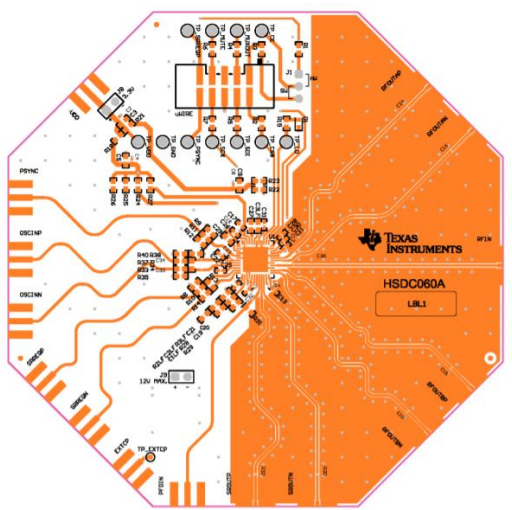
1. Identify the package sizes of devices
2. Determine the external components needed
3. Budget for routing clock signals



LMX2820 package dimensions



LMX2820 loop filter



LMX2820 routing

System-level constraints

- Power consumption
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- Area
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- Free-running vs synchronous

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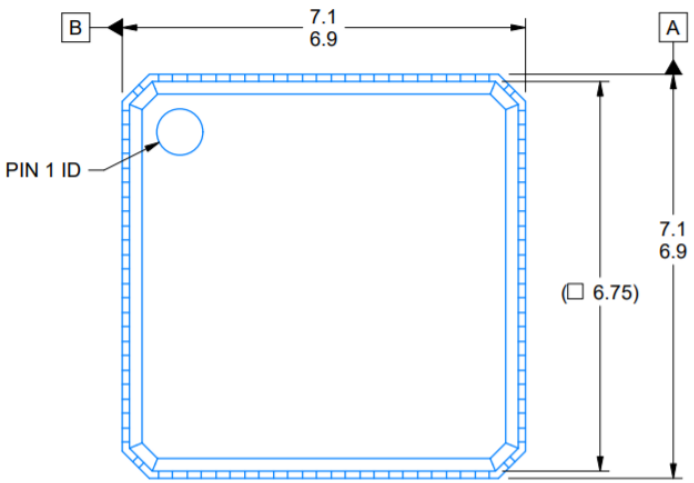
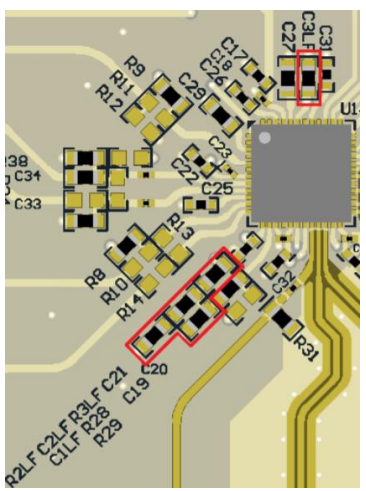


LMX2820 package dimensions



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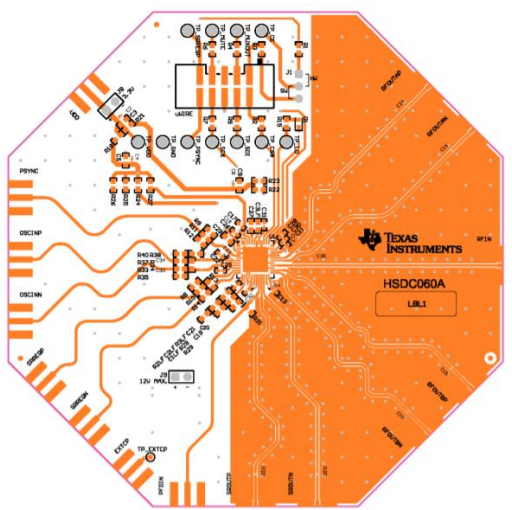

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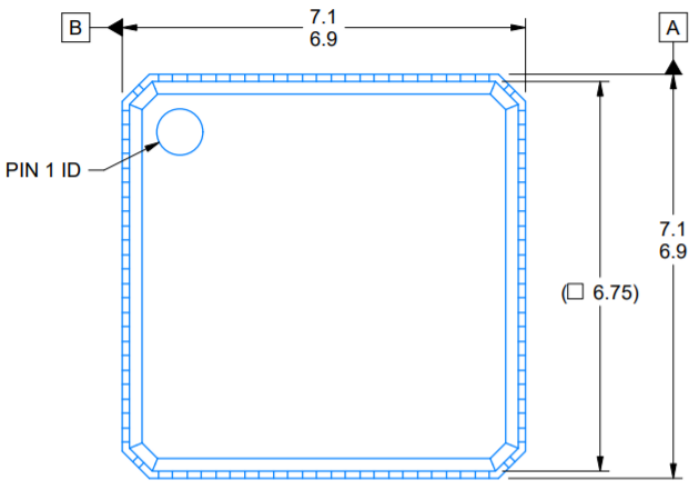

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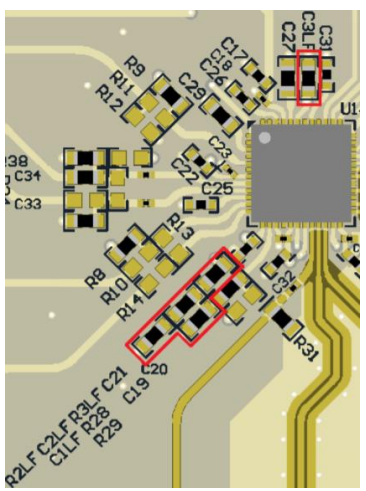
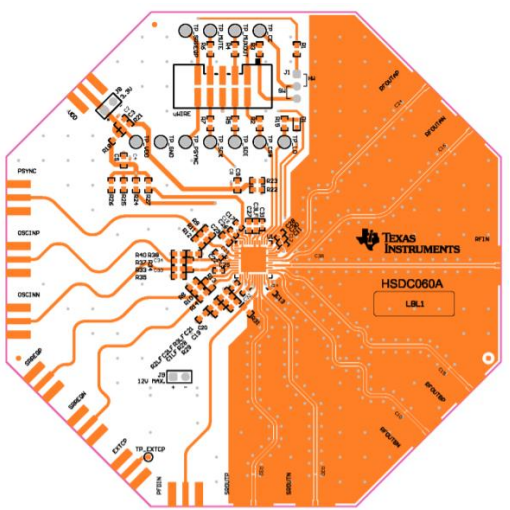


LMX2820 loop filter



LMX2820 routing

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- Area
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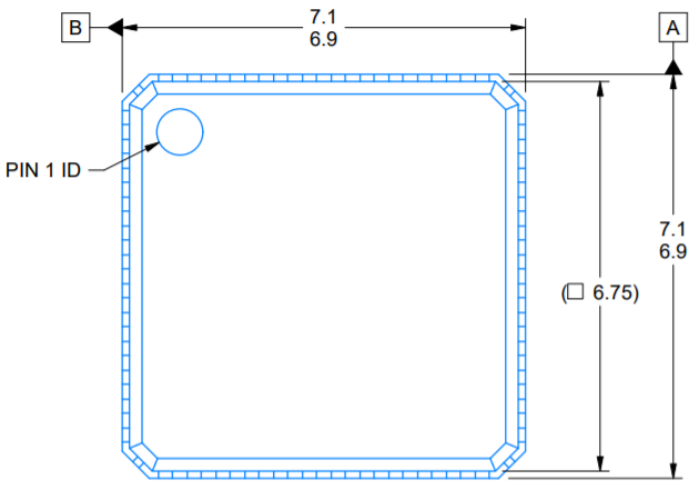
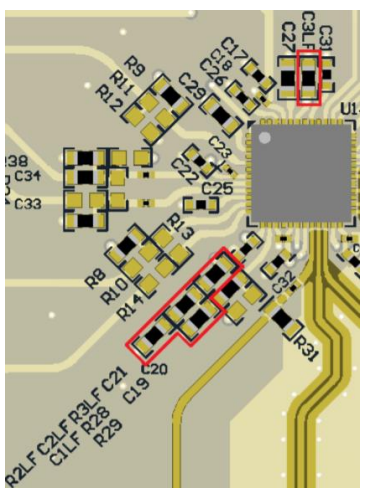
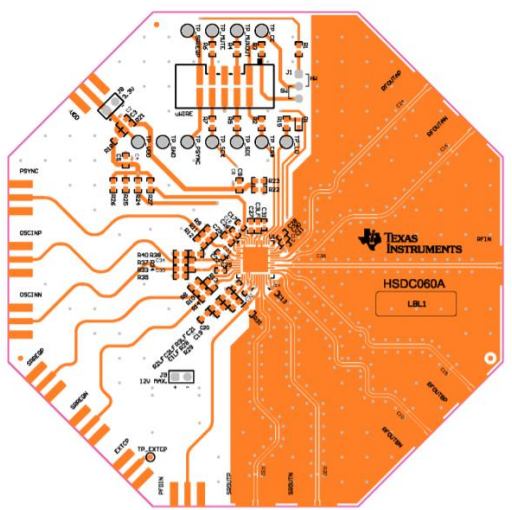


LMX2820 package dimensions



LMX2820 loop filter



LMX2820 routing

System-level constraints

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- Price
- Area
- High reliability
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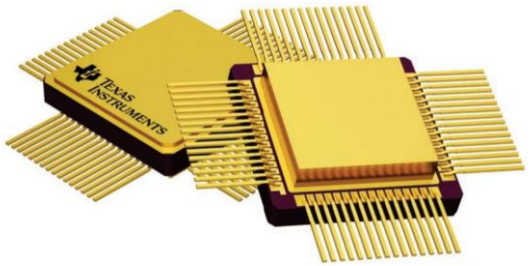


LMK04832-SP package

		MIN	NOM	MAX	UNIT
VDD_VCO	Core supply voltage	1.71	1.8, 2.5, 3.3	3.465	V
VDDO_12, VDDO_34	Output supply voltage	1.71	1.8, 2.5, 3.3	3.465	V
VDD_REF	Reference supply voltage	1.71	1.8, 2.5, 3.3	3.465	V
T_A	Ambient temperature	-40		105	°C
T_J	Junction temperature	-40		125	°C

CDCE6214-Q1 operating conditions

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002, HBM ESD Classification Level 2(1)	2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C5	750	

CDCE6214-Q1 ESD ratings

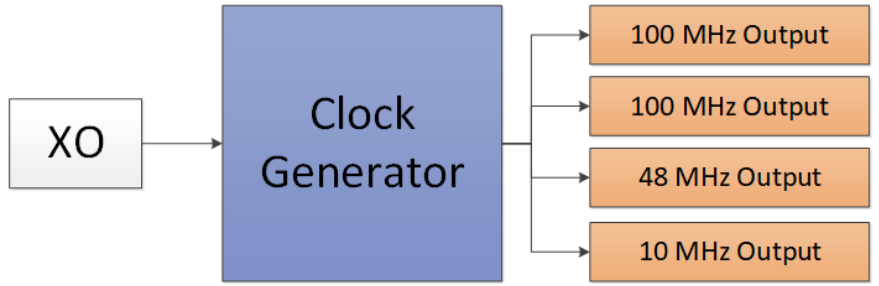
System-level constraints

- Power consumption
- Price
- Area
- High reliability
- Free-running vs synchronous

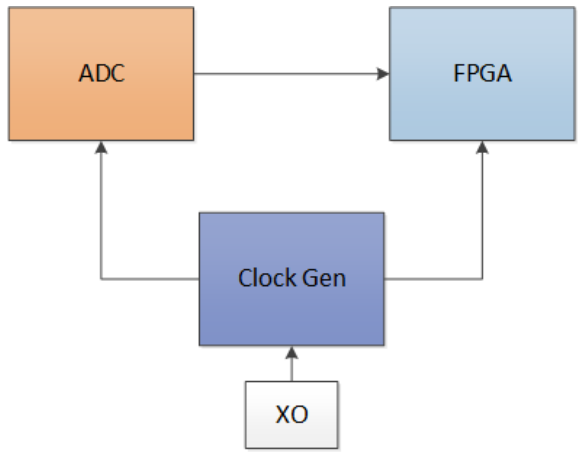
System-level constraints

- Power consumption
- Price
- Area
- High reliability
- Free-running vs synchronous

Free-running: Output clocks' phase is unknown



Synchronous: Output clocks have deterministic phases



System-level constraints

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- Price
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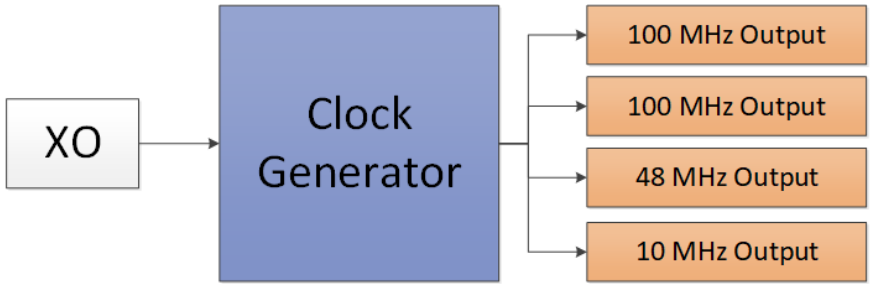

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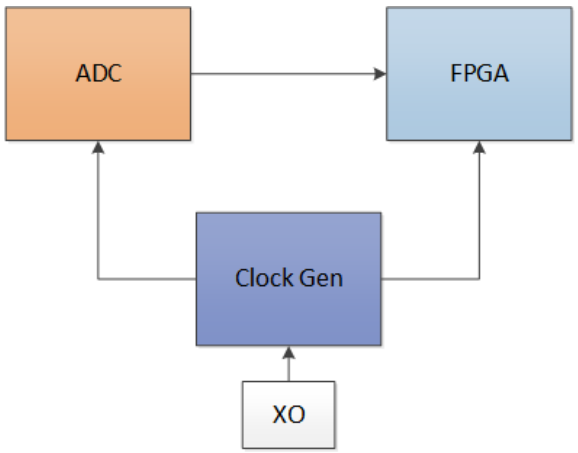

Output clock requirements

- Output frequencies
- Number of outputs
- Jitter/noise performance
- Output formats

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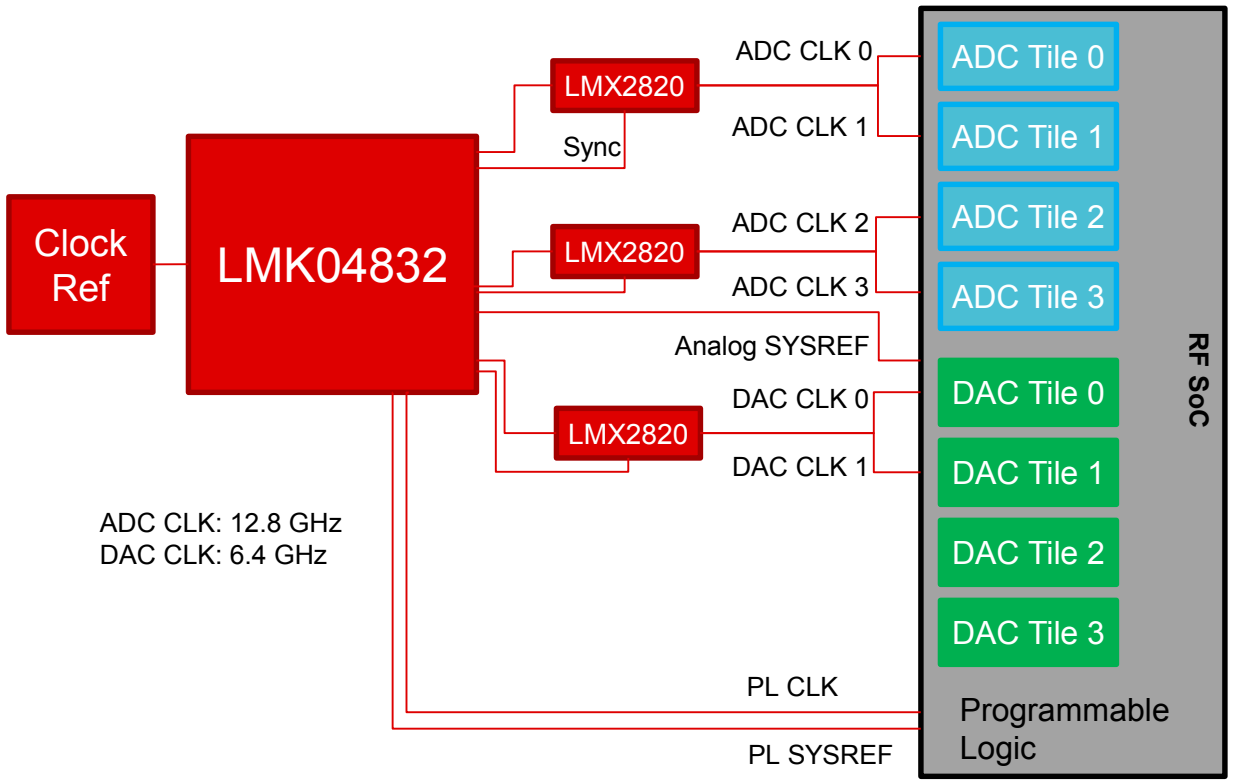

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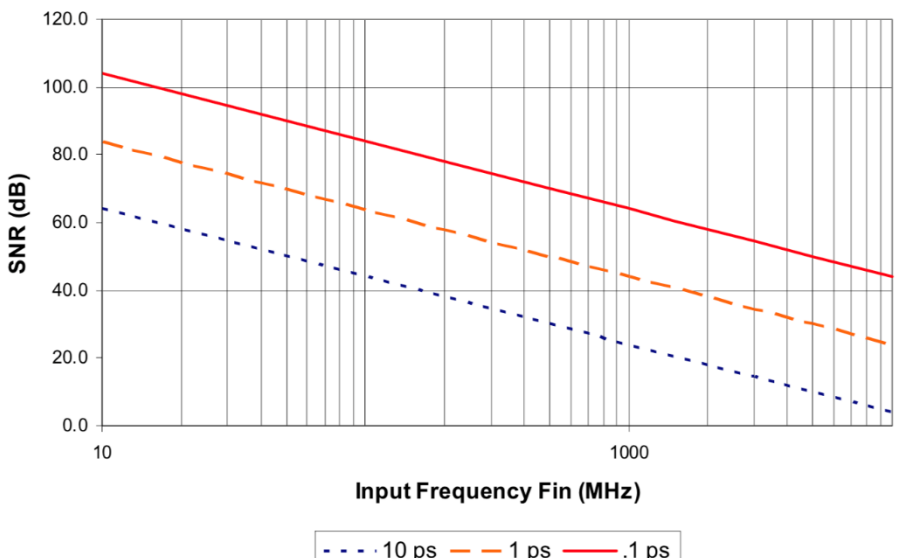
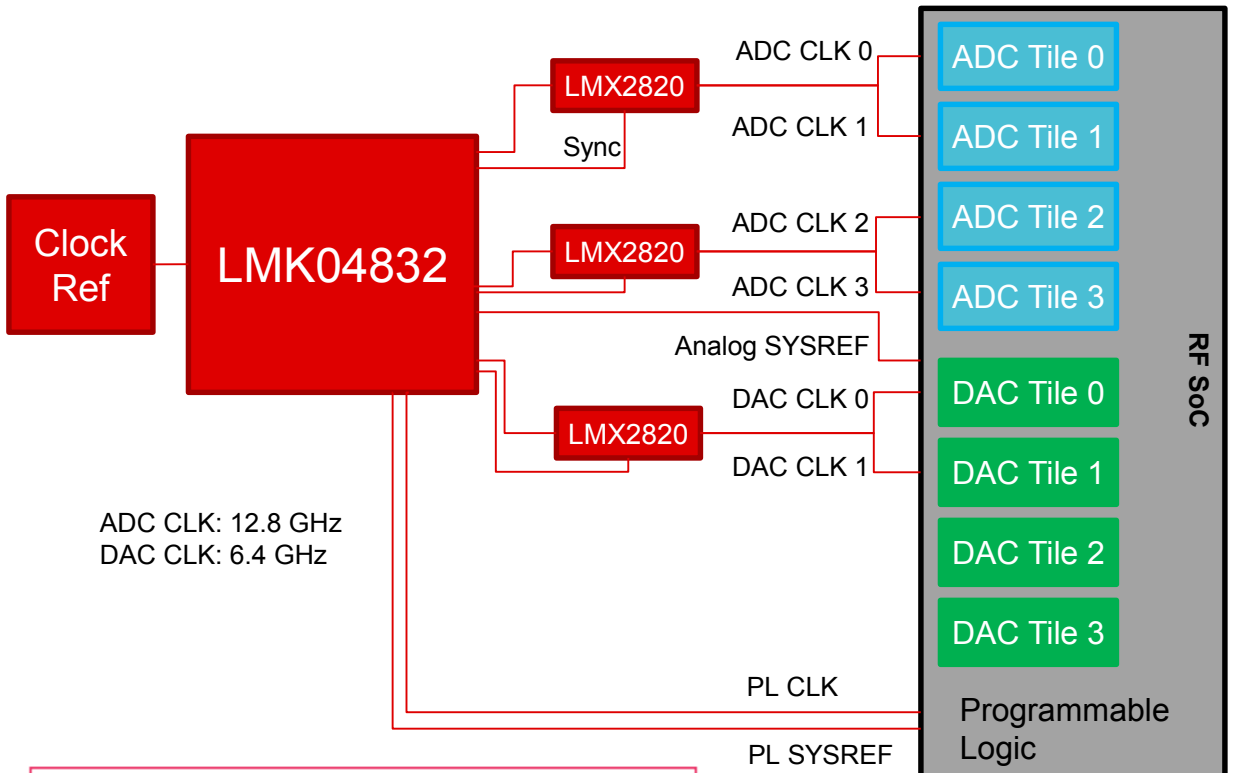




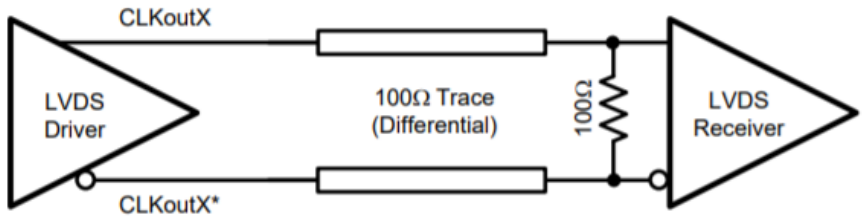
$$SNR_{jitter} = 20log_{10}\left[\frac{1}{2\pi f_{max}\sigma}\right]$$

Output clock requirements

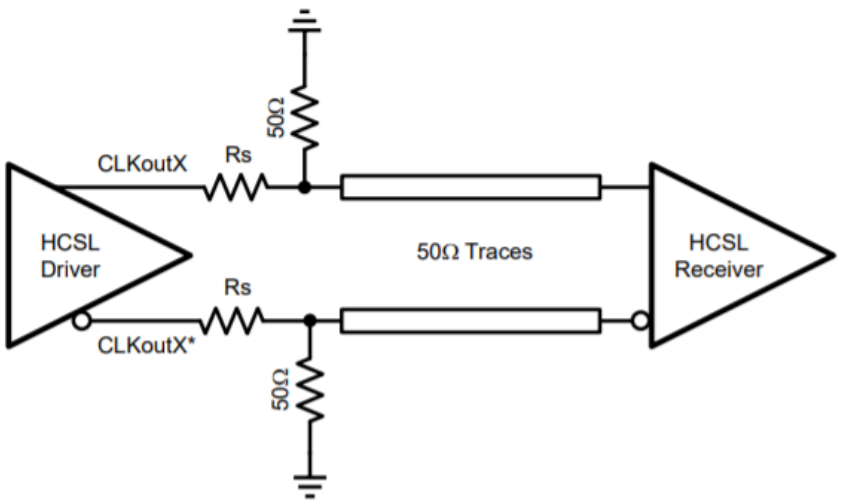
- Output frequencies
- Number of outputs
- Jitter/noise performance
- Output formats

			MIN	NOM	MAX	UNIT
V_{DD}	Supply Voltage Range	VA19, Analog 1.9V supply(1)	1.8	1.9	2.0	V
		VA11, Analog 1.1V supply(1)	1.05	1.1	1.15	V
		VD11, Digital 1.1V supply(2)	1.05	1.1	1.15	V
V_{CMI}	Input common mode voltage	INA+, INA–, INB+, INB–(1)	-50	0	100	mV
		CLK+, CLK–, SYSREF+, SYSREF–(1)(3)	0.0	0.3	0.55	V
		TMSTP+, TMSTP–(1)(4)	0.0	0.3	0.55	V
V_{ID}	Input voltage, peak-to-peak differential	CLK+ to CLK–, SYSREF+ to SYSREF–, TMSTP+ to TMSTP–	0.4	1.0	2.0	$V_{PP-DIFF}$
		INA+ to INA–, INB+ to INB–			1.0(5)	$V_{PP-DIFF}$
V_{IH}	High level input voltage	CALTRIG, NCOA0, NCOA1, NCOB0, NCOB1, PD, SCLK, SCS, SDI, SYNCSE(1)	0.7			V
V_{IL}	Low level input voltage	CALTRIG, NCOA0, NCOA1, NCOB0, NCOB1, PD, SCLK, SCS, SDI, SYNCSE(1)			0.45	V

ADC12DJ3200 input voltage requirements



LVDS termination



HCSL termination

Input considerations

- Input frequency
- Input format
- Input jitter/noise performance

Input considerations

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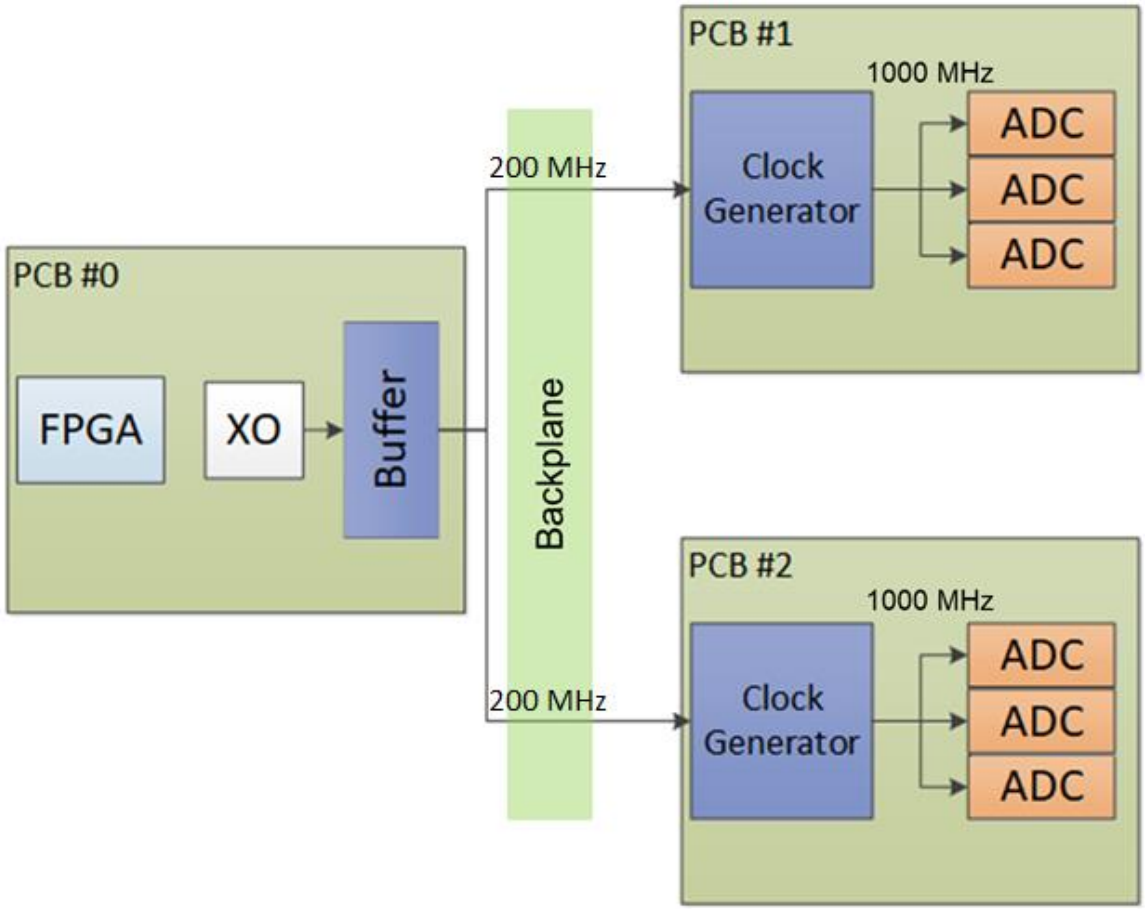

Input considerations

- Input frequency
- Input format
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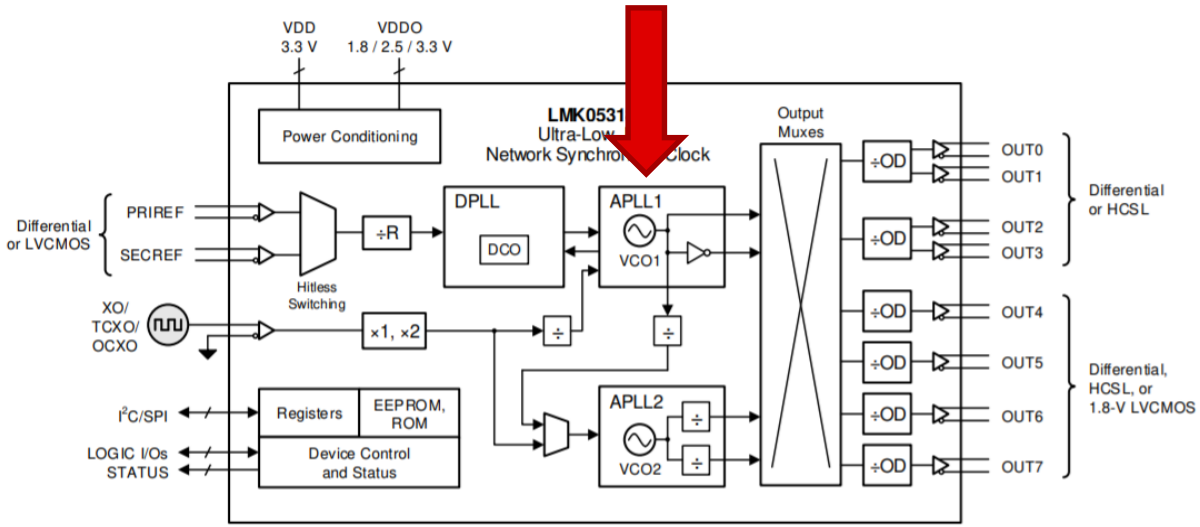
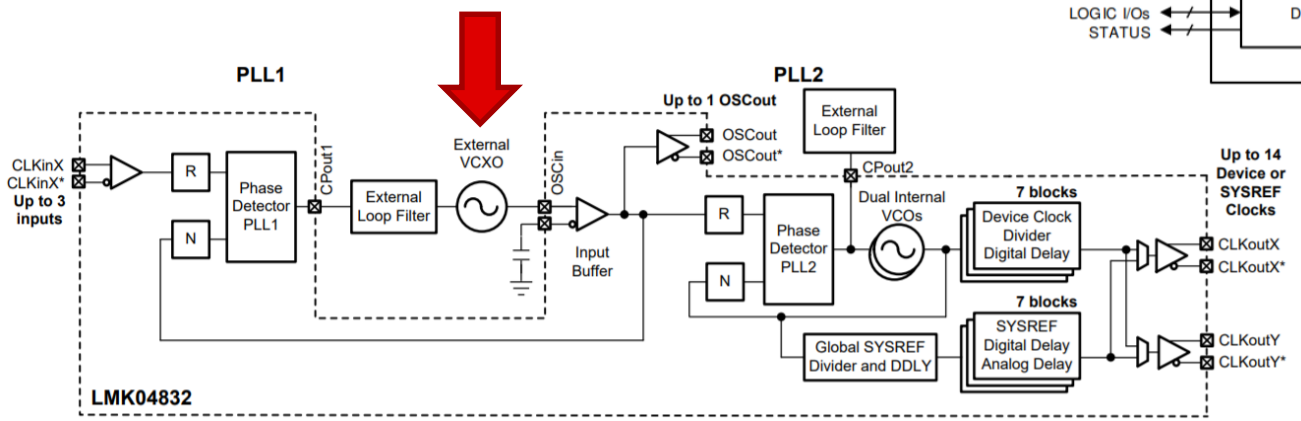
BAW VCO1 for jitter cleaning



LMK05318B block diagram

External VCXO for jitter cleaning



LMK04832 block diagram

Key resources

- Generate clock tree solutions on **webench.ti.com/clock-tree-architect**
- Download PLLatinum Sim at **ti.com/tool/PLLATINUMSIM-SW**
- For all clocking related questions reach us at **e2e.ti.com/support/clock-and-timing**
- To find more technical resources and search products, visit **ti.com/clocks**
- Related videos from the TI Precision Labs – Clocks and Timing series:

1.1 Systems Overview

4.1 Frequency Planning

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Clock Tree Design

TI Precision Labs – Clocks and Timing

Short quiz

1. True or false: There are clocking devices where the jitter at the output is better than the jitter at the input

2. True or false: For a device that has higher current consumption, the power consumption will also be higher.

3. True or false: Provided a driving output meets signal swing and differential/single-ended requirements it will be compatible to drive an input

4. True or false: The clock jitter can limit the maximum achievable SNR for a data converter.

TI Information – Selective Disclosure

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