I3C Technology Training

Presented by Saminah Chaudhry

Systems Engineer - Member, Group Technical Staff (MGTS)

Transceiver Interface (Texas Instruments)

Agenda

- Introduction to MIPI I3C
- I3C motivation
- I3C vs I^2C
- I3C protocol overview
- I3C applications in different end equipment
- TRX I3C roadmap
- Summary & key resources

I3C | MIPI I3C vs JEDEC

I3C v1.0 (2016)

- MIPI I3C: Improved inter integrated circuit - Next gen communication interface supports:
  - 12.5MHz SDR (Single data rate)
  - In-band Interrupt & Hot-join
  - HDR-DDR (Double data rate) mode
  - Timing control
  - HDR Ternary symbol modes

I3C v1.1 (2019)

- Advancement of MIPI I3C v1.0 spec
- New features added to address broader set of use cases and industries:
  - HDR-BT (Bulk transport) Mode
  - Group Addressing
  - Multi-Lane for Speed
  - Target Reset
  - Device to device(s) Tunneling

I3C v1.1.1 (2021)

- No new features or capabilities added
- Improves on I3C v1.1. spec with additional clarification of features and requirements

I3C basic v1.0 (2018)

- Feature-reduced, lower-complexity version of MIPI 13C v1.0 specification
- Functions Not Included in I3C Basic v1.0
  - HDR-DDR (Double data rate) Mode
  - HDR Ternary symbol modes
  - Timing control
- Royalty free licensing for non-MIPI member
- I3C Basic Mode is used by **JEDEC** for DDR5 Interface

I3C basic v1.1.1 (2021)

- Synchronized with I3C v1.1.1 Spec
- Subset of I3C v1.1.1, and adds key features and capabilities:
  - HDR-DDR Mode & HDR-BT (Bulk transport) Mode
  - Grouped addressing
  - Target reset
  - Timing control (Async mode 0 only)
- Royalty free licensing for non-MIPI member

Features	JEDEC (adoption of MIPI I3C basic 1.0)	MIPI I3C (v1.0)
12.5MHz SDR	Yes	Yes
High Data Rate modes	No	Yes
Dynamic Address Assignment	No	Yes
In-Band-Interrupt	Yes	Yes
Hot-Join	No	Yes
Target Reset	No	Yes (MIPI I3C v1.1)
Timing Control	No	Yes
Common Command Controls (CCC)	Small subset of MIPI I3C (8 CCCs)	>50 CCCs
Error Detection/Recovery	TE1,TE2	TE0-TE5
Clock LOW timeout	Yes	No

Evolution of MIPI I3C interface specification

I3C standard status

- I3C v1.1.1
  - I3C spec is mature and not sensitive to spec changes. No revisions of I3C v1.1.1 expected, no new approved features.
- I3C Basic v1.1.1
  - Synchronized with I3C v1.1.1; subset of MIPI 13C v1.1.1 specification, royalty free licensing for non-MIPI members.
- MIPI I3C Ecosystem / support with:
  - Conformance Test Suite (CTS) for I3C v1.1.1 and I3C Basic v1.1.1

Comparison of Features

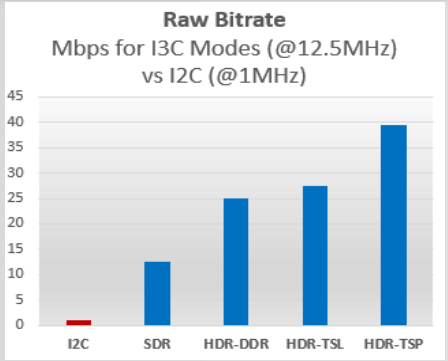
Feature	I3C v1.0	I3C Basic v1.0	I3C v1.1.1	I3C Basic v1.1.1
12.5 MHz SDR (Controller, Target and Legacy I²C Target Compatibility)	✓	✓	✓	✓
Target can operate as I²C device on I²C bus and on I3C bus using HDR modes	✓	✓	✓	✓
Target Reset	✓	✓	✓	✓
Specified 1.2V-3.3V Operation for 50pf C load	✓	✓	✓	✓
In-Band Interrupt (w/MDB)	✓	✓	✓	✓
Dynamic Address Assignment	✓	✓	✓	✓
Error Detection and Recovery	✓	✓	✓	✓
Secondary Controller	✓	✓	✓	✓
Hot-Join Mechanism	✓	✓	✓	✓
Common Command Codes (Required/Optional)	✓	✓ ✓	✓	✓ ✓
Specified 1.0V Operation for 100pf C load	✓	✓	✓	✓
Set Static Address as Dynamic Address CCC (SETAASA)	✓	✓	✓	✓
Synchronous Timing Control	✓	✓	✓	✓
Asynchronous Timing Control (Mode 0)	✓	✓	✓	✓
Asynchronous Timing Control (Mode 1-3)	✓	✓	✓	✓
HDR-DDR	✓	✓	✓	✓
HDR-TSL/TSP	✓	✓	✓	✓
HDR-BT (Multi-Lane Bulk Transport)	✓	✓	✓	✓
Grouped Addressing	✓	✓	✓	✓
Device to Device(s) Tunneling	✓	✓	✓	✓
Multi-Lane for Speed (Dual/Quad for SDR and HDR-DDR)	✓	✓	✓	✓
Monitoring Device Early Termination	✓	✓	✓	✓

I3C vs I²C

Feature	I3C	I²C
SCL max frequency	12.5 MHz	1 MHz (FM+ mode)
IO topology	SCL: Push pull; SDA: Open drain and push pull	SCL & SDA: Open drain only
Capacitive load per bus line	50 pF	400 pF for FM; 550 pF for FM+
Bus pull-up resistor	Integrated in the host controller	External pull up
Interrupt	In band	Dedicated pin
Compatibility	Supports I²C target devices with 50 ns glitch filter	No support
Dynamic addressing	Yes	No
9th bit function	ACK or NACK (address), Parity (write) and Bus control (read)	ACK or NACK
Bus functions	Common code commands (CCC)	Special address
Device feature support	3 mandatory registers: BCR, DCR, LVR	No
Bus compliance	Yes, established as interoperability rules	No
Target reset	Unique pattern based	Hard-reset line
Target device clock stretching	Not allowed on I3C	Yes
Extended address (10 bit)	Not used on I3C	Optional
20 mA open drain driver	Not used on I3C	Supported in FM+ mode

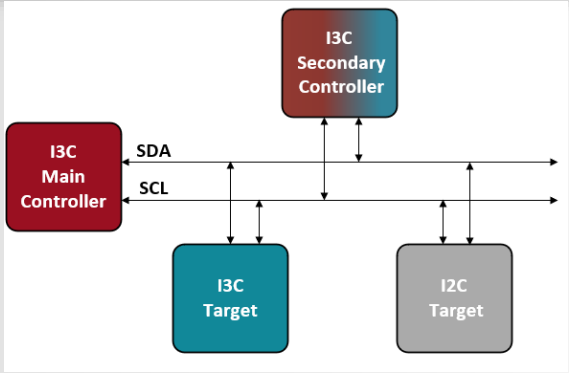
I3C | Motivation

Fast efficient communication channel



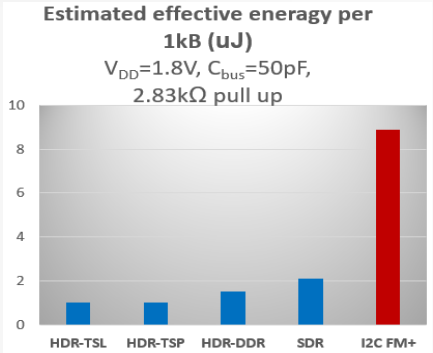
- Multidrop SDA/SCL 2-wire interface
  - 12.5 MHz max clock rate
  - 1.2V-3.3V voltage supported
- Physical layer CMOS I/O compatible
- Dynamic switch between pullup/push pull/Hi-Z
- SDR (Single Data Rate) – 12.5 Mbps
- HDR (High Data Rate) modes for higher throughput (HDR-DDR, HDR-TSL, HDR-TSP, HDR-BT)

System management & backward compatibility



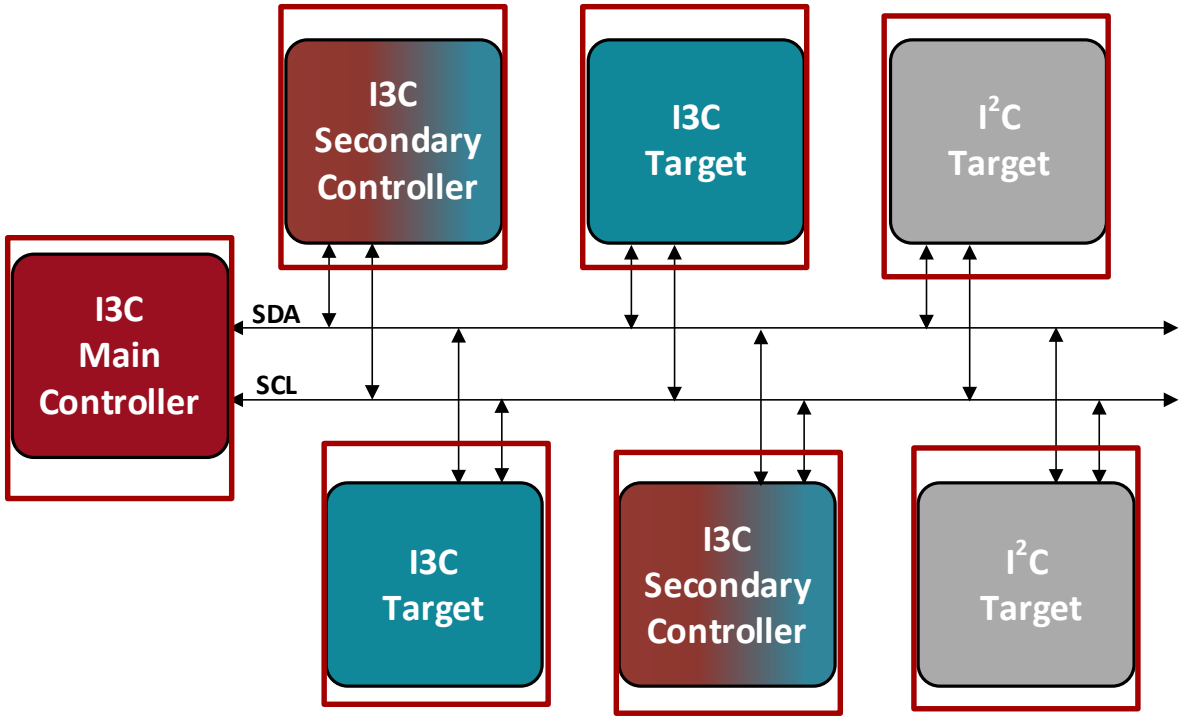
- Device Roles: I3C primary & secondary Controllers
- Dynamic address assignment (including group addressing)
- Standardized commands for bus management, configuration and control
- Backwards compatible allowing mixed bus operation

Advanced functions



- Broadcast & direct messages
- Error detection & recovery, parity, CRC
- Target reset
- In-band interrupt (IBI)
- Hot-join
- Timing control
- Power efficiency

I3C | Controller and target device roles



I3C bus with I²C devices and I3C devices

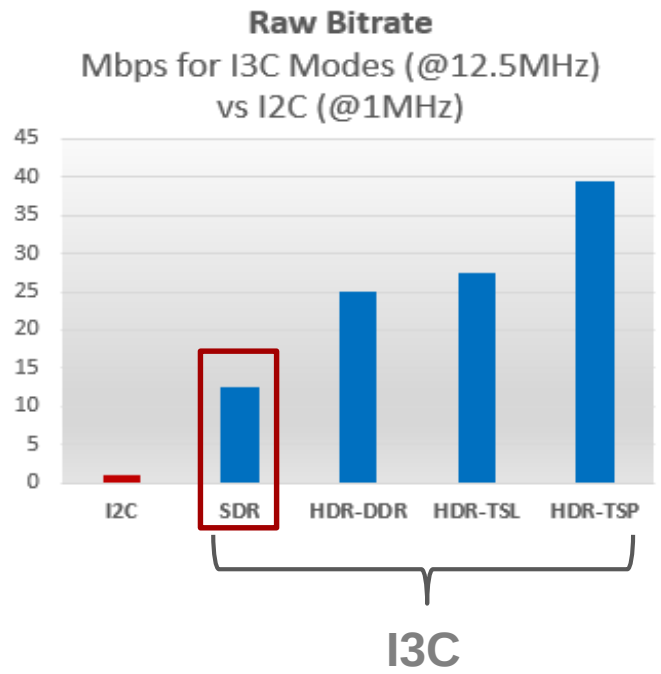
I3C protocol

Single Data Rate (SDR) Mode

I3C | Bus communication - (SDR) mode

Communication protocols for all defined I3C Modes include:

- **Single data rate (SDR) mode** – 12.5 Mbit/s
- **High data rate (HDR) modes**
  - **HDR-DDR** (Dual data rate) – 25 Mbit/s
  - **HDR-TSL** (Ternary symbol legacy) – 27.5 Mbit/s
  - **HDR-TSP** (Ternary symbol pure) – 39.5 Mbit/s
  - **HDR-BT** (Bulk transport) - data rate up to 100 Mbps
- **ML data transfer -** available for any I3C Mode (e.g., SDR, HDR-DDR, HDR-TSP, or HDR-BT)



Single Data Rate (SDR)

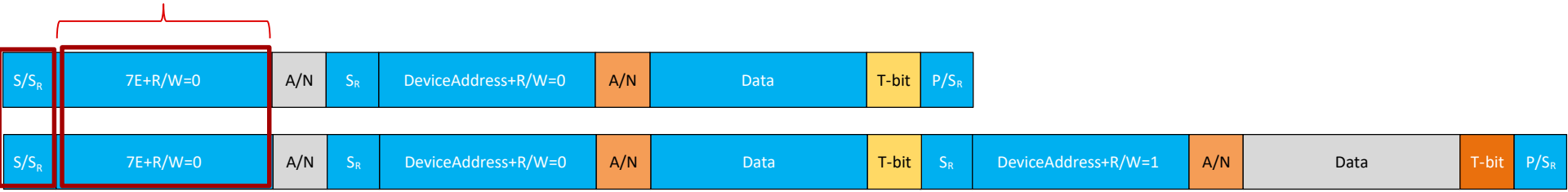
- Default Mode of the I3C Bus
- SCL wire operates as Clock signal driven by Controller, while data is transferred using SDA wire
- Used to enter other modes, sub-modes, and states for built-in features

I3C | Frame structure vs I²C

I²C write packet

I²C read packet

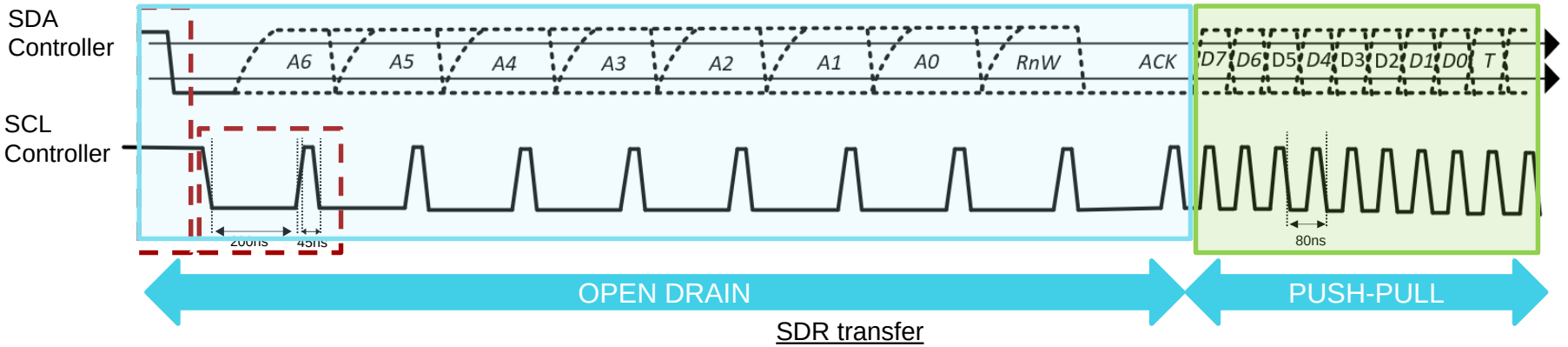
I3C broadcast address



I3C | SDR address arbitration

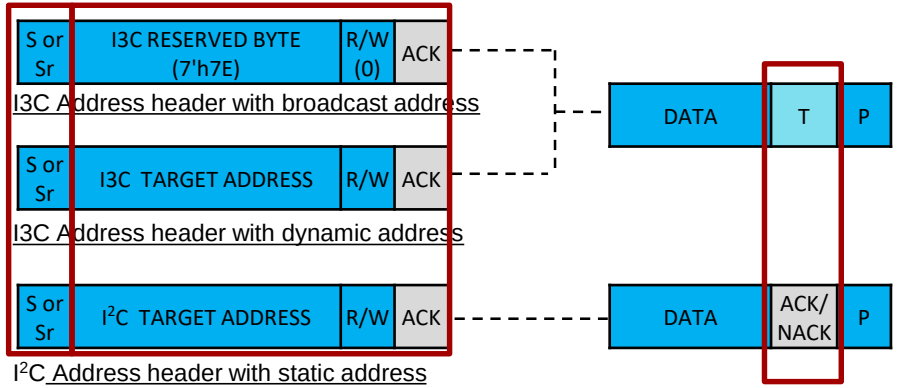
- Address Header following a START is an arbitrable address header
- I3C Uses Clock Speed to Prevent Legacy I²C Devices from Seeing I3C Traffic
  - SCL high-period is <45ns, well below 50ns glitch filter required by I²C, enabling up to ~ 4MHz
- After ACK, the controller changes SDA to push-pull mode and increases its clock to 12.5MHz
  - I3C maximum bus frequency: 12.5MHz (80 ns) clock period

➢ SDR Mode is backwards compatible with legacy I²C devices; to coexist in the same bus, spike suppression filter of 50ns avoids any interference to the bus when communicating with I3C device



SDR transfer

I3C | Bus communication - (SDR) mode



I3C bus communication format

- I3C START and STOP: Identical to the I²C START and STOP in their signaling, but they may vary from I²C in their timing
- I3C Address Header: Identical to the I²C address header in bit form and in signaling, but it may vary from I²C in its timing.
- Data 9-bit Words: Same bit count as I²C, but differ in the ninth bit

I3C | SDR data word – 9th bit

In I3C SDR, the data words match I²C only in the sense that they are both 9 bits long.

Ninth Bit of SDR Controller written data as parity:

- In I3C the ninth data bit written by the controller is the **parity** of the preceding eight data bits.
- In SDR terms, the ninth bit of write data is referred to as the **T-Bit (for 'Transition')**

➢ Parity can help in detecting noise-caused errors on the line

	1 bit	8 bits	1 bit	8 bits	1 bit	…	1 bit
MIPI I3C	S/S_R	Addr + W	ACK/NACK	1 Byte data	T bit = Parity	More data	S_R or P
I²C					ACK/NACK		

Ninth Bit of SDR target returned (read) data as end-of-data:

- In I3C 9th bit allows the target to end a read, and allows the controller to abort a read.
- In SDR terms, the ninth bit of read data is referred to as the **T-Bit (for 'Transition')**

➢ T-bit allows negotiation between host and device for read data

	1 bit	8 bits	1 bit	8 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit	…	1 bit
MIPI I3C	S/S_R	Addr + W	ACK/ NACK	1 Byte data	T bit = Parity	S_R	Addr + R	ACK/ NACK	1 Byte data from target	T bit = 1 (Target to continue) T bit = 0 (Target ends transmission	More data	S_R or P (Controller ends read)
I²C					ACK/ NACK					ACK/NACK **Target can't abort read**		(Controller ends read)

I3C | Characteristic registers

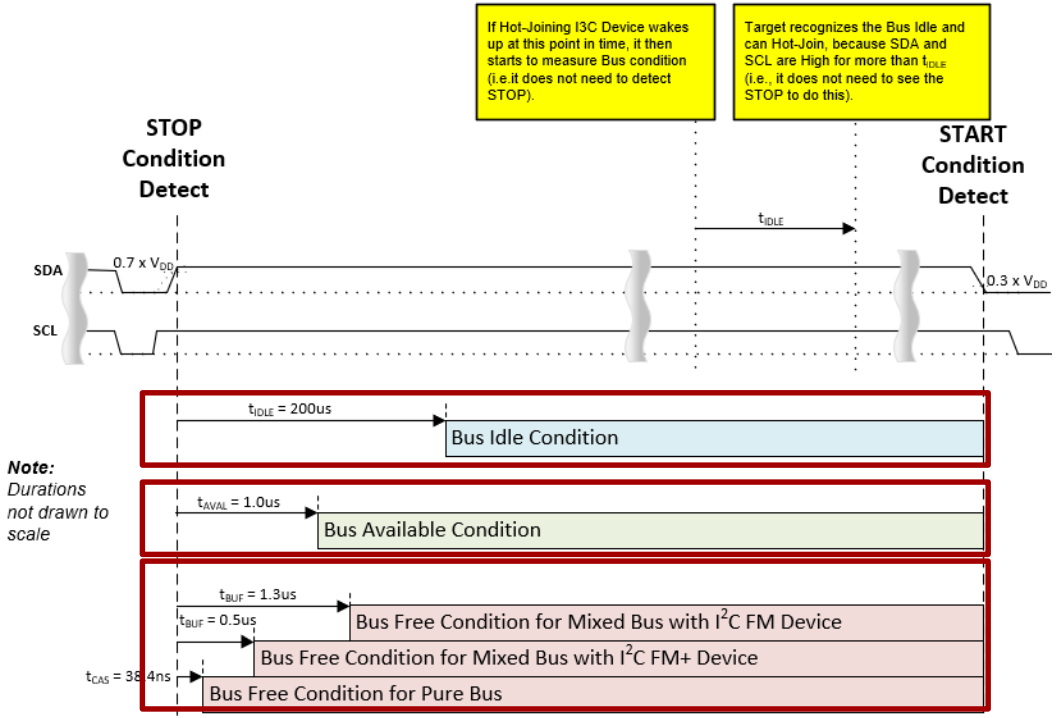
I3C characteristics registers describe and define an I3C compatible device's **capabilities and functions** on the I3C bus, as the device services a given system.

Bus characteristics register (BCR)	Device characteristics register (DCR)	Legacy virtual register (LVR)
Describes I3C compliant device's role and capabilities for use in dynamic address assignment and common command codes • For example, IBI request capable, max data speed limitation)	Describes the I3C compliant device type (For example, accelerometer, gyroscope, etc.) • 255 available codes for describing the type of sensor, or device. • Default value is 8'b0: generic device	Describes I^2C legacy device's significant features • allowed I^2C modes and maximum SCL clock frequency of I^2C device connected on an I3C bus)

I3C | Bus condition timing definitions

Bus conditions are defined from STOP on the bus:

- **t_{CAS}** is referred as **bus free time** and period occurring after a STOP and before a START
  - For Pure bus: A duration of at least t_{CAS}
  - For Mixed bus (i.e., at least one legacy I^2C device is present on the I3C Bus): A duration of atleast t_{BUF}
- **t_{AVAL}** is referred as **bus available time** and is the minimum time the target device must wait before asserting in-band-interrupt
- **t_{IDLE}** is referred as **bus Idle time** and is the minimum time a non-participating device must wait before requesting hot-join
  - A requesting device does not need to monitor Stop if it sees bus idle for t_{IDLE} duration.



Bus condition timing

I3C | Dynamic address assignment (DAA)

- Regular exchanges on the I3C bus require a dynamic 7-bit address
- In order to support dynamic address assignment procedure, each MIPI I3C device to be connected to I3C bus shall be uniquely identifiable in one of two ways before starting the procedure:

1. Device has static address

- **SETDASA:** (Direct CCC) The primary controller assigns dynamic addresses to ANY I3C devices with a known static address using SETDASA
- **SETAASA:** (Broadcast CCC) The primary controller assigns ALL I3C devices their known I^2C static address using SETAASA

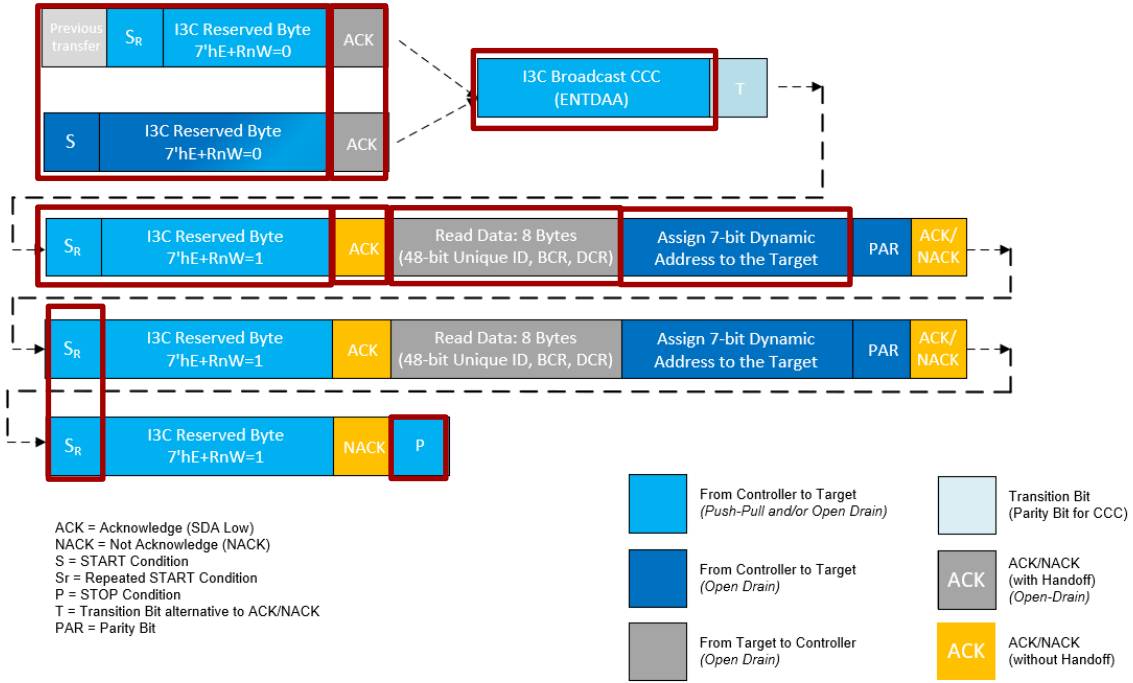
2. Device supports ENTDAA

Device that supports broadcast command code **ENTDAA** shall have its own 48-bit provisional ID (PID)

- 15 bits for MIPI manufacturer ID
- 1 bit indication if the below values are random or not
- 32 bits for part ID, instance ID and some bits reserved for vendor definition

- PID, BCR and DCR will be advertised during the DAA procedure

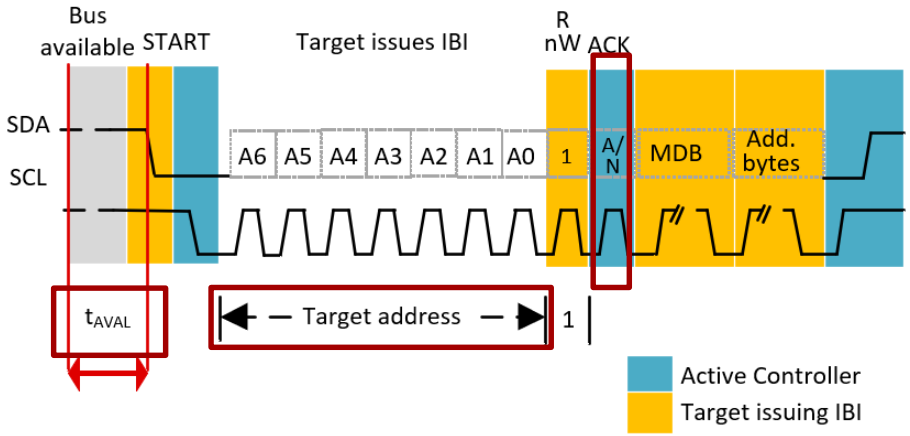
I3C | Dynamic address assignment (DAA)



Dynamic address assignment transaction

I3C | In band interrupt (IBI)

- Device driven in-band interrupts handled through I3C BUS
- The device can raise an interrupt in the following condition:
  - Target device can issue START request when in “bus available” state and waits for the controller to acknowledge the interrupt by pulling SCL low to end the start condition
- Controller provides interface clock for target to drive it’s controller-assigned address onto the bus
- Lowest assigned address wins arbitration in open-drain configuration; controller ACKs or NACKs the interrupt
- Some devices may also provide a mandatory byte that the controller must read

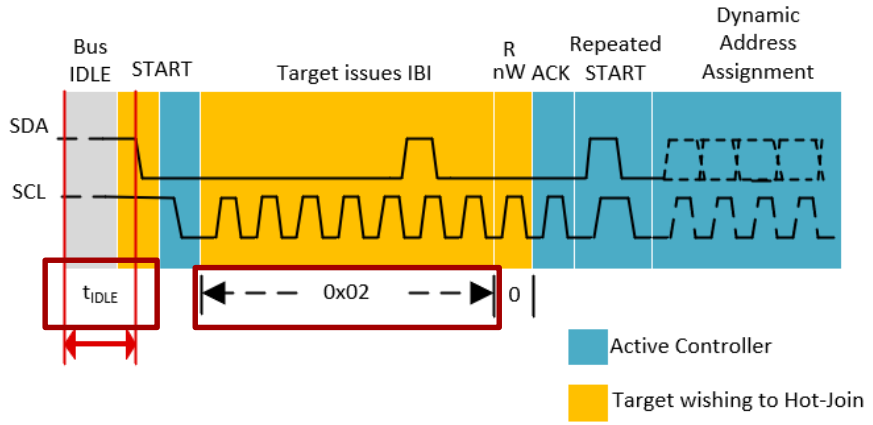


- Fast and efficient asynchronous data acquisition, and event processing
- Avoids extra dedicated wires or inefficient polling mechanism

I3C | Hot-join (HJ)

Allows I3C targets to join the bus after it has already been configured

- Target must wait for a bus idle condition before sending the hot-join request
- Target sends a special in-band-interrupt (IBI) request to trigger the hot-join procedure.
- Joining target issues reserved target address with predefined high-priority
- Controller initiate a new dynamic address assignment (DAA) procedure.
- Unlike typical IBI, hot-join does not have data payload or mandatory data byte



- Improved power management, energy savings
  - Selective powering of sub-units
  - Wake-up only when needed

Ideal for I3C Devices:

- Mounted on the same board, but de-powered until needed
- Mounted on module/board that is physically inserted after I3C bus has already been configured

I3C | Timing control

I3C includes optional timing control and timestamping of events generated by I3C devices resident on the I3C Bus

Synchronous time control

- Controller periodically emits a synchronization pulse
- Targets collect the data at synchronized times, so that the controller can read several targets' data in a single system awake period

➢Avoids drift of individual targets' clocks
➢Ensures that samples occur close together in time

Asynchronous timing control

Target device timestamps events occurring within that target at a particular frequency, and then notifies the controller about it by generating an In-band interrupt (IBI)

- ➢ Four Async modes
  - ➢ Basic – Async mode 0
  - ➢ Enhanced – Async mode 1, 2 & 3

➢ Controller always has the time information at which target data acquisition occurred

I3C | Common command codes (CCC)

I3C standardized command set for interaction between host and device(s).

- Used for standard operations like enabling/disabling events, managing I3C-specific features, and other Bus operations
- In I^2C the similar function was achieved using special address

➢ Built-in Commands (>40) in separate “space” to avoid collision with normal controller to target messages

Type of command frames

Broadcast CCC ➔ Host to all I3C devices

- All Broadcast CCCs are write CCCs (Command codes 0x00 to 0x7F)

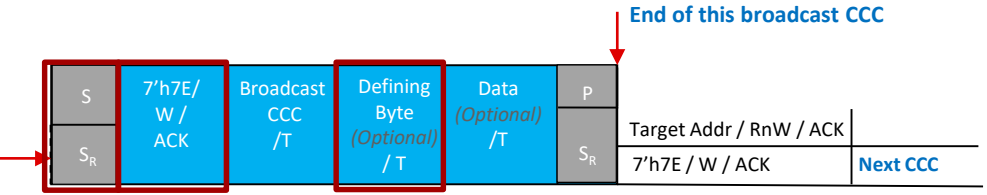
Direct CCC ➔ Host to specific devices

- Three types of Direct CCCs: Read, write, and read/write (command codes from 0x80 to 0xFE)

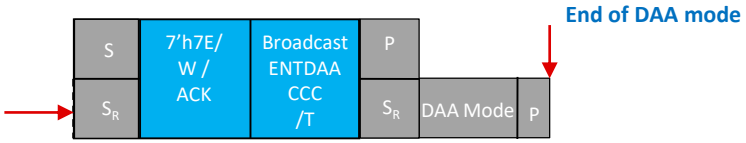
CCC Implementation

Mandatory: Every I3C device must support it. E.g., ENEC for enabling events for interrupt.
Conditional: If certain features are required, then these must be implemented. E.g. SETNEWDA for dynamic address reassignment and implemented only if ENTDAA is supported.
Optional: Implementation specific. E.g. SETDASA for dynamic address assignment to a device with a known static address.

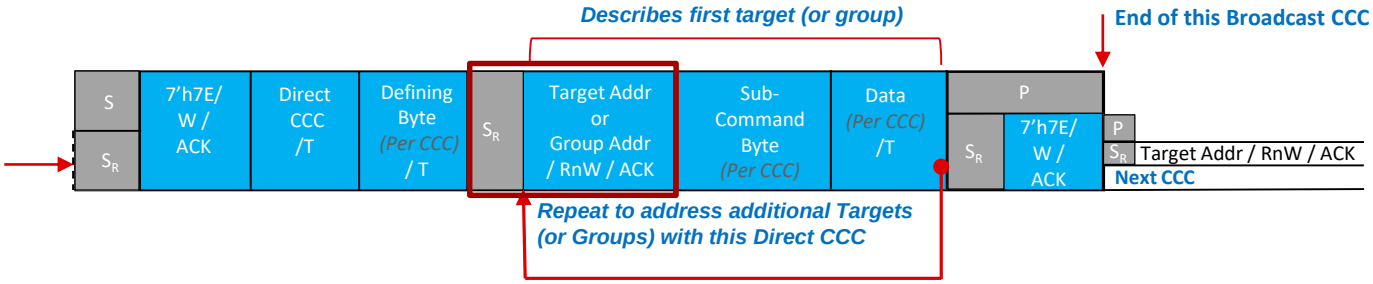
I3C | Common command codes (CCC) format



CCC broadcast general frame format



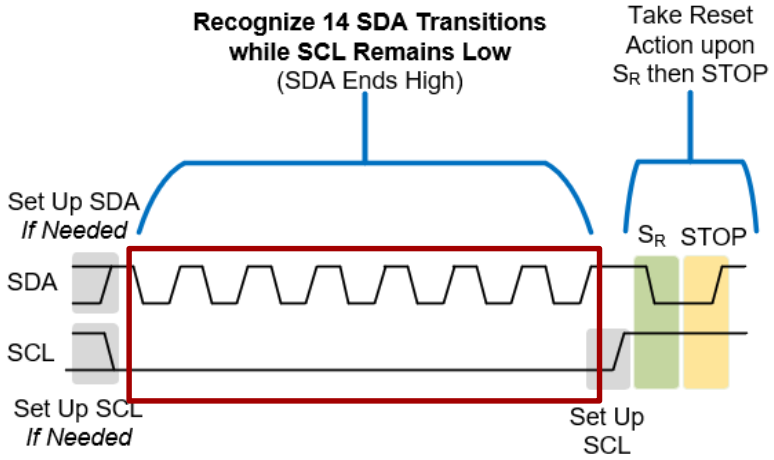
Example: "ENTDAA" format



CCC direct general frame format

I3C | Target reset

- Allows the controller to reset one or more selected targets
- Target reset pattern is used to trigger the default or configured reset action
- RSTACT CCC specifies how the targets should react to a “reset pattern”:
  - Discard
  - Reset the bus controller
  - Reset the entire chip
- **Target Reset Pattern** begins with 14 SDA transitions while SCL is kept Low, and ends with a repeated START followed by a STOP which triggers the actual reset action.



Target Reset Pattern

- Useful in avoiding deadlocks on the bus due to an unresponsive device
- Avoids extra dedicated wires for reset

I3C | Error detection & recovery

- The MIPI I3C bus specification details error detection and error recovery methods for an SDR target, the I3C controller and HDR mode(s)
- A set of 6 mandated methods and 2 optional methods are specified for MIPI I3C target devices, and a separate set of required methods is specified for MIPI I3C controller devices.

➢ Help avoid fatal conditions when errors occur

Error Type	Description
CE0	Transaction after sending CCC
CE1 (optional)	Monitoring error
CE2	No response to broadcast address (7'h7E)
CE3	Failed controller handoff

SDR controller error types

Error Type	Description
TE0	Invalid broadcast address/W (7'h7E/W) or dynamic address/RnW after dynamic address assignment
TE1	CCC code
TE2	Write data
TE3	Assigned address during dynamic address arbitration
TE4	7'h7E/R missing after Sr during dynamic address arbitration
TE5	Transaction after detecting CCC
TE6 (optional)	Monitoring error
DBR (optional)	Dead bus recovery

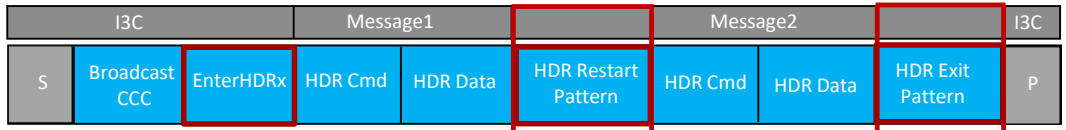
SDR target error types

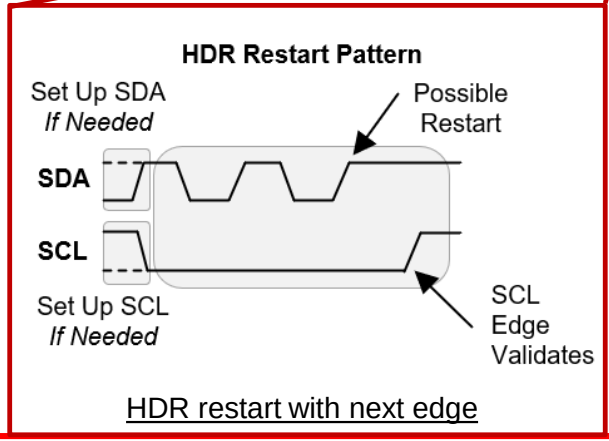
I3C Protocol

High data rate (HDR) modes & multi-lane (ML) data transfer

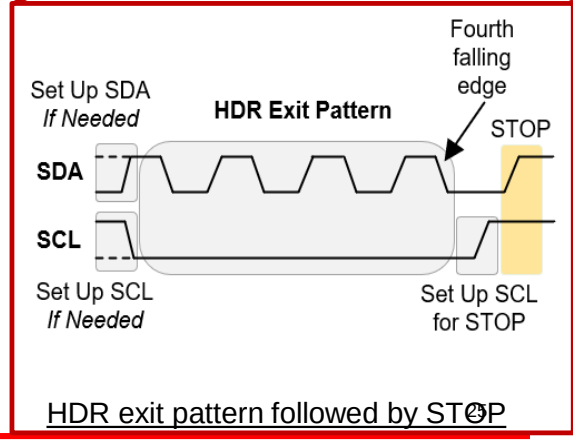
I3C | High data rate (HDR) modes

- MIPI I3C HDR modes allow to transfer more data while preserving SDR frequency
  - **HDR-DDR (Double data rate)**
    - data rate up to 25 Mbps
  - **HDR-TSL (Ternary symbol legacy-inclusive-bus)**
    - data rate up to 27.5 Mbps
  - **HDR-TSP (Ternary symbol pure-bus)**
    - data rate up to 39.5 Mbps
  - **HDR-BT (Bulk transport)**
    - data rate up to 100 Mbps
- Each I3C bus transaction begins in SDR mode, but the I3C controller may issue an "Enter HDR" CCC broadcast command which tells all I3C targets that the transaction will continue in a specified HDR mode
- While in HDR mode, repeated START and STOP are replaced with HDR Restart and HDR Exit patterns





HDR restart with next edge



HDR exit pattern followed by STOP

I3C | Multi lane (ML) mode

- ML mode employs any available additional physical wires to transfer the data payload faster.
- In ML the normal I3C SDA line is referred to as SDA[0], and the additional wires are called SDA[1], SDA[2], and SDA[3].
- During ML data transfers, activity on the additional data wire(s) (i.e., SDA[1], SDA[2], and SDA[3]) would not be visible to any non-ML Devices that might be resident on that Bus
- Reduced energy consumption and increased flexibility in adding features
  - An application with a camera module using quad Lanes, IMU using Dual lanes

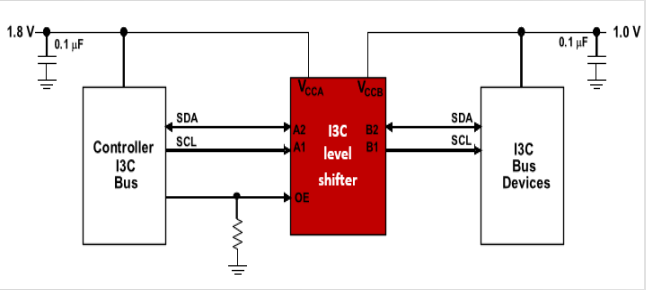
No. of Additional Data Wires	Lane Configuration	Description	Multi-Lane?	Data Wires	Total Wires	Wires Supported				
						SCL	SDA[0]	SDA[1]	SDA[2]	SDA[3]
0	SINGLE	Ordinary 2-Wire I3C	N	1	2	✓	✓	-	-	-
1	DUAL	Multi-Lane Data Transfer	Y	2	3	✓	✓	✓	-	-
3	QUAD		Y	4	5	✓	✓	✓	✓	✓
2, 4 through 7	Reserved for future definition by MIPI Alliance									

ML configurations

I3C applications in different end equipment

I3C | Applications in servers

I3C translation

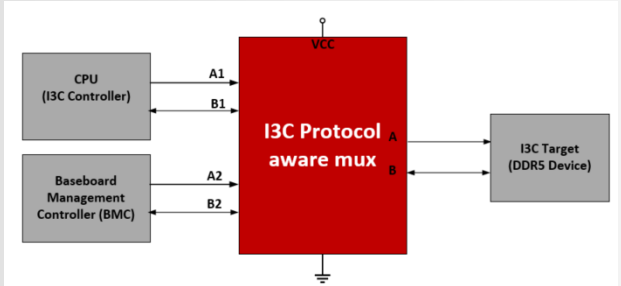


Use case:

- Node voltages on either A or B side could be
  - 1.2V and 1.0V
  - 1.8V and 1.0V

JEDEC DDR5 spec requires operation at I3C speeds (12.5MHz) and IO level at 1.0V

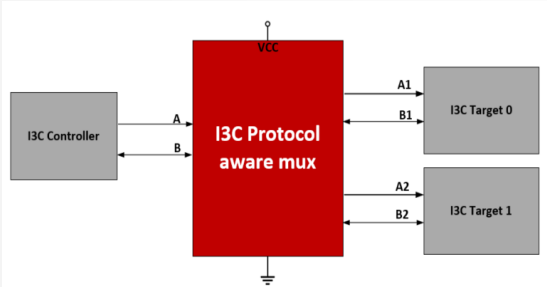
I3C protocol aware switching/multiplexing



Use case:

Used in various motherboard applications.

- Switching for the CPU and BMC to the DDR5 device; Either CPU or BMC can be selected as Active Controller which has control of the Target port as well as the I3C mux

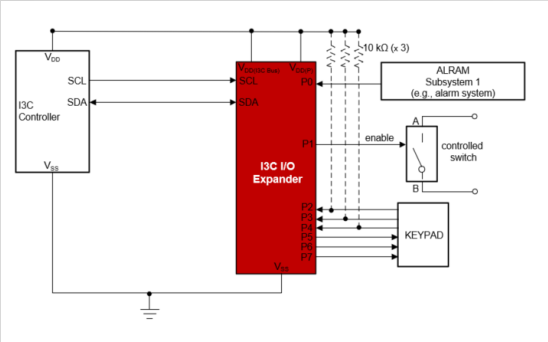


Use case:

- I3CTarget devices that share the same address can use the I3C protocol aware multiplexer to prevent Target address conflicts

I3C | Applications in servers & memory

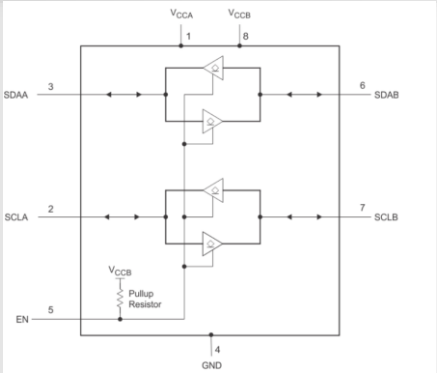
I3C IO expansion



Use case:

- Used when there is need for additional GPIO input and output in an application.
  - I/O pins to be configured as input only, output only or Input/output

I3C protocol aware buffer

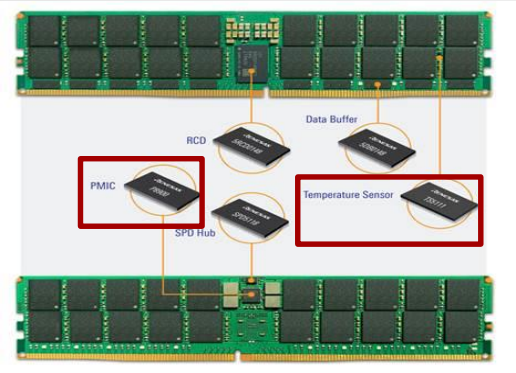


Use case:

- Buffering I3C signal, allowing the connection of multiple I3C Targets to the downstream bus (especially when using long buses)

MIPI I3C specifies bus loading of 50pF

DDR5 DIMM

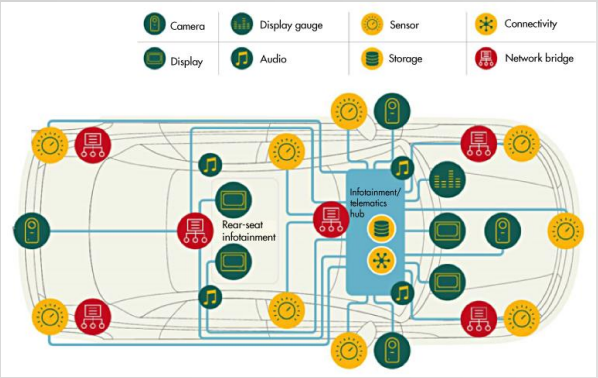


Use case:

- Using temperature sensor to monitor thermal changes in DIMM. PMIC enables configurability of voltage ramps and level and provides voltage regulation

I3C | Applications in other end equipment's

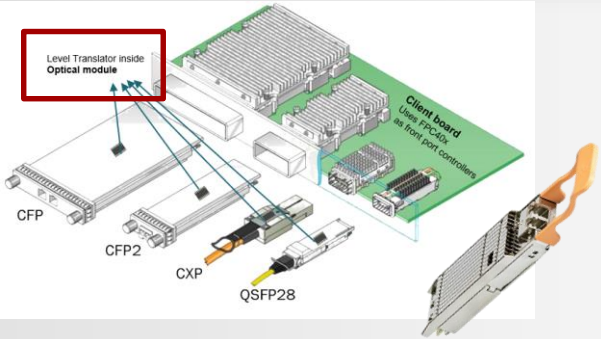
Automotive



Use case:

- Physical sensors such as Inertial measurement unit (IMU) is co-located with an ECU), I3C can be used for sensor data transport and control for its reliability, low-latency, and low-cost connectivity

Communications equipment



Octal small factor pluggable (OSFP)

Use case:

- OSFP pluggable optical modules use I3C as optical interface
- I3C Level translator provides translation between host controller at 3.3V and OSFP module at I3C speeds and low IO voltage

Other EE

Wearables

Healthcare

Smart home

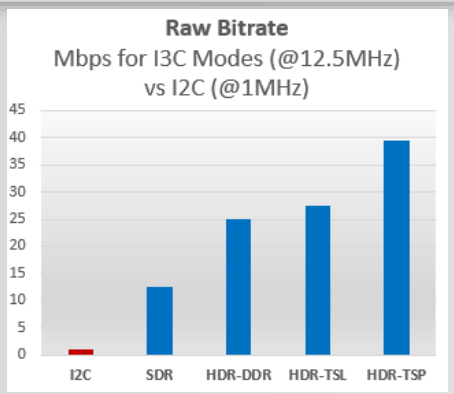
Drone controllers

Use case:

- I3C provides a shared, two wire interface, to connect sensors, and simple UI components such as LEDs and buttons
- High speed data transfer at very low power levels is highly desirable for any embedded system

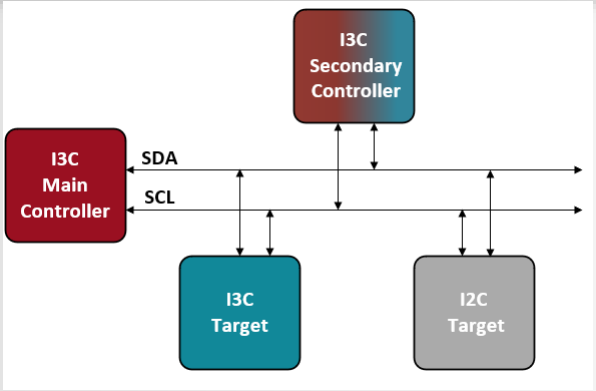
I3C | Summary

Fast efficient communication channel with advanced functions



- Multidrop SDA/SCL 2-wire interface
  - 12.5 MHz max clock rate
- Dynamic switch between pullup/push pull/Hi-Z
- SDR (Single Data Rate) – 12.5 Mbps
- HDR modes for higher throughput
- Broadcast & direct messages
- Error detection & Recovery
- Target reset, in-band interrupt, jot-join
- Timing control

System management & backward compatibility



- Device roles: I3C primary & secondary controllers
- Dynamic address assignment (including group addressing)
- Standardized commands for bus management, configuration and control
- Backwards compatible allowing mixed bus operation

Key Resources

- **MIPI I3C Basic Specification v1.1.1**
  - https://resources.mipi.org/mipi-i3c-basic
- **MIPI I3C Specification v1.1.1**
  - https://www.mipi.org/specifications/i3c-sensor-specification
- **Application brief:** I3C – Next Generation Serial Communication Interface
- **Application brief:** Enhance Thermal Sensing Performance With I3C Bus