UART Protocol Overview
TI Precision Labs – Microcontrollers

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The UART

- UART – Universal Asynchronous Receiver Transmitter
- Requires only 2-pins, RXD and TXD
- No additional synchronization pin or clock signal is needed
- Synchronization by adding START and STOP bits to data
UART Hardware Protocol

- UART Data Frame
- Start bit – synchronizes receiver to start of frame
- Data bits - data
- Parity bit – single bit error detection (optional)
- Stop bit – signals end of the frame
- Second Stop bit (optional)
UART Parity Example

• PARITY provides single bit error detection (optional)
• PARITY options are Even, Odd, None
• Both UARTs must be configured the same
• Transmitter generates PARITY bit
  – Even Parity configuration
  – Sum of frame = 6 (even)
  – PARITY bit set to 0

• Received packet
  – Count number of ‘1’s
  – Add PARITY bit value
  – If sum is even, data is valid

<table>
<thead>
<tr>
<th>START</th>
<th>D0</th>
<th>D1</th>
<th>D2</th>
<th>D3</th>
<th>D4</th>
<th>D5</th>
<th>D6</th>
<th>D7</th>
<th>PARITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>1+1+1+1+0+1+1+0</td>
<td>6</td>
<td>so PARITY bit set to 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tbody>
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<th>D6</th>
<th>D7</th>
<th>PARITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>1+1+1+1+0+1+1+0</td>
<td>6+0 (parity)</td>
<td>6, so data is valid</td>
<td></td>
<td></td>
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</table>
UART Parity Example – Error Detected

• Transmitter generates PARITY bit
  – Even parity configuration
  – Sum of frame = 6
  – PARITY bit set to 0

• Received packet
  – Noise changes bit D1
  – Count number of ‘1’s
  – Add PARITY bit value
  – Sum is odd, data is not valid
  – Parity error flag set
Baud Rates

• Common Baud Rates are 9600, 19200, 115200
• UARTs must use same baud rate
• System clock and Baud Rate Divisor (BRD)

\[ \text{Fclk} = 1\text{MHz} \]
\[ \text{BRD} = X \]

\[ \text{Fclk} = 8\text{MHz} \]
\[ \text{BRD} = Y \]
Baud Rate - Maximum Error Tolerance

- Typical maximum baud rate error tolerance is 2-3%
- Bit error accumulation
- START bit synchronization
- RX Signal rise and fall times
Baud Rate Accumulation Errors

- Receiver uses oversample clock (16x baud rate clock)
- Faster baud
- Slower baud rate
Baud Rate Accumulation Errors

- Theoretical Maximum Accumulated bit tolerance
- Bit error margin or margin of error
- Example with a faster clock:
  - Accumulated error = ± 40% over 10 bit periods
Start bit Synchronization Error

• START bit falling edge
• Sampling clock synchronization tolerance
• 1/16 clock cycle or 6.25% of the START bit period
RX Signal slew rate (rise/fall times)

- Rise/Fall timing delays
- Caused by added capacitance

![Diagram showing RX signal slew rate with rise/fall errors and sampling clock.]
Example Baud Rate Error Tolerance Calculation

Receiver = Transmitter Baud Rate (Ideal)

±50% margin

Example calculation
Find actual margin:

- 50% (Ideal Margin) - 6.25% (Synchronization error) - 2% (Rise/fall error) = 41.75% (Actual margin)

Calculate baud rate margin:

41.75% ÷ 10 = ±4.175%

Transmitter and receiver clock can vary by 4.175% without any bit errors
Summary

• UART Interface and Synchronization
• UART Hardware Protocol
• Parity Examples
• Baud rate calculations
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