ADS5474-SP Class V, 14-bit, 400MSPS Analog-to-Digital Converter

1 Features

- Sample rate: 400MSPS
- 14-Bit resolution, 10.9 bits effective number of bits (ENOB)
- 5962R13208:
  - Radiation hardness assurance (RHA): up to TID 100krad (Si)
  - Total ionizing dose: 100krad (Si)
  - ELDRS free: 100krad (Si)
  - SEL/SEU Characterized
- Input bandwidth: 1.28GHz
- SFDR = 78dBc at 230MHz and 400MSPS
- SNR = 69.8dBFS at 230MHz and 400MSPS
- Differential input voltage: $2.2V_{PP}$
- LVDS-Compatible outputs
- Total power dissipation: 2.5W
- Power down mode: 50mW
- Offset binary output format
- Output data transitions on the rising and falling edges of a half-rate output clock
- On-chip analog buffer, track-and-hold, and reference circuit
- Available in an 84-pin ceramic non-conductive tie-bar package (HFG)
- Military temperature range: –55°C to 125°C T_{case}
- Engineering evaluation (/EM) samples are available [1]
- Pin-similar and compatible with 12- and 14-bit family: ADS5463-SP and ADS5444-SP

2 Applications

- Test and measurement instrumentation
- Software defined radio
- Data acquisition
- Power amplifier linearization
- Communication instrumentation
- Radar

3 Description

The ADS5474 is a 14-bit, 400MSPS analog-to-digital converter (ADC) that operates from both a 5V supply and 3.3V supply while providing LVDS-compatible digital outputs. This ADC is one of a family of 12-, 13-, 14-bit ADCs that operate from 210MSPS to 500MSPS. The ADS5474 input buffer isolates the internal switching of the onboard track and hold (T&H) from disturbing the signal source while providing a high-impedance input. An internal reference generator is also provided to simplify the system design.

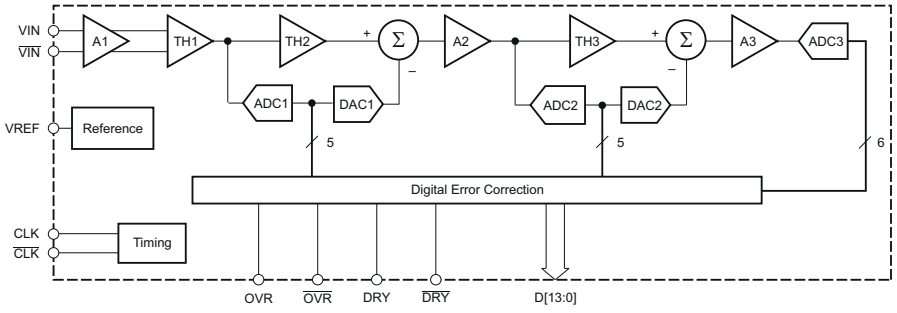
Designed with a 1.4GHz input bandwidth for the conversion of wide-bandwidth signals that exceed 400MHz of input frequency at 400MSPS, the ADS5474 has outstanding low noise performance and spurious-free dynamic range over a large input frequency range.

The ADS5474 is available in an 84-pin ceramic non-conductive tie-bar package (HFG). The device is built on Texas Instruments complementary bipolar process (BiCom3) and is specified over the full military temperature range (–55°C to 125°C T_{case}).

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
ADS5474-SP	CFP (HFG, 84)	19.05mm × 19.05mm

(1) For all available packages, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

[1] These units are intended for engineering evaluation only. They are processed to a non-compliant flow (e.g. No Burn-In, etc.) and are tested to a temperature rating of 25°C only. These units are not suitable for qualification, production, radiation testing or flight use. Parts are not warranted for performance over the full MIL specified temperature range of –55°C to 125°C or operating life.

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4 Pin Configuration and Functions

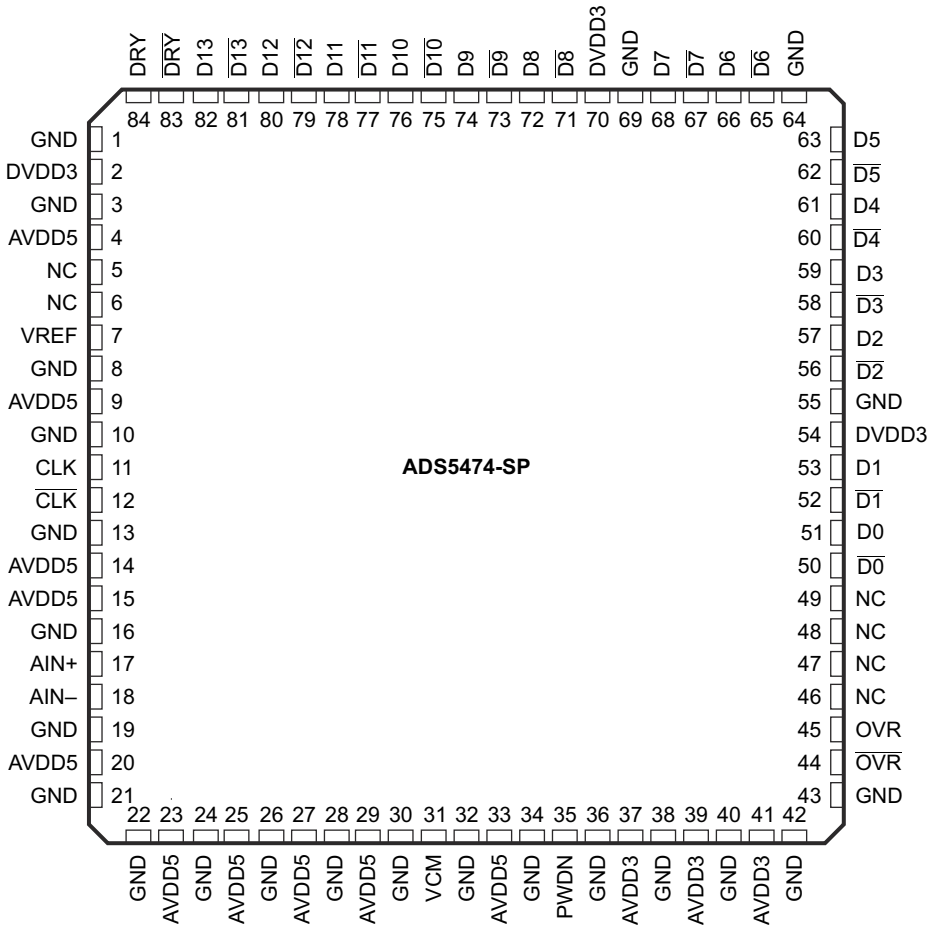


Figure 4-1. HFG Package, 84-Pin CFP (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
AIN	17	I	Differential input signal (positive)
$\overline{\text{AIN}}$	18	I	Differential input signal (negative)
AVDD3	37, 39, 41	P	Analog power supply (3.3V)
AVDD5	4, 9, 14, 15, 20, 23, 25, 27, 29, 33	P	Analog power supply (5V)
CLK	11	I	Differential input clock (positive). Conversion is initiated on rising edge.
$\overline{\text{CLK}}$	12	I	Differential input clock (negative)
$\overline{\text{D0}}$, D0	50, 51	O	LVDS digital output pair, least-significant bit (LSB)
$\overline{\text{D1}}$, D1, $\overline{\text{D2}}$–D5, $\overline{\text{D6}}$-D7, $\overline{\text{D8}}$-D12	52, 53, 56–63, 65–68, 71–82	O	LVDS digital output pairs
$\overline{\text{D13}}$, D13	81, 82	O	LVDS digital output pair, most significant bit (MSB)
DRY, $\overline{\text{DRY}}$	84, 83	O	Data ready LVDS output pair
DVDD3	2, 54, 70	P	Digital and output driver power supply (3.3V)

Table 4-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
GND	1,3, 8, 10, 13, 16, 19, 21, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40, 42, 43, 55, 64, 69	GND	Ground
NC	5, 6, 46, 47, 48, 49	N/A	No connect
OVR, $\overline{\text{OVR}}$	45, 44	O	Over-range indicator LVDS output. A logic high signals an analog input in excess of the full-scale range.
PDWN	35	I	Power-down (active high). Device is in sleep mode when PDWN pin is logic HIGH. ADC converter is awake when PDWN is logic LOW (grounded). (This pin is not used on the ADS5463-SP and ADS5444-SP)
VCM	31	O	Common-mode voltage output (3.1V nominal). Commonly used in DC-coupled applications to set the input signal to the correct common-mode voltage. (This pin is not used on the ADS5463-SP and ADS5444-SP)
VREF	7	I/O	Reference voltage input/output (2.4V nominal)

(1) I = input, O = output, GND = ground, P = power, I/O = bidirectional, N/A = not applicable

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted(1)

		MIN	MAX	UNIT
Supply voltage	AVDD5 to GND		6	V
	AVDD3 to GND		5	V
	DVDD3 to GND		5	V
Analog input to GND		–0.3	AVDD5 + 0.3	V
Clock input to GND		–0.3	AVDD5 + 0.3	V
CLK to $\overline{CLK}$		–2.5	2.5	V
Digital data output to GND		–0.3	DVDD3 + 0.3	V
Operating case temperature	T_C	–55	125	°C
Maximum junction temperature	T_J		150	°C
Storage temperature	T_{stg}	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
SUPPLIES					
AVDD5	Analog supply voltage	4.75	5	5.25	V
AVDD3	Analog supply voltage	3.1	3.3	3.6	V
DVDD3	Output driver supply voltage	3	3.3	3.6	V
ANALOG INPUT					
	Differential input range		2.2		V_{PP}
VCM	Input common mode		3.1		V
DIGITAL OUTPUT (DRY, DATA, OVR)					
	Maximum differential output load		10		pF
CLOCK INPUT (CLK)					
	CLK input sample rate (sine wave)	20(1)		400	MSPS
	Clock amplitude, differential sine wave(1)	0.5		5	V_{PP}
	Clock duty cycle (1)	40%	50%	60%	
T_C	Operating case temperature range	–55		125	°C

(1) Parameters are assured by characterization, but not production tested.

5.4 Thermal Information

(1)

THERMAL METRIC		TEST CONDITIONS	TYP	UNIT
$R_{\theta JA}$	Junction-to-free-air thermal resistance	Junction-to-case thermal resistance	21.81	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	MIL-STD-883 Test Method 1012	0.849	

(1) This CQFP package has built-in vias that electrically and thermally connect the bottom of the die to a pad on the bottom of the package. To efficiently remove heat and provide a low-impedance ground path, a thermal land is required on the surface of the PCB directly underneath the body of the package. During normal surface mount flow solder operations, the heat pad on the underside of the package is soldered to this thermal land creating an efficient thermal path. Normally, the PCB thermal land has a number of thermal vias within it that provide a thermal path to internal copper areas (or to the opposite side of the PCB) that provide for more efficient heat removal. TI typically recommends an 11.9mm^2 board-mount thermal pad. This allows maximum area for thermal dissipation, while keeping leads away from the pad area to prevent solder bridging. A sufficient quantity of thermal/electrical vias must be included to keep the device within recommended operating conditions. This pad must be electrically at ground potential.

5.5 Electrical Characteristics

Typical values at T_C = 25°C: minimum and maximum values over full temperature range $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 400MSPS, 50% clock duty cycle, AVDD5 = 5V, AVDD3 = 3.3V, DVDD3 = 3.3V, –1dBFS differential input, and 3V_{PP} differential clock, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution				14		bits
ANALOG INPUTS						
	Differential input range			2.2		V_{PP}
	Analog input common-mode voltage	Self-biased; see VCM specification below		3.1		V
	Input resistance (dc)	Each input to VCM		500		Ω
	Input capacitance	Each input to GND		2.8		pF
	Analog input bandwidth (–3dB)			1.28		GHz
CMRR	Common-mode rejection ratio	Common-mode signal < 50MHz (see Figure 5-28)		100		dB
INTERNAL REFERENCE VOLTAGE						
VREF	Reference voltage			2.4		V
VCM	Analog input common-mode voltage reference output	With internal VREF. Provided as an output via the VCM pin for dc-coupled applications.	2.9	3.1	3.3	V
	VCM temperature coefficient			–0.8		mV/°C
DYNAMIC ACCURACY						
	No missing codes			Assured		
DNL	Differential linearity error	f_{IN} = 10MHz	–0.99	±0.7	2.5	LSB
INL	Integral linearity error	f_{IN} = 10MHz	–7.0	±1.5	7.0	LSB
	Offset error		–16		16	mV
	Offset temperature coefficient			0.02		mV/°C
	Gain error		–5		5	%FS
	Gain temperature coefficient			–0.02		%FS/°C
POWER SUPPLY						
I_{AVDD5}	5V analog supply current	V_{IN} = full-scale, f_{IN} = 70MHz, f_S = 400MSPS		338	380	mA
I_{AVDD3}	3.3V analog supply current			185	210	mA
I_{DVDD3}	3.3V digital supply current (includes LVDS)			75	85	mA
	Total power dissipation			2.5	2.835	W
	Power-up time	From turn-on of AVDD5		50		µs

5.5 Electrical Characteristics (continued)

Typical values at T_C = 25°C: minimum and maximum values over full temperature range $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 400MSPS, 50% clock duty cycle, AVDD5 = 5V, AVDD3 = 3.3V, DVDD3 = 3.3V, –1dBFS differential input, and $3V_{PP}$ differential clock, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Wake-up time	From PDWN pin switched from HIGH (PDWN active) to LOW (ADC awake) (see Figure 5-29)		5		µs
	Power-down power dissipation	PDWN pin = logic HIGH		50	350	mW
PSRR	Power-supply rejection ratio, AVDD5 supply	Without 0.1µF board supply capacitors, with < 1MHz supply noise		75		dB
PSRR	Power-supply rejection ratio, AVDD3 supply			90		dB
PSRR	Power-supply rejection ratio, DVDD3 supply			110		dB
DYNAMIC AC CHARACTERISTICS						
SNR	Signal-to-noise ratio	f_{IN} = 30MHz		70.5		dBFS
		f_{IN} = 70MHz	65	68.7		
		f_{IN} = 130MHz		69.9		
		f_{IN} = 230MHz	65	69.8		
		f_{IN} = 351MHz		69.2		
		f_{IN} = 451MHz		68.8		
		f_{IN} = 651MHz		67.3		
		f_{IN} = 751MHz		66.6		
		f_{IN} = 999MHz		64.4		
SFDR	Spurious-free dynamic range	f_{IN} = 30MHz		79.4		dBc
		f_{IN} = 70MHz	69	76.3		
		f_{IN} = 130MHz		78.8		
		f_{IN} = 230MHz	64.5	78		
		f_{IN} = 351MHz		74.3		
		f_{IN} = 451MHz		70.5		
		f_{IN} = 651MHz		58.6		
		f_{IN} = 751MHz		54.3		
		f_{IN} = 999MHz		46		
HD2	Second-harmonic	f_{IN} = 30MHz		92		dBc
		f_{IN} = 70MHz		87		
		f_{IN} = 130MHz		87		
		f_{IN} = 230MHz		84		
		f_{IN} = 351MHz		77		
		f_{IN} = 451MHz		75		
		f_{IN} = 651MHz		68		
		f_{IN} = 751MHz		64		
		f_{IN} = 999MHz		53		

5.5 Electrical Characteristics (continued)

Typical values at T_C = 25°C: minimum and maximum values over full temperature range $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 400MSPS, 50% clock duty cycle, AVDD5 = 5V, AVDD3 = 3.3V, DVDD3 = 3.3V, –1dBFS differential input, and $3V_{PP}$ differential clock, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD3	Third-harmonic	f_{IN} = 30MHz		81		dBc
		f_{IN} = 70MHz		86		
		f_{IN} = 130MHz		80		
		f_{IN} = 230MHz		80		
		f_{IN} = 351MHz		76		
		f_{IN} = 451MHz		72		
		f_{IN} = 651MHz		60		
		f_{IN} = 751MHz		56		
		f_{IN} = 999MHz		48		
	Worst harmonic/spur (other than HD2 and HD3)	f_{IN} = 30MHz		93		dBc
		f_{IN} = 70MHz		91		
		f_{IN} = 130MHz		91		
		f_{IN} = 230MHz		88		
		f_{IN} = 351MHz		87		
		f_{IN} = 451MHz		87		
		f_{IN} = 651MHz		91		
		f_{IN} = 751MHz		87		
		f_{IN} = 999MHz		80		
THD	Total harmonic distortion	f_{IN} = 30MHz		77		dBc
		f_{IN} = 70MHz		73.5		
		f_{IN} = 130MHz		74.9		
		f_{IN} = 230MHz		74.9		
		f_{IN} = 351MHz		71.3		
		f_{IN} = 451MHz		68.4		
		f_{IN} = 651MHz		57.8		
		f_{IN} = 751MHz		53.6		
		f_{IN} = 999MHz		45		
SINAD	Signal-to-noise and distortion	f_{IN} = 30MHz		69.8		dBc
		f_{IN} = 70MHz	62.5	67.7		
		f_{IN} = 130MHz		68.9		
		f_{IN} = 230MHz	60.5	68.9		
		f_{IN} = 351MHz		67.5		
		f_{IN} = 451MHz		66.1		
		f_{IN} = 651MHz		58.2		
		f_{IN} = 751MHz		54.3		
		f_{IN} = 999MHz		45.9		
	Two-tone SFDR	f_{IN1} = 69MHz, f_{IN2} = 70MHz, each tone at –7dBFS		84.2		dBFS
		f_{IN1} = 69MHz, f_{IN2} = 70MHz, each tone at –16dBFS		98.5		
		f_{IN1} = 297.5MHz, f_{IN2} = 302.5MHz, each tone at –7dBFS		82.5		
		f_{IN1} = 297.5MHz, f_{IN2} = 302.5MHz, each tone at –16dBFS		99		

5.5 Electrical Characteristics (continued)

Typical values at T_C = 25°C: minimum and maximum values over full temperature range $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 400MSPS, 50% clock duty cycle, AVDD5 = 5V, AVDD3 = 3.3V, DVDD3 = 3.3V, –1dBFS differential input, and $3V_{PP}$ differential clock, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENOB	Effective number of bits	f_{IN} = 70MHz	10.1	10.9		bits
		f_{IN} = 230MHz	9.77	10.5		
	RMS idle-channel noise	Inputs tied to common-mode		1.8		LSB
LVDS DIGITAL OUTPUTS						
V_{OD}	Differential output voltage (±)		247	350	454	mV
V_{OC}	Common-mode output voltage		1.115		1.375	V
DIGITAL INPUTS						
V_{IH}	High level input voltage	PWD (pin 33)	2.0			V
V_{IL}	Low level input voltage				0.8	V
I_{IH}	High level input current				1	µA
I_{IL}	Low level input current		-1			µA
C_{IN}	Input capacitance			2.2		pF

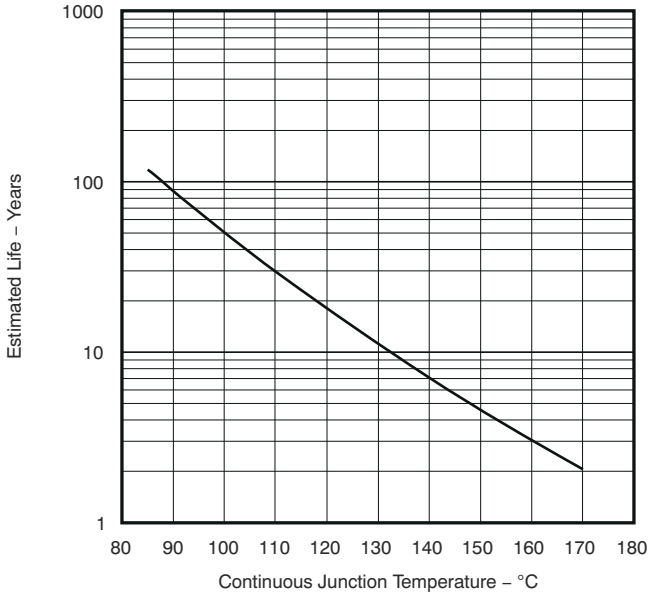


Figure 5-1. Operating Life Derating Chart, Electromigration Fail Mode

5.6 Timing Characteristics

Typical values at T_C = 25°C: minimum and maximum values over full temperature range $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 400MSPS, 50% clock duty cycle, AVDD5 = 5V, AVDD3 = 3.3V, DVDD3 = 3.3V, and $3V_{PP}$ differential clock, unless otherwise noted.

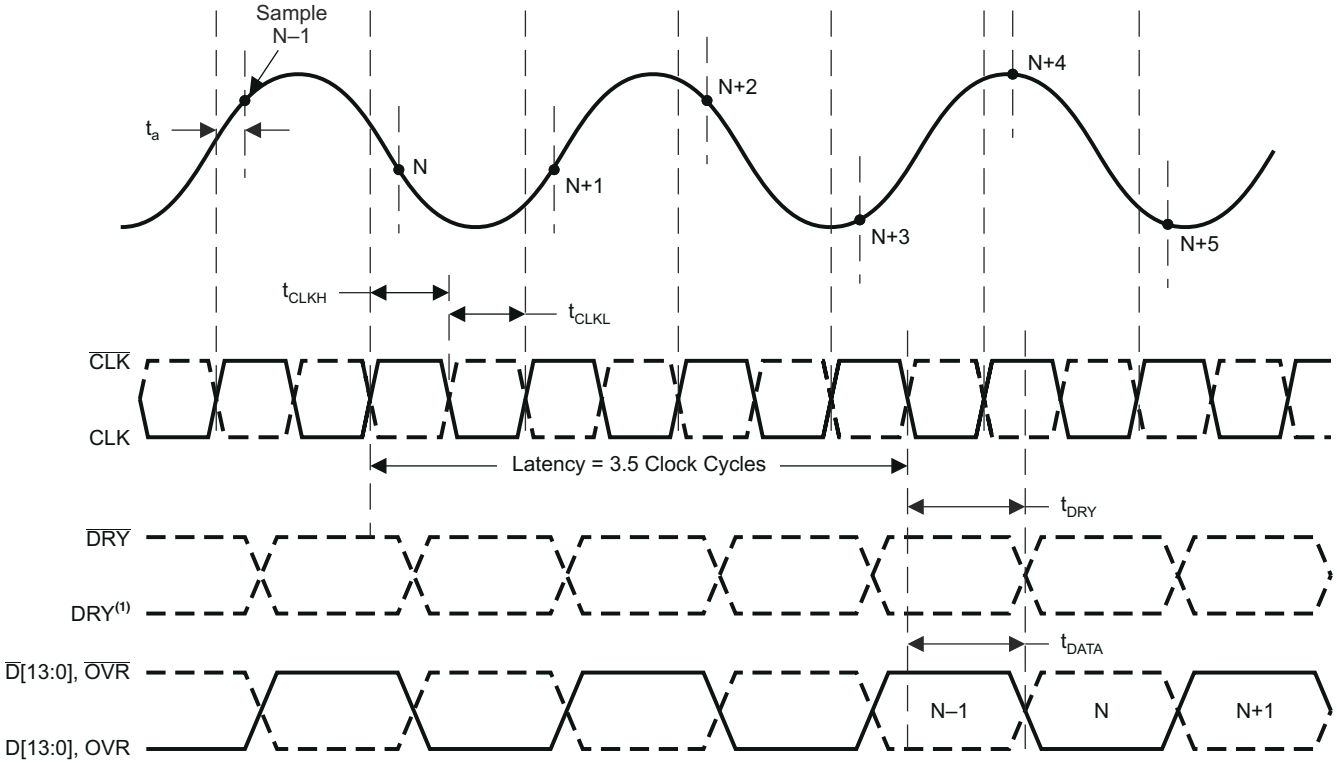
PARAMETER[1]		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_a	Aperture delay			200		ps
	Aperture jitter, rms	Internal jitter of the ADC		103		fs
	Latency			3.5		cycles
t_{CLK}	Clock period		2.5		50	ns
t_{CLKH}	Clock pulse duration, high		1			ns
t_{CLKL}	Clock pulse duration, low		1			ns

5.6 Timing Characteristics (continued)

Typical values at T_C = 25°C: minimum and maximum values over full temperature range $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 400MSPS, 50% clock duty cycle, AVDD5 = 5V, AVDD3 = 3.3V, DVDD3 = 3.3V, and $3V_{PP}$ differential clock, unless otherwise noted.

PARAMETER(1)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DRY}	CLK to DRY delay(2)	Zero crossing, 10pF parasitic loading to GND on each output pin	700	1600	2500	ps
t_{DATA}	CLK to DATA/OVR delay(2)	Zero crossing, 10pF parasitic loading to GND on each output pin	650	1600	2600	ps
t_{SKEW}	DATA to DRY skew	t_{DATA} – t_{DRY}, 10pF parasitic loading to GND on each output pin	-700	0	700	ps
t_{RISE}	DRY/DATA/OVR rise time	10pF parasitic loading to GND on each output pin		500		ps
t_{FALL}	DRY/DATA/OVR fall time	10pF parasitic loading to GND on each output pin		500		ps

(1) Timing parameters are assured by characterization, but not production tested.
(2) DRY, DATA, and OVR are updated on the falling edge of CLK. The latency must be added to t_{DATA} to determine the overall propagation delay.



A. Polarity of DRY is undetermined. For further information, see *Section 6.1.3*.

Figure 5-2. Timing Diagram

5.7 Typical Characteristics

At T_A = 25°C, sampling rate = 400MSPS, 50% clock duty cycle, $3V_{PP}$ differential sinusoidal clock, analog input amplitude = –1dBFS, AVDD5 = 5V, AVDD3 = 3.3V, and DVDD3 = 3.3V, unless otherwise noted.

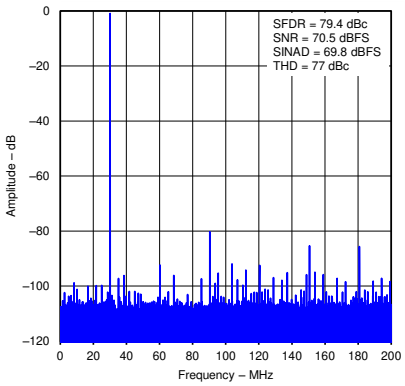


Figure 5-3. Spectral Performance FFT for 30MHz Input Signal

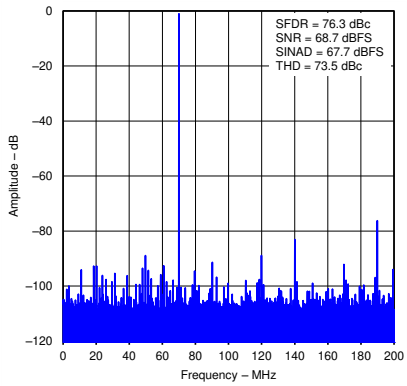


Figure 5-4. Spectral Performance FFT for 70MHz Input Signal

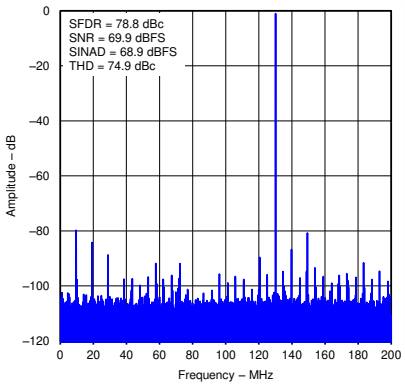


Figure 5-5. Spectral Performance FFT for 130MHz Input Signal

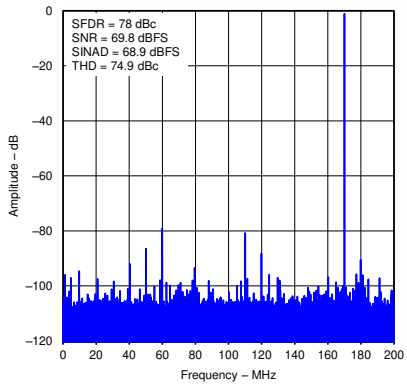


Figure 5-6. Spectral Performance FFT for 230MHz Input Signal

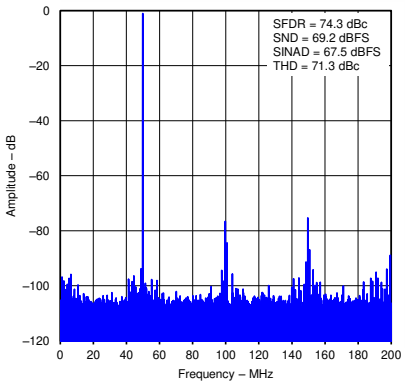


Figure 5-7. Spectral Performance FFT for 351MHz Input Signal

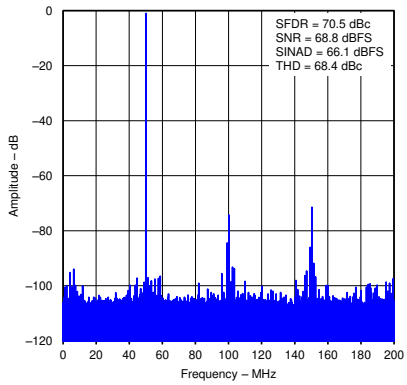


Figure 5-8. Spectral Performance FFT for 451MHz Input Signal

5.7 Typical Characteristics (continued)

At T_A = 25°C, sampling rate = 400MSPS, 50% clock duty cycle, $3V_{PP}$ differential sinusoidal clock, analog input amplitude = –1dBFS, AVDD5 = 5V, AVDD3 = 3.3V, and DVDD3 = 3.3V, unless otherwise noted.

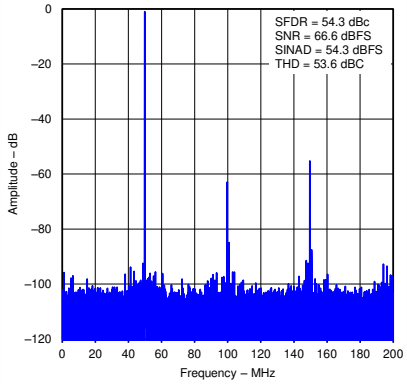


Figure 5-9. Spectral Performance FFT for 751MHz Input Signal

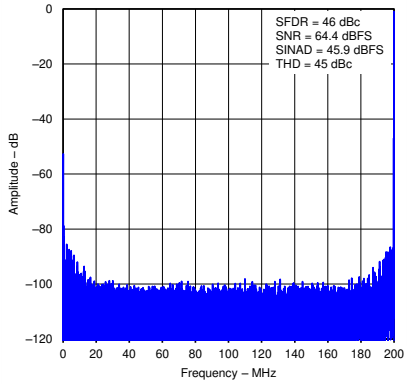


Figure 5-10. Spectral Performance FFT for 999MHz Input Signal

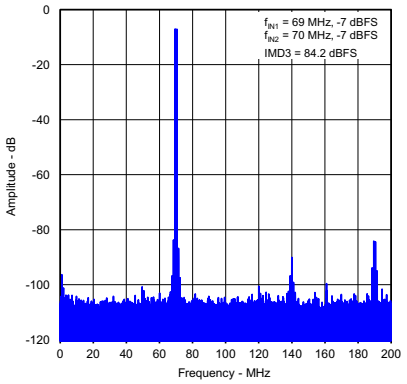


Figure 5-11. Two-Tone Intermodulation Distortion (FFT for 69MHz and 70MHz at –7 DBFS)

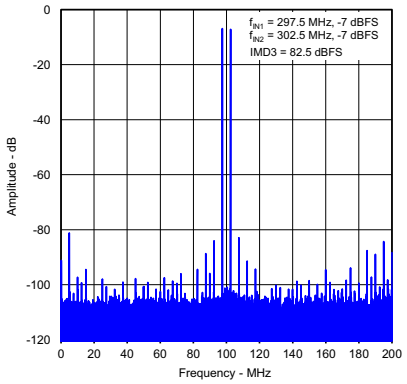


Figure 5-12. Two-Tone Intermodulation Distortion (FFT for 297.5MHz and 302.5MHz at –7 DBFS)

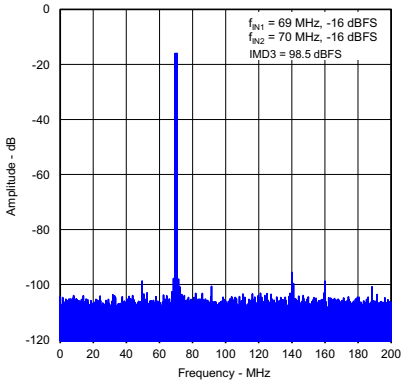


Figure 5-13. Two-Tone Intermodulation Distortion (FFT for 69MHz and 70MHz At –16 DBFS)

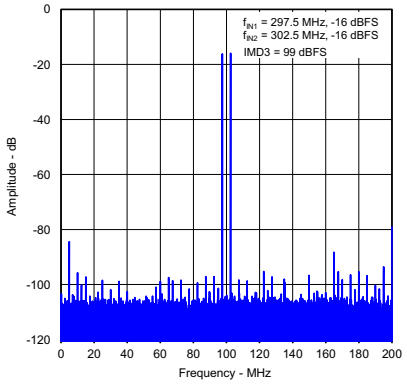


Figure 5-14. Two-Tone Intermodulation Distortion (FFT for 297.5MHz and 302.5MHz at –16 DBFS)

5.7 Typical Characteristics (continued)

At T_A = 25°C, sampling rate = 400MSPS, 50% clock duty cycle, $3V_{PP}$ differential sinusoidal clock, analog input amplitude = –1dBFS, AVDD5 = 5V, AVDD3 = 3.3V, and DVDD3 = 3.3V, unless otherwise noted.

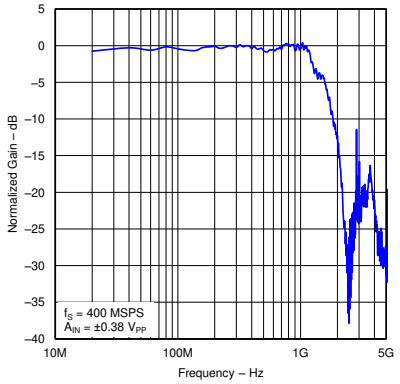


Figure 5-15. Normalized Gain Response vs Input Frequency

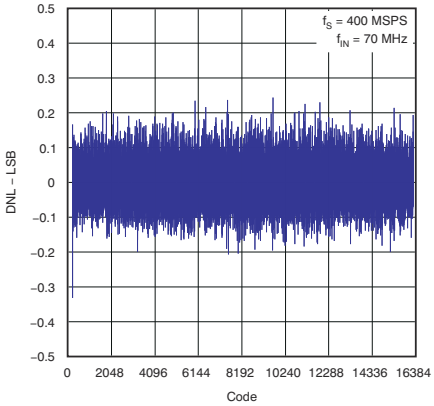


Figure 5-16. Differential Nonlinearity

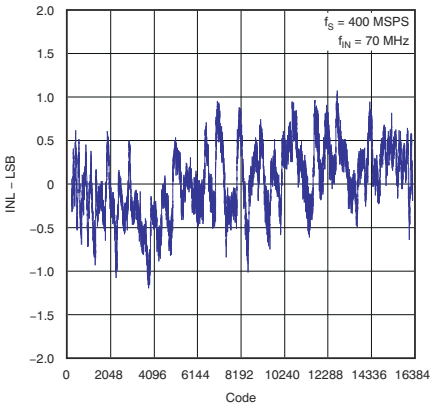


Figure 5-17. Integral Nonlinearity

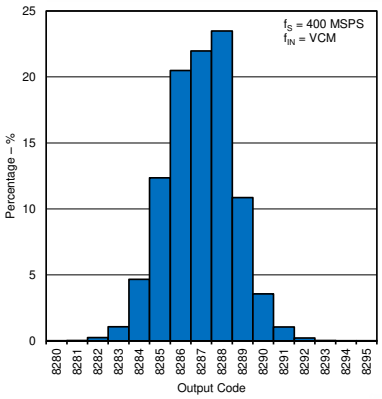


Figure 5-18. Noise Histogram With Inputs Shorted

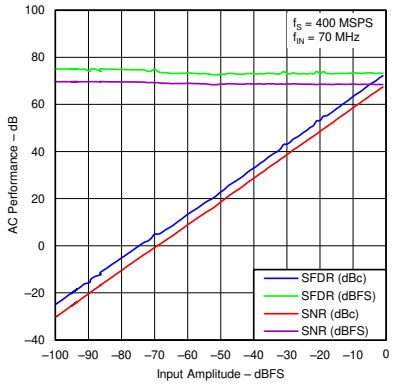


Figure 5-19. AC Performance vs Input Amplitude (70MHz Input Signal)

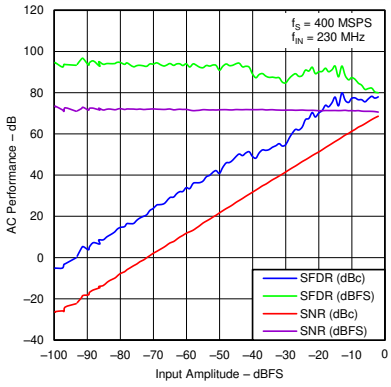


Figure 5-20. AC Performance vs Input Amplitude (230MHz Input Signal)

5.7 Typical Characteristics (continued)

At T_A = 25°C, sampling rate = 400MSPS, 50% clock duty cycle, $3V_{PP}$ differential sinusoidal clock, analog input amplitude = –1dBFS, AVDD5 = 5V, AVDD3 = 3.3V, and DVDD3 = 3.3V, unless otherwise noted.

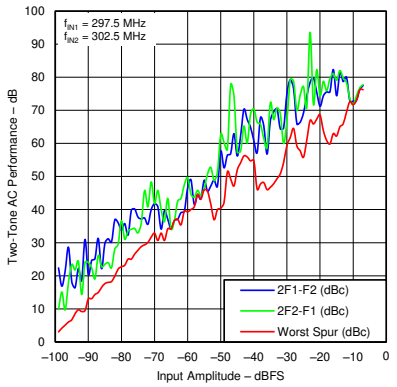


Figure 5-21. Two-Tone Performance vs Input Amplitude (F1 = 297.5MHz and F2 = 302.5MHz)

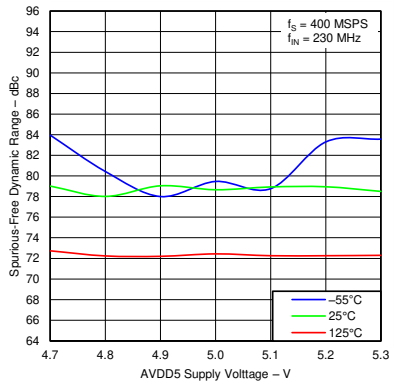


Figure 5-22. SFDR vs AVDD5 Over Temperature

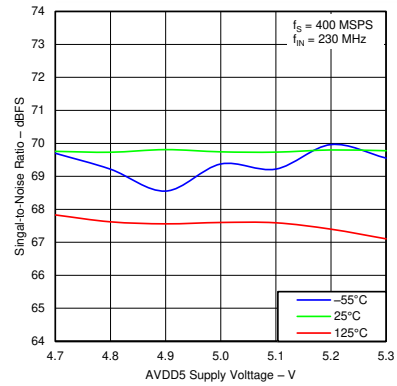


Figure 5-23. SNR vs AVDD5 Over Temperature

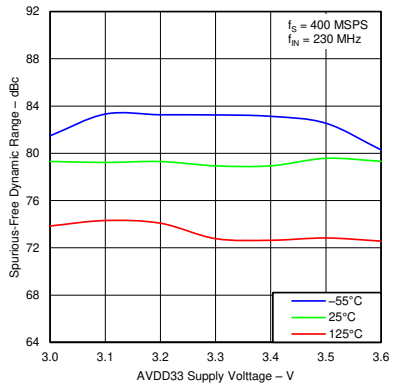


Figure 5-24. SFDR vs AVDD33 Over Temperature

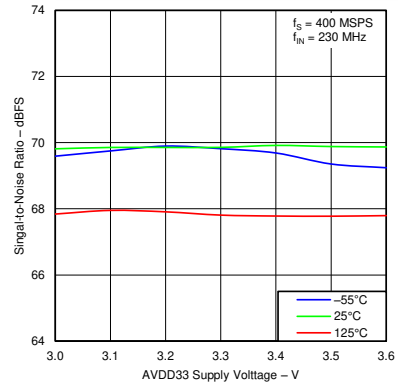


Figure 5-25. SNR vs AVDD33 Over Temperature

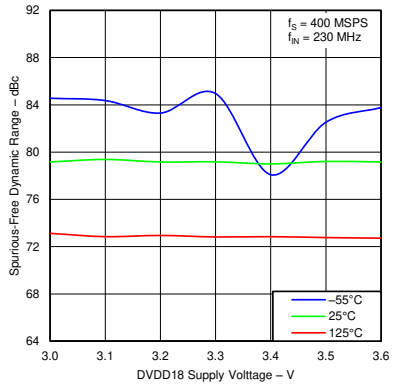


Figure 5-26. SFDR vs DVDD18 Over Temperature

5.7 Typical Characteristics (continued)

At T_A = 25°C, sampling rate = 400MSPS, 50% clock duty cycle, $3V_{PP}$ differential sinusoidal clock, analog input amplitude = –1dBFS, AVDD5 = 5V, AVDD3 = 3.3V, and DVDD3 = 3.3V, unless otherwise noted.

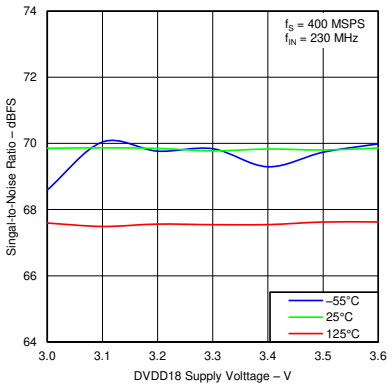


Figure 5-27. SNR vs DVDD18 Over Temperature

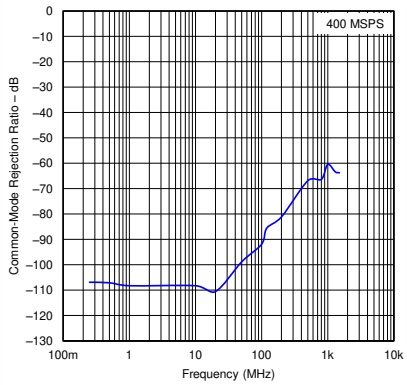


Figure 5-28. CMRR vs Common-Mode Input Frequency

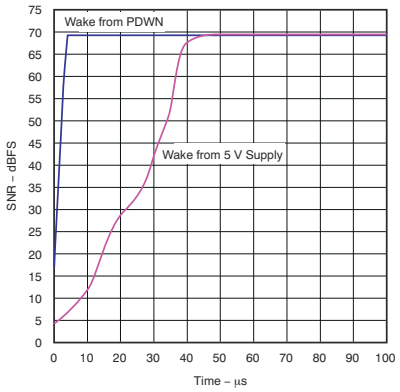


Figure 5-29. ADC Wakeup Time

6 Detailed Description

6.1 Overview

The ADS5474 is a 14-bit, 400MSPS, monolithic pipeline ADC. The bipolar analog core operates from 5V and 3.3V supplies, while the output uses a 3.3V supply to provide LVDS-compatible outputs. The rising edge of the external input clock initiates the conversion process. At the instant of the conversion process, the differential input signal is captured by the input track-and-hold (T&H), and the input sample converts sequentially by a series of lower resolution stages, with the outputs combined in a digital correction logic block. Both the rising and the falling clock edges propagate the sample through the pipeline every half clock cycle. The process results in a data latency of 3.5 clock cycles, after which the output data is available as a 14-bit parallel word, coded in offset binary format.

6.1.1 Input Configuration

The analog input for the ADS5474 consists of an analog pseudo-differential buffer followed by a bipolar transistor T&H. The analog buffer isolates the source driving the input of the ADC from any internal switching and presents a high impedance that is easy to drive at high input frequencies, compared to an ADC without a buffered input. The input common-mode is set internally through a 500Ω resistor, connected from 3.1V to each of the inputs (common-mode is ≅2.4V on 12- and 13-bit members of this family). The configuration results in a differential input impedance of 1kΩ.

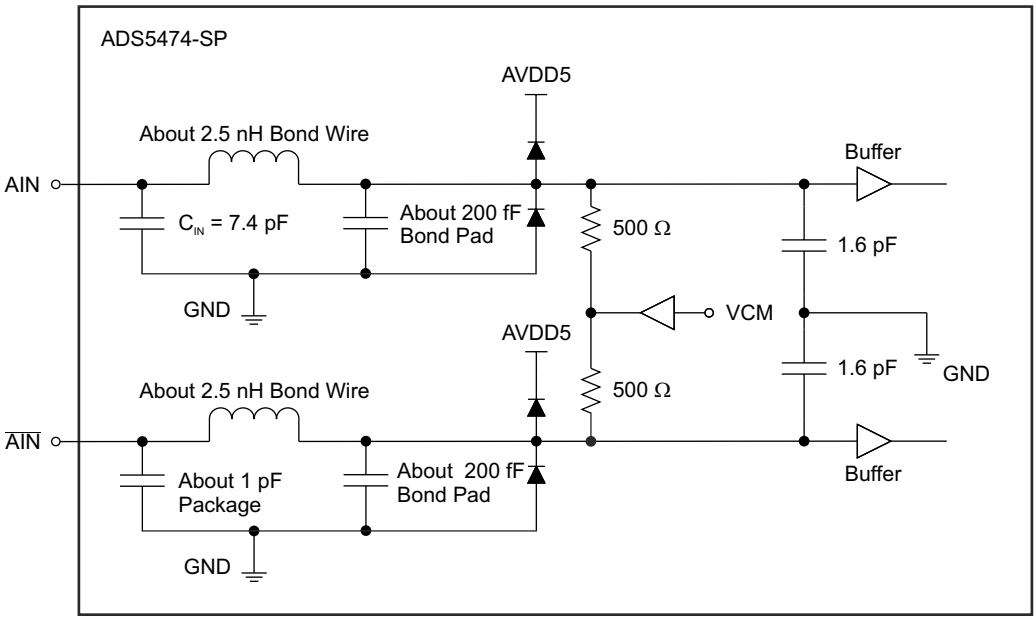


Figure 6-1. Analog Input Equivalent Circuit

For a full-scale differential input, each of the differential lines of the input signal (pins 16 and 17) swings symmetrically between (3.1V + 0.55V) and (3.1V – 0.55V). This range means that each input has a maximum signal swing of $1.1V_{PP}$ for a total differential input signal swing of $2.2V_{PP}$. Operation below $2.2V_{PP}$ is allowable, with the characteristics of performance versus input amplitude demonstrated in Figure 5-19 and Figure 5-20. For instance, for performance at $1.1V_{PP}$ rather than $2.2V_{PP}$, refer to the SNR and SFDR at –6dBFS (0dBFS = 2.2 V_{PP}). The maximum swing is determined by the internal reference voltage generator, eliminating the need for any external circuitry for this purpose.

Top performance for the ADS5474 performs is when the analog inputs are driven differentially. The circuit in Figure 6-2 shows one possible configuration using an RF transformer with termination either on the primary or on the secondary of the transformer. In addition, the configuration of the evaluation module is with two back-to-back transformers, further demonstrating good performance. If voltage gain is required, use a step-up transformer.

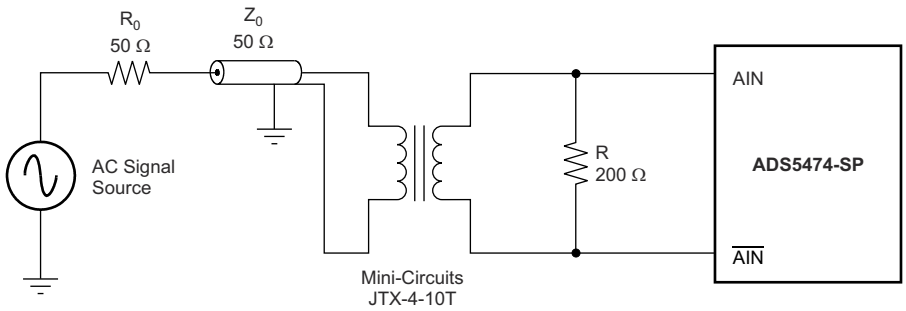


Figure 6-2. Converting a Single-Ended Input to a Differential Signal Using an RF Transformer

In addition to the transformer configurations, Texas Instruments offers a wide selection of single-ended operational amplifiers that can be selected depending on the application. Use an RF gain-block amplifier, such as THS9001, for high-input-frequency applications. Use the configuration shown in Figure 6-3 for large voltage gains at intermediate-frequencies in the range from 50MHz to 400MHz. Tune the component values for different intermediate frequencies. The example Figure 6-3 shows is located on the evaluation module and is tuned for an IF of 170MHz. More information regarding this configuration is found in the *ADS5474 EVM User's Guide* and the *THS9001 50MHz to 350MHz Cascadeable Amplifier* data sheet.

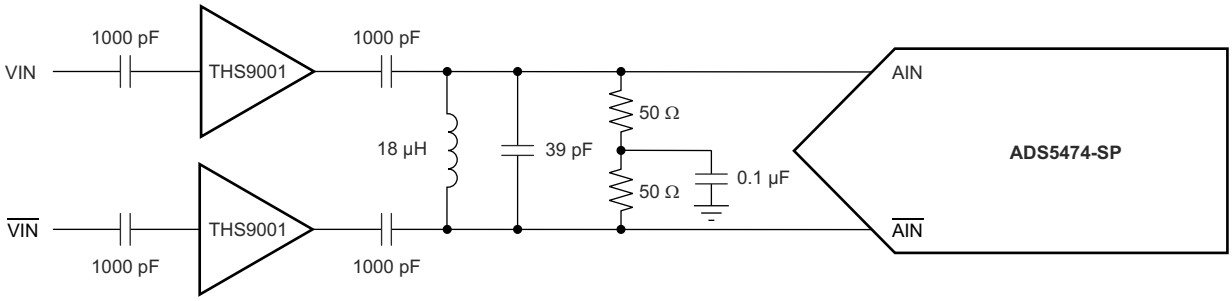


Figure 6-3. Using the THS9001 if Amplifier With the ADS5474

For applications requiring DC-coupling with the signal source, a differential input or differential output amplifier, such as the THS4509 (shown in Figure 6-4) provides good harmonic performance and low noise over a wide range of frequencies.

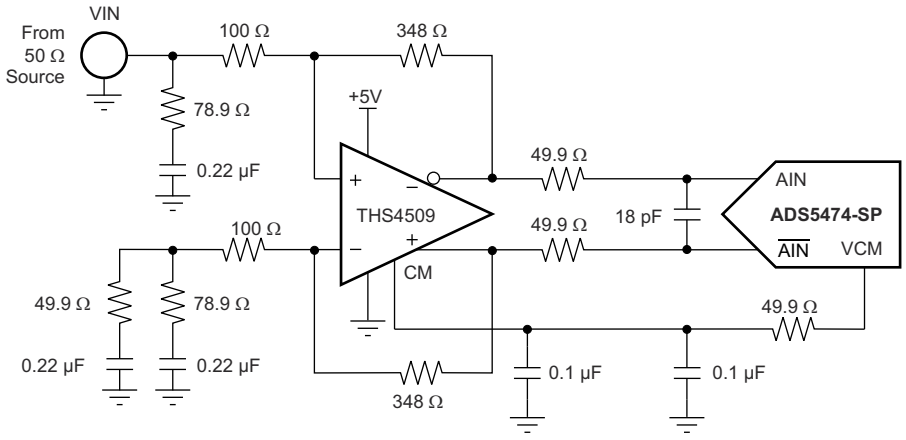


Figure 6-4. Using the THS4509 or THS4520 With the ADS5474

In this configuration, the THS4509 amplifier circuit provides 10dB of gain, converts the single-ended input to differential, and sets the proper input common-mode voltage to the ADS5474 using the VCM output pin of the ADC. The 50Ω resistors and 18pF capacitor between the THS4509 outputs and ADS5474 inputs (along with the input capacitance of the ADC) limit the bandwidth of the signal to approximately 70MHz (–3dB). Input

termination is accomplished through the 78.9Ω resistor and 0.22µF capacitor to ground, in conjunction with the input impedance of the amplifier circuit.

A 0.22µF capacitor and 49.9Ω resistor are inserted to ground across the 78.9Ω resistor and 0.22µF capacitor on the alternate input to balance the circuit. Gain is a function of the source impedance, termination, and 348Ω feedback resistor. See the *THS4509 Wideband, Low-Noise, Low-Distortion, Fully-Differential Amplifier* data sheet for further component values to set proper 50Ω termination for other common gains.

Because the ADS5474 recommended input common-mode voltage is 3.1V, the THS4509 operates from a single power-supply input with V_{S+} = 5V and $V_{S–}$ = 0V (ground). This configuration has the potential to slightly exceed the recommended output voltage from the THS4509 of 3.6V due to the ADC input common-mode of 3.1V and the +0.55V full-scale signal. Exceeding the voltage does not harm the THS4509 but can result in degradation in the harmonic performance of the THS4509.

An amplifier with a wider recommended output voltage range is the THS4520, which is optimized for low noise and low distortion in the range of frequencies up to ≅20MHz. Applications that are not sensitive to harmonic distortion can consider either device at higher frequencies.

6.1.2 Clock Inputs

Drive the ADS5474 clock input with either a differential clock signal or a single-ended clock input. The characterization of the ADS5474 is typically performed with a $3V_{PP}$ differential clock, but the ADC perfoRMS well with a differential clock amplitude down to ≅$0.5V_{PP}$. The clock amplitude becomes more of a factor in performance as the analog input frequency increases. In low-input-frequency applications, where jitter may not be a big concern, the use of a single-ended clock can save cost and board space without much performance tradeoff. When clocked with this configuration, TI recommends connecting $\overline{CLK}$ to ground with a 0.01µF capacitor, while CLK is AC-coupled with a 0.01µF capacitor to the clock source, as shown in Figure 6-6.

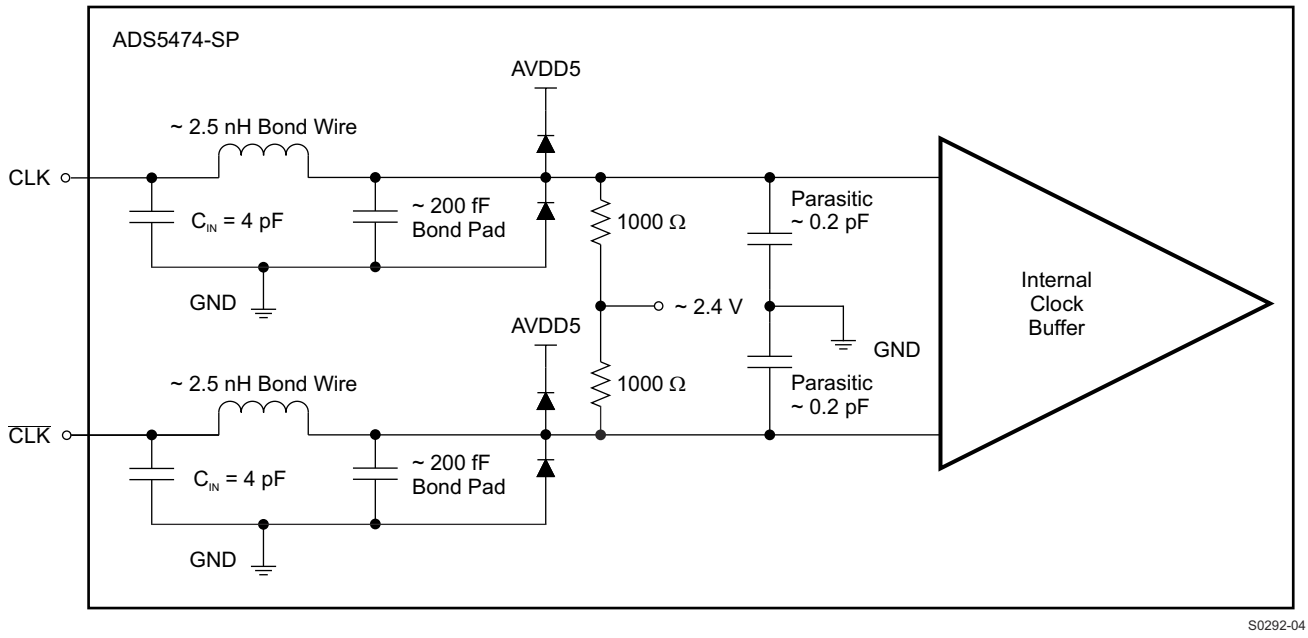


Figure 6-5. Clock Input Circuit

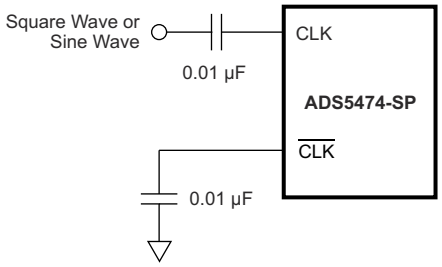


Figure 6-6. Single-Ended Clock

For jitter-sensitive applications, the use of a differential clock has some advantages at the system level. The differential clock allows for common-mode noise rejection at the printed circuit board (PCB) level. With a differential clock, the signal-to-noise ratio of the ADC is better for jitter-sensitive, high-frequency applications because the board level clock jitter is best.

Larger clock amplitude levels are recommended for high analog input frequencies or slow clock frequencies. In the case of a sinusoidal clock, larger amplitudes result in higher clock slew rates and reduces the impact of clock noise on jitter. At high analog input frequencies, the sampling process is sensitive to jitter. At slow clock frequencies, a small amplitude sinusoidal clock has a lower slew rate and can create jitter-related SNR degradation. Figure 6-7 demonstrates a recommended method for converting a single-ended clock source into a differential clock. The method is similar to the configuration found on the evaluation board and was used for much of the characterization. See the *Clocking High Speed Data Converters* analog design journal for more details.

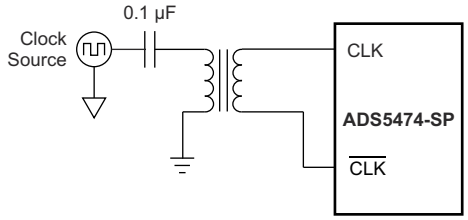


Figure 6-7. Differential Clock

The common-mode voltage of the clock inputs is set internally to 2.4V using internal 1kΩ resistors. TI recommends using AC coupling. If AC coupling is not possible, the ADS5474 features good tolerance to clock common-mode variation. Additionally, the internal ADC core uses both edges of the clock for the conversion process. An excellent choice is a 50% duty-cycle clock signal.

The ADS5474 is capable of achieving 69.2dBFS SNR at 350MHz of analog input frequency. To achieve the SNR at 350MHz, verify that the clock source RMS jitter is at least 144fs for the total RMS jitter to be 177fs. A summary of maximum recommended RMS clock jitter as a function of analog input frequency is provided in Table 6-1. Equation 1 and Equation 2 used in creating the table are below.

Table 6-1. Recommended RMS Clock Jitter

INPUT FREQUENCY (MHz)	MEASURED SNR (dBc)	TOTAL JITTER (fsec RMS)	MAXIMUM CLOCK JITTER (fsec RMS)
30	69.3	1818	1816
70	69.1	798	791
130	69.1	429	417
230	68.8	251	229
350	68.2	177	144
450	67.4	151	110
750	65.6	111	42
1000	63.7	104	14

Use Equation 1 and Equation 2 to estimate the required clock source jitter.

$$\text{SNR(dBc)} = -20 \times \log_{10}(2 \times \pi \times f_{IN} \times j_{TOTAL}) \quad (1)$$

$$j_{TOTAL} = \left[j_{ADC}{}^2 + j_{CLOCK}{}^2 \right]^{\frac{1}{2}} \quad (2)$$

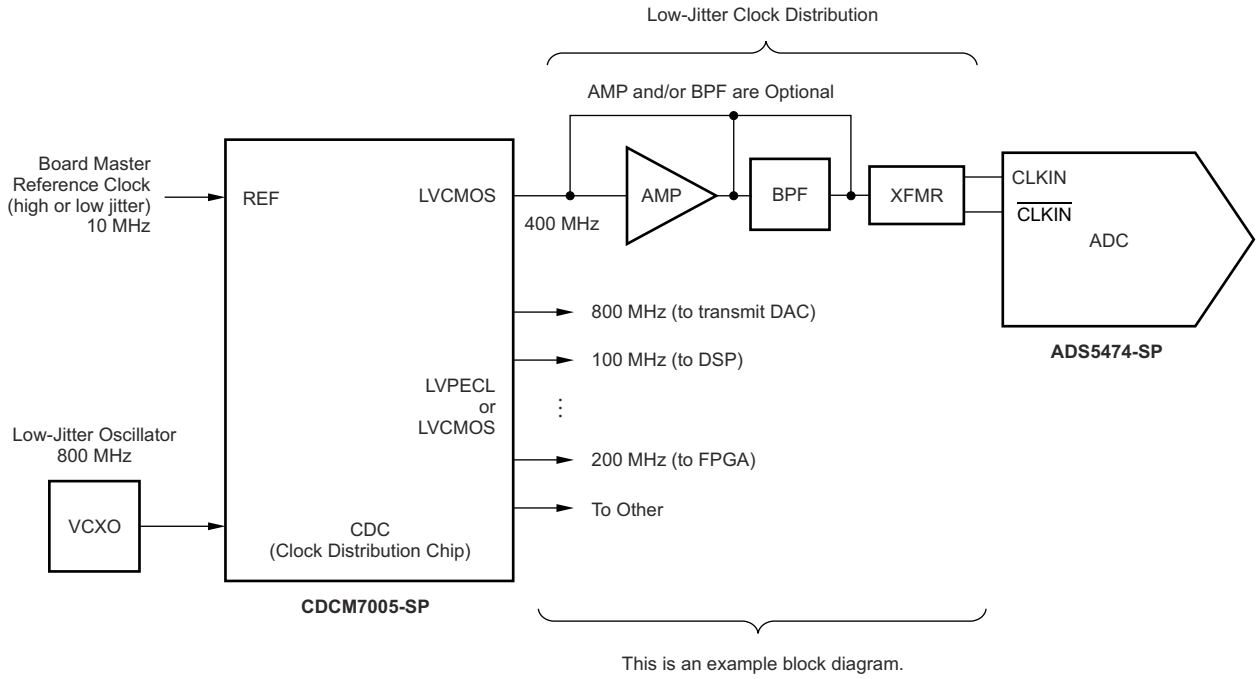
where

- j_{TOTAL} = RMS summation of the clock and ADC aperture jitter
- f_{IN} = analog input frequency
- j_{ADC} = ADC internal aperture jitter, located in the data sheet
- j_{CLOCK} = RMS jitter of the clock at the clock input pins to the ADC

The SNR is a strong function of the analog input frequency, not the clock frequency. The slope of the clock source edges can have a mild impact on SNR as well and is not taken into account for these estimates. For this reason, maximizing clock source amplitudes at the ADC clock inputs is recommended, though not required (faster slope is desirable for jitter-related SNR). For more information on clocking high-speed ADCs, see *Implementing a CDC7005 Low Jitter Clock Solution For High-Speed, High-IF ADC Devices* application note. Recommended clock distribution chips (CDCs) are the TI CDC7005, the CDCM7005-SP and CDCE72010.

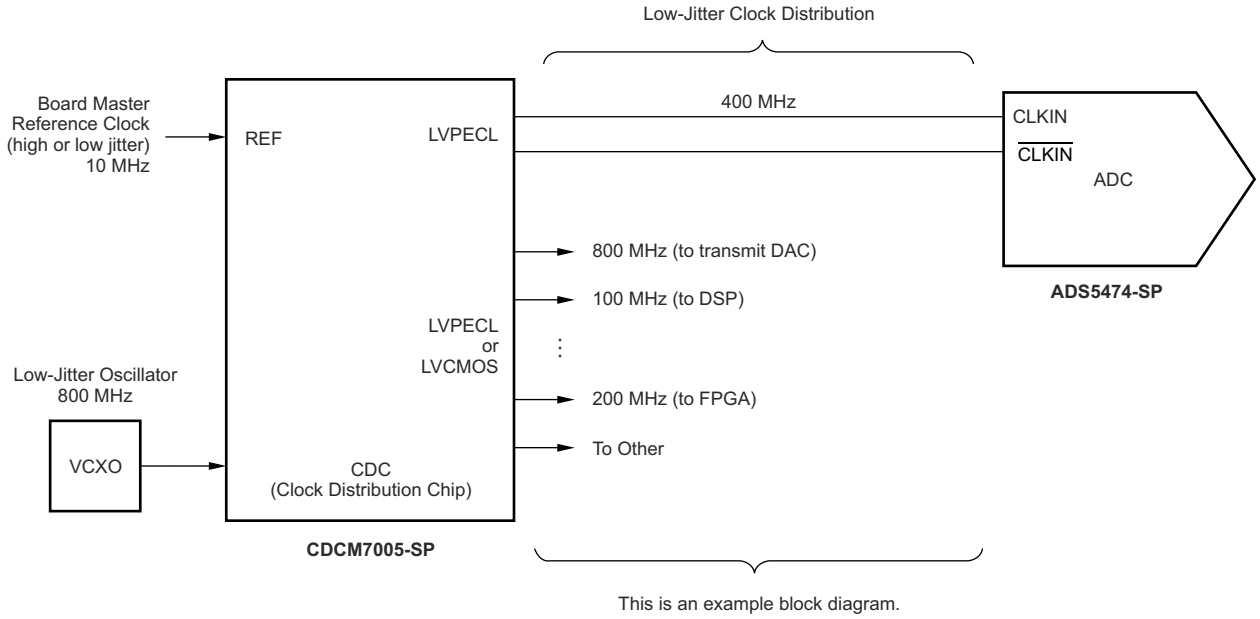
Depending on the jitter requirements, a band pass filter (BPF) is sometimes required between the CDC and the ADC. If the insertion loss of the BPF causes the clock amplitude to be too low for the ADC, or the clock source amplitude is too low to begin with, place an inexpensive amplifier between the CDC and the BPF.

Figure 6-8 represents a scenario where an LVCMOS single-ended clock output is used from a TI CDCM7005-SP with the clock signal path optimized for maximum amplitude and minimum jitter. This type of conditioning can be well-suited for use with greater than 150MHz of input frequency. The jitter of this setup is difficult to estimate and requires a careful phase noise analysis of the clock path. The BPF (and possibly a low-cost amplifier because of insertion loss in the BPF) can improve the jitter between the CDC and ADC when the jitter provided by the CDC is still not adequate. The total jitter at the CDCM7005-SP output depends largely on the phase noise of the VCXO selected, as well as the CDCM7005-SP, and typically has 50 to 100fs of RMS jitter. If the user determines that the jitter from the CDCM7005-SP with a VCXO is sufficient without further conditioning, clocking the ADS5474 directly from the CDCM7005-SP using differential LVPECL outputs is possible, as illustrated in Figure 6-9 (see the *CDCM7005-SP 3.3V High Performance Clock Synchronizer and Jitter Cleaner* data sheet for the exact schematic). This scenario can be an excellent choice for less than 150MHz of input frequency where jitter is not as critical. TI recommends carefully analyzing the required jitter before determining the proper approach.



Consult the *CDCM7005 3.3V High Performance Clock Synchronizer and Jitter Cleaner* data sheet for proper schematic and specifications regarding allowable input and output frequency and amplitude ranges.

Figure 6-8. Best Jitter Clock Circuit



Consult the *CDCM7005 3.3V High Performance Clock Synchronizer and Jitter Cleaner* data sheet for proper schematic and specifications regarding allowable input and output frequency and amplitude ranges.

Figure 6-9. Acceptable Jitter Clock Circuit

6.1.3 Digital Outputs

The ADC provides 14 LVDS-compatible, offset binary data outputs (D13 to D0; D13 is the MSB and D0 is the LSB), a data-ready signal (DRY), and an over-range indicator (OVR). TI recommends using the DRY signal to

capture the output data of the ADS5474. DRY is source-synchronous to the DATA/OVR outputs and operates at the same frequency, creating a half-rate DDR interface that updates data on both the rising and falling edges of DRY. TI recommends minimizing the capacitive loading on the digital outputs. Higher capacitance shortens the data-valid timing window. The values given for timing (see Figure 5-2) are obtained with a measured 10pF parasitic board capacitance to ground on each LVDS line (or 5pF differential parasitic capacitance). When setting the time relationship between DRY and DATA at the receiving device, TI recommends maximizing setup time, but this time partially depends on the setup and hold times of the device receiving the digital data (such as an FPGA or Field Programmable Field Array). Because DRY and DATA are coincident, TI recommends delaying either DRY or DATA to maximize setup time.

Referencing Figure 5-2, the polarity of DRY with respect to the sample N data output transition is undetermined because of the unknown Startup logic level of the clock divider that generates the DRY signal (DRY is a frequency divide-by-two of CLK). Either the rising or the falling edge of DRY coincide with sample N and the polarity of DRY can invert when power is cycled off and on, or when the power-down pin cycle. Data capture from the transition and not the polarity of DRY is recommended, but not required. If the synchronization of multiple ADS5474 devices is required, it can be necessary to use a form of the CLKIN signal rather than DRY to capture the data.

The DRY frequency is identical on the ADS5474 and ADS5463 (where DRY equals ½ the CLK frequency), but different than it is on the pin-similar ADS5444 (where DRY equals the CLK frequency). The LVDS outputs all require an external 100Ω load between each output pair to meet the expected LVDS voltage levels. For long trace lengths, it may be necessary to place a 100Ω load on each digital output as close to the ADS5474 as possible and another 100Ω differential load at the end of the LVDS transmission line to provide matched impedance and avoid signal reflections. The effective load in this case reduces the LVDS voltage levels by half.

The OVR output equals a logic high when the 14-bit output word attempts to exceed either all 0s or all 1s. This flag is provided as an indicator that the analog input signal exceeded the full-scale input limit of approximately $2.2V_{PP}$ (± gain error). The OVR indicator is provided for systems that use gain control to keep the analog input signal within acceptable limits.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Power Supply Recommendations

The ADS5474 uses three power supplies. For the analog portion of the design, a 5V and 3.3V supply (AVDD5 and AVDD3) are used, while the digital portion uses a 3.3V supply (DVDD3). The use of low-noise power supplies with adequate decoupling is recommended. Linear supplies are preferred to switched supplies; switched supplies tend to generate more noise components that can be coupled to the ADS5474. The user may be able to supply power to the device with a less-than-ideal supply and still achieve good performance. It is not possible to make a single recommendation for every type of supply and level of decoupling for all systems. The power consumption of the ADS5474 does not change substantially over clock rate or input frequency as a result of the architecture and process.

Because there are two diodes connected in reverse between AVDD3 and DVDD3 internally, a power-up sequence is recommended. When there is a delay in power up between these two supplies, the one that lags could have current sinking through an internal diode before it powers up. The sink current can be large or small depending on the impedance of the external supply and could damage the device or affect the supply source.

The best power up sequence is one of the following options (regardless of when AVDD5 powers up):

1. Power up both AVDD3 and DVDD3 at the same time (best scenario), OR
2. Keep the voltage difference less than 0.8V between AVDD3 and DVDD3 during the power up (0.8V is not a hard specification - a smaller delta between supplies is safer).

If the above sequences are not practical then the sink current from the supply needs to be controlled or protection added externally. The max transient current (on the order of µs) for DVDD3 or AVDD3 pin is 500mA to avoid potential damage to the device or reduce its lifetime.

Values for analog and clock input given in the *Section 5.1* are valid when the supplies are on. When the power supplies are off and the clock or analog inputs are still alive, the input voltage and current needs to be limited to avoid device damage. If the ADC supplies are off, the max/min continuous DC voltage is ±0.95V and max DC current is 20mA for each input pin (clock or analog), relative to ground.

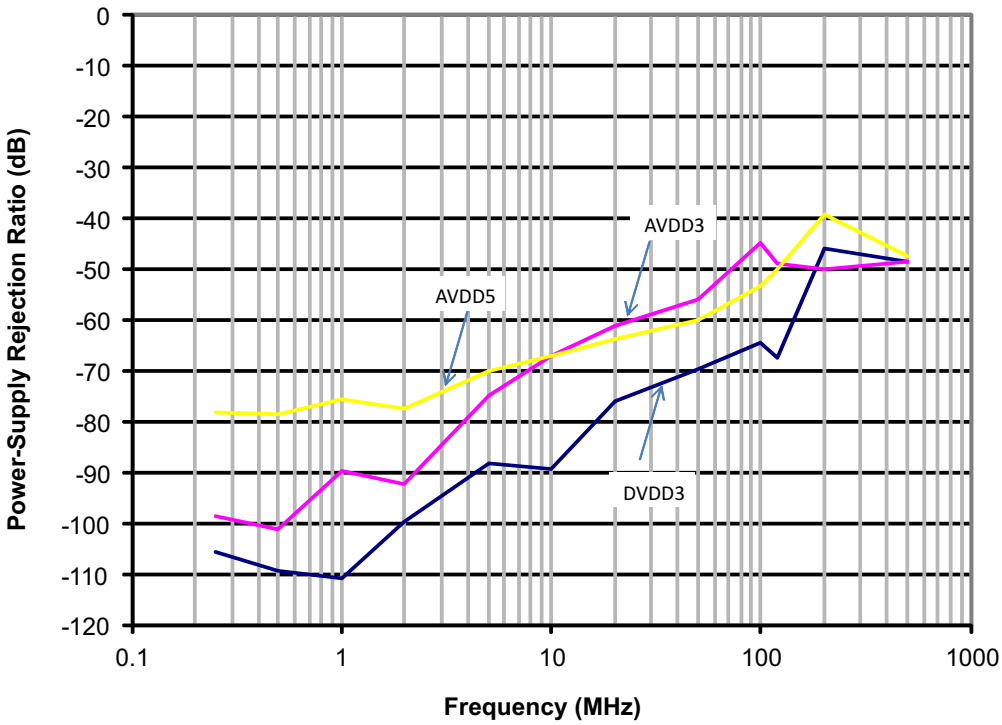


Figure 7-1. PSRR vs Supply Injected Frequency

8 Device and Documentation Support

8.1 Device Support

8.1.1 Definition of Specifications

Analog Bandwidth The analog input frequency at which the power of the fundamental is reduced by 3dB with respect to the low-frequency value.

Aperture Delay The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs.

Aperture Uncertainty (Jitter) The sample-to-sample variation in aperture delay.

Clock Pulse Duration/Duty Cycle The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse duration) to the period of the clock signal, expressed as a percentage.

Differential Nonlinearity (DNL) An ideal ADC exhibits code transitions at analog input values spaced exactly 1LSB apart. DNL is the deviation of any single step from this ideal value, measured in units of LSB.

Common-Mode Rejection Ratio (CMRR) CMRR measures the ability to reject signals that are presented to both analog inputs simultaneously. The injected common-mode frequency level is translated into dBFS, the spur in the output FFT is measured in dBFS, and the difference is the CMRR in dB.

Effective Number of Bits (ENOB) ENOB is a measure in units of bits of converter performance as compared to the theoretical limit based on quantization noise:

$$\text{ENOB} = [\text{SINAD} - 1.76] \div 6.02 \tag{3}$$

Gain Error Gain error is the deviation of the ADC actual input full-scale range from its ideal value, given as a percentage of the ideal input full-scale range.

Integral Nonlinearity (INL) INL is the deviation of the ADC transfer function from a best-fit line determined by a least-squares curve fit of that transfer function. The INL at each analog input value is the difference between the actual transfer function and this best-fit line, measured in units of LSB.

Offset Error Offset error is the deviation of output code from mid-code when both inputs are tied to common-mode.

Power-Supply Rejection Ratio (PSRR) PSRR is a measure of the ability to reject frequencies present on the power supply. The injected frequency level is translated into dBFS, the spur in the output FFT is measured in dBFS, and the difference is the PSRR in dB. The measurement calibrates out the benefit of the board supply decoupling capacitors.

Signal-to-Noise Ratio (SNR) SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and in the first five harmonics.

$$\text{SNR} = 10\log_{10}\frac{P_S}{P_N} \tag{4}$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Signal-to-Noise and Distortion (SINAD) SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$\text{SINAD} = 10\log_{10}\frac{P_S}{P_N + P_D} \tag{5}$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Temperature Drift Temperature drift (with respect to gain error and offset error) specifies the change from the value at the nominal temperature to the value at T_{MIN} or T_{MAX}. It is computed as the maximum variation the parameters over the whole temperature range divided by $T_{MIN} – T_{MAX}$.

Total Harmonic Distortion (THD) THD is the ratio of the power of the fundamental (P_S) to the power of the first five harmonics (P_D).

$$\text{THD} = 10\log_{10}\frac{P_S}{P_D} \quad (6)$$

THD is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion (IMD3) IMD3 is the ratio of the power of the fundamental (at frequencies f_1, f_2) to the power of the worst spectral component at either frequency $2f_1 – f_2$ or $2f_2 – f_1$). IMD3 is given in units of either dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

8.2 Documentation Support

8.2.1 Related Documentation

- Texas Instruments, *50MHz to 750MHz Cascadeable Amplifier* data sheet
- Texas Instruments, *ADS5440/44/63/74 EVM* user's guide
- Texas Instruments, *CDCM7005 3.3V High Performance Clock Synchronizer and Jitter Cleaner* data sheet
- Texas Instruments, *CDCM7005-SP 3.3V High Performance Rad-Tolerant Class V, Clock Synchronizer and Jitter Cleaner* data sheet
- Texas Instruments, *Clocking high-speed data converters* analog design journal
- Texas Instruments, *Implementing a CDC7005 Low Jitter Clock Solution For High-Speed, High-IF ADC Devices* application note
- Texas Instruments, *THS4509 Wideband, Low-Noise, Low-Distortion, Fully-Differential Amplifier* data sheet

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.5 Trademarks

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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 2013) to Revision B (November 2025) — **Page**

- Updated title from: Class V, 14-BIT 400-MSPS ANALOG-TO-DIGITAL CONVERTER to: ADS5474-SP Class V, 14-bit, 400MSPS Analog-to-Digital Converter ... 1
- Updated the numbering format for tables, figures, and cross-references throughout the document ... 1
- Updated Pin Configuration figure pins 1, 22, 43, and 64 from: AGND to: GND ... 3
- Moved *Pin Configuration and Functions* section before *Specifications* section ... 3
- Added *ESD Ratings* section ... 5
- Moved ESD data from *Absolute Maximum Ratings* section to *ESD Ratings* section ... 5
- Moved *Recommended Operating Conditions* section after *ESD Ratings* section ... 5
- Updated title from: Thermal Characteristics to: Thermal Information ... 6
- Moved *Thermal Information* section after *Recommended Operating Conditions* section ... 6
- Updated $R_{\theta JA}$ from: 21.81°C/W to: 19°C/W ... 6
- Updated $R_{\theta JC}$ from: 0.849°C/W to: 1.8°C/W ... 6
- Changed the typical value for *Input Capacitance* under analog inputs from: 7.4 pF to: 2.8pF ... 6
- Moved Operating Life Derating Chart, Electromigration Fail Mode from *Thermal Characteristics* section to *Electrical Characteristics* section ... 6
- Moved Timing Diagram to *Timing Characteristics* section ... 9
- Updated section title from Application Information to Detailed Description ... 16
- Updated section title from Theory of Operation to Overview ... 16
- Changed capacitance in Figure 6-1 to "about 1pF package" ... 16
- Changed (where DRY equals the CLK frequency) to (where DRY equals ½ the CLK frequency) in *Digital Outputs* ... 21
- Added *Application and Implementation* section ... 23
- Updated title from Power Supplies to Power Supply Recommendations ... 23
- Moved *Power Supply Recommendations* section to *Application and Implementation* section ... 23
- Moved Electrostatic Discharge Caution to *Device and Documentation Support* section ... 25

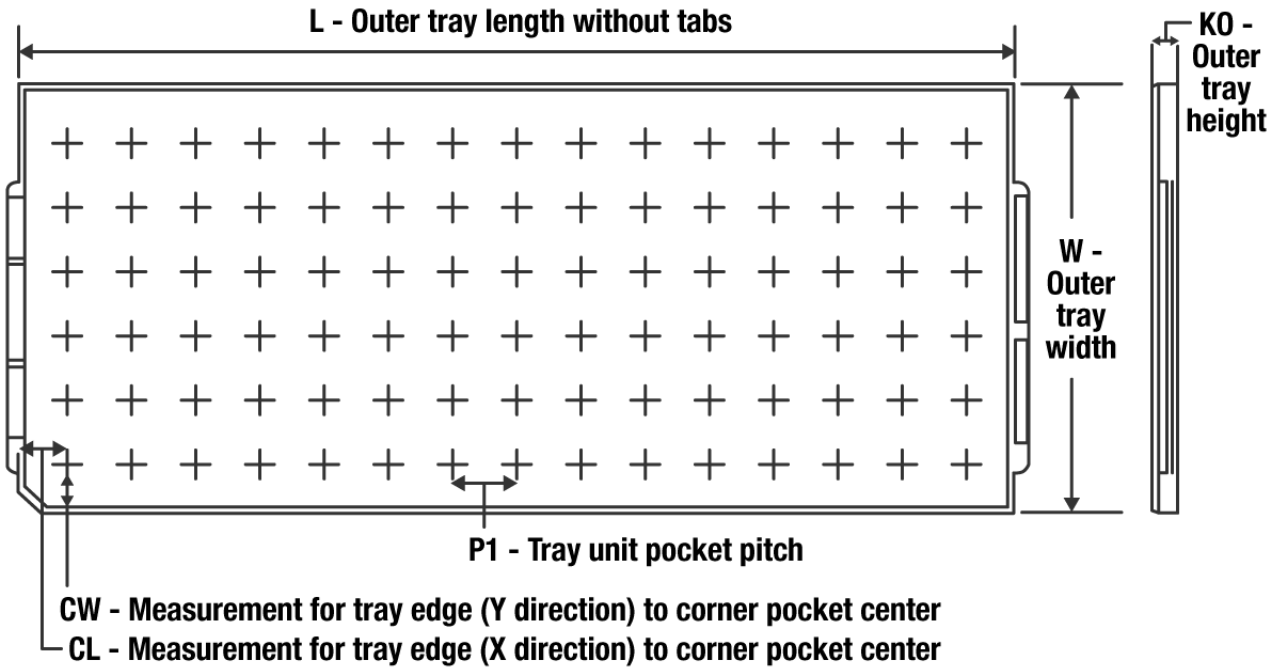
Changes from Revision * (September 2013) to Revision A (December 2013) — **Page**

- Added bullet Engineering evaluation (/EM) to *Features* list ... 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
ADS5474HFG/EM	HFG	CFP	84	1	2 x 5	150	315	135.9	7620	57	43.5	39.45

DATA BOOK
PACKAGE OUTLINE

SUBSTRATE EXAMPLE
4041137

DRAFTER:	ANIS FAUZI	DATE:	07/10/2025
DESIGNER:		DATE:	
CHECKER:	K. SINCERBOX	DATE:	07/10/2025
ENGINEER:	LI JIANG	DATE:	07/10/2025
APPROVED:	NICK CHU	DATE:	07/10/2025
RELEASED:	ANIS FAUZI	DATE:	07/10/2025
TEMPLATE INFO:	EDGE# 4218519	DATE:	03/20/2013

DIMENSIONS IN MILLIMETERS

TEXAS INSTRUMENTS
SEMICONDUCTOR OPERATIONS

CODE IDENTITY NUMBER 01295

ePOD, HFG0084B / CFP,
84 PIN, 0.635 MM PITCH

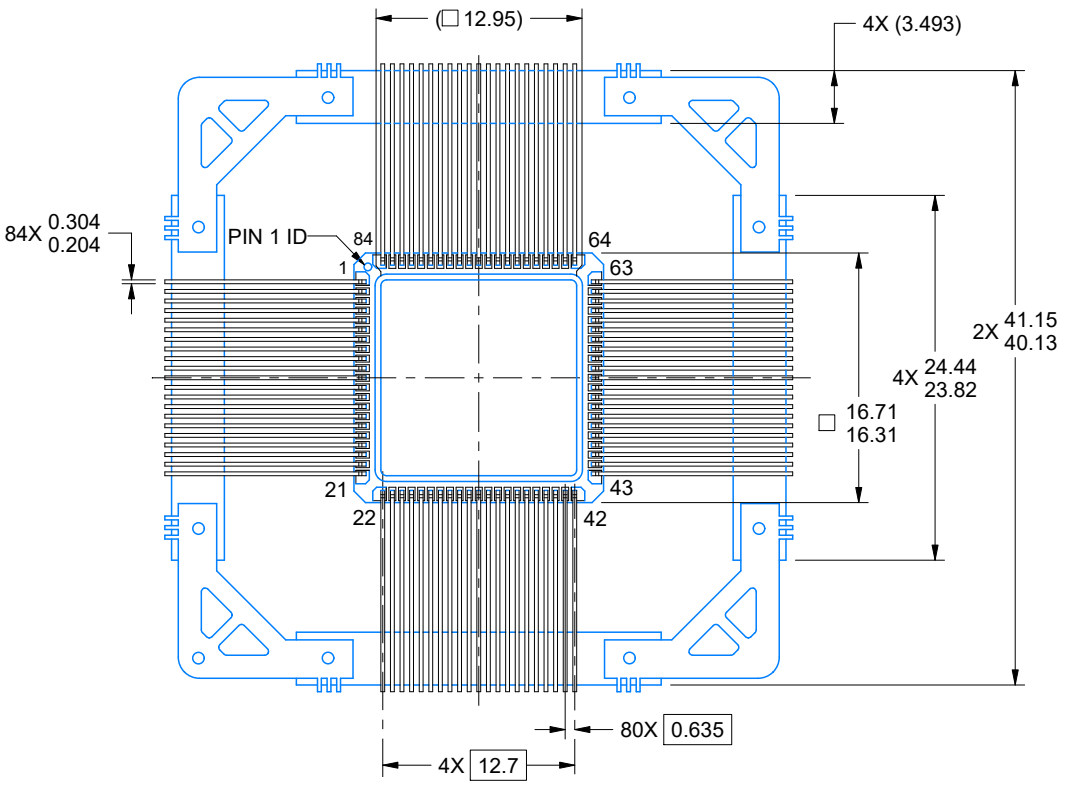
SCALE	SIZE		REV	PAGE
2X	A	4231974	A	1 OF 3

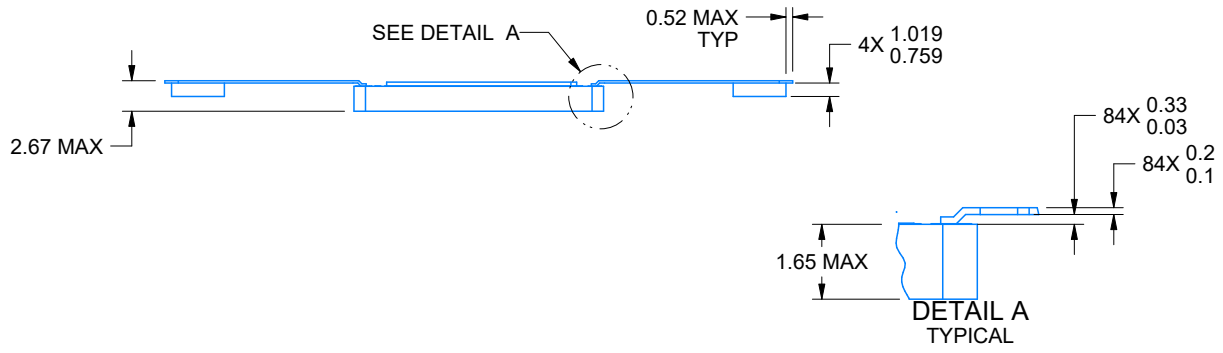
HFG0084B

PACKAGE OUTLINE

CFP - 2.67 mm max height

CFP





4231974/A 07/2025

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid.
4. The lid and the heat sink are connected to ground leads.
5. The leads are gold plated and can be solder dipped.

REVISIONS

REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTSMAN
A	RELEASE NEW DRAWING	2213474	07/10/2025	LI JIANG / ANIS FAUZI

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Last updated 10/2025