AM26C32-EP
QUADRUPLE DIFFERENTIAL LINE RECEIVER

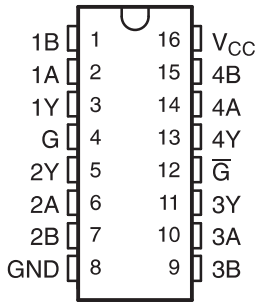
SLLS870–NOVEMBER 2007

FEATURES

- **Controlled Baseline**
  - **One Assembly**
  - **One Test Site**
  - **One Fabrication Site**
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree** (1)
- **Meets or Exceeds the Requirements of ANSI TIA/EIA-422-B, TIA/EIA-423-B, and ITU Recommendation V.10 and V.11**
- **Low Power, I_{CC} = 10 mA Typ**
- **±7 V Common-Mode Range With ±200 mV Sensitivity**
- **Input Hysteresis . . . 60 mV Typ**
- **t_{pd} = 17 ns Typ**
- **Operates From a Single 5 V Supply**
- **3-State Outputs**
- **Input Fail-Safe Circuitry**
- **Improved Replacements for AM26LS32**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

AM26C32... D PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The AM26C32 is a quadruple differential line receiver for balanced or unbalanced digital data transmission. The enable function is common to all four receivers and offers a choice of active-high or active-low input. The 3-state outputs permit connection directly to a bus-organized system. Fail-safe design specifies that if the inputs are open, the outputs always are high.

The AM26C32 devices are manufactured using a BiCMOS process, which is a combination of bipolar and CMOS transistors. This process provides the high voltage and current of bipolar with the low power of CMOS to reduce the power consumption to about one-fifth that of the standard AM26LS32, while maintaining ac and dc performance.

The AM26C32 is characterized for operation over the extended temperature range of –55°C to 125°C.

ORDERING INFORMATION(1)

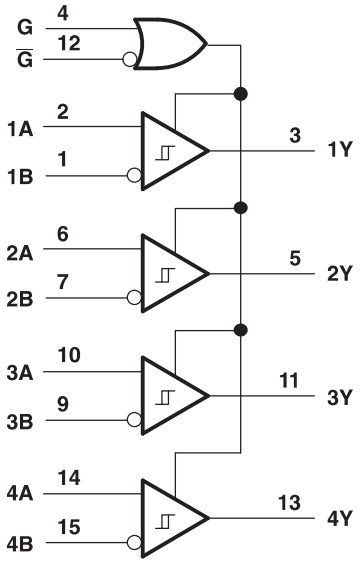
T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOIC – D	Reel of 2500	AM26C32MDREP	26C32EP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

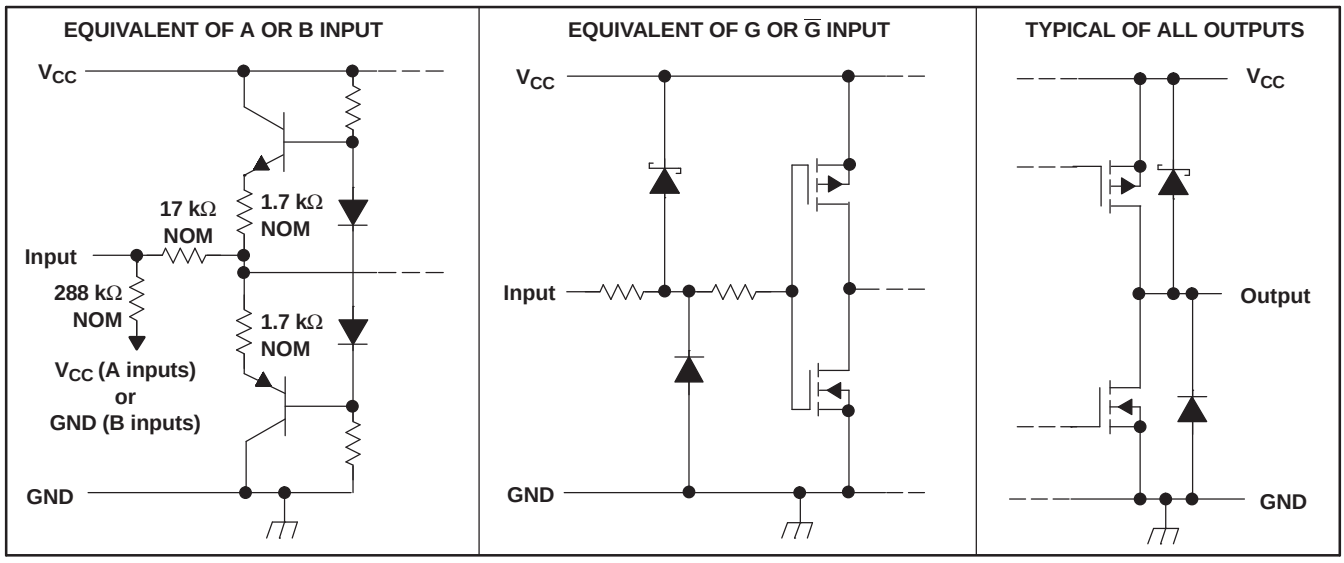
FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUT	ENABLES		OUTPUT Y
	G	$\overline{G}$	
$V_{ID} \geq V_{IT+}$	H	X	H
	X	L	H
$V_{IT-} < V_{ID} < V_{IT+}$	H	X	?
	X	L	?
$V_{ID} \leq V_{IT-}$	H	X	L
	X	L	L
X	L	H	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



SCHEMATICS



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)			7	V
V_I	Input voltage range	A or B inputs	–11	14	V
		G or $\overline{G}$ inputs	–0.5	V_{CC} + 0.5	V
V_{ID}	Differential input voltage range		–14	14	V
V_O	Output voltage range		–0.5	V_{CC} + 0.5	V
I_O	Output current			±25	mA
θ_{JA}	Package thermal impedance(3)(4)	D package		73	°C/W
		PW package		108	
T_J	Operating virtual junction temperature			150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential output voltage, V_{OD}, are with respect to network GND. Currents into the device are positive and currents out of the device are negative.
(3) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_{IC}	Common-mode input voltage			±7	V
I_{OH}	High-level output current			–6	mA
I_{OL}	Low-level output current			6	mA
T_A	Operating free-air temperature	–55		125	°C

ELECTRICAL CHARACTERISTICS

over recommended ranges of V_{CC}, V_{IC}, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Differential input high-threshold voltage	V_O = V_{OH} (min),	V_{IC} = –7 V to 7 V			0.2	V
		I_{OH} = –440 µA	V_{IC} = 0 to 5.5 V			0.1	
$V_{IT–}$	Differential input low-threshold voltage	V_O = 0.45 V,	V_{IC} = –7 V to 7 V	–0.2(2)			V
		I_{OL} = 8 mA	V_{IC} = 0 to 5.5 V	–0.1(2)			
V_{hys}	Hysteresis voltage (V_{IT+} – $V_{IT–}$)				60		mV
V_{IK}	Enable input clamp voltage	V_{CC} = 4.5 V,	I_I = –18 mA			–1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = –6 mA	3.8			V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV,	I_{OL} = 6 mA		0.2	0.3	V
I_{OZ}	Off-state (high-impedance state) output current	V_O = V_{CC} or GND			±0.5	±5	µA
I_I	Line input current	V_I = 10 V,	Other input at 0 V			1.5	mA
		V_I = –10 V,	Other input at 0 V			–2.5	
I_{IH}	High-level enable current	V_I = 2.7 V				20	µA
I_{IL}	Low-level enable current	V_I = 0.4 V				–100	µA
r_I	Input resistance	One input to ground		12	17		kΩ
I_{CC}	Supply current	V_{CC} = 5.5 V			10	15	mA

(1) All typical values are at V_{CC} = 5 V, V_{IC} = 0, and T_A = 25°C.
(2) The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage.

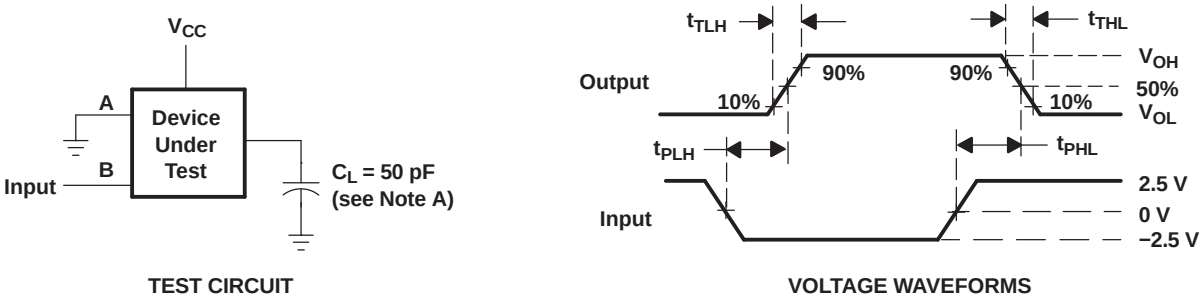
SWITCHING CHARACTERISTICS

over recommended ranges of operation conditions, C_L = 50 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 1	9	17	27	ns
t_{PHL}	Propagation delay time, high- to low-level output		9	17	27	ns
t_{TLH}	Output transition time, low- to high-level output	See Figure 1		4	10	ns
t_{THL}	Output transition time, high- to low-level output			4	9	ns
t_{PZH}	Output enable time to high level	See Figure 2		13	22	ns
t_{PZL}	Output enable time to low level			13	22	ns
t_{PHZ}	Output disable time from high level	See Figure 2		13	26	ns
t_{PLZ}	Output disable time from low level			13	25	ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

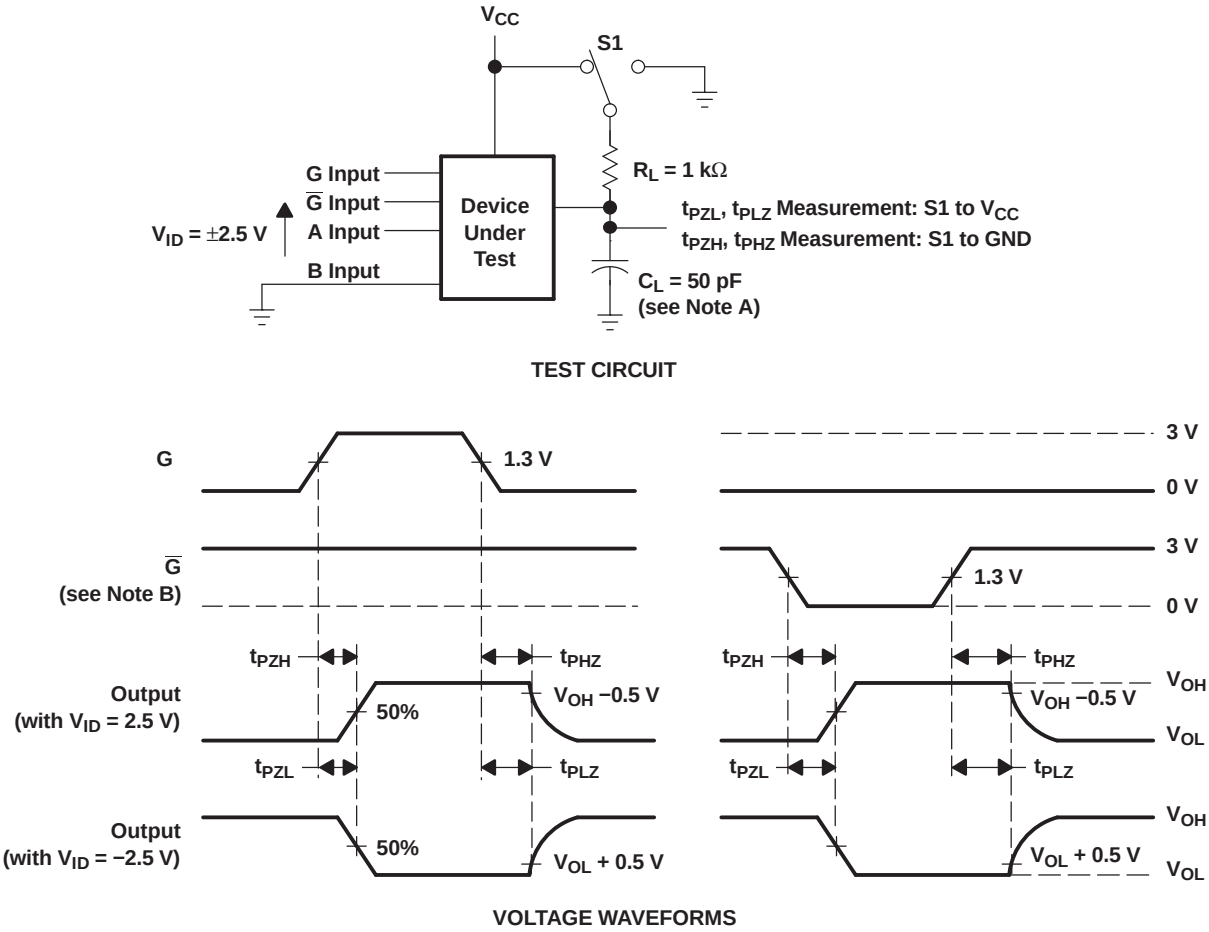
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

Figure 1. Switching Test Circuit and Voltage Waveforms



A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle ≤ 50%, $t_r = t_f$ = 6 ns.

Figure 2. Enable/Disable Time Test Circuit and Output Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AM26C32MDREP	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	26C32EP
AM26C32MDREP.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	26C32EP
V62/07648-01XE	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	26C32EP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF AM26C32-EP :

- Catalog : AM26C32

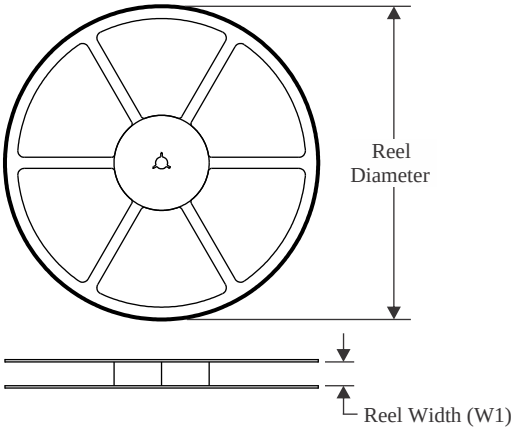
- Military : AM26C32M

NOTE: Qualified Version Definitions:

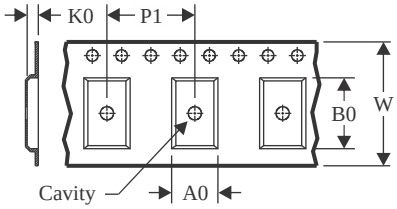
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

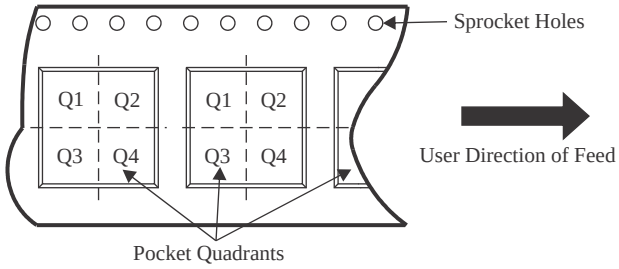


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

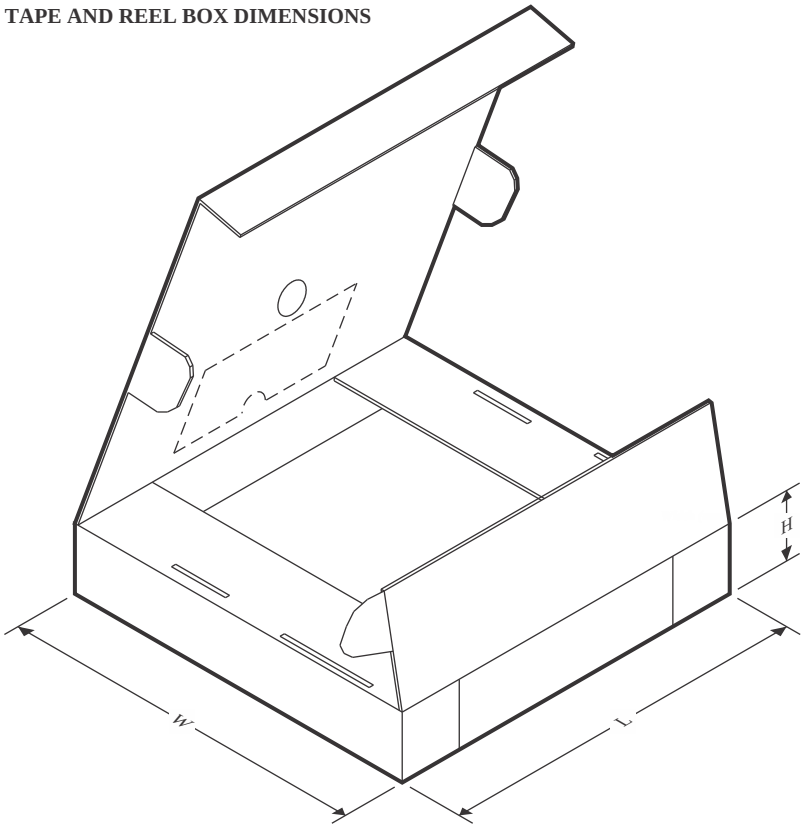
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AM26C32MDREP	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

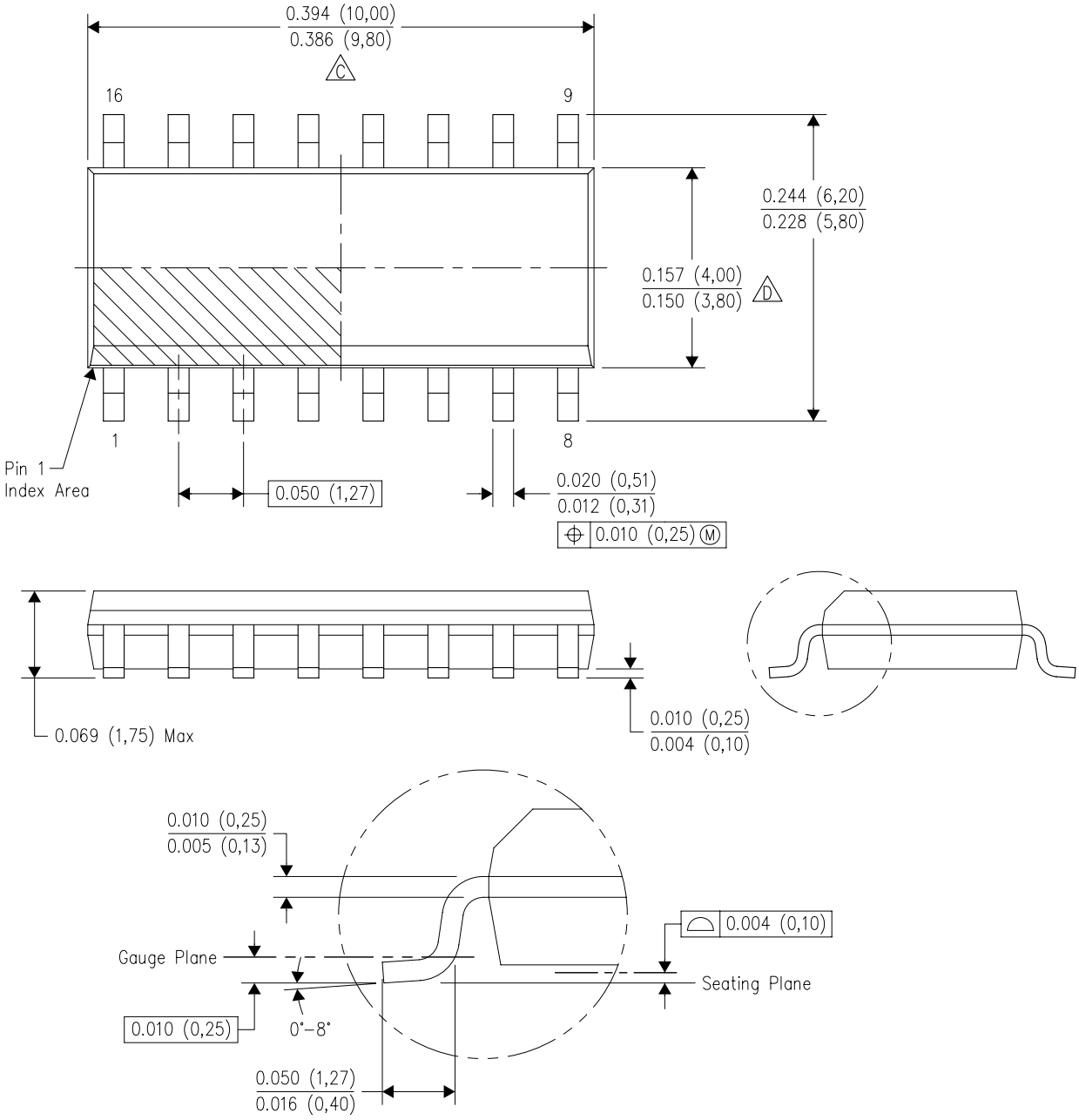
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AM26C32MDREP	SOIC	D	16	2500	353.0	353.0	32.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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