CDx4AC283, CDx4ACT283 4-Bit Binary Fill Adder with Fast Carry

1 Features

- Buffered inputs
- Exceeds 2kV ESD protection MIL-STD-883, method 3015
- SCR-latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST™/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5V to 5.5V operation and balanced noise immunity at 30% of the supply
- ±24mA output drive current
  - Fanout to 15 FAST™ ICs
  - Drives 50Ω transmission lines

2 Description

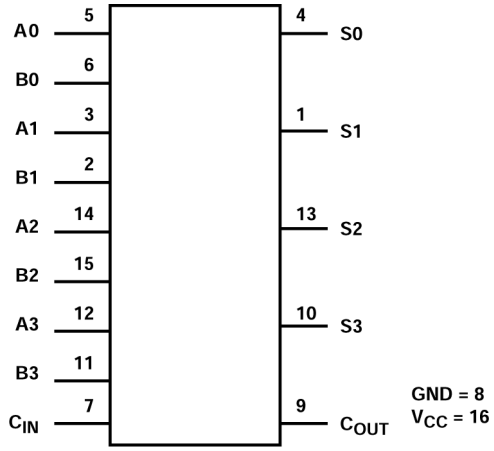
The ’AC283 and ’ACT283 4-bit binary adders with fast carry that utilize Advanced CMOS Logic technology. These devices add two 4-bit binary numbers and generate a carryout bit if the sum exceeds 15.

Because of the symmetry of the add function, this device can be used with either all active-HIGH operands (positive logic) or with all active-LOW operands (negative logic). When using positive logic, the carry-in input must be tied LOW if there is no carry-in.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
CDx4AC283/ CDx4ACT283	D (SOIC,16)	9.9mm x 6mm	9.9mm x 3.90mm
	N (PDIP,16)	19.3mm x 9.4mm	19.3mm x 6.35mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Functional Block Diagram

Table of Contents

3 Pin Configuration and Functions

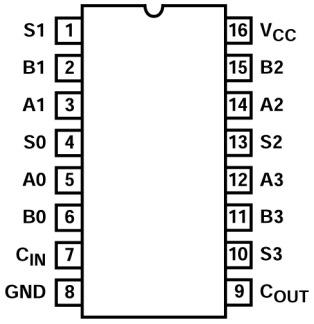


Figure 3-1. CD54AC283, CD54ACT283 J Package; CD74AC283, CD74ACT283 D or N Package; 16-Pin CDIP, PDIP, or SOIC (Top View)

Table 3-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
S1	1	O	Sum output 1
B1	2	I	1 bit input for binary number B
A1	3	I	1 bit input for binary number A
S0	4	O	Sum output 0
A0	5	I	0 bit input for binary number A
B0	6	I	0 bit input for binary number B
C_{IN}	7	I	Carry input
GND	8	G	Ground
C_{OUT}	9	O	Carry output
S3	10	O	Sum output 3
B3	11	I	3 bit input for binary number B
A3	12	I	3 bit input for binary number A
S2	13	O	Sum output 2
A2	14	I	2 bit input for binary number A
B2	15	I	2 bit input for binary number B
V_{CC}	14	P	V_{CC}

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	DC Supply Voltage		-0.5	6	V
I_{IK}	DC Input Diode Current	For V_I < -0.5V or V_I > V_{CC} + 0.5V		±20	mA
I_{OK}	DC Output Diode Current	For V_O < -0.5V or V_O > V_{CC} + 0.5V		±50	mA
I_O	DC Output Source or Sink Current per Output Pin	For V_O > -0.5V or V_O < V_{CC} + 0.5V		±50	mA
I_{CC} or I_{GND} (2)	DC V_{CC} or Ground Current			±100	mA
T_J	Junction temperature (Plastic Package)			150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
(2) For up to 4 outputs per device, add ±25mA for each additional output.

4.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC} (1)	Supply Voltage Range			V
	AC Types	1.5	5.5	
	ACT Types	4.5	5.5	
V_I, V_O	DC Input or Output Voltage	0	V_{CC}	V
dt/dv	Input Rise and Fall Slew Rate			ns (Max)
	AC Types, 1.5V to 3V		±50	
	AC Types, 3.6V to 5.5V		±20	
	ACT Types, 4.5V to 5.5V		±10	
T_A	Temperature Range	-55	125	°C

(1) Unless otherwise specified, all voltages are referenced to ground.

4.4 Thermal Information

THERMAL METRIC(1)		D (SOIC) 16 PINS	N (PDIP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73	67	°C/W

(1) The package thermal impedance is calculated in accordance with JESD 51.

4.5 DC Electrical Specifications

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC} (V)	25°C		-40°C TO 85 °C		-55°C TO 125°C		UNIT
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
	AC TYPES										
V_{IH}	High Level Input Voltage	-	-	1.5	1.2	-	1.2	-	1.2	-	V
				3	2.1	-	2.1	-	2.1	-	V
				5.5	3.85	-	3.85	-	3.85	-	V
V_{IL}	Low Level Input Voltage	-	-	1.5	-	0.3	-	0.3	-	0.3	V
				3	-	0.9	-	0.9	-	0.9	V
				5.5	-	1.65	-	1.65	-	1.65	V
V_{OH}	High Level Output Voltage	V_{IH} or V_{IL}	-0.05	1.5	1.4	-	1.4	-	1.4	-	V
			-0.05	3	2.9	-	2.9	-	2.9	-	V
			-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-4	3	2.58	-	2.48	-	2.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75[1], [2]	5.5	-	-	3.85	-	-	-	V
			-50[1], [2]	5.5	-	-	-	-	3.85	-	V
V_{OL}	Low Level Output Voltage	V_{IH} or V_{IL}	0.05	1.5	-	0.1	-	0.1	-	0.1	V
			0.05	3	-	0.1	-	0.1	-	0.1	V
			0.05	4.5	-	0.1	-	0.1	-	0.1	V
			12	3	-	0.36	-	0.44	-	0.5	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75[1], [2]	5.5	-	-	-	1.65	-	-	V
			50[1], [2]	5.5	-	-	-	-	-	1.65	V
I_I	Input Leakage Current	V_{CC} or GND	-	5.5	-	±0.1	-	±1	-	±1	µA
I_{CC}	Quiescent Supply Current MSI	V_{CC} or GND	0	5.5	-	8	-	80	-	160	µA
	ACT TYPES										
V_{IH}	High Level Input Voltage	-	-	4.5 to 5.5	2	-	2	-	2	-	V
V_{IL}	Low Level Input Voltage	-	-	4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
V_{OH}	High Level Output Voltage	V_{IH} or V_{IL}	-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75[1], [2]	5.5	-	-	3.85	-	-	-	V
			-50[1], [2]	5.5	-	-	-	-	3.85	-	V
V_{OL}	Low Level Output Voltage	V_{IH} or V_{IL}	0.05	4.5	-	0.1	-	0.1	-	0.1	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75[1], [2]	5.5	-	-	-	1.65	-	-	V
			50[1], [2]	5.5	-	-	-	-	-	1.65	V
I_I	Input Leakage Current	V_{CC} or GND	-	5.5	-	±0.1	-	±1	-	±1	µA
I_{CC}	Quiescent Supply Current MSI	V_{CC} or GND	0	5.5	-	8	-	80	-	160	µA

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC} (V)	25°C		-40°C TO 85 °C		-55°C TO 125°C		UNIT
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
ΔI_{CC}	Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load	V_{CC} -2.1	-	4.5 to 5.5	-	2.4	-	2.8	-	3	mA

(1) Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
(2) Test verifies a minimum 50Ω transmission-line-drive capability at 85°C, 75Ω at 125°C.

Table 4-1. ACT Input Load Table

INPUT	UNIT LOAD
A0, B0, A2, B2	1.66
A1, B1	1.9
A3, B3	1.4
C_{IN}	1.1

Note

Unit load is ΔI_{CC} limit specified in DC Electrical Specifications Table, e.g., 2.4mA max at 25°C.

4.6 Switching Specifications

Input t_r, t_f = 3ns, C_L = 50pF (Worst Case)

PARAMETER	SYMBOL	V_{CC} (V)	-40°C TO 85°C			-55°C TO 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
AC TYPES									
Propagation Delay, An or Bn to C_{OUT} C_{IN} to Sn C_{IN} to C_{OUT}	t_{PLH}, t_{PHL}	1.5	-	-	199	-	-	219	ns
		3.3(1)	6.3	-	22.4	6.2	-	24.6	ns
		5(2)	4.5	-	16	4.4	-	17.6	ns
Propagation Delay, An or Bn to Sn	t_{PLH}, t_{PHL}	1.5	-	-	207	-	-	228	ns
		3.3	6.6	-	23.2	6.4	-	25.5	ns
		5	4.7	-	16.5	4.6	-	18.2	ns
Input Capacitance	C_I	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	C_{PD} (3)	-	-	120	-	-	120	-	pF
ACT TYPES									
Propagation Delay, An or Bn to C_{OUT} C_{IN} to Sn C_{IN} to C_{OUT}	t_{PLH}, t_{PHL}	5(2)	4.5	-	16	2.7	-	17.6	ns
Propagation Delay, An or Bn to Sn	t_{PLH}, t_{PHL}	5	4.7	-	16.5	3.3	-	18.2	ns
Input Capacitance	C_I	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	C_{PD} (3)	-	-	120	-	-	120	-	pF

(1) 3.3V Min is at 3.6V, Max is at 3V.
(2) 5V Min is at 5.5V, Max is at 4.5V.
(3) C_{PD} is used to determine the dynamic power consumption per function.

Note

AC: $P_D = V_{CC}{}^2 f_i (C_{PD} + C_L)$

ACT: $P_D = V_{CC}{}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.

5 Parameter Measurement Information

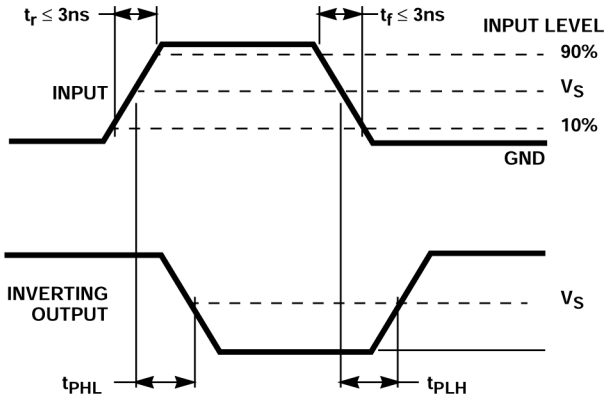
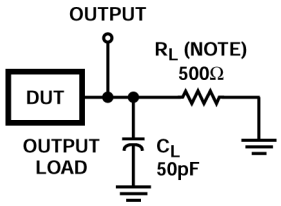


Figure 5-1. Propagation Delay Times



A. For AC Series Only: When V_{CC} = 1.5V, R_L = 1kΩ.

Figure 5-2. Propagation Delay Times

	AC	ACT
Input Level	V_{CC}	3V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

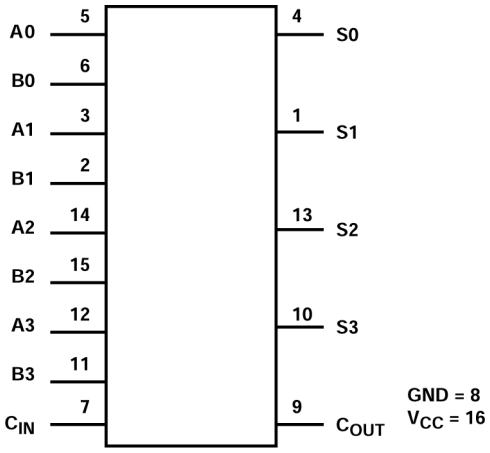
6 Detailed Description

6.1 Overview

The ’AC283 and ’ACT283 4-bit binary adders with fast carry that utilize Advanced CMOS Logic technology. These devices add two 4-bit binary numbers and generate a carryout bit if the sum exceeds 15.

Because of the symmetry of the add function, this device can be used with either all active-HIGH operands (positive logic) or with all active-LOW operands (negative logic). When using positive logic, the carry-in input must be tied LOW if there is no carry-in.

6.2 Functional Block Diagram



7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

7.2 Layout

7.2.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer signals that must branch separately

7.2.2 Layout Example

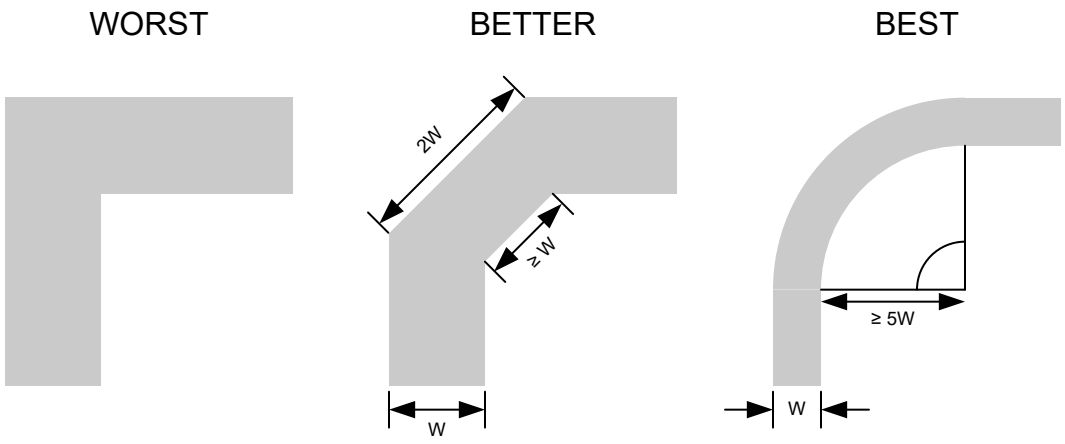


Figure 7-1. Example Trace Corners for Improved Signal Integrity

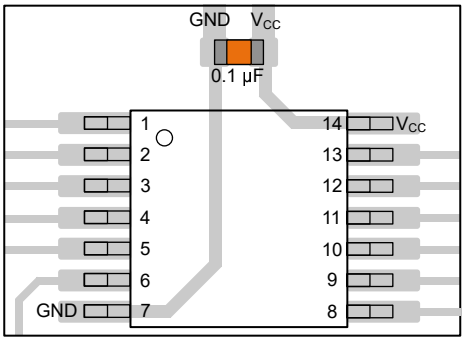


Figure 7-2. Example Bypass Capacitor Placement for TSSOP and Similar Packages

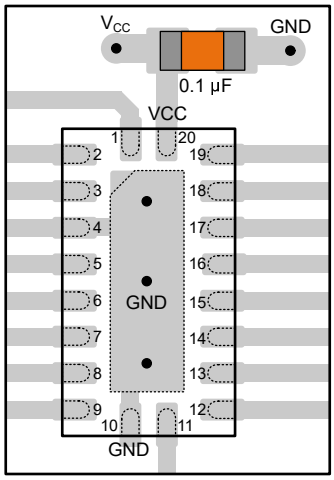


Figure 7-3. Example Bypass Capacitor Placement for WQFN and Similar Packages

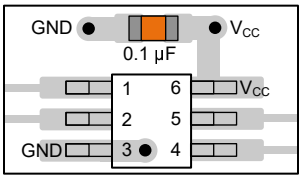


Figure 7-4. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

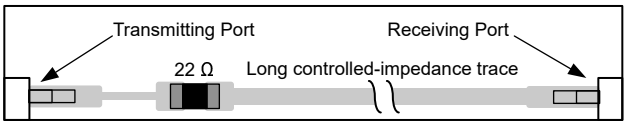


Figure 7-5. Example Damping Resistor Placement for Improved Signal Integrity

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application report
- Texas Instruments, *Designing With Logic* application report
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application report

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (May 2000) to Revision E (January 2025)	Page
• Added *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Device Functional Modes,*Application and Implementation section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD54AC283F3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54AC283F3A
CD54AC283F3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54AC283F3A
CD54ACT283F3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54ACT283F3A
CD54ACT283F3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54ACT283F3A
CD74AC283E	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74AC283E
CD74AC283E.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74AC283E
CD74AC283M	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	AC283M
CD74AC283M96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC283M
CD74AC283M96.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC283M
CD74ACT283E	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74ACT283E
CD74ACT283E.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74ACT283E
CD74ACT283EE4	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74ACT283E
CD74ACT283M	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT283M
CD74ACT283M.A	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT283M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF CD54AC283, CD54ACT283, CD74AC283, CD74ACT283 :

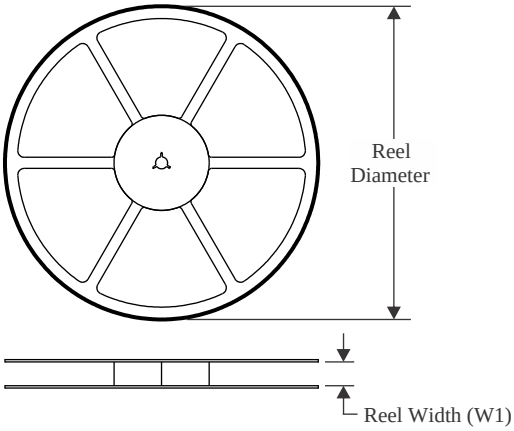
- Catalog : CD74AC283, CD74ACT283
- Military : CD54AC283, CD54ACT283

NOTE: Qualified Version Definitions:

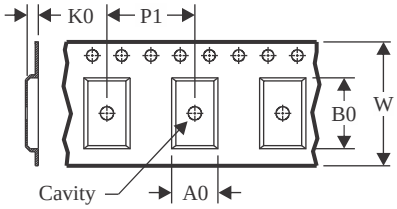
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

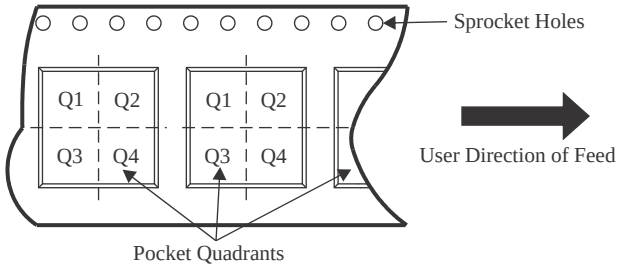


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

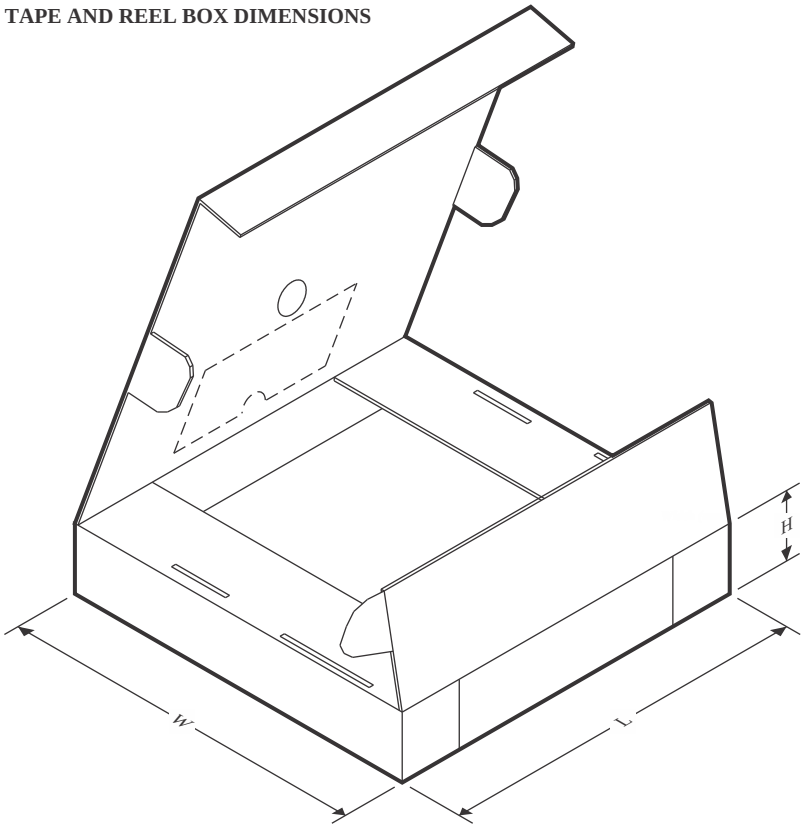
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC283M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

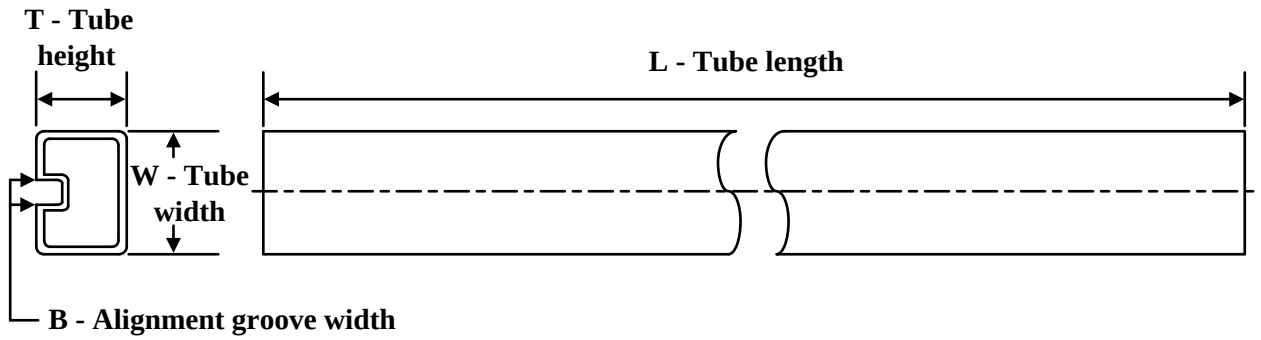
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC283M96	SOIC	D	16	2500	353.0	353.0	32.0

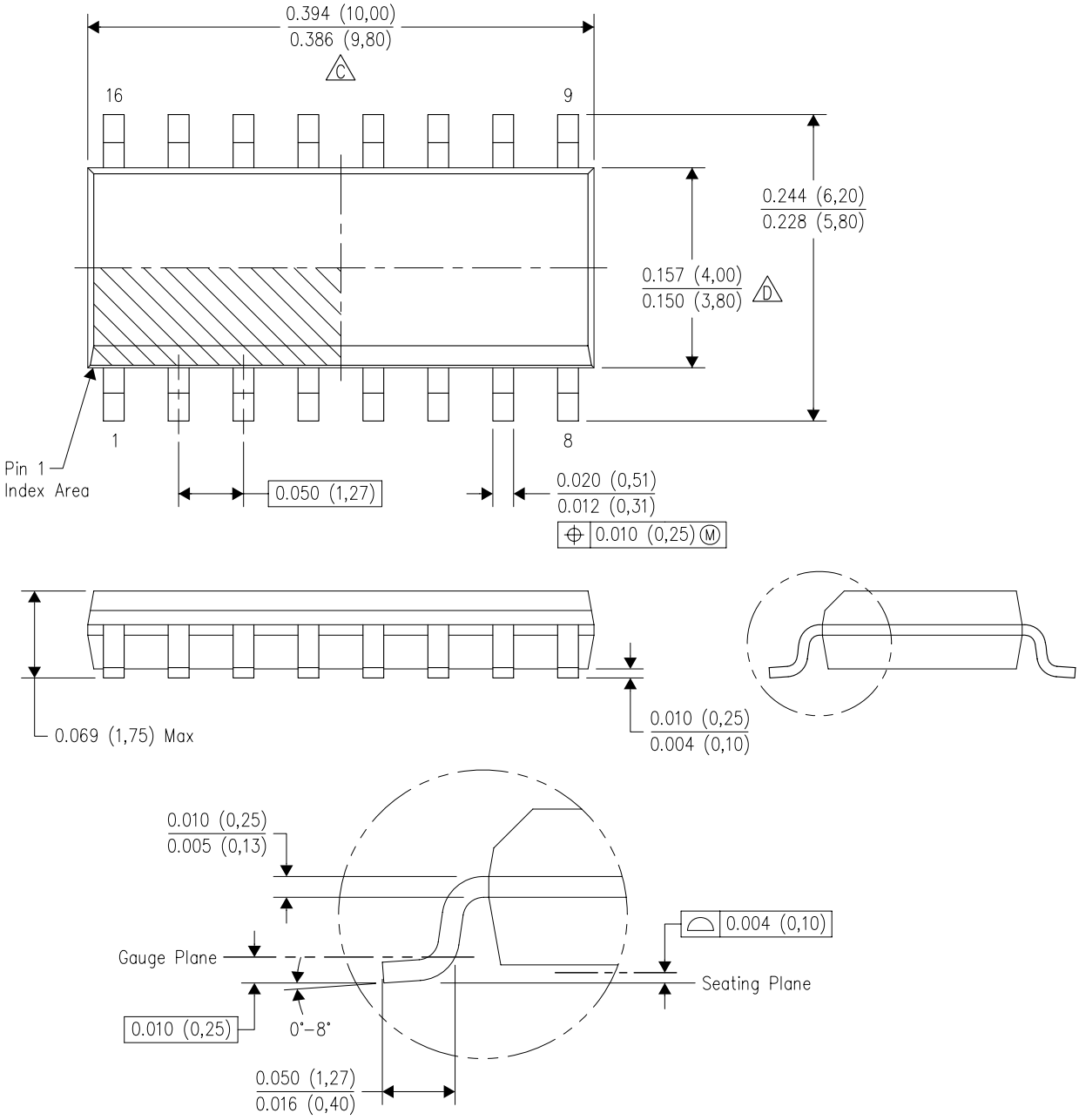
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74AC283E	N	PDIP	16	25	506	13.97	11230	4.32
CD74AC283E	N	PDIP	16	25	506	13.97	11230	4.32
CD74AC283E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74AC283E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74ACT283E	N	PDIP	16	25	506	13.97	11230	4.32
CD74ACT283E	N	PDIP	16	25	506	13.97	11230	4.32
CD74ACT283E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74ACT283E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74ACT283EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74ACT283EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74ACT283M	D	SOIC	16	40	507	8	3940	4.32
CD74ACT283M.A	D	SOIC	16	40	507	8	3940	4.32

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

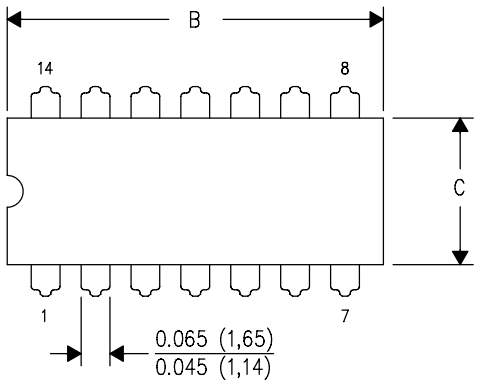


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

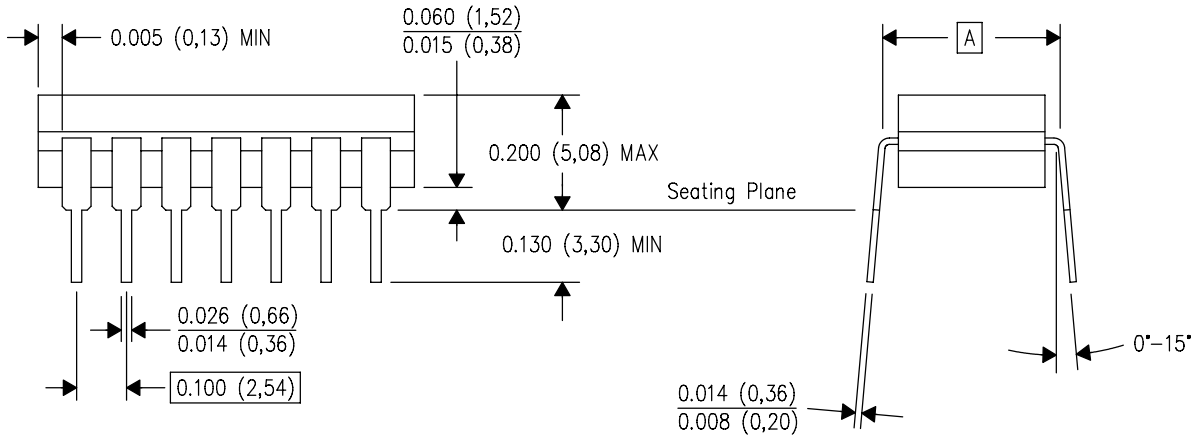
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



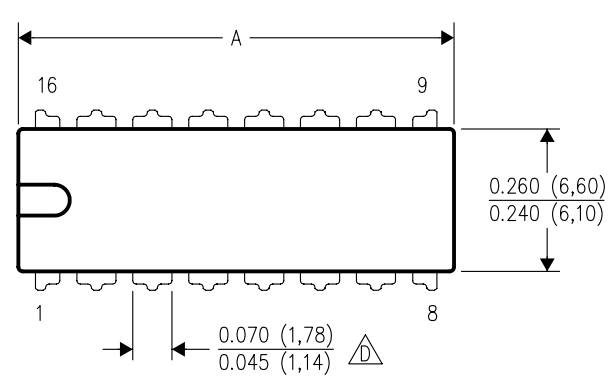
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

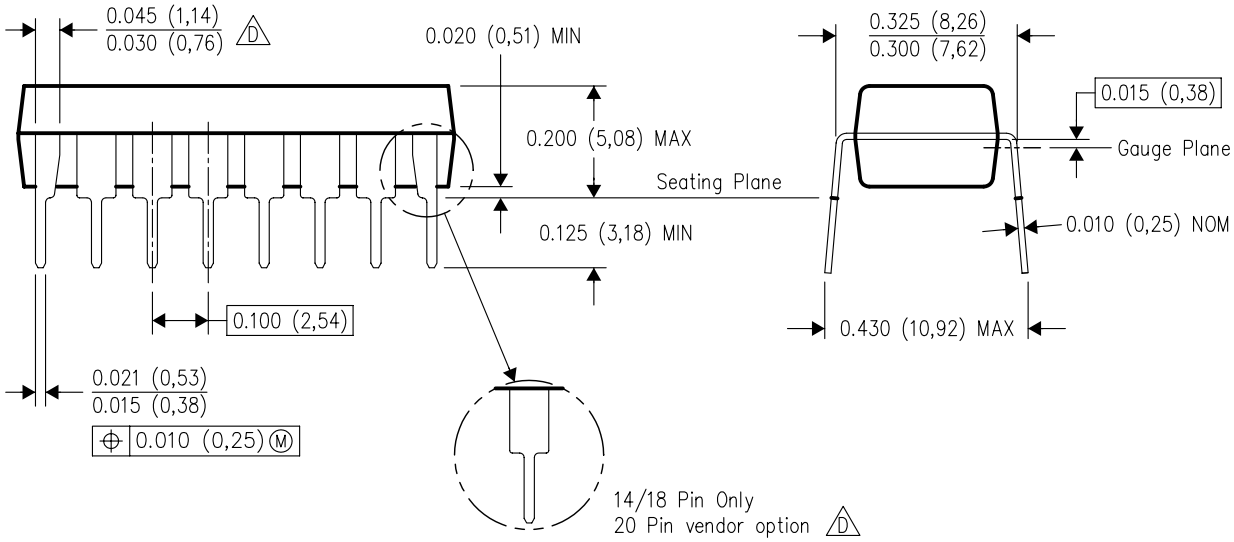
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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