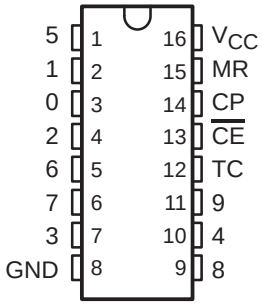
- **2-V to 6-V Operation**
- **Fully Static Operation**
- **Buffered Inputs**
- **Common Reset**
- **Positive-Edge Clocking**
- **Balanced Propagation Delay and Transition Times**
- **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5 V**
- **Packaged in Ceramic (F) DIP Package and Also Available in Chip Form (H)**

F PACKAGE
(TOP VIEW)



description

The CD54HC4017 is a high-speed silicon-gate CMOS 5-stage Johnson counter with ten decoded outputs. Each decoded output normally is low and sequentially goes high on the low-to-high transition of the clock (CP) input. Each output stays high for one clock period of the ten-clock-period cycle. The terminal count (TC) output transitions low to high after output ten (9) goes low, and can be used in conjunction with the clock enable ($\overline{CE}$) input to cascade several stages. $\overline{CE}$ disables counting when in the high state. The master reset (MR) input, when taken high, sets all the decoded outputs, except 0, to low.

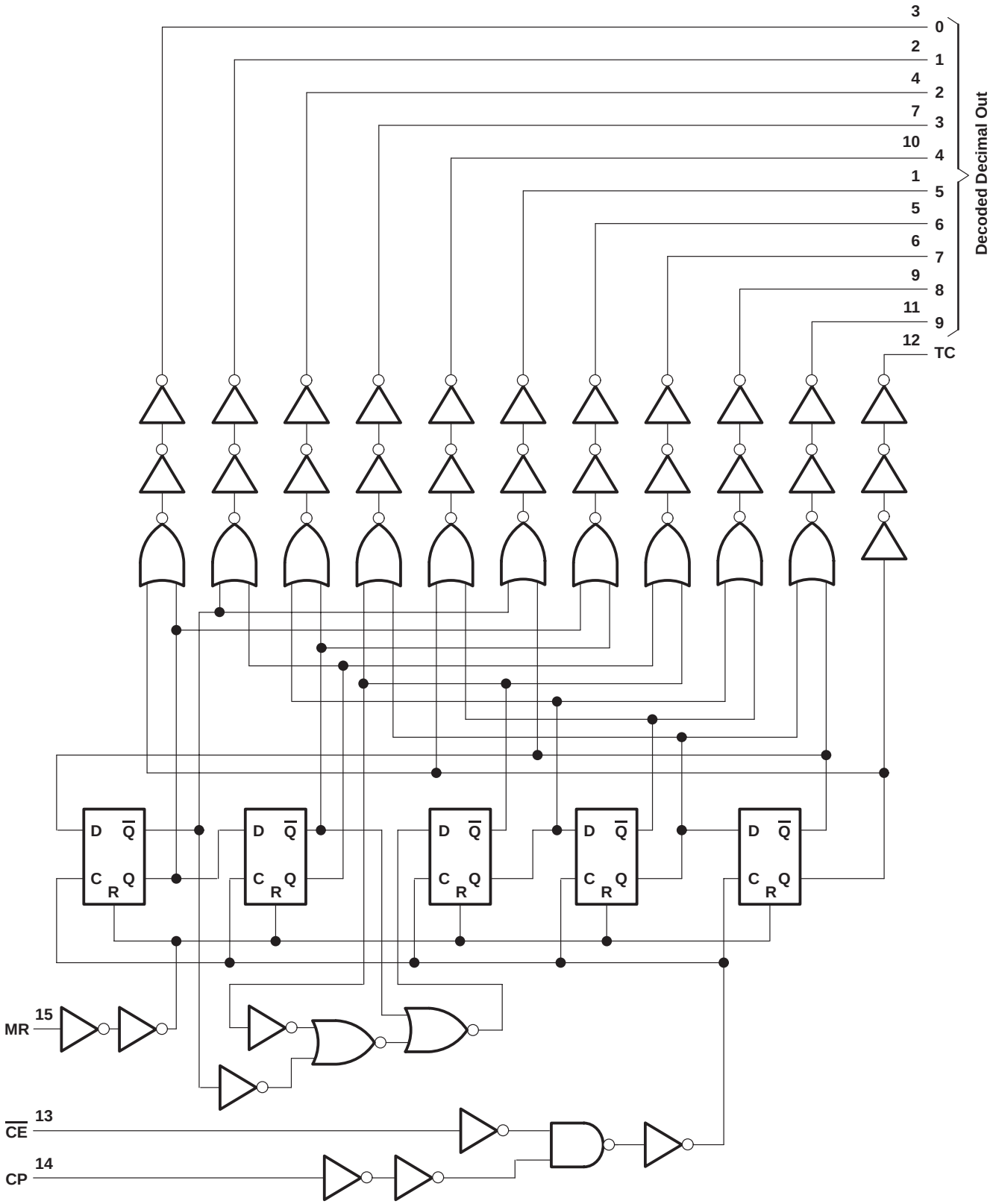
The CD54HC4017 is characterized for operation over the full military temperature range of –55°C to 125°C.

FUNCTION TABLE

INPUTS			OUTPUT STATE†
CP	$\overline{CE}$	MR	
L	X	L	No change
X	H	L	No change
X	X	H	0 = H 1–9 = L
↑	L	L	Increments counter
↓	X	L	No change
X	↑	L	No change
H	↓	L	Increments counter

† If n < 5, TC = H; otherwise, TC = L.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input clamp current, I_{IK} (V_I < 0 V or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 V or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, each output pin, I_O (V_O > –0.5 V or V_O < V_{CC} + 0.5 V) . . . . . ±25 mA
V_{CC} or ground current, I_{CC} . . . . . ±50 mA
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating (see Note 1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 4.5 V	3.15		
		V_{CC} = 6 V	4.2		
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0	0.5	V
		V_{CC} = 4.5 V	0	1.35	
		V_{CC} = 6 V	0	1.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0	1000	ns
		V_{CC} = 4.5 V	0	500	
		V_{CC} = 6 V	0	400	
T_A	Operating free-air temperature		–55	125	°C

NOTE 1: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

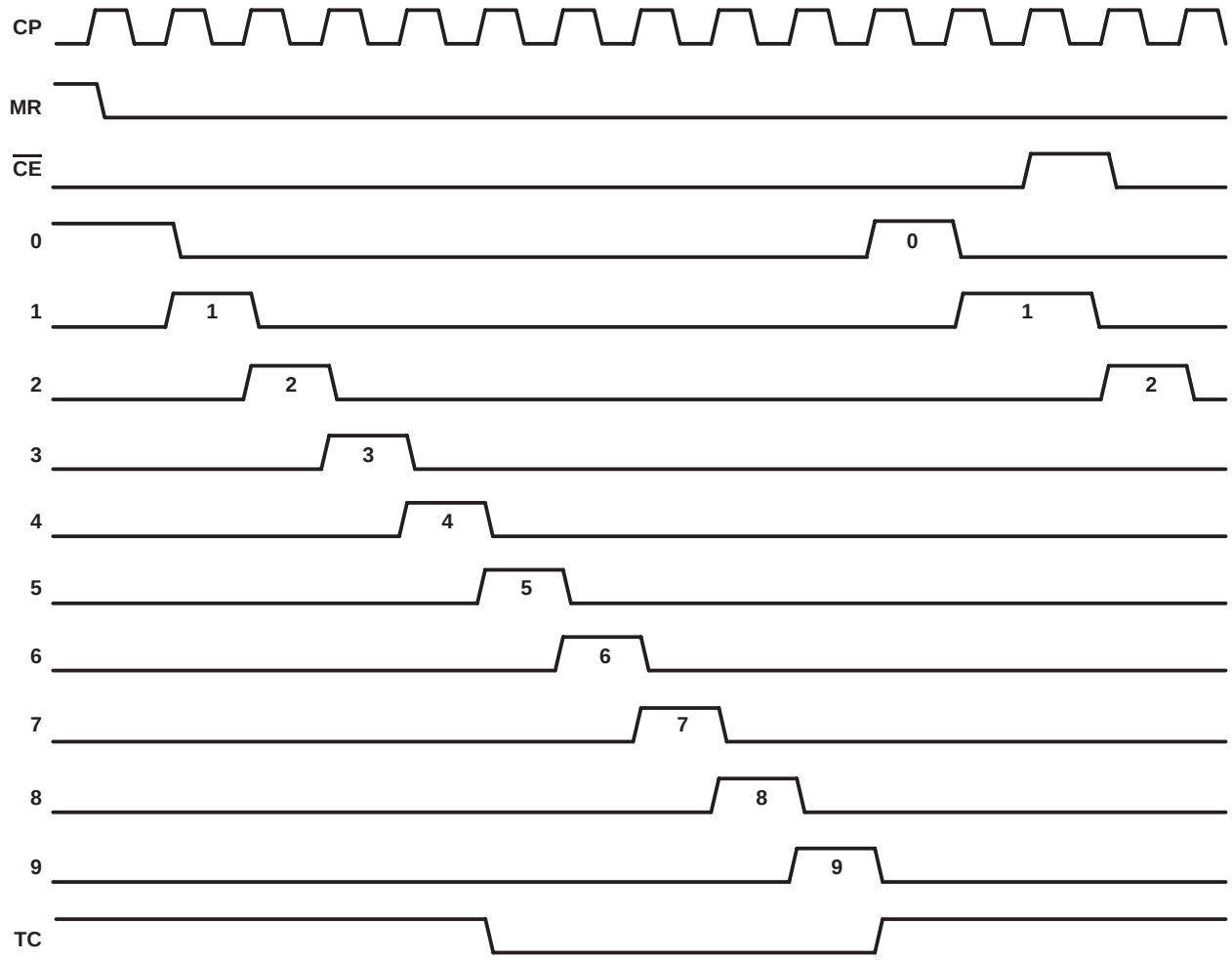
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	T_A = 25°C		MIN	MAX	UNIT
					MIN	MAX			
V_{OH}	CMOS loads	V_I = V_{IH} or V_{IL},	I_{OH} = –0.02 mA	2 V	1.9		1.9		V
				4.5 V	4.4		4.4		
				6 V	5.9		5.9		
	TTL loads	V_I = V_{IH} or V_{IL}	I_{OH} = –4 mA	4.5 V	3.98		3.7		
			I_{OH} = –5.2 mA	6 V	5.48		5.2		
V_{OL}	CMOS loads	V_I = V_{IH} or V_{IL},	I_{OL} = 0.02 mA	2 V		0.1		0.1	V
				4.5 V		0.1		0.1	
				6 V		0.1		0.1	
	TTL loads	V_I = V_{IH} or V_{IL}	I_{OL} = 4 mA	4.5 V		0.26		0.4	
			I_{OL} = 5.2 mA	6 V		0.26		0.4	
I_I		V_I = V_{CC} or 0		6 V		±100		±1000	nA
I_{CC}		V_I = V_{CC} or 0,	I_O = 0	6 V		8		160	µA
C_i				2 V to 6 V		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			V_{CC}	T_A = 25°C		MIN	MAX	UNIT
				MIN	MAX			
f_{clock}	Maximum clock frequency		2 V		6		4	MHz
			4.5 V		30		20	
			6 V		35		23	
t_w	Pulse duration	CP	2 V	80		120		ns
			4.5 V	16		24		
			6 V	14		20		
		MR	2 V	80		120		
			4.5 V	16		24		
			6 V	14		20		
t_{su}	Setup time, $\overline{CE}$ to CP		2 V	75		110		ns
			4.5 V	15		22		
			6 V	13		19		
t_h	Hold time, $\overline{CE}$ to CP		2 V	0		0		ns
			4.5 V	0		0		
			6 V	0		0		
t_{rem}	Removal time, MR		2 V	5		5		ns
			4.5 V	5		5		
			6 V	5		5		

timing requirements



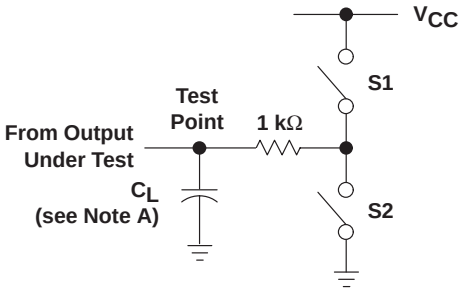
switching characteristics, C_L = 50 pF, T_A = 25°C (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C		T_A = –55°C TO 125°C		UNIT
				MIN	MAX	MIN	MAX	
f_{max}			2 V	6		4		MHz
			4.5 V	20		20		
			6 V	35		23		
t_{pd}	CP	Any output	2 V		230		345	ns
			4.5 V		46		69	
			6 V		39		59	
t_{pd}		TC	2 V		230		345	ns
			4.5 V		46		69	
			6 V		39		59	
t_{pd}	$\overline{CE}$	Any output	2 V		250		375	ns
			4.5 V		50		75	
			6 V		43		64	
t_{pd}		TC	2 V		250		375	ns
			4.5 V		50		75	
			6 V		43		64	
t_{pd}	MR	Any output	2 V		230		345	ns
			4.5 V		46		69	
			6 V		39		59	
t_{pd}		TC	2 V		230		345	ns
			4.5 V		46		69	
			6 V		39		59	

operating characteristics

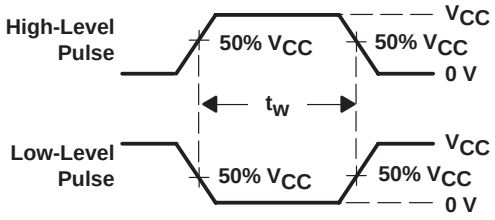
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	39	pF

PARAMETER MEASUREMENT INFORMATION

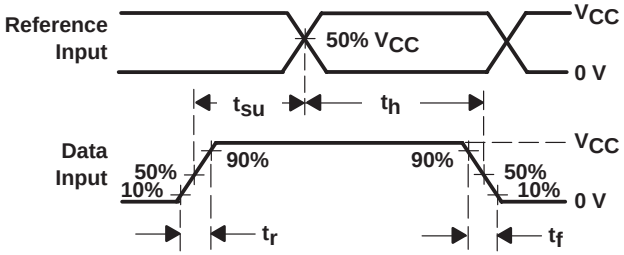


LOAD CIRCUIT

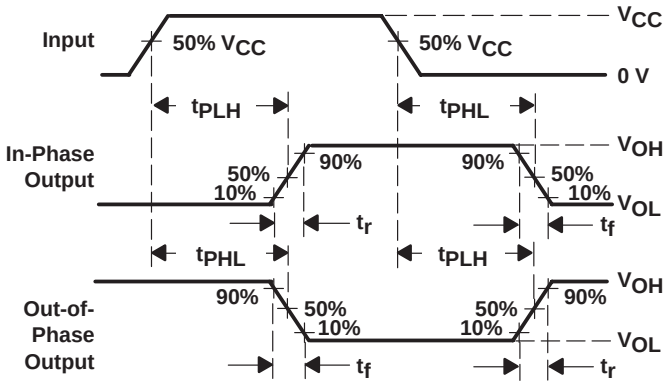
PARAMETER		S1	S2
t_{en}	t_{PZH}	Open	Closed
	t_{PZL}	Closed	Open
t_{dis}	t_{PHZ}	Open	Closed
	t_{PLZ}	Closed	Open
t_{pd} or t_t		Open	Open



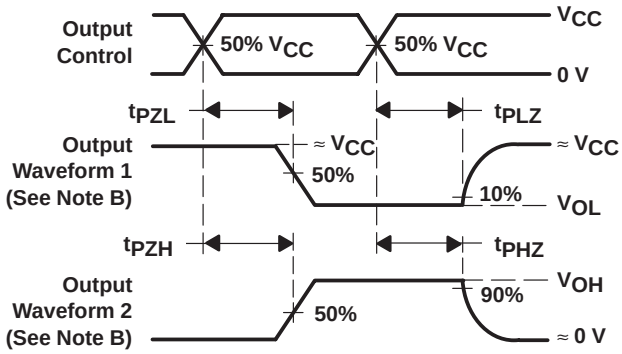
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

INPUT LEVEL	V_{CC}
V_S	0.5 V_{CC}

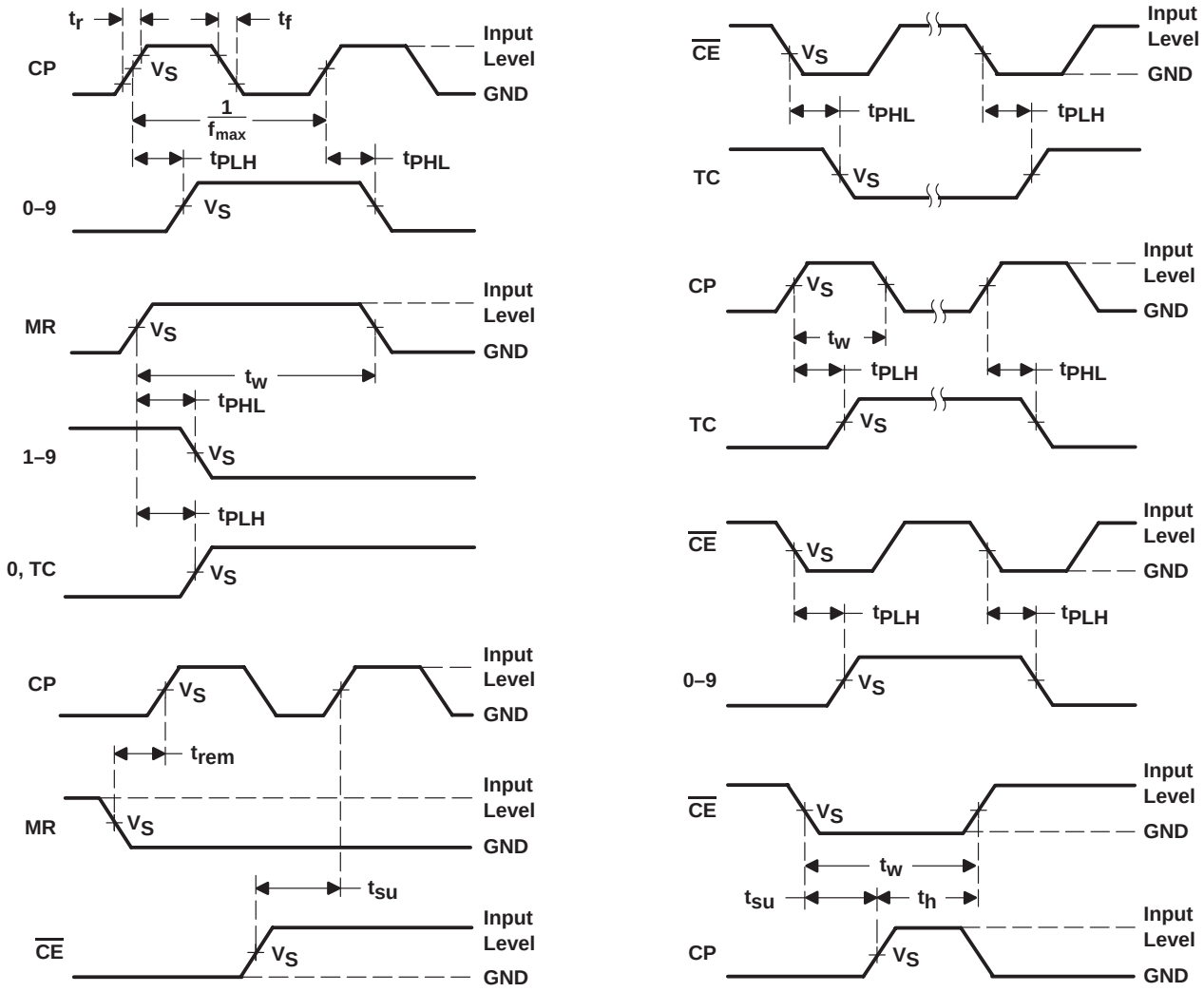


Figure 2. Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
8601101EA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8601101EA CD54HC4017F3A
CD54HC4017F3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8601101EA CD54HC4017F3A
CD54HC4017F3A.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8601101EA CD54HC4017F3A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF CD54HC4017 :

- Catalog : CD74HC4017
- Automotive : CD74HC4017-Q1
- Enhanced Product : CD74HC4017-EP

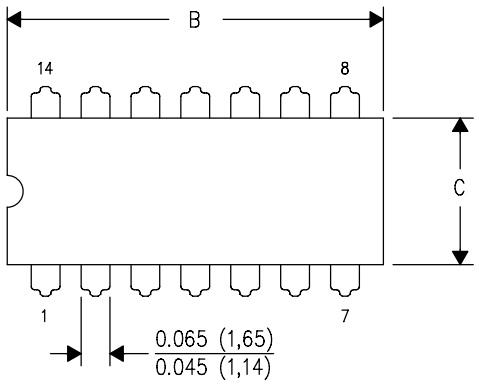
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

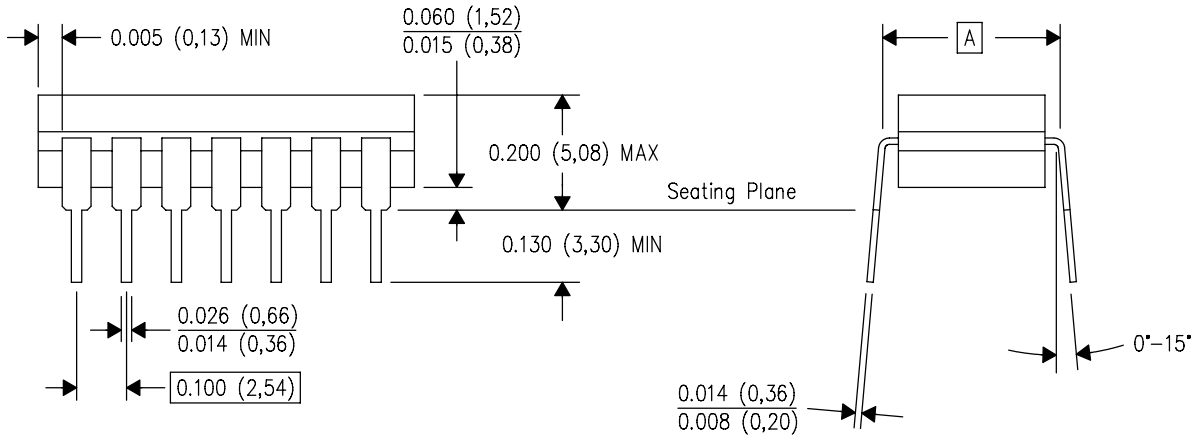
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

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