

CDC339 Clock Driver with 3-State Outputs

1 Features

- Low Output Skew, Low Pulse Skew for Clock-Distribution and Clock-Generation Applications
- TTL-Compatible Inputs and Outputs
- Distributes One Clock Input to Eight Outputs
 - Four Same-Frequency Outputs
 - Four Half-Frequency Outputs
- Distributed V_{CC} and Ground Pins Reduce Switching Noise
- High-Drive Outputs ($-48\text{-mA } I_{OH}$, $48\text{-mA } I_{OL}$)
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages

2 Applications

- Data center switch and server motherboard

3 Description

The CDC339 is a high-performance, low-skew clock driver. It is specifically designed for applications requiring synchronized output signals at both the primary clock frequency and one-half the primary clock frequency. The four Y outputs switch in phase and at the same frequency as the clock (CLK) input. The four Q outputs switch at one-half the frequency of CLK.

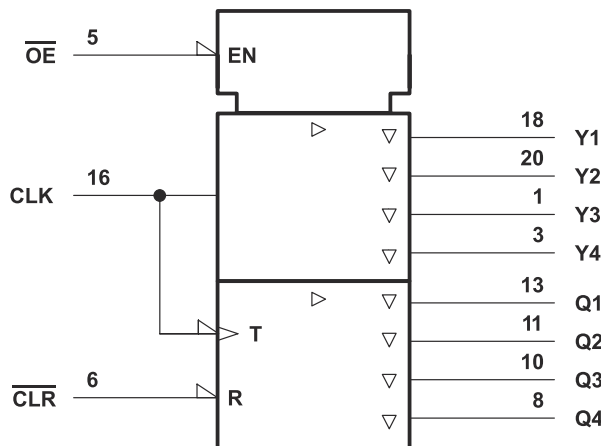
When the output-enable (\overline{OE}) input is low and the clear (\overline{CLR}) input is high, the Y outputs follow CLK and the Q outputs toggle on low-to-high transitions of CLK. Taking \overline{CLR} low asynchronously resets the Q outputs to the low level. When \overline{OE} is high, the outputs are in the high-impedance state.

The CDC339 is characterized for operation from -40°C to 85°C .

Device Information

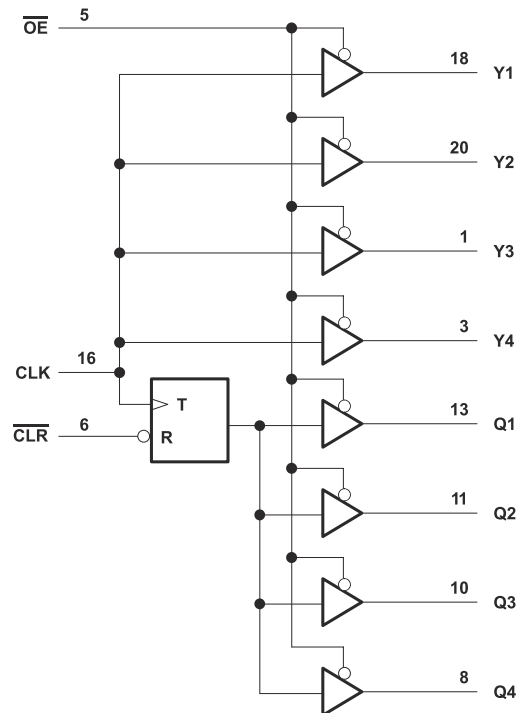
PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
CDC339DW	SOIC (20)	132 mm ² 12.8 x 10.3
CDC339DB	SSOP (20)	38 mm ² 5.3 x 7.2

- (1) For all available packages, see the orderable addendum at the end of the data sheet.



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Logic Symbol



Logic Diagram (Positive Logic)



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 1994) to Revision A (May 2020)	Page
• Updated to new TI standard.....	1
• Added Application bullet.....	1

5 Pin Configuration and Functions

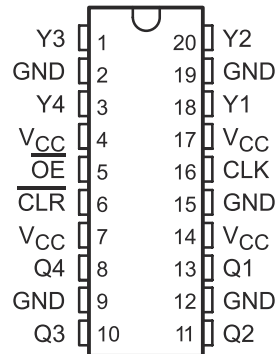


Figure 5-1. DB OR DW PACKAGE (TOP VIEW)

Function Table

INPUTS			OUTPUTS	
$\overline{\text{OE}}$	$\overline{\text{CLR}}$	CLK	Y1–Y4	Q1–Q4
H	X	X	Z	Z
L	L	L	L	L
L	L	H	H	L
L	H	L	L	Q ₀ ⁽¹⁾
L	H	↑	H	$\overline{\text{Q}}_0$ ⁽¹⁾

(1) The level of the Q outputs before the indicated steady-state input conditions were established.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	7	V
V _I	Input voltage range ⁽²⁾	-0.5	7	V
V _O	Voltage range applied to any output in the disabled or power-off state	-0.5	5.5	V
I _O	Current into any output in the low state		96	mA
I _{IK} (V _I < 0)	Input clamp current		-18	mA
I _{OK} (V _O < 0)	Output clamp current		-50	mA
	Maximum power dissipation at T _A = 55°C (in still air) ⁽³⁾	DB Package	0.6	W
		DW Package	1.6	W
T _{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the Package Thermal Considerations application note in the [1994 ABT Advanced BiCMOS Technology Data Book](#), literature number SCBD002B.

6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	4.75	5.25	V
V _{IH}	High-level input voltage	2		V
V _{IL}	Low-level input voltage		0.8	V
V _I	Input voltage	0	V _{CC}	V
I _{OH}	High-level output current		-48	mA
I _{OL}	Low-level output current		48	mA
f _{clock}	Input clock frequency		80	MHz
T _A	Operating free-air temperature	-40	85	°C

- (1) Unused pins (input or I/O) must be held high or low.

6.3 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IK}	V _{CC} = 4.75 V	I _I = -18 mA			-1.2	V
V _{OH}	V _{CC} = 4.75 V	I _{OH} = -48 mA	2			V
V _{OL}	V _{CC} = 4.75 V	I _{OL} = 48 mA			0.5	V
I _{IH}	V _{CC} = 5.25 V	V _I = 2.7 V			50	μA
I _{IL}	V _{CC} = 5.25 V	V _I = 0.5 V			-50	μA
I _{OZ}	V _{CC} = 5.25 V	V _O = 2.7 V or 0.5 V			±50	μA
I _O ⁽²⁾	V _{CC} = 5.25 V	V _O = 2.5 V	-50		-180	mA
I _{CC}	V _{CC} = 5.25 V V _I = V _{CC} or GND	I _O = 0	Outputs high		70	mA
			Outputs low		85	
			Outputs disabled		70	
C _i	V _I = 2.5 V or 0.5 V			3		pF
C _o	V _O = 2.5 V or 0.5 V			8		pF

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

(2) Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

6.4 Timing Requirements

over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
f _{clock}	Clock frequency		80	MHz
t _w	Pulse duration	CLR low	4	ns
		CLK low	4	
		CLK high	4	
t _{su}	Setup time	CLR inactive before CLK↑	2	ns
Clock duty cycle		40%	60%	

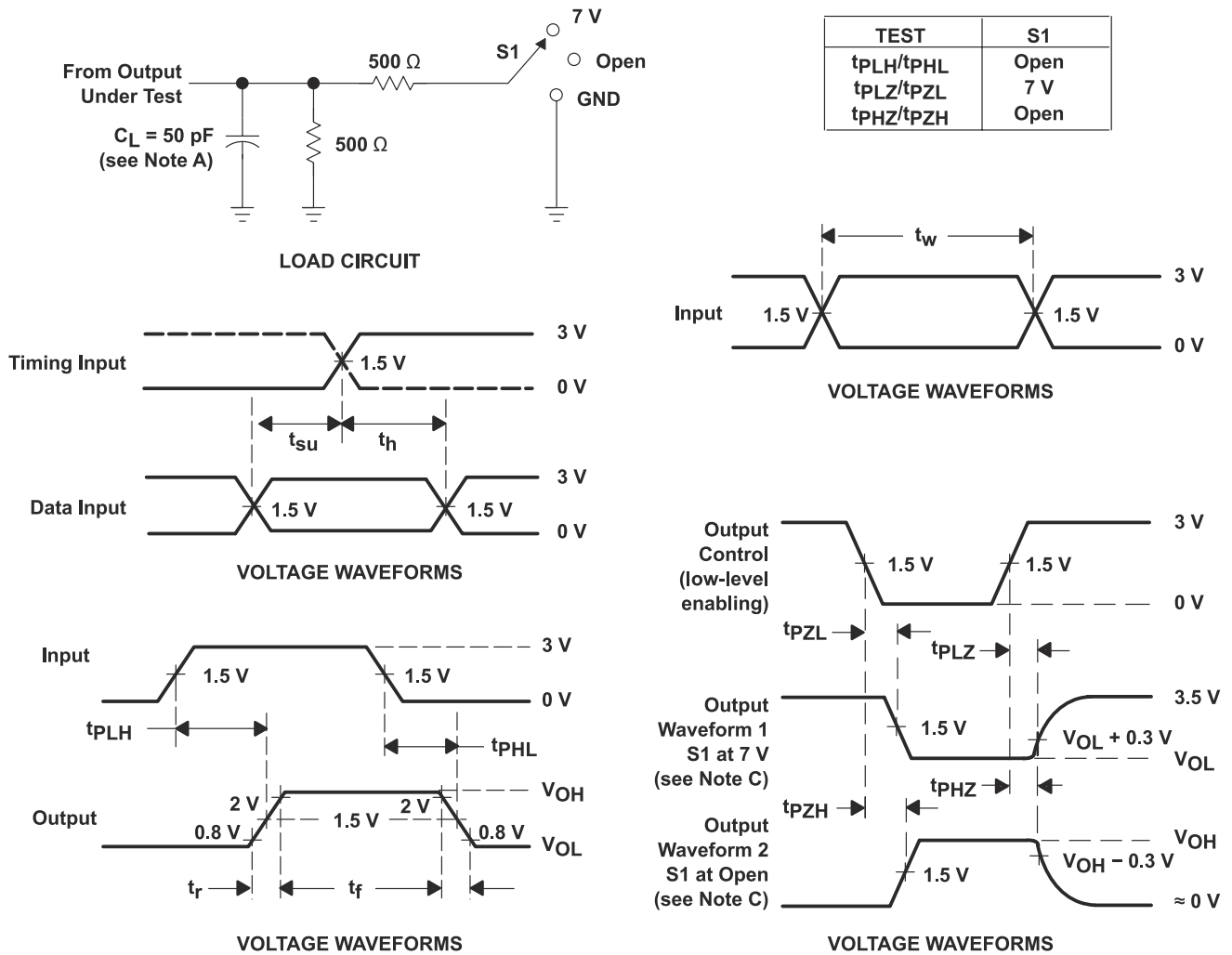
6.5 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (see [Figure 6-1](#) and [Figure 6-2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP ⁽¹⁾	MAX	UNIT
f _{max}			80			MHz
t _{PLH}	CLK	Any Y or Q	3		9	ns
t _{PHL}			3		9	
t _{PHL}	CLR	Any Q	4		9	ns
t _{PZH}	OE	Any Y or Q	2		7	ns
t _{PZL}			3		7	
t _{PHZ}	OE	Any Y or Q	2		7	ns
t _{PLZ}			2		7	
t _{sk(o)}	CLK↑	Y↑			0.75	ns
		Q↑			0.9	
		Y↑ and Q↑			0.9	
t _r				0.9		ns
t _f				0.7		ns

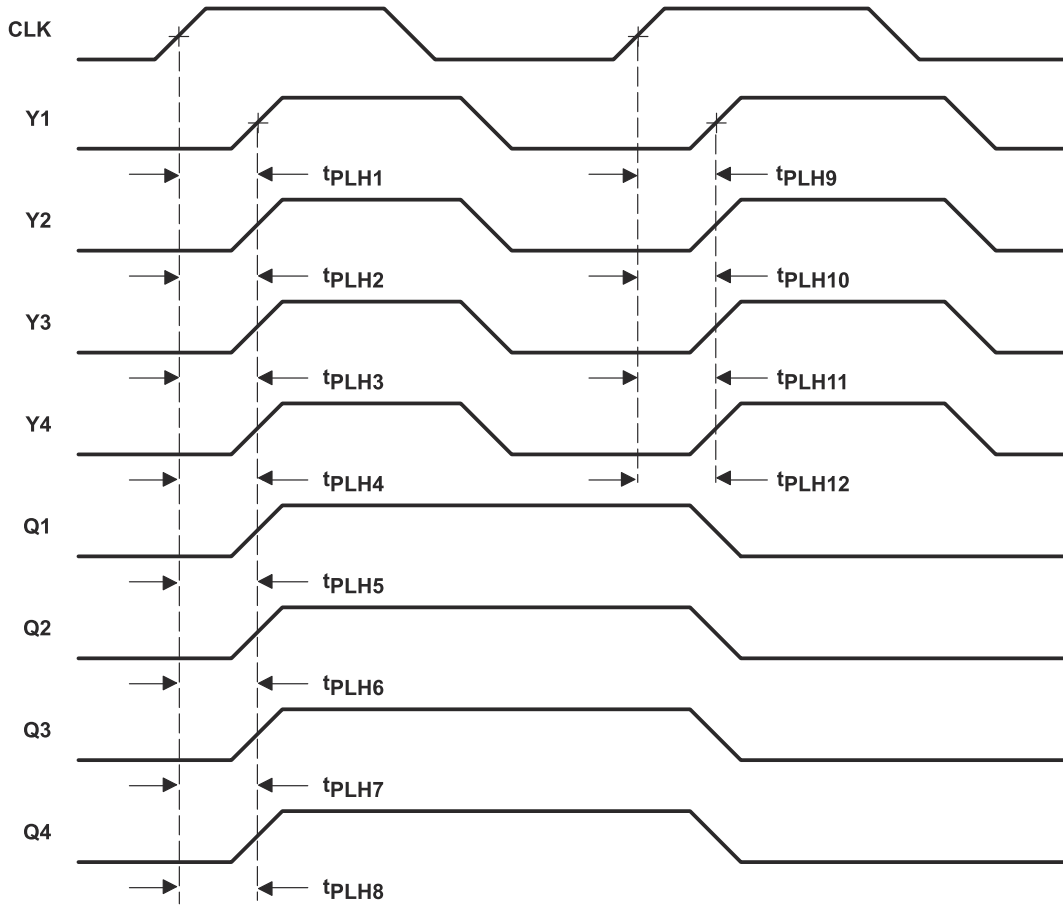
(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

7 Parameter Measurement Information



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - D. The outputs are measured one at a time with one transition per measurement.

Figure 7-1. Load Circuit and Voltage Waveforms



- NOTES:
- Output skew, $t_{sk(o)}$, from $CLK \uparrow$ to $Y \uparrow$, is calculated as the greater of the difference between the fastest and slowest of t_{PLHn} ($n = 1, 2, 3, 4$) or t_{PLHn} ($n = 9, 10, 11, 12$).
 - Output skew, $t_{sk(o)}$, from $CLK \uparrow$ to $Q \uparrow$, is calculated as the greater of the difference between the fastest and slowest of t_{PLHn} ($n = 5, 6, 7, 8$).
 - Output skew, $t_{sk(o)}$, from $CLK \uparrow$ to $Y \uparrow$ and $Q \uparrow$, is calculated as the greater of the difference between the fastest and slowest of t_{PLHn} ($n=1,2, \dots, 8$).

Figure 7-2. Skew Waveforms and Calculations

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.3 Trademarks

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8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CDC339DB	Active	Production	SSOP (DB) 20	70 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CK339
CDC339DB.B	Active	Production	SSOP (DB) 20	70 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CK339
CDC339DW	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDC339
CDC339DW.B	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDC339

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CDC339DB	DB	SSOP	20	70	530	10.5	4000	4.1
CDC339DB.B	DB	SSOP	20	70	530	10.5	4000	4.1
CDC339DW	DW	SOIC	20	25	507	12.83	5080	6.6
CDC339DW.B	DW	SOIC	20	25	507	12.83	5080	6.6

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.

DB0020A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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