

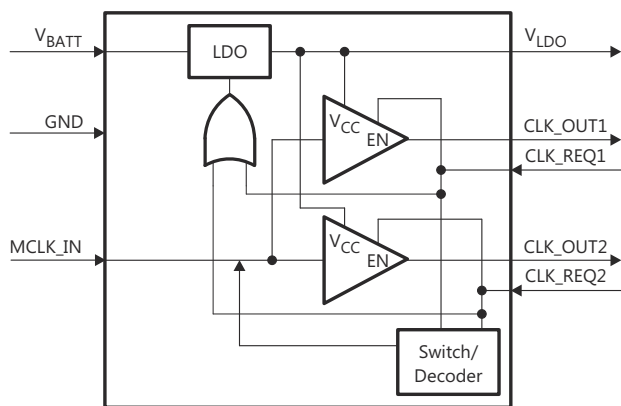
CDC3RL02 Low Phase-Noise Two-Channel Clock Fan-Out Buffer

1 Features

- Low Additive Noise:
 - -149dBc/Hz at 10kHz Offset Phase Noise
 - 0.37ps (RMS) Output Jitter
- Limited Output Slew Rate for EMI Reduction (1ns to 5ns Rise/Fall Time for 10pF to 50pF Loads)
- Adaptive Output Stage Controls Reflection
- Regulated 1.8V Externally Available I/O Supply
- Ultra-Small 8-bump YFP 0.4mm Pitch WCSP (0.8mm × 1.6mm)
- ESD Performance Exceeds JESD 22
 - 2000V Human-Body Model (A114-A)
 - 1000V Charged-Device Model (JESD22-C101-A Level III)

2 Applications

- Cellular Phones
- Global Positioning Systems (GPS)
- Wireless LAN
- FM Radio
- WiMAX
- W-BT



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Simplified Block Diagram

3 Description

The CDC3RL02 is a two-channel clock fan-out buffer and is designed for use in portable end-equipment, such as mobile phones, that require clock buffering with minimal additive phase noise and fan-out capabilities. The device buffers a single clock source, such as a temperature compensated crystal oscillator (TCXO) to multiple peripherals. The device has two clock request inputs (CLK_REQ1 and CLK_REQ2), each input can enable a single clock output.

The CDC3RL02 accepts square or sine waves at the master clock input (MCLK_IN), eliminating the need for an AC coupling capacitor. The smallest acceptable sine wave is a 0.3V signal (peak-to-peak). CDC3RL02 is designed to offer minimal channel-to-channel skew, additive output jitter, and additive phase noise. The adaptive clock output buffers offer controlled slew-rate over a wide capacitive loading range which minimizes EMI emissions, maintains signal integrity, and minimizes ringing caused by signal reflections on the clock distribution lines.

The CDC3RL02 has an integrated Low-Drop-Out (LDO) voltage regulator which accepts input voltages from 2.3V to 5.5V and outputs 1.8V, 50mA. This 1.8V supply is externally available to provide regulated power to peripheral devices such as a TCXO.

The CDC3RL02 is offered in a 0.4mm pitch die size ball grid array (DSBGA) package (0.8mm × 1.6mm), also known as wafer-level chip-scale (WCSP) package, and is optimized for very low standby current consumption.

Package Information

PART NUMBER ⁽¹⁾	PACKAGE	PACKAGE SIZE ⁽²⁾
CDC3RL02	YFP (DSBGA, 8)	0.80mm × 1.60mm

(1) For more information, see [Section 11](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



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4 Device Comparison

Table 4-1. Device Comparison

T _A	PACKAGE ⁽¹⁾	ORDERABLE PART NUMBER	BACKSIDE COATING ⁽²⁾
-40°C to 85°C	YFP	CDC3RL02BYFPR	Yes
-40°C to 85° C	YFP	CDC3RL02YFPR	No

- (1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
 (2) CSP (DSBGA) devices manufactured with backside coating have an increased resistance to cracking due to the increased physical strength of the package. Devices with backside coating are highly encouraged for new designs.

5 Pin Configuration and Functions

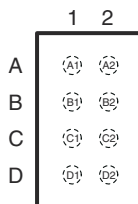


Figure 5-1. YFP Package 8-Pin DSBGA Top View

Table 5-1. Pin Functions

PIN		Type ⁽¹⁾	DESCRIPTION
NAME	NO.		
V _{BATT}	A1	I	Input to internal LDO
CLK_OUT1	A2	O	Clock output 1
V _{LDO}	B1	O	1.8V I/O supply for CDC3RL02 and external TCXO
CLK_REQ1	B2	I	Clock request 1 (from peripheral) for Clock output 1
MCLK_IN	C1	I	Master clock input
CLK_REQ2	C2	I	Clock request 2 (from peripheral) for Clock output 2
GND	D1	–	Ground
CLK_OUT2	D2	O	Clock output 2

- (1) I = Input, O = Output

Table 5-2. YFP Package Pin Assignments

	1	2
A	V _{BATT}	CLK_OUT1
B	V _{LDO}	CLK_REQ1
C	MCLK_LIN	CLK_REQ2
D	GND	CLK_OUT2

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted. ⁽¹⁾

		MIN	MAX	UNIT
V _{BATT}	Voltage range ⁽²⁾	−0.3	7	V
	Voltage range ⁽³⁾	CLK_REQ_1/2, MCLK_IN	−0.3	V _{BATT} + 0.3
		V _{LDO} , CLK_OUT_1/2 ⁽²⁾	−0.3	V _{BATT} + 0.3
I _{IK}	Input clamp current at V _{BATT} , CLK_REQ_1/2, and MCLK_IN	V _I < 0	−50	mA
I _O	Continuous output current	CLK_OUT1/2	±20	mA
	Continuous current through GND, V _{BATT} , V _{LDO}		±50	mA
T _J	Operating virtual junction temperature	−40	150	°C
T _A	Operating ambient temperature range	−40	85	°C
T _{stg}	Storage temperature range	−55	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input negative-voltage and output voltage ratings can be exceeded if the input and output current ratings are observed.
- (3) All voltage values are with respect to network ground pin.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000
		Machine Model	200

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500V HBM is possible with the necessary precautions.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

See ⁽¹⁾

		MIN	MAX	UNIT
V _{BATT}	Input voltage to internal LDO	2.3	5.5	V
V _I	Input voltage	MCLK_IN, CLK_REQ1/2	0	1.89
V _O	Output voltage	CLK_OUT1/2	0	1.8
V _{IH}	High-level input voltage	CLK_REQ1/2	1.3	1.89
V _{IL}	Low-level input voltage	CLK_REQ1/2	0	0.5
I _{OH}	High-level output current, DC current	−8		mA
I _{OL}	Low-level output current, DC current		8	mA

- (1) All unused inputs of the device must be held at V_{CC} or GND to verify proper device operation. See the [Implications of Slow or Floating CMOS Inputs](#) application note.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		CDC3RL02	UNIT
		YFP (TSSOP)	
		8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	107.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	1.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	18.1	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	4.5	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	18.1	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

over operating free air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
LDO							
V _{OUT}	LDO output voltage	I _{OUT} = 50mA		1.71	1.8	1.89	V
C _{LDO}	External load capacitance			1		10	μF
I _{OUT(SC)}	Short circuit output current	R _L = 0Ω			100		mA
I _{OUT(PK)}	Peak output current	V _{BATT} = 2.3V, V _{LDO} = V _{OUT} – 5%				100	mA
PSR	Power supply rejection	V _{BATT} = 2.3V, I _{OUT} = 2mA,	f _{IN} = 217Hz and 1kHz	60			dB
			f _{IN} = 3.25MHz	40			
t _{su}	LDO startup time	V _{BATT} = 2.3V, C _{LDO} = 1μF, CLK_REQ_n to V _{IH} = 1.71V			0.2		ms
		V _{BATT} = 5.5V, C _{LDO} = 10μF, CLK_REQ_n to V _{IH} = 1.71V				1	
POWER CONSUMPTION							
I _{SB}	Standby current	Device in standby (all V _{CLK_REQ_n} = 0V)			0.2	1	μA
I _{CCS}	Static current consumption	Device active but not switching			0.4	1	mA
I _{OB}	Output buffer average current	f _{IN} = 26MHz, C _{LOAD} = 50pF			4.2		mA
C _{PD}	Output power dissipation capacitance	f _{IN} = 26MHz				44	pF
MCLK_IN INPUT							
I _I	MCLK_IN, CLK_REQ_1/2 leakage current	V _I = V _{IH} or GND				1	μA
C _I	MCLK_IN capacitance	f _{IN} = 26MHz			4.75		pF
R _I	MCLK_IN impedance	f _{IN} = 26MHz			6		kΩ
f _{IN}	MCLK_IN frequency range			10	26	100	MHz
MCLK_IN LVCMOS SOURCE							
	Additive phase noise	f _{IN} = 26MHz, t _r /t _f ≤ 1ns	1kHz offset	–140		dBc/Hz	
			10kHz offset	–149			
			100kHz offset	–153			
			1MHz offset	–148			
	Additive jitter	f _{IN} = 26MHz, V _{PP} = 0.8V, BW = 10MHz to 5MHz		0.37		ps (rms)	
t _{DL}	MCLK_IN to CLK_OUT_n propagation delay			11		ns	
DC _L	Output duty cycle	f _{IN} = 26MHz, DC _{IN} = 50%		45%	50%	55%	

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
MCLK_IN SINUSOIDAL SOURCE							
V _{MA}	Input amplitude			0.3		1.8	V
Additive phase noise	f _{IN} = 26MHz, V _{MA} = 1.8V _{PP}	1kHz offset		–141		dBc/Hz	
		10kHz offset		–149			
		100kHz offset		–152			
		1MHz offset		–148			
	f _{IN} = 26MHz, V _{MA} = 0.8V _{PP}	1kHz offset		–139			
		10kHz offset		–146			
		100kHz offset		–150			
		1MHz offset		–146			
Additive jitter	f _{IN} = 26MHz, V _{MA} = 1.8V _{PP} , BW = 10MHz to 5MHz		0.41			ps (RMS)	
t _{DS}	MCLK_IN to CLK_OUT_1/2 propagation delay			12			ns
DC _s	Output duty cycle	f _{IN} = 26MHz, V _{MA} > 1.8V _{PP}		45%	50%	55%	
CLK_OUT_N OUTPUTS							
t _r	20% to 80% rise time	C _L = 10pF to 50pF		1		5.2	ns
t _f	20% to 80% fall time	C _L = 10pF to 50pF		1		5.2	ns
t _{sk}	Channel-to-channel skew	C _L = 10pF to 50pF (C _{L1} = C _{L2})		–0.5		0.5	ns
V _{OH}	High-level output voltage	I _{OH} = –100μA, reference to V _{LDO}		–0.1			V
		I _{OH} = –8mA		1.2			
V _{OL}	Low-level output voltage	I _{OL} = 20μA				0.2	V
		I _{OL} = 8mA				0.55	

6.6 Typical Characteristics

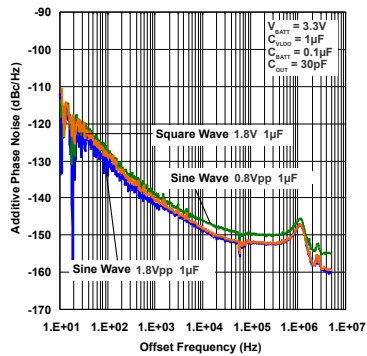


Figure 6-1. Additive Phase Noise vs Offset Frequency

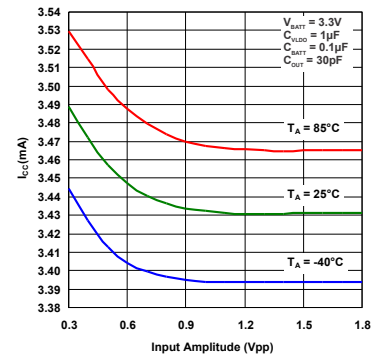


Figure 6-2. Supply Current vs Input Amplitude

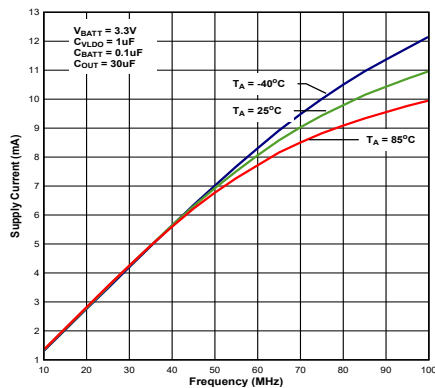


Figure 6-3. Supply Current vs Input Frequency

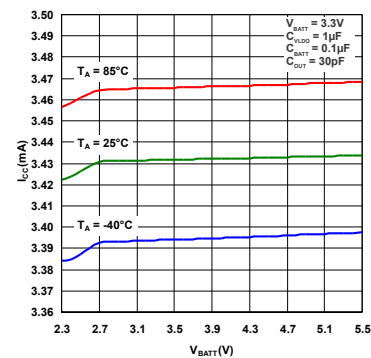


Figure 6-4. Supply Current vs Supply Voltage

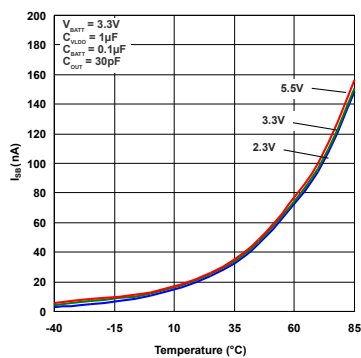


Figure 6-5. Standby Current vs Temperature

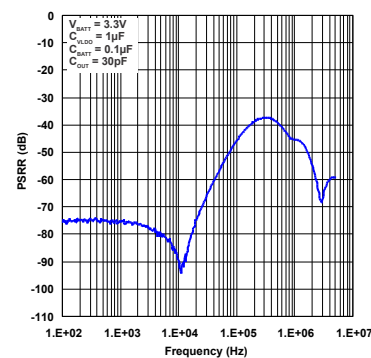


Figure 6-6. Power Supply Rejection vs Input Frequency

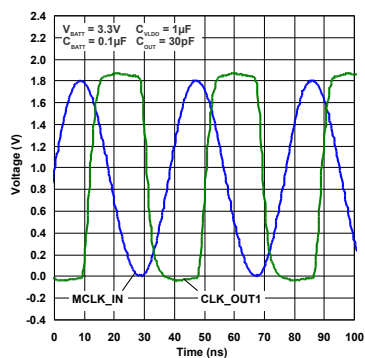


Figure 6-7. Sine-Wave Input vs Square-Wave Output

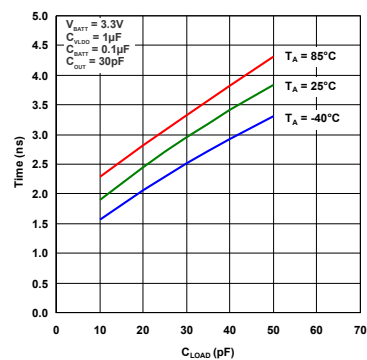


Figure 6-8. Rise Time vs Load

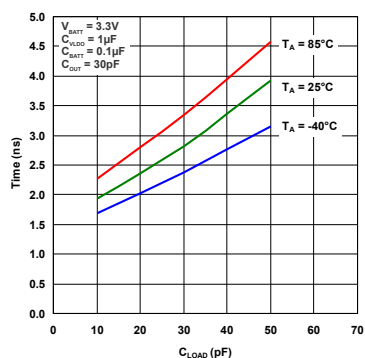


Figure 6-9. Fall Time vs Load

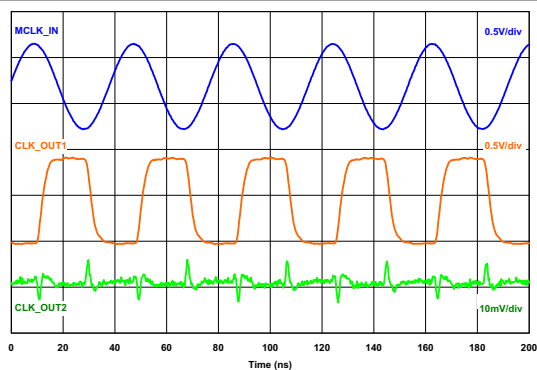


Figure 6-10. Digital Cross-Talk Scope Shot

7 Detailed Description

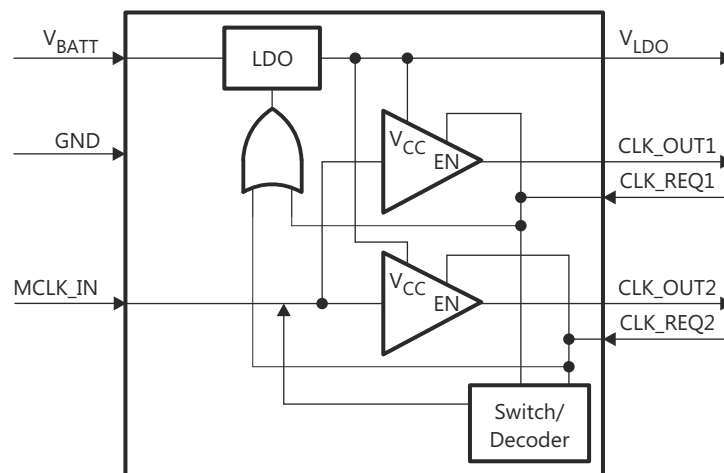
7.1 Overview

The CDC3RL02 is a two-channel clock fan-out buffer and is designed for use in portable end-equipment, such as mobile phones, that require clock buffering with minimal additive phase noise and fan-out capabilities. The device buffers a single master clock, such as a temperature compensated crystal oscillator (TCXO) to multiple peripherals. The device has two clock request inputs (CLK_REQ1 and CLK_REQ2), each of which enable a single clock output.

The CDC3RL02 accepts square or sine waves at the master clock input (MCLK_IN), eliminating the need for an AC coupling capacitor. The smallest acceptable sine wave is a 0.3V signal (peak-to-peak). CDC3RL02 is designed to offer minimal channel-to-channel skew, additive output jitter, and additive phase noise. The adaptive clock output buffers offer controlled slew-rate over a wide capacitive loading range which minimizes EMI emissions, maintains signal integrity, and minimizes ringing caused by signal reflections on the clock distribution lines.

The CDC3RL02 has an integrated Low-Drop-Out (LDO) voltage regulator which accepts input voltages from 2.3V to 5.5V and outputs 1.8V, 50mA. This 1.8V supply is externally available to provide regulated power to peripheral devices such as a TCXO.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Low Additive Noise

The CDC3RL02 features –149dBc/Hz at 10kHz offset phase noise and 0.37ps (RMS) of output jitter, to provide low noise buffered signals.

7.3.2 Regulated 1.8V Externally Available I/O Supply

The CDC3RL02 allows users to connect to the output of the internal LDO, for providing power to other ICs. For more information, refer to [LDO](#).

7.3.3 Ultra-Small 8-bump YFP 0.4mm Pitch WCSP Package

Using the ultra-small YFP package, the CDC3RL02 is very small and allows the device to be placed on a board with minimum work.

7.4 Device Functional Modes

Table 7-1 is the function table for CDC3RL02.

Table 7-1. Function Table

INPUTS			OUTPUTS	
CLK_REQ1 ⁽¹⁾	CLK_REQ2 ⁽¹⁾	MCLK_IN	CLK_OUT1	CLK_OUT2
L	L	X	L	L
L	H	CLK	L	CLK
H	L	CLK	CLK	L
H	H	CLK	CLK	CLK

(1) If a CLK_OUT is always enabled, tying the CLK_REQ pin to an external 1.8V source (not VLDO) is acceptable.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Input Clock Squarer

Figure 8-1 shows the input stage of the CDC3RL02. The input signal at MCLK_IN can be a square wave or sine wave. C_{MCLK} is an internal AC coupling capacitor that allows a direct connection from the TCXO to the CDC3RL02 without an external capacitor.

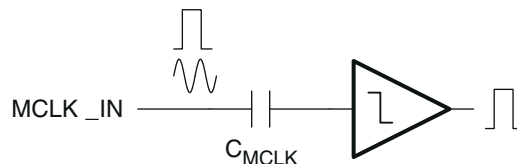


Figure 8-1. Input Stage With Internal AC Coupling Capacitor

Any external component added in the series path of the clock signal potentially adds phase noise and jitter. The error source associated with the internal decoupling capacitor is included in the specification of the CDC3RL02. The recommended clock frequency band of the CDC3RL02 is 10MHz to 80MHz for specified functionality. All performance metrics are specified at 26MHz. The lowest acceptable sinusoidal signal amplitude is 0.8V_{PP} for specified performance. Amplitudes as low as 0.3V_{PP} are acceptable but with reduced phase-noise and jitter performance.

8.1.2 Output Stage

Each output drives 1.8V LVCMOS levels. Adaptive output buffers limit the rise/fall time of the output to within 1ns to 5ns with load capacitance between 10pF and 50pF. Fast slew rates introduce EMI into the system. Each output buffer limits EMI by keeping the rise/fall time above 1ns. Slow rise/fall times can induce additive phase noise and duty cycle errors in the load device. The output buffer limits these errors by keeping the rise/fall time below 5ns. In addition, the output stage dynamically alters impedance based on the instantaneous voltage level of the output. This dynamic change limits reflections keeping the output signal monotonic during transitions. Each output is active low when not requested to avoid false clocking of the load device.

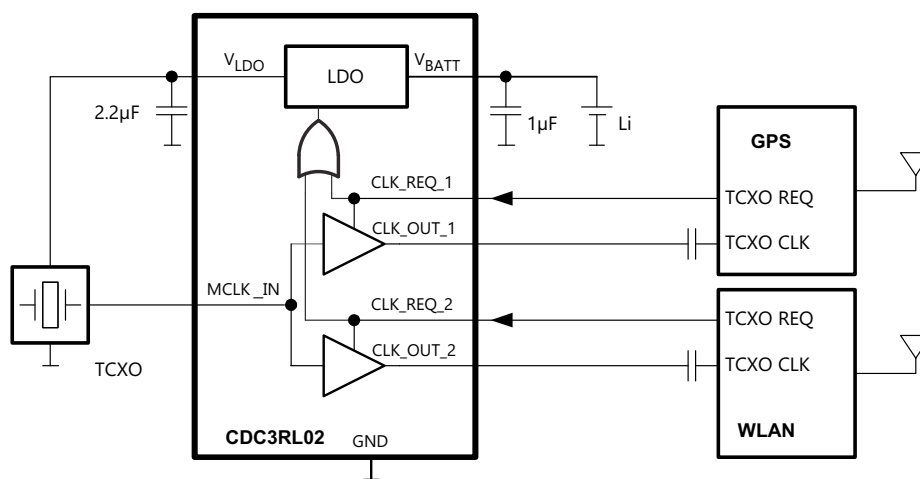
8.1.3 LDO

A low noise 1.8V LDO is integrated to provide the I/O supply for the output buffers. The LDO output is externally available to power a clock source such as a TCXO. A clean supply is provided to the clock buffers and the clock

source for optimum phase noise performance. The input range of the LDO allows the device to be powered directly from a single cell Li battery. The LDO is enabled by either of the CLK_REQ_N signals. When disabled, the device enters a low power shutdown mode consuming less than 1µA from the battery. The LDO requires an output decoupling capacitor in the range of 1µF to 10µF with an equivalent series resistance (ESR) of at least 0.1Ω for compensation and high-frequency PSR. This capacitor must stay within the specified range for capacitance and ESR over the entire operating temperature range. A ceramic capacitor can be used if a small external resistance is added in series with the capacitor to increase the effective ESR. An input bypass capacitor of 1µF or larger is recommended.

8.2 Typical Application

The CDC3RL02 is designed for use in mobile applications as shown in Figure 8-2. In this example, a single low noise TCXO system clock source is buffered to drive a mobile GPS receiver and WLAN transceiver. Each peripheral independently requests an active clock by asserting a single clock request line (CLK_REQ_1 or CLK_REQ_2). When both clock request lines are inactive, the CDC3RL02 enters a low current shutdown mode. In this mode, the LDO output, CLK_OUT_1, and CLK_OUT_2 are pulled to GND and the TCXO is not powered.



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Figure 8-2. Mobile Application

When either peripheral requests the clock, the CDC3RL02 enables the LDO and powers the TCXO. The TCXO output (square wave, sine wave, or clipped sine wave) is converted to a square wave and buffered to the requested output.

8.2.1 Design Requirements

For the typical application, the user must know the following parameters.

Table 8-1. Design Parameters

PARAMETER	DESCRIPTION	EXAMPLE VALUE
V _{BATT}	Input voltage from battery or power supply	3.7V
MCLK_IN	Input frequency from a TCXO	26MHz

8.2.2 Detailed Design Procedure

The designer must verify that all parameters are within the ranges specified in [Recommended Operating Conditions](#).

Each device which receives a clock output from the CDC3RL02 must have the CLK request pin connected to the appropriate CLK_REQ pin on the CDC3RL02. This pin enables the output buffer when a device requests the clock signal.

Control of the clock outputs is possible by using a GPIO from a controller to control the CLK_REQ pins.

If one of the outputs is unused, then tie the CLK_REQ and CLK_OUT pins to ground. If the user wants a CLK_OUT pin always enabled, tie the paired CLK_REQ pin to an external 1.8V source (not V_{LDO} because the LDO output is not enabled until at least one CLK_REQ pin is high).

8.2.3 Application Curve

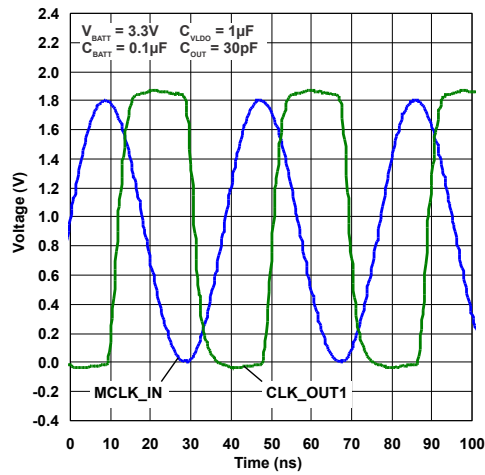


Figure 8-3. Sine Wave Input vs Output

8.3 Power Supply Recommendations

General power supply recommendations are to be considered for the CDC3RL02. These include:

- Decoupling capacitors placed close to the V_{BATT} pin of typical values (1μF)
- V_{BATT} be within the recommended voltage range

8.4 Layout

8.4.1 Layout Guidelines

To provide reliability of the device, following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors must be used on power supplies and must be placed as close as possible to the V_{BATT} pin
- Short trace-lengths must be used to avoid excessive loading
- For improved performance on the clock output lines, use a ground trace on the sides of the clock trace to minimize crosstalk and EMI

8.4.2 Layout Example

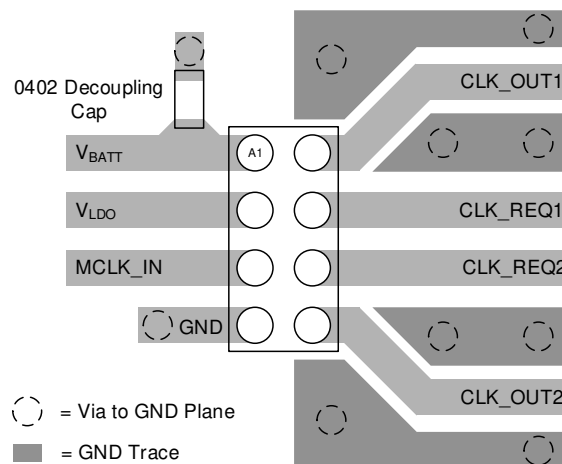


Figure 8-4. Example Layout for YFP Package

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

- Texas Instruments, [AN-2028 LMH2191 Evaluation Board](#), compatible EVM user's guide

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (November 2022) to Revision H (October 2024) Page

- | | |
|---|---|
| • Updated the numbering format for tables, figures, and cross-references throughout the document..... | 1 |
| • Updated the Electrical Characteristics for increased 100MHz MCLK_IN maximum frequency..... | 5 |

Changes from Revision F (August 2019) to Revision G (November 2022) Page

- | | |
|--|----|
| • Updated the numbering format for tables, figures, and cross-references throughout the document..... | 1 |
| • Changed MCLK_IN frequency maximum value from: 54MHz to: 80MHz..... | 5 |
| • Changed the x-axis range in Figure 6-3 | 7 |
| • Moved the <i>Power Supply Recommendations</i> and <i>Layout</i> sections to the <i>Application and Implementation</i> section..... | 13 |

Changes from Revision E (August 2018) to Revision F (August 2019) Page

- | | |
|--|---|
| • Changed MCLK_IN frequency maximum value from: 52MHz to: 54MHz..... | 5 |
|--|---|

Changes from Revision D (April 2017) to Revision E (August 2018)	Page
• Changed V_{LDO} test conditions to V_{IH} conditions in the <i>Electrical Characteristics</i> table	5
• Added a tablenote to the <i>Function Table</i>	10
• Added content to the <i>LDO</i> section	10
• Changed the last sentence in the <i>Detailed Design Procedure</i> section	12

Changes from Revision C (January 2016) to Revision D (April 2017)	Page
• Updated clock request descriptions in the <i>Pin Functions</i> table.....	3
• Added <i>Receiving Notification of Documentation Updates</i> section.....	14

Changes from Revision B (December 2015) to Revision C (January 2016)	Page
• Added the <i>Device Comparison</i>	3

Changes from Revision A (September 2015) to Revision B (November 2015)	Page
• Added <i>Thermal Information</i> table, <i>Overview</i> , <i>Feature Description</i> section, <i>Power Supply Recommendations</i> section, and <i>Layout</i> section.....	1

Changes from Revision * (November 2009) to Revision A (September 2015)	Page
• Formatted document to new standards.....	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CDC3RL02BYFPR	Active	Production	DSBGA (YFP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	4LN
CDC3RL02BYFPR.A	Active	Production	DSBGA (YFP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	4LN
CDC3RL02BYFPR.B	Active	Production	DSBGA (YFP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	4LN
CDC3RL02YFPR	Active	Production	DSBGA (YFP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	4LN
CDC3RL02YFPR.A	Active	Production	DSBGA (YFP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	4LN
CDC3RL02YFPR.B	Active	Production	DSBGA (YFP) 8	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	4LN

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDC3RL02BYFPR	DSBGA	YFP	8	3000	178.0	9.2	0.9	1.75	0.6	4.0	8.0	Q1
CDC3RL02YFPR	DSBGA	YFP	8	3000	178.0	9.2	0.9	1.75	0.6	4.0	8.0	Q1

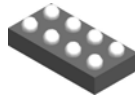
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDC3RL02BYFPR	DSBGA	YFP	8	3000	220.0	220.0	35.0
CDC3RL02YFPR	DSBGA	YFP	8	3000	220.0	220.0	35.0

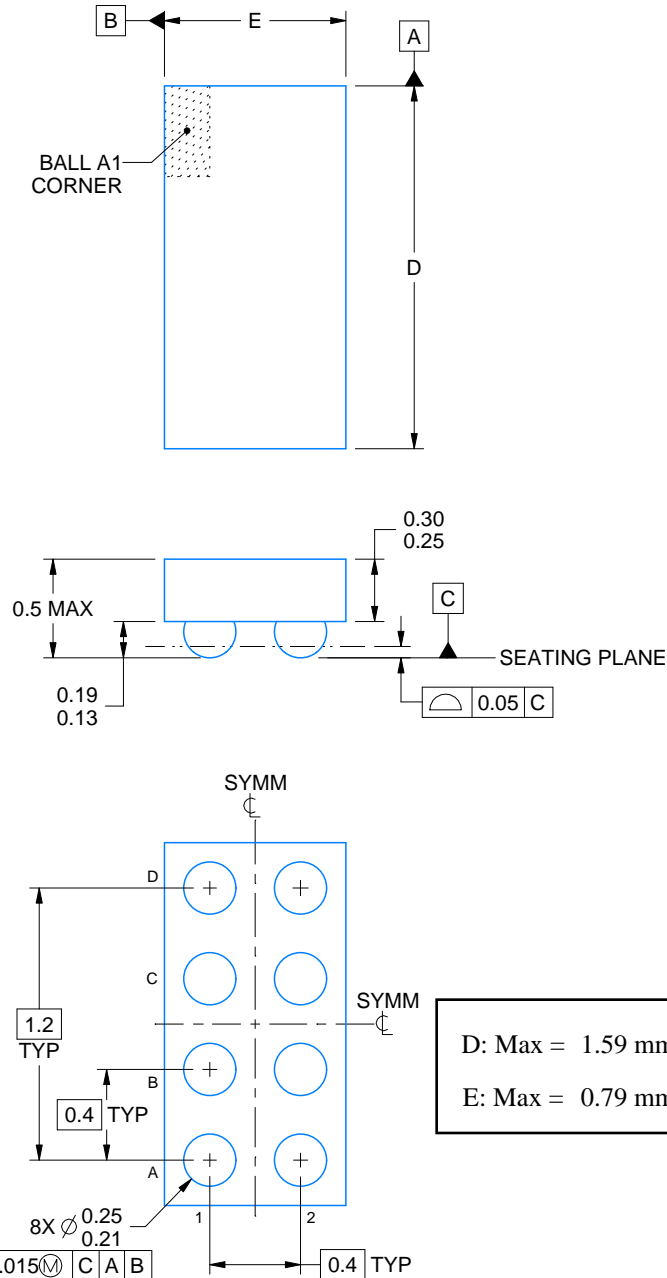
YFP0008



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



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NOTES:

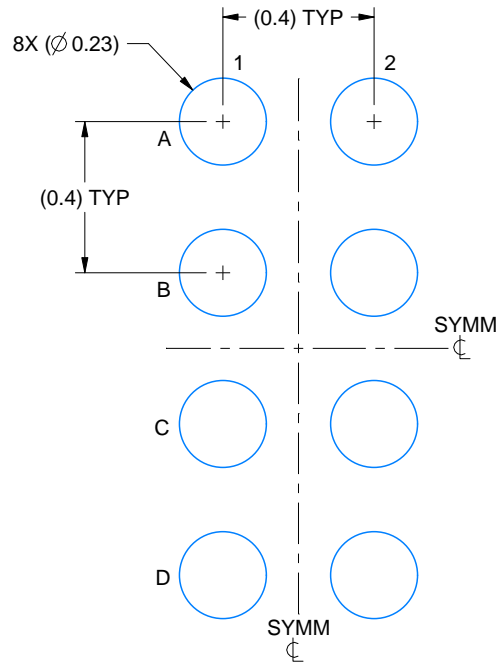
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

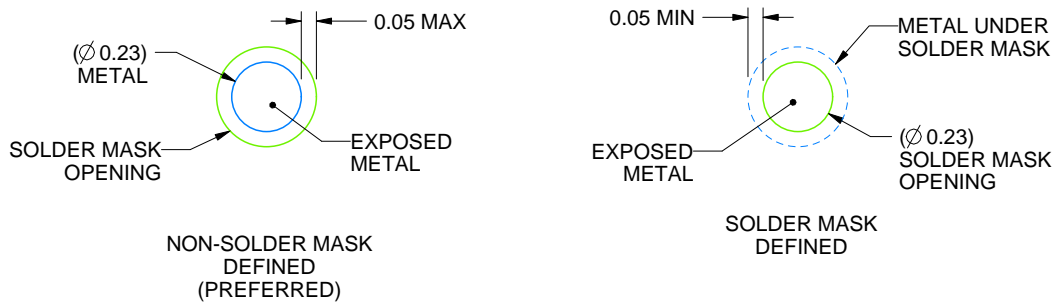
YFP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X

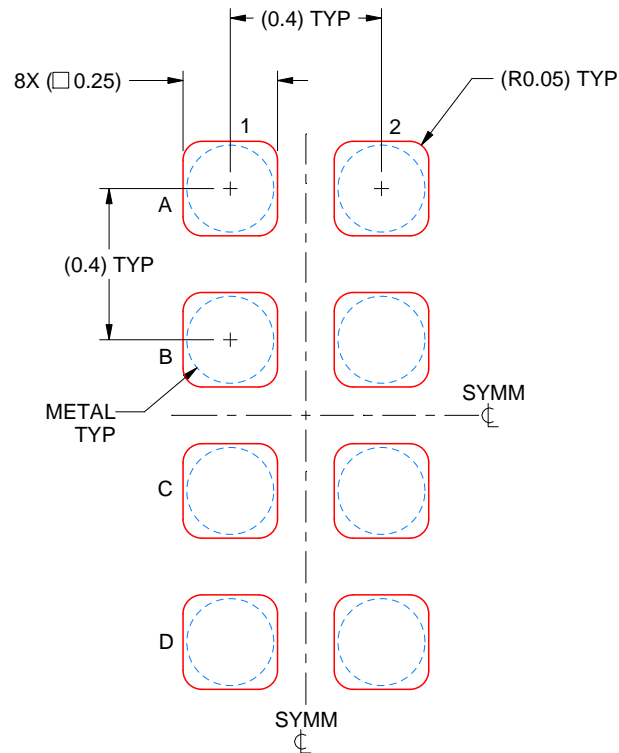


SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
 BASED ON 0.1 mm THICK STENCIL
 SCALE: 50X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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