# CSD16556Q5B 25-V N-Channel NexFET™ Power MOSFET

## 1 Features

- Extremely Low Resistance
- Ultralow $Q_g$ and $Q_{gd}$
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm × 6-mm Plastic Package

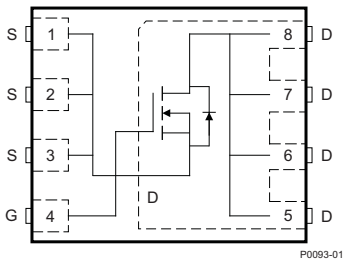
## 2 Applications

- Point-of-Load Synchronous Buck in Networking, Telecom, and Computing Systems
- Optimized for Synchronous FET Applications

## 3 Description

This 25 V, 0.9 mΩ, 5 × 6 mm SON NexFET™ power MOSFET is designed to minimize losses in synchronous rectification and other power conversion applications.

**Top View**




### Product Summary

| $T_A$ = 25°C | | TYPICAL VALUE | | UNIT |
|---|---|---|---|---|
| $V_{DS}$ | Drain-to-Source Voltage | 25 | | V |
| $Q_g$ | Gate Charge Total (4.5 V) | 36 | | nC |
| $Q_{gd}$ | Gate Charge Gate-to-Drain | 12 | | nC |
| $R_{DS(on)}$ | Drain-to-Source On-Resistance | $V_{GS}$ = 4.5 V | 1.2 | mΩ |
| | | $V_{GS}$ = 10 V | 0.9 | mΩ |
| $V_{GS(th)}$ | Threshold Voltage | 1.4 | | V |

### Ordering Information[1]

| Device | Media | Qty | Package | Ship |
|---|---|---|---|---|
| CSD16556Q5B | 13-Inch Reel | 2500 | SON 5 x 6 mm Plastic Package | Tape and Reel |
| CSD16556Q5BT | 7-Inch Reel | 250 | | |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

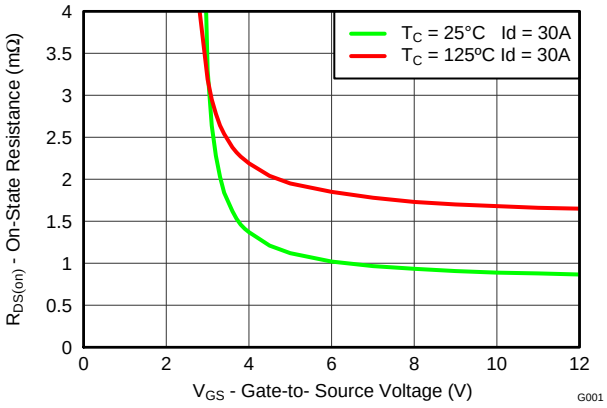
### Absolute Maximum Ratings

| $T_A$ = 25°C | | VALUE | UNIT |
|---|---|---|---|
| $V_{DS}$ | Drain-to-Source Voltage | 25 | V |
| $V_{GS}$ | Gate-to-Source Voltage | ±20 | V |
| $I_D$ | Continuous Drain Current (Package limited) | 100 | A |
| | Continuous Drain Current (Silicon limited), $T_C$ = 25°C | 263 | |
| | Continuous Drain Current[1] | 40 | A |
| $I_{DM}$ | Pulsed Drain Current[2] | 400 | A |
| $P_D$ | Power Dissipation[1] | 3.2 | W |
| | Power Dissipation, $T_C$ = 25°C | 191 | |
| $T_J$, $T_{stg}$ | Operating Junction and Storage Temperature Range | –55 to 150 | °C |
| $E_{AS}$ | Avalanche Energy, single pulse $I_D$ = 103 A, L = 0.1 mH, $R_G$ = 25 Ω | 530 | mJ |

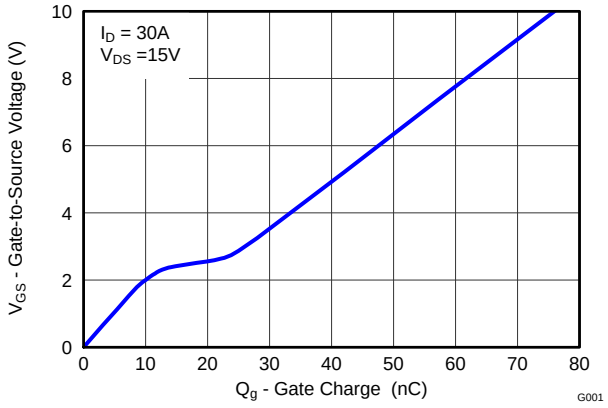
(1) Typical $R_{\theta JA}$ = 40°C/W on 1-inch$^2$ (6.45-cm$^2$), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.

(2) Max $R_{\theta JC}$ = 1.3°C/W, Pulse duration ≤100 µs, duty cycle ≤1%

**$R_{DS(on)}$ vs $V_{GS}$**




**Gate Charge**



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision B (January 2013) to Revision C** — **Page**

- Added part number to title ... 1
- Added 7 inch reel in Ordering Information ... 1
- Increase max pulsed current to 400 A ... 1
- Added line for max power dissipation with case temperature held to 25ºC ... 1
- Updated pulsed current conditions ... 1
- Updated Figure 1 to a normalized $R_{\theta JC}$ curve ... 4
- Updated the SOA in Figure 10 ... 6
- Updated the mechanical drawing and dimensions table ... 8

**Changes from Revision A (December 2012) to Revision B** — **Page**

- Changed $g_{fs}$, Transconductance TYP value From: 2 S To: 191 S ... 3

**Changes from Original (November 2012) to Revision A** — **Page**

- Changed the device from product preview to: Production ... 1

# 5 Specifications

## 5.1 Electrical Characteristics

($T_A$ = 25°C unless otherwise stated)

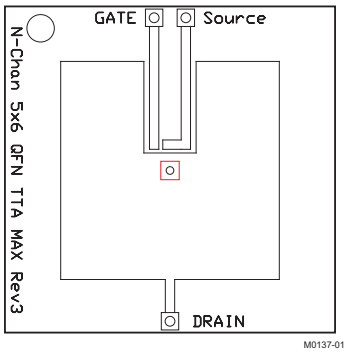
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **STATIC CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain-to-Source Voltage | $V_{GS}$ = 0 V, $I_{DS}$ = 250 µA | 25 | | | V |
| $I_{DSS}$ | Drain-to-Source Leakage Current | $V_{GS}$ = 0 V, $V_{DS}$ = 24 V | | | 1 | µA |
| $I_{GSS}$ | Gate-to-Source Leakage Current | $V_{DS}$ = 0 V, $V_{GS}$ = 20 V | | | 100 | nA |
| $V_{GS(th)}$ | Gate-to-Source Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_{DS}$ = 250 µA | 1.2 | 1.4 | 1.7 | V |
| $R_{DS(on)}$ | Drain-to-Source On-Resistance | $V_{GS}$ = 4.5 V, $I_{DS}$ = 30 A | | 1.2 | 1.5 | mΩ |
| | | $V_{GS}$ = 10 V, $I_{DS}$ = 30 A | | 0.9 | 1.07 | mΩ |
| $g_{fs}$ | Transconductance | $V_{DS}$ = 15 V, $I_{DS}$ = 30 A | | 191 | | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$ = 0 V, $V_{DS}$ = 15 V, $f$ = 1MHz | | 4750 | 6180 | pF |
| $C_{oss}$ | Output Capacitance | | | 2270 | 2950 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 220 | 280 | pF |
| $R_G$ | Series Gate Resistance | | | 0.7 | 1.4 | Ω |
| $Q_g$ | Gate Charge Total (4.5 V) | $V_{DS}$ = 15 V, $I_{DS}$ = 30 A | | 36 | 47 | nC |
| $Q_{gd}$ | Gate Charge Gate-to-Drain | | | 12 | | nC |
| $Q_{gs}$ | Gate Charge Gate-to-Source | | | 11 | | nC |
| $Q_{g(th)}$ | Gate Charge at Vth | | | 7 | | nC |
| $Q_{oss}$ | Output Charge | $V_{DS}$ = 15 V, $V_{GS}$ = 0 V | | 45 | | nC |
| $t_{d(on)}$ | Turn On Delay Time | $V_{DS}$ = 15 V, $V_{GS}$ = 4.5 V, $I_{DS}$ = 30 A,$R_G$ = 2 Ω | | 17 | | ns |
| $t_r$ | Rise Time | | | 34 | | ns |
| $t_{d(off)}$ | Turn Off Delay Time | | | 25 | | ns |
| $t_f$ | Fall Time | | | 13 | | ns |
| **DIODE CHARACTERISTICS** | | | | | | |
| $V_{SD}$ | Diode Forward Voltage | $I_{SD}$ = 30 A, $V_{GS}$ = 0 V | | 0.8 | 1 | V |
| $Q_{rr}$ | Reverse Recovery Charge | $V_{DD}$= 15 V, $I_F$ = 30 A, di/dt = 300 A/µs | | 84 | | nC |
| $t_{rr}$ | Reverse Recovery Time | | | 41 | | ns |

## 5.2 Thermal Information

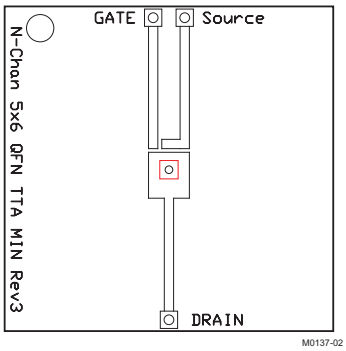
($T_A$ = 25°C unless otherwise stated)

| THERMAL METRIC | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case Thermal Resistance(1) | | | 1.3 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient Thermal Resistance(1)(2) | | | 50 | |

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch$^2$ (6.45-cm$^2$), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inches × 1.5-inches (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-inch$^2$ (6.45-cm$^2$), 2-oz. (0.071-mm thick) Cu.




Max $R_{\theta JA}$ = 50°C/W when mounted on 1 inch$^2$ (6.45 cm$^2$) of 2-oz. (0.071-mm thick) Cu.




Max $R_{\theta JA}$ = 125°C/W when mounted on a minimum pad area of 2-oz. (0.071-mm thick) Cu.

## 5.3 Typical MOSFET Characteristics

($T_A$ = 25°C unless otherwise stated)

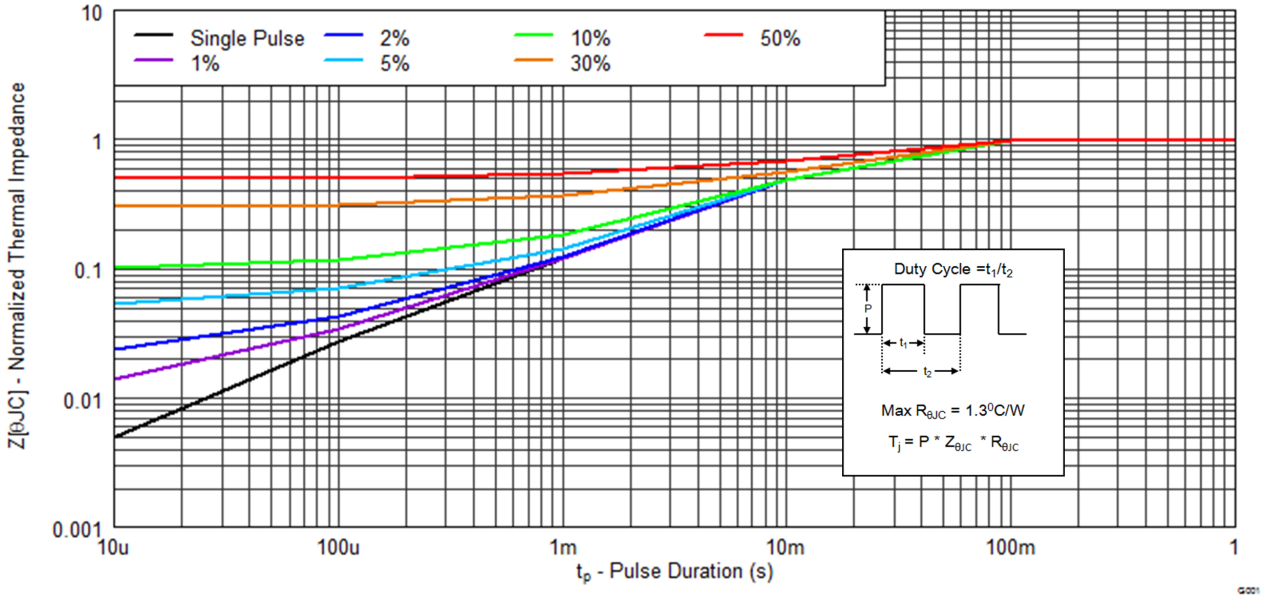



**Figure 1. Transient Thermal Impedance**

## Typical MOSFET Characteristics (continued)

($T_A$ = 25°C unless otherwise stated)

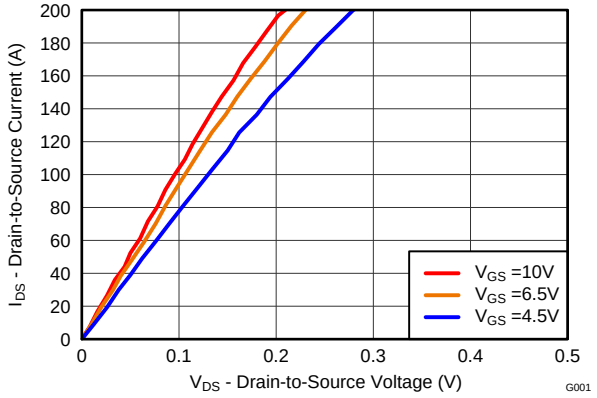



**Figure 2. Saturation Characteristics**

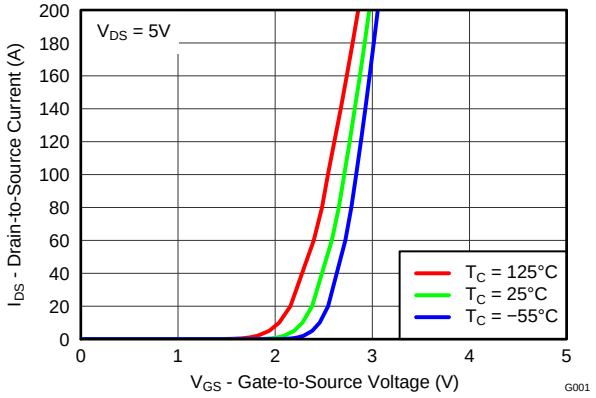



**Figure 3. Transfer Characteristics**

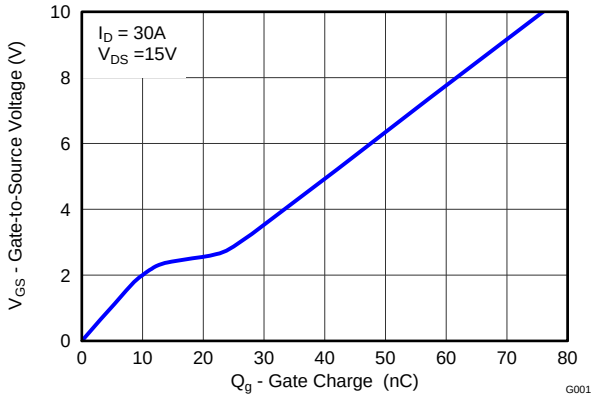



**Figure 4. Gate Charge**

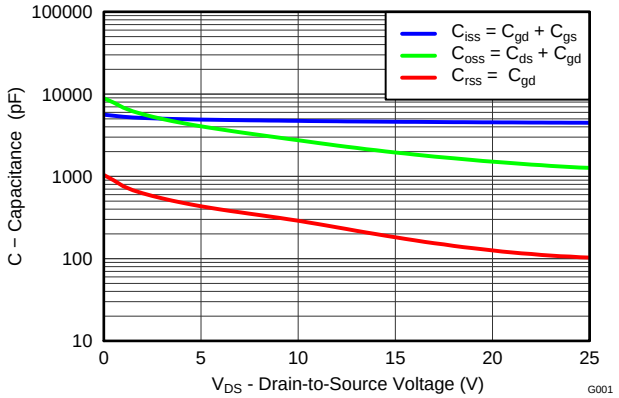



**Figure 5. Capacitance**

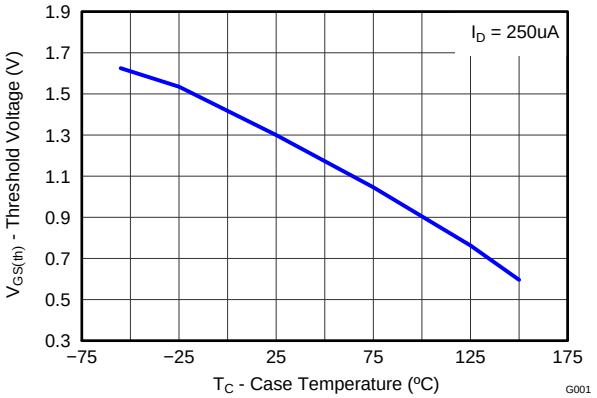



**Figure 6. Threshold Voltage vs Temperature**

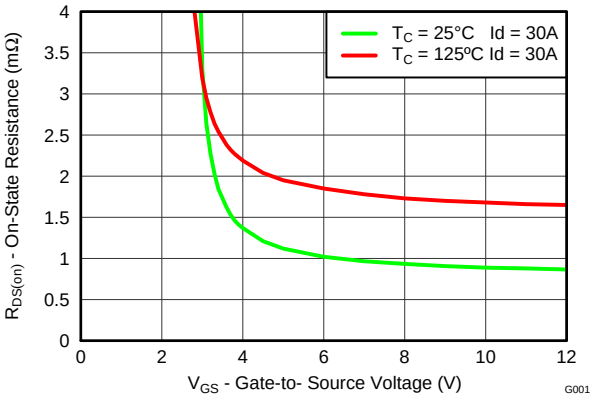



**Figure 7. On-State Resistance vs Gate-to-Source Voltage**

## Typical MOSFET Characteristics (continued)

($T_A$ = 25°C unless otherwise stated)

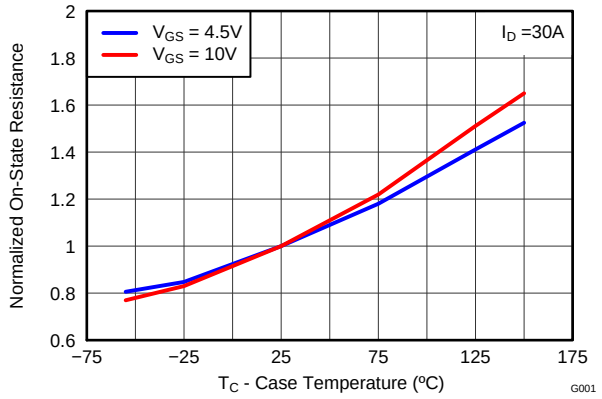



**Figure 8. Normalized On-State Resistance vs Temperature**

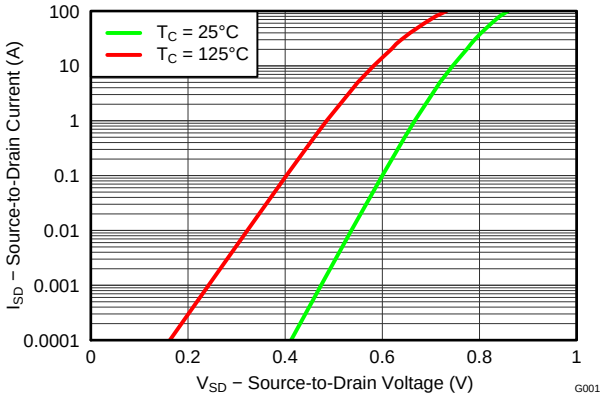



**Figure 9. Typical Diode Forward Voltage**

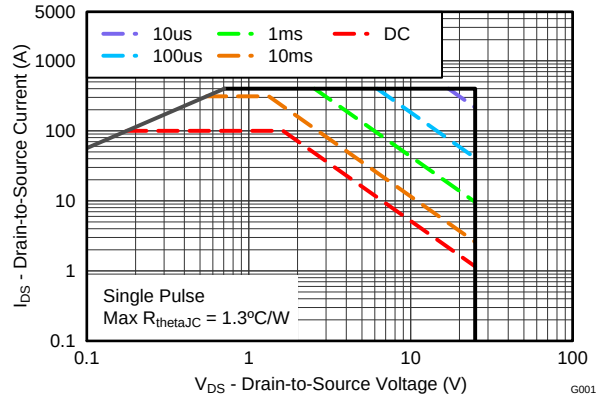



**Figure 10. Maximum Safe Operating Area (SOA)**

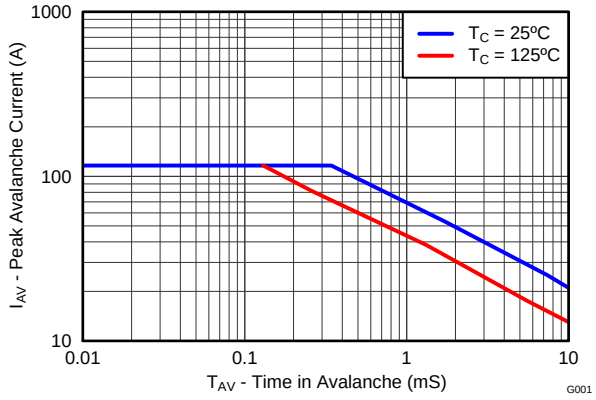



**Figure 11. Single Pulse Unclamped Inductive Switching**

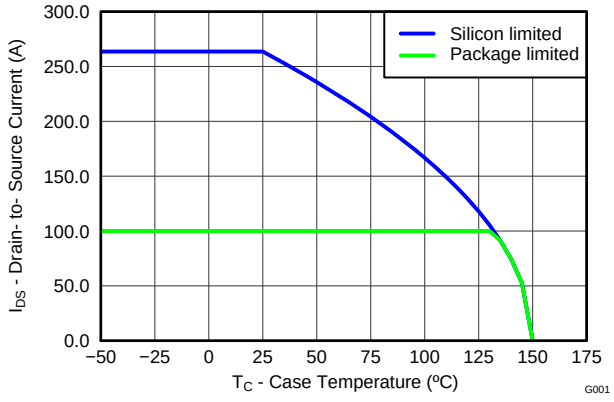



**Figure 12. Maximum Drain Current vs Temperature**

# 6 Device and Documentation Support

## 6.1 Trademarks

NexFET is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 6.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 6.3 Glossary

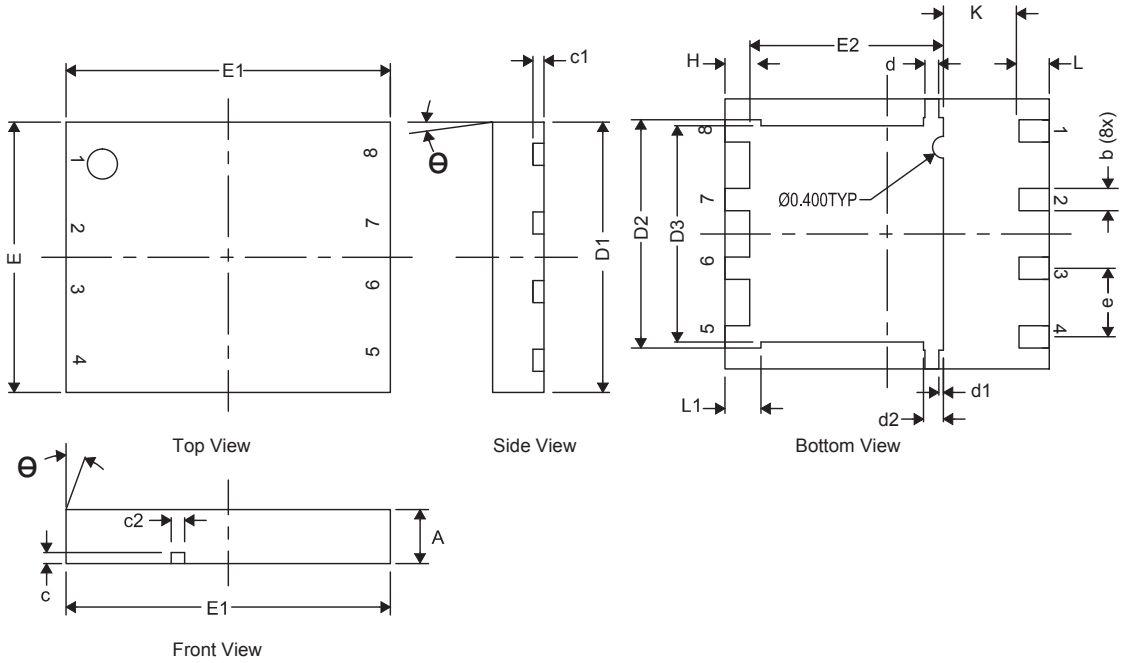
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 7 Mechanical, Packaging, and Orderable Information

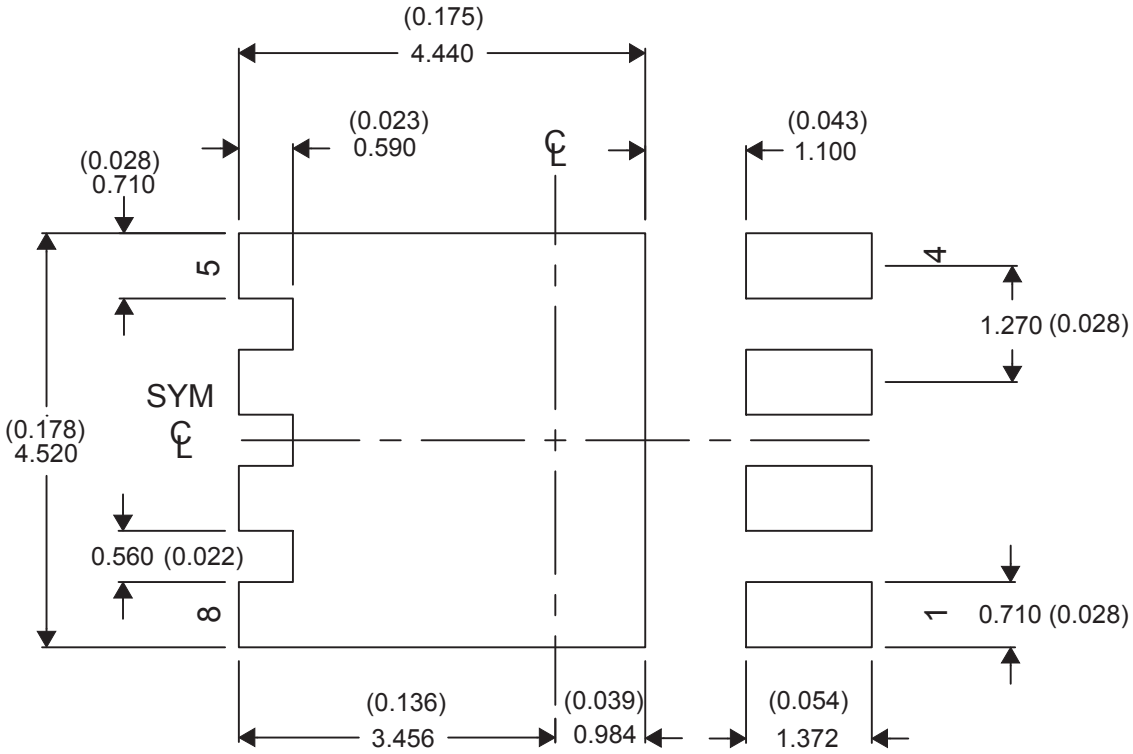
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 7.1 Q5B Package Dimensions



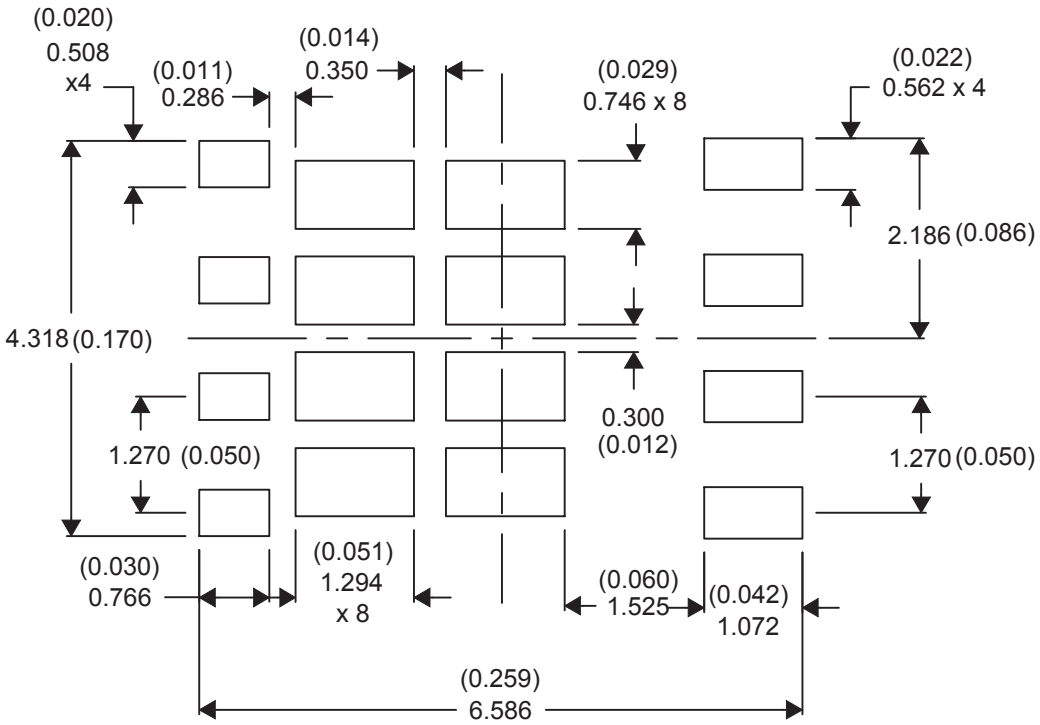

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.80 | 1.00 | 1.05 |
| b | 0.36 | 0.41 | 0.46 |
| c | 0.15 | 0.20 | 0.25 |
| c1 | 0.15 | 0.20 | 0.25 |
| c2 | 0.20 | 0.25 | 0.30 |
| D1 | 4.90 | 5.00 | 5.10 |
| D2 | 4.12 | 4.22 | 4.32 |
| D3 | 3.90 | 4.00 | 4.10 |
| d | 0.20 | 0.25 | 0.30 |
| d1 | 0.085 TYP | | |
| d2 | 0.319 | 0.369 | 0.419 |
| E | 4.90 | 5.00 | 5.10 |
| E1 | 5.90 | 6.00 | 6.10 |
| E2 | 3.48 | 3.58 | 3.68 |
| e | 1.27 TYP | | |
| H | 0.36 | 0.46 | 0.56 |
| L | 0.46 | 0.56 | 0.66 |
| L1 | 0.57 | 0.67 | 0.77 |
| θ | 0° | — | — |
| K | 1.40 TYP | | |

## 7.2 Recommended PCB Pattern

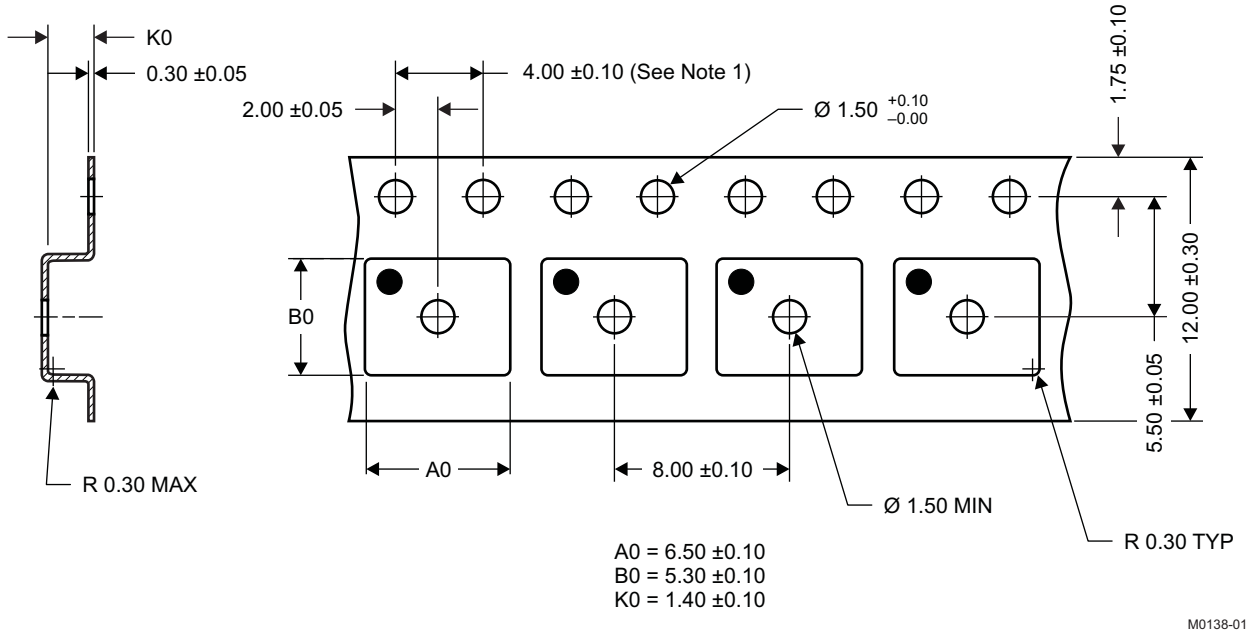



For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

## 7.3 Recommended Stencil Pattern



## 7.4 Q5B Tape and Reel Information




**Notes:**

1. 10-sprocket hole-pitch cumulative tolerance ±0.2
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified).
5. A0 and B0 measured on a plane 0.3 mm above the bottom of the pocket.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| CSD16556Q5B | Active | Production | VSON-CLIP (DNK) \| 8 | 2500 \| LARGE T&R | ROHS Exempt | SN | Level-1-260C-UNLIM | -55 to 150 | CSD16556 |
| CSD16556Q5B.B | Active | Production | VSON-CLIP (DNK) \| 8 | 2500 \| LARGE T&R | ROHS Exempt | SN | Level-1-260C-UNLIM | -55 to 150 | CSD16556 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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