



**CY54FCT827T, CY74FCT827T**  
**10-BIT BUFFERS**  
**WITH 3-STATE OUTPUTS**

SCCS034A – SEPTEMBER 1994 – REVISED OCTOBER 2001

**ORDERING INFORMATION**

T <sub>A</sub>	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
–40°C to 85°C	QSOP – Q	Tape and reel	4.4	CY74FCT827CTQCT	FCT827C	
	SOIC – SO	Tube	4.4	CY74FCT827CTSOC	FCT827C	
		Tape and reel	4.4	CY74FCT827CTSOCT		
	–40°C to 85°C	QSOP – Q	Tape and reel	8	CY74FCT827ATQCT	FCT827A
		SOIC – SO	Tube	8	CY74FCT827ATSOC	FCT827A
			Tape and reel	8	CY74FCT827ATSOCT	
–55°C to 125°C	LCC – L	Tube	9	CY54FCT827ATLMB		

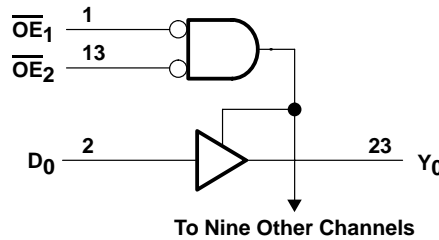
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

**FUNCTION TABLE**

INPUTS			OUTPUT Y	FUNCTION
$\overline{OE}_1$	$\overline{OE}_2$	D		
L	L	L	L	Transparent
L	L	H	H	
H	X	X	Z	3-state
X	H	X	Z	

H = High logic level, L = Low logic level, X = Don't care, Z = High-impedance state

**logic diagram (positive logic)**



Pin numbers shown are for the Q and SO packages.

**absolute maximum rating over operating free-air temperature range (unless otherwise noted)‡**

Supply voltage range to ground potential	–0.5 V to 7 V
DC input voltage range	–0.5 V to 7 V
DC output voltage range	–0.5 V to 7 V
DC output current (maximum sink current/pin)	120 mA
Package thermal impedance, $\theta_{JA}$ (see Note 1): Q package	61°C/W
SO package	46°C/W
Ambient temperature range with power applied, T <sub>A</sub>	–65°C to 135°C
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.



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## recommended operating conditions (see Note 2)

		CY54FCT827T			CY74FCT827T			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage				0.8			V
I <sub>OH</sub>	High-level output current				-12			mA
I <sub>OL</sub>	Low-level output current				32			mA
T <sub>A</sub>	Operating free-air temperature	-55			125			°C

NOTE 2: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	CY54FCT827T			CY74FCT827T			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA	-0.7			-1.2			V
	V <sub>CC</sub> = 4.75 V, I <sub>IN</sub> = -18 mA				-0.7			
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -12 mA	2.4	3.3					V
	V <sub>CC</sub> = 4.75 V	I <sub>OH</sub> = -32 mA		2				
		I <sub>OH</sub> = -15 mA		2.4	3.3			
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 32 mA	0.3			0.55			V
	V <sub>CC</sub> = 4.75 V, I <sub>OL</sub> = 64 mA				0.3			
V <sub>hys</sub>	All inputs	0.2			0.2			V
I <sub>I</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = V <sub>CC</sub>	5						μA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = V <sub>CC</sub>				5			
I <sub>IH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 2.7 V				±1			μA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 2.7 V				±1			
I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.5 V				±1			μA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 0.5 V				±1			
I <sub>OZH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 2.7 V	10						μA
	V <sub>CC</sub> = 5.25 V, V <sub>OUT</sub> = 2.7 V				10			
I <sub>OZL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 0.5 V	-10						μA
	V <sub>CC</sub> = 5.25 V, V <sub>OUT</sub> = 0.5 V				-10			
I <sub>OS</sub> ‡	V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 0 V	-60	-120	-225				mA
	V <sub>CC</sub> = 5.25 V, V <sub>OUT</sub> = 0 V				-60	-120	-225	
I <sub>off</sub>	V <sub>CC</sub> = 0 V, V <sub>OUT</sub> = 4.5 V	±1			±1			μA
I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> ≤ 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V	0.1			0.2			mA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> ≤ 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V				0.1			
ΔI <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 3.4 V§, f <sub>1</sub> = 0, Outputs open	0.5			2			mA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 3.4 V§, f <sub>1</sub> = 0, Outputs open				0.5			

† Typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

§ Per TTL-driven input (V<sub>IN</sub> = 3.4 V); all other inputs at V<sub>CC</sub> or GND



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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)**

PARAMETER	TEST CONDITIONS		CY54FCT827T		CY74FCT827T		UNIT	
			MIN	TYP†	MAX	MIN		TYP†
I <sub>CCD</sub> ††	V <sub>CC</sub> = 5.5 V, One input switching at 50% duty cycle, Outputs open, $\overline{OE}_1$ or $\overline{OE}_2 = \text{GND}$ , V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V		0.06	0.12			mA/MHz	
	V <sub>CC</sub> = 5.25 V, One input switching at 50% duty cycle, Outputs open, $\overline{OE}_1$ or $\overline{OE}_2 = \text{GND}$ , V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V				0.06	0.12		
I <sub>C</sub> #	V <sub>CC</sub> = 5.5 V, Outputs open, $\overline{OE}_1$ or $\overline{OE}_2 = \text{GND}$	One bit switching at f <sub>1</sub> = 10 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V	0.7	1.4		mA	
			V <sub>IN</sub> = 3.4 V or GND	1	2.4			
		10 bits switching at f <sub>1</sub> = 2.5 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V	1.6	3.2			
	V <sub>IN</sub> = 3.4 V or GND		4.1	13.2				
	V <sub>CC</sub> = 5.25 V, Outputs open, $\overline{OE}_1$ or $\overline{OE}_2 = \text{GND}$	One bit switching at f <sub>1</sub> = 10 MHz at 50% duty cycle	V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V			0.7		1.4
			V <sub>IN</sub> = 3.4 V or GND			1		2.4
10 bits switching at f <sub>1</sub> = 2.5 MHz at 50% duty cycle		V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V			1.6	3.2		
	V <sub>IN</sub> = 3.4 V or GND			4.1	13.2			
C <sub>i</sub>			5	10	5	10	pF	
C <sub>o</sub>			9	12	9	12	pF	

†† This parameter is derived for use in total power-supply calculations.

# I<sub>C</sub> = I<sub>CC</sub> + ΔI<sub>CC</sub> × D<sub>H</sub> × N<sub>T</sub> + I<sub>CCD</sub> (f<sub>0</sub>/2 + f<sub>1</sub> × N<sub>1</sub>)

Where:

- I<sub>C</sub> = Total supply current
- I<sub>CC</sub> = Power-supply current with CMOS input levels
- ΔI<sub>CC</sub> = Power-supply current for a TTL high input (V<sub>IN</sub> = 3.4 V)
- D<sub>H</sub> = Duty cycle for TTL inputs high
- N<sub>T</sub> = Number of TTL inputs at D<sub>H</sub>
- I<sub>CCD</sub> = Dynamic current caused by an input transition pair (HLH or LHL)
- f<sub>0</sub> = Clock frequency for registered devices, otherwise zero
- f<sub>1</sub> = Input signal frequency
- N<sub>1</sub> = Number of inputs changing at f<sub>1</sub>

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I<sub>CC</sub> formula.



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**switching characteristics over operating free-air temperature range (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST LOAD	CY54FCT827AT		CY74FCT827AT		CY74FCT827CT		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	D	Y	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω	1.5	9	1.5	8	1.5	4.4	ns
t <sub>PHL</sub>				1.5	9	1.5	8	1.5	4.4	
t <sub>PLH</sub>	D	Y	C <sub>L</sub> = 300 pF, R <sub>L</sub> = 500 Ω	1.5	17	1.5	15	1.5	10	ns
t <sub>PHL</sub>				1.5	17	1.5	15	1.5	10	
t <sub>PZH</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω	1.5	13	1.5	12	1.5	7	ns
t <sub>PZL</sub>				1.5	13	1.5	12	1.5	7	
t <sub>PZH</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 300 pF, R <sub>L</sub> = 500 Ω	1.5	25	1.5	23	1.5	14	ns
t <sub>PZL</sub>				1.5	25	1.5	23	1.5	14	
t <sub>PHZ</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 5 pF, R <sub>L</sub> = 500 Ω	1.5	9	1.5	9	1.5	5.7	ns
t <sub>PHL</sub>				1.5	9	1.5	9	1.5	5.7	
t <sub>PHZ</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω	1.5	10	1.5	10	1.5	6	ns
t <sub>PHL</sub>				1.5	10	1.5	10	1.5	6	



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**PARAMETER MEASUREMENT INFORMATION**



**LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS**

**LOAD CIRCUIT FOR 3-STATE OUTPUTS**



**VOLTAGE WAVEFORMS PULSE DURATION**



**VOLTAGE WAVEFORMS SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9224701M3A	Active	Production	LCCC (FK)   28	42   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9224701M3A
CY74FCT827ATQCT	Active	Production	SSOP (DBQ)   24	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT827A
CY74FCT827ATQCT.B	Active	Production	SSOP (DBQ)   24	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT827A
CY74FCT827ATSOC	Active	Production	SOIC (DW)   24	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT827A
CY74FCT827ATSOC.B	Active	Production	SOIC (DW)   24	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT827A
CY74FCT827ATSOCT	Active	Production	SOIC (DW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT827A
CY74FCT827ATSOCT.B	Active	Production	SOIC (DW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT827A
CY74FCT827CTQCT	Active	Production	SSOP (DBQ)   24	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT827C
CY74FCT827CTQCT.B	Active	Production	SSOP (DBQ)   24	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT827C
CY74FCT827CTSOC	Active	Production	SOIC (DW)   24	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT827C
CY74FCT827CTSOC.B	Active	Production	SOIC (DW)   24	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT827C
CY74FCT827CTSOCT	Active	Production	SOIC (DW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT827C
CY74FCT827CTSOCT.B	Active	Production	SOIC (DW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT827C

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT827ATQCT	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT827ATSOCT	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
CY74FCT827CTQCT	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT827CTSOCT	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT827ATQCT	SSOP	DBQ	24	2500	353.0	353.0	32.0
CY74FCT827ATSOCT	SOIC	DW	24	2000	350.0	350.0	43.0
CY74FCT827CTQCT	SSOP	DBQ	24	2500	353.0	353.0	32.0
CY74FCT827CTSOCT	SOIC	DW	24	2000	350.0	350.0	43.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CY74FCT827ATSOC	DW	SOIC	24	25	506.98	12.7	4826	6.6
CY74FCT827ATSOC.B	DW	SOIC	24	25	506.98	12.7	4826	6.6
CY74FCT827CTSOC	DW	SOIC	24	25	506.98	12.7	4826	6.6
CY74FCT827CTSOC.B	DW	SOIC	24	25	506.98	12.7	4826	6.6

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