

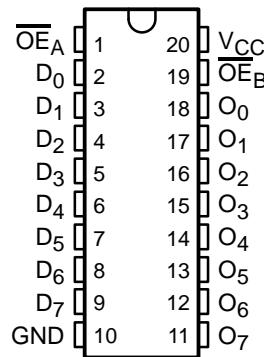
- Function, Pinout, and Drive Compatible With FCT and F Logic
- Reduced  $V_{OH}$  (Typically = 3.3 V) Versions of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- CY54FCT541T
  - 48-mA Output Sink Current
  - 12-mA Output Source Current
- CY74FCT541T
  - 64-mA Output Sink Current
  - 32-mA Output Source Current
- 3-State Outputs

#### description

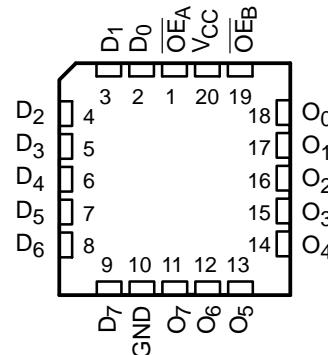
The 'FCT541T noninverting buffers/line drivers can be employed as memory address drivers, clock drivers, and bus-oriented transmitters/receivers. These devices provide speed and drive capabilities equivalent to their fastest bipolar-logic counterparts, while reducing power dissipation. The input and output voltage levels allow direct interface with TTL, NMOS, and CMOS devices without external components.

These devices are fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

**CY54FCT541T . . . D PACKAGE**  
**CY74FCT541T . . . P, Q, OR SO PACKAGE**  
**(TOP VIEW)**



**CY54FCT541T . . . L PACKAGE**  
**(TOP VIEW)**



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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 On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

**CY54FCT541T, CY74FCT541T  
8-BIT BUFFERS/LINE DRIVERS  
WITH 3-STATE OUTPUTS**

SCCS072 – OCTOBER 2001

**ORDERING INFORMATION**

TA	PACKAGE <sup>†</sup>		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QSOP – Q	Tape and reel	4.1	CY74FCT541CTQCT	FCT541C
	SOIC – SO	Tube	4.1	CY74FCT541CTS0C	FCT541C
		Tape and reel	4.1	CY74FCT541CTS0CT	
	DIP – P	Tube	4.8	CY74FCT541ATPC	CY74FCT541ATPC
	QSOP – Q	Tape and reel	4.8	CY74FCT541ATQCT	FCT541A
	SOIC – SO	Tube	4.8	CY74FCT541ATS0C	FCT541A
		Tape and reel	4.8	CY74FCT541ATS0CT	
	SOIC – SO	Tube	8	CY74FCT541TS0C	FCT541
		Tape and reel	8	CY74FCT541TS0CT	
-55°C to 125°C	CDIP – D	Tube	4.6	CY54FCT541CTDMB	
	CDIP – D	Tube	8	CY54FCT541TDMB	
	LCC – L	Tube	8	CY54FCT541TLMB	

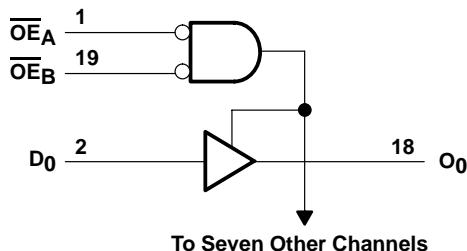
<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

**FUNCTION TABLE**

INPUTS			OUTPUT
$\overline{OE}_A$	$\overline{OE}_B$	D	O
L	L	L	L
L	L	H	H
H	H	X	Z

H = High logic level, L = Low logic level,  
X = Don't care, Z = High-impedance state

**logic diagram (positive logic)**



absolute maximum rating over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

#### **recommended operating conditions (see Note 2)**

		CY54FCT541T			CY74FCT541T			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage		2		2			V
V <sub>IL</sub>	Low-level input voltage			0.8			0.8	V
I <sub>OH</sub>	High-level output current			-12			-32	mA
I <sub>OL</sub>	Low-level output current			48			64	mA
T <sub>A</sub>	Operating free-air temperature	-55		125	-40		85	°C

NOTE 2: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation.

**CY54FCT541T, CY74FCT541T  
8-BIT BUFFERS/LINE DRIVERS  
WITH 3-STATE OUTPUTS**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	CY54FCT541T			CY74FCT541T			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA		-0.7	-1.2				V
	V <sub>CC</sub> = 4.75 V, I <sub>IN</sub> = -18 mA				-0.7	-1.2		
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -12 mA	2.4	3.3					V
	V <sub>CC</sub> = 4.75 V	I <sub>OH</sub> = -32 mA			2			
		I <sub>OH</sub> = -15 mA			2.4	3.3		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 48 mA	0.3	0.55					V
	V <sub>CC</sub> = 4.75 V, I <sub>OL</sub> = 64 mA				0.3	0.55		
V <sub>hys</sub>	All inputs	0.2			0.2			V
I <sub>I</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = V <sub>CC</sub>		5					μA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = V <sub>CC</sub>						5	
I <sub>IH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 2.7 V		±1					μA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 2.7 V						±1	
I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.5 V		±1					μA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 0.5 V						±1	
I <sub>OZH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 2.7 V	10						μA
	V <sub>CC</sub> = 5.25 V, V <sub>OUT</sub> = 2.7 V				10			
I <sub>OZL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 0.5 V		-10					μA
	V <sub>CC</sub> = 5.25 V, V <sub>OUT</sub> = 0.5 V						-10	
I <sub>OS</sub> ‡	V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 0 V	-60	-120	-225				mA
	V <sub>CC</sub> = 5.25 V, V <sub>OUT</sub> = 0 V				-60	-120	-225	
I <sub>off</sub>	V <sub>CC</sub> = 0 V, V <sub>OUT</sub> = 4.5 V		±1				±1	μA
I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> ≤ 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V	0.1	0.2					mA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> ≤ 0.2 V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V				0.1	0.2		
ΔI <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 3.4 V§, f <sub>1</sub> = 0, Outputs open	0.5	2					mA
	V <sub>CC</sub> = 5.25 V, V <sub>IN</sub> = 3.4 V§, f <sub>1</sub> = 0, Outputs open				0.5	2		
I <sub>CCD</sub> ¶	V <sub>CC</sub> = 5.5 V, 50% duty cycle, Outputs open, One bit switching at f <sub>1</sub> = 10 MHz, $\overline{OE}_A = \overline{OE}_B = GND$ or $\overline{OE}_A = GND$ and $\overline{OE}_B = V_{CC}$ , V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V		0.06	0.12				mA/ MHz
	V <sub>CC</sub> = 5.25 V, 50% duty cycle, Outputs open, One bit switching at f <sub>1</sub> = 10 MHz, $\overline{OE}_A = \overline{OE}_B = GND$ or $\overline{OE}_A = GND$ and $\overline{OE}_B = V_{CC}$ , V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V				0.06	0.12		

† Typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

§ Per TTL-driven input (V<sub>IN</sub> = 3.4 V); all other inputs at V<sub>CC</sub> or GND

¶ This parameter is derived for use in total power-supply calculations.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)**

PARAMETER	TEST CONDITIONS	CY54FCT541T			CY74FCT541T			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
$I_C^{\#}$	$V_{CC} = 5.5\text{ V}$ , Outputs open, $OE_A = OE_B = GND$ or $OE_A = GND$ and $OE_B = V_{CC}$	One bit switching at $f_1 = 10\text{ MHz}$ at 50% duty cycle	$V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$	0.7	1.4			mA
			$V_{IN} = 3.4\text{ V}$ or GND	1	2.4			
		Eight bits switching at $f_1 = 2.5\text{ MHz}$ at 50% duty cycle	$V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$	1.3	2.6			
			$V_{IN} = 3.4\text{ V}$ or GND	3.3	10.6			
	$V_{CC} = 5.25\text{ V}$ , Outputs open, $OE_A = OE_B = GND$ or $OE_A = GND$ and $OE_B = V_{CC}$	One bit switching at $f_1 = 10\text{ MHz}$ at 50% duty cycle	$V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$			0.7	1.4	
			$V_{IN} = 3.4\text{ V}$ or GND			1	2.4	
		Eight bits switching at $f_1 = 2.5\text{ MHz}$ at 50% duty cycle	$V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$			1.3	2.6	
			$V_{IN} = 3.4\text{ V}$ or GND			3.3	10.6	
$C_i$						5	10	pF
$C_o$						9	12	pF

† Typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

#  $I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

$I_C$  = Total supply current

$I_{CC}$  = Power-supply current with CMOS input levels

$\Delta I_{CC}$  = Power-supply current for a TTL high input ( $V_{IN} = 3.4\text{ V}$ )

$D_H$  = Duty cycle for TTL inputs high

$N_T$  = Number of TTL inputs at  $D_H$

$I_{CCD}$  = Dynamic current caused by an input transition pair (HLH or LHL)

$f_0$  = Clock frequency for registered devices, otherwise zero

$f_1$  = Input signal frequency

$N_1$  = Number of inputs changing at  $f_1$

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the  $I_{CC}$  formula.

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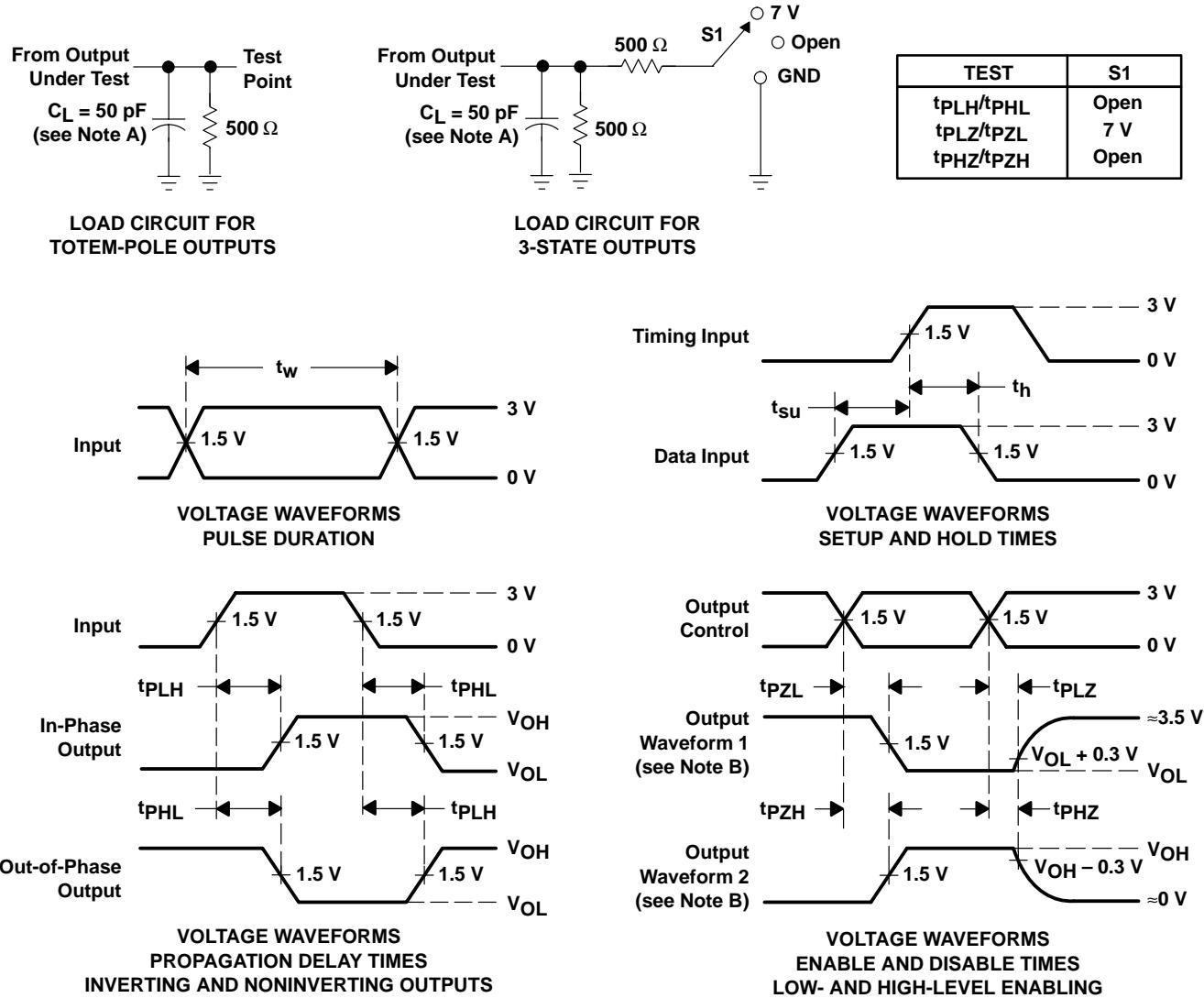
**switching characteristics over operating free-air temperature range (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY54FCT541T		CY54FCT541CT		UNIT
			MIN	MAX	MIN	MAX	
$t_{PLH}$	D	O	1.5	8	1.5	4.6	ns
$t_{PHL}$			1.5	8	1.5	4.6	
$t_{PZH}$	$\overline{OE}$	O	1.5	10.5	1.5	6.5	ns
$t_{PZL}$			1.5	10.5	1.5	6.5	
$t_{PHZ}$	$\overline{OE}$	O	1.5	10	1.5	5.7	ns
$t_{PLZ}$			1.5	10	1.5	5.7	

**switching characteristics over operating free-air temperature range (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT541T		CY74FCT541AT		CY74FCT541CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	D	O	1.5	8	1.5	4.8	1.5	4.1	ns
$t_{PHL}$			1.5	8	1.5	4.8	1.5	4.1	
$t_{PZH}$	$\overline{OE}$	O	1.5	10	1.5	6.2	1.5	5.8	ns
$t_{PZL}$			1.5	10	1.5	6.2	1.5	5.8	
$t_{PHZ}$	$\overline{OE}$	O	1.5	9.5	1.5	5.6	1.5	5.2	ns
$t_{PLZ}$			1.5	9.5	1.5	5.6	1.5	5.2	

PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9223701M2A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9223701M2A CY54FCT541TLMB
5962-9223701MRA	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9223701MR A CY54FCT541TDMB
5962-9223705MRA	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9223705MR A
CY54FCT541TDMB	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9223701MR A CY54FCT541TDMB
CY54FCT541TLMB	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9223701M2A CY54FCT541TLMB
CY74FCT541ATPC	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	CY74FCT541ATPC
CY74FCT541ATPC.B	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	CY74FCT541ATPC
CY74FCT541ATQCT	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT541A
CY74FCT541ATQCT.B	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT541A
CY74FCT541ATSOC	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT541A
CY74FCT541ATSOC.B	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT541A
CY74FCT541ATSOCT	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT541A
CY74FCT541ATSOCT.B	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT541A
CY74FCT541CTQCT	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT541C
CY74FCT541CTQCT.B	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT541C
CY74FCT541CTQCTG4	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT541C
CY74FCT541CTQCTG4.B	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT541C
CY74FCT541CTSOC	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT541C
CY74FCT541CTSOC.B	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT541C
CY74FCT541CTSOCT	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT541C
CY74FCT541CTSOCT.B	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT541C

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">CY74FCT541TQCT</a>	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT541
<a href="#">CY74FCT541TQCT.B</a>	Active	Production	SSOP (DBQ)   20	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT541
<a href="#">CY74FCT541TSOC</a>	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT541
<a href="#">CY74FCT541TSOC.B</a>	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT541

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

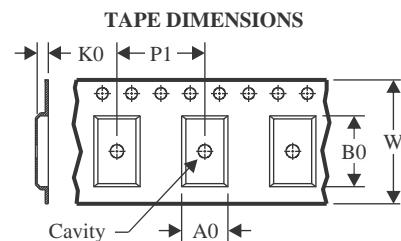
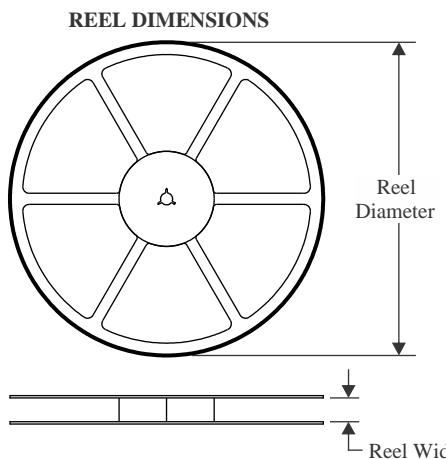
<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

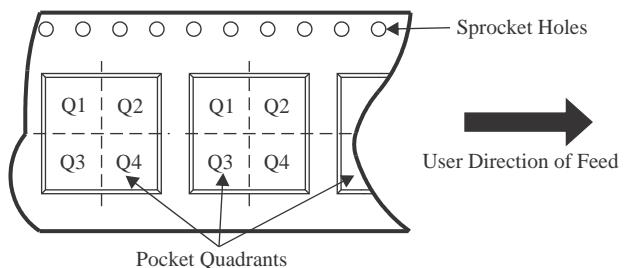
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT541ATQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT541ATSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CY74FCT541CTQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT541CTQCTG4	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT541CTSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CY74FCT541TQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT541ATQCT	SSOP	DBQ	20	2500	353.0	353.0	32.0
CY74FCT541ATSOCT	SOIC	DW	20	2000	356.0	356.0	45.0
CY74FCT541CTQCT	SSOP	DBQ	20	2500	353.0	353.0	32.0
CY74FCT541CTQCTG4	SSOP	DBQ	20	2500	353.0	353.0	32.0
CY74FCT541CTSOCT	SOIC	DW	20	2000	356.0	356.0	45.0
CY74FCT541TQCT	SSOP	DBQ	20	2500	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9223701M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
CY54FCT541TLMB	FK	LCCC	20	55	506.98	12.06	2030	NA
CY74FCT541ATPC	N	PDIP	20	20	506	13.97	11230	4.32
CY74FCT541ATPC.B	N	PDIP	20	20	506	13.97	11230	4.32
CY74FCT541ATSOC	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT541ATSOC.B	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT541CTSOC	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT541CTSOC.B	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT541TSOC	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT541TSOC.B	DW	SOIC	20	25	507	12.83	5080	6.6

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