DP83TD535-Q1 Automotive 10BASE-T1S Multidrop OA PMD Transceiver with TC10

1 Features

- IEEE 802.3cg compliant 10Mbps 10BASE-T1S
  - Multidrop or point-to-point half-duplex
  - Supports >25m cable and >16 nodes depending on channel
- Host controller interface: OA compliant 3-pin interface
- AEC-Q100 qualified for automotive applications:
  - Temperature: –40 to 125°C, T_A (grade 1)
- Single supply operation from 3.3V with 1.8/2.5/3.3V options for I/O voltage
- OA TC10 local and remote wake-up support
  - Low power wake pins: VBAT, WAKE and INH
  - OA compliant ultra-low sleep current
  - 12/24/48V direct V_{BAT} support
- Support OA TC14 PHY features when paired with appropriate external host
  - Topology discovery
  - Signal Quality Indicator (SQI)
  - Harness Defect Detection (HDD)
- Robust PHY architecture with protection and fault detection features
  - Bus wires short to GND or 48V VBAT protection
  - Overtemperature, undervoltage detection
  - ±8kV HBM ESD for MDI pins
  - ±8kV ISO10605 /IEC61000-4-2 ESD contact discharge on MDI pins
  - Extended CMV support for MDI pins
  - OA PMA, and EMC compliant

2 Applications

- Automotive:
  - Body electronics and lighting
  - Automotive gateway
  - Short range radars
  - Robotics
  - Hybrid, electric, and powertrain systems
- Industrial:
  - Factory automation
  - HVAC systems
  - Motor drives

3 Description

The DP83TD535-Q1 is 10BASE-T1S OA TC-14 compliant PMD transceiver with MDC/MDIO management port and direct VBAT supply connection. This device provides full analog front end functionality while relying on the host system for MAC, digital PHY, and management functions. This solution, similar to the CAN transceiver approach, features a simple and cost effective 3-pin clock-less interface between the host controller and the PMD transceiver chip. The device supports 10Mbps multi-drop or point-to-point half-duplex communication over unshielded twisted pair cables with extended common mode voltage (CMV) tolerance. The device communicates to a host controller or switch using OA-3pin interface. The host must have the 10BASE-T1S digital PHY incorporated.

Additionally MDC/MDIO pins allow host-independent configurations, enhanced diagnostics, and flexible power-domain design while maintaining full compatibility with the OA3-pin PMD digital interface in the MCU.

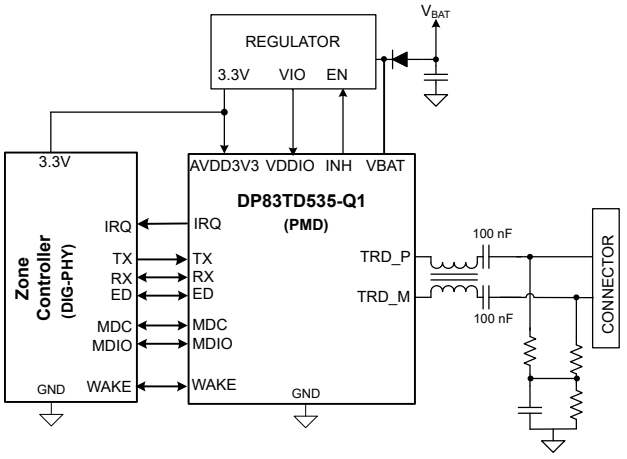
The DP83TD535-Q1 incorporates TC10 wake/sleep features to enable efficient system-level power consumption. The device supports remote wake-up over the Ethernet data line. When a wake-up event is detected, the DP83TD535-Q1 initiates system start-up by driving INH high.

The DP83TD535-Q1 is equipped with diagnostic features such as cable fault detection, undervoltage and overtemperature monitoring to streamline system development and maintenance.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
DP83TD535-Q1	VSON (DMT) (14)	4.5mm x 3mm

(1) For more information, see Section 8.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Application Diagram

ADVANCE INFORMATION

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4 Related Products

PART NUMBER	PACKAGE	10BASE-T1S PHY TYPE
DP83TD555J-Q1	QFN-20, 4mm × 4mm	OA SPI MAC-PHY transceiver
DP83TD535-Q1	VSON-14, 4.5mm × 3mm	OA PMD transceiver with MDIO and TC10 pins
DP83TD530-Q1	VSON-8, 3mm × 3mm	OA PMD transceiver

5 Pin Configuration and Functions

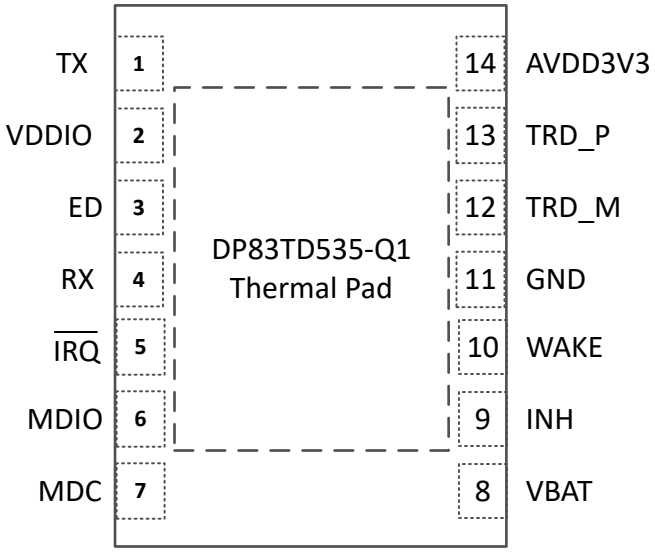

Figure 5-1. DP83TD535-Q1 Pinout (Top View)

Table 5-1. Pin Functions

PIN		TYPE[1]	Internal R_{PU}/R_{PD}	DESCRIPTION
NAME	NO.			
Media Dependent Differential Interface				
TRD_P	13	I/O	-	Positive terminal differential of transmit and receive: bidirectional differential signaling configured for 10BASE-T1S
TRD_M	12	I/O	-	Negative terminal of differential transmit and receive: bidirectional differential signaling configured for 10BASE-T1S
3-PIN Interface/Serial Management Interface Pins				
TX	1	I	R_{PU} = 15kΩ	**TX** is Ethernet Transmit Data Input
ED	3	I/O	R_{PU} = 15kΩ	**ED (Energy Detect):**Energy Detect for line activity/ collision detection **MDIO (Management Data Input and Output):**In configuration mode, this pin behaves as an MDIO bidirectional management data signal, this pin is connected to the host controller.
RX	4	I/O	R_{PU} / R_{PD}= 15kΩ	**RX:**Ethernet Receive Data Output when in non-configuration operating mode. This pin has internal a pull up resistor (15kΩ) when this pin is not used as MDC for device configuration. **MDC (Management Data Clock):**In configuration mode, this pin behaves as an MDC synchronous clock to the MDIO serial management input and output data. This pin has internal pull down (15kΩ) during configuration mode.
MDIO	6	I/O	R_{PU} = 15kΩ	This pin behaves as an MDIO (Management Data Input and Output) bidirectional management data signal that is sourced by the management station of the PHY. This pin has an internal pull-up resistor 15kΩ. In configuration mode, this pin is disabled from communicating with the device until host exists configuration mode.

Table 5-1. Pin Functions (continued)

PIN		TYPE[1]	Internal R_{PU}/R_{PD}	DESCRIPTION
NAME	NO.			
MDC	7	I	R_{PD} = 15kΩ	This pin behaves as an MDC (Management Data Clock) synchronous clock to the MDIO serial management input and output data. In configuration mode initiated by the host, this pin is disabled from communicating with the device until host exists configuration mode.
TC10 Support/Control Pins				
WAKE	9	I/O	-	**WAKE** is a bidirectional pin used for local wake as input and wake forwarding as output. This pin can be controlled by the SPI-host for local wake. A pulse of width >40µs on this pin wakes up the PMD. During low-power mode the default state of this pin is an input until a WAKE UP event occurs when this pin changes to an output for wake-forwarding. As an output the PMD drives the pin high for >40µs and transitions back to input mode. An external pull down resistance of 10kΩ is needed for proper operation.
INH	11	O - Open Drain	-	**INH** is an open drain output pin which indicates whether the device is in sleep mode. When the device is in sleep mode, the driver is turned off (Hi-Z). External pull-down resistance is needed for proper operation (10kΩ recommended). When the device is out of sleep, the INH pin transitions to high.
IRQ_N	5	O - Open Drain	R_{PU} = 40kΩ	**IRQ_N (Interrupt):**This pin behaves as an Interrupt indicator after power-up. A logic low indicates an interrupt event has occurred. This pin require an external pull up resistor (10kΩ) to VDDIO
Power/Ground				
VBAT	8	P	-	Always on Supply (Battery Supply Voltage Input 12V, 24V or 48V)
AVDD3V3	14	P	-	3.3V Device Supply Voltage
VDDIO	2	P	-	Input/output Supply Voltage (1.8V, 2.5V or 3.3V)
GND	11	G	-	Ground

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

ADVANCE INFORMATION

Table 5-2. Pin Voltage Domain

PIN NAME	VOLTAGE DOMAIN	OUTPUT VOLTAGE RANGE
TRD_P	AVDD3V3	0.5xAVD3V3 ±(0.4V - 0.6V)
TRD_M	AVDD3V3	0.5xAVD3V3 ±(0.4V - 0.6V)
TX	VDDIO	0V - VDDIO
RX	VDDIO	0V - VDDIO
ED	VDDIO	0V - VDDIO
MDIO	VDDIO	0V - VDDIO
MDC	VDDIO	0V - VDDIO
WAKE	V_{BAT}	0V - 3.3V
INH	V_{BAT}	0V - 3.3V
IRQ_N	VDDIO	0V - VDDIO

6 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

7 Revision History

DATE	REVISION	NOTES
December 2025	*	Initial Release

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/Ball material (4)	MSL rating/Peak reflow (5)	Op temp (°C)	Part marking (6)
PDP83TD535DMTTC	Active	Preproduction	VSON(DMT)|14	250 | small T&R	-	Call TI	Call TI	-40 to 125°C	P535 / TC301

(1) **Status:** For more details on status, see our product life cycle.
(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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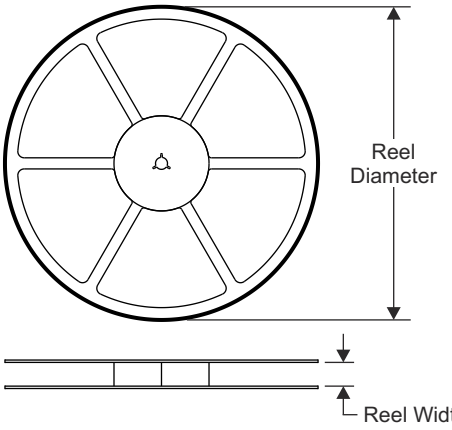
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

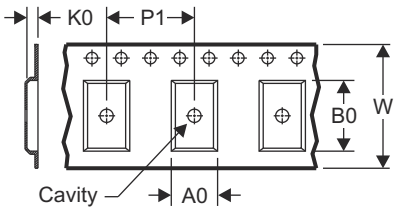
ADVANCE INFORMATION

8.1 Tape and Reel Information

REEL DIMENSIONS

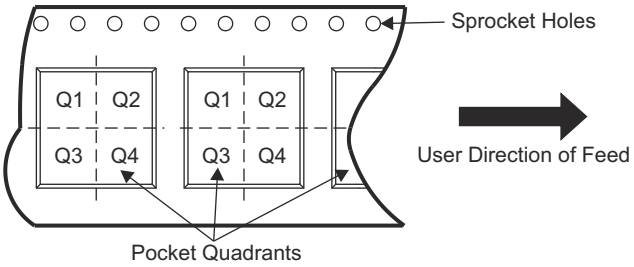


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PDP83TD535DMTTC	DMT	VSON	14	250	180	12.4	3.3	4.8	1.2	8.0	12.0	1

ADVANCE INFORMATION

ADVANCE INFORMATION

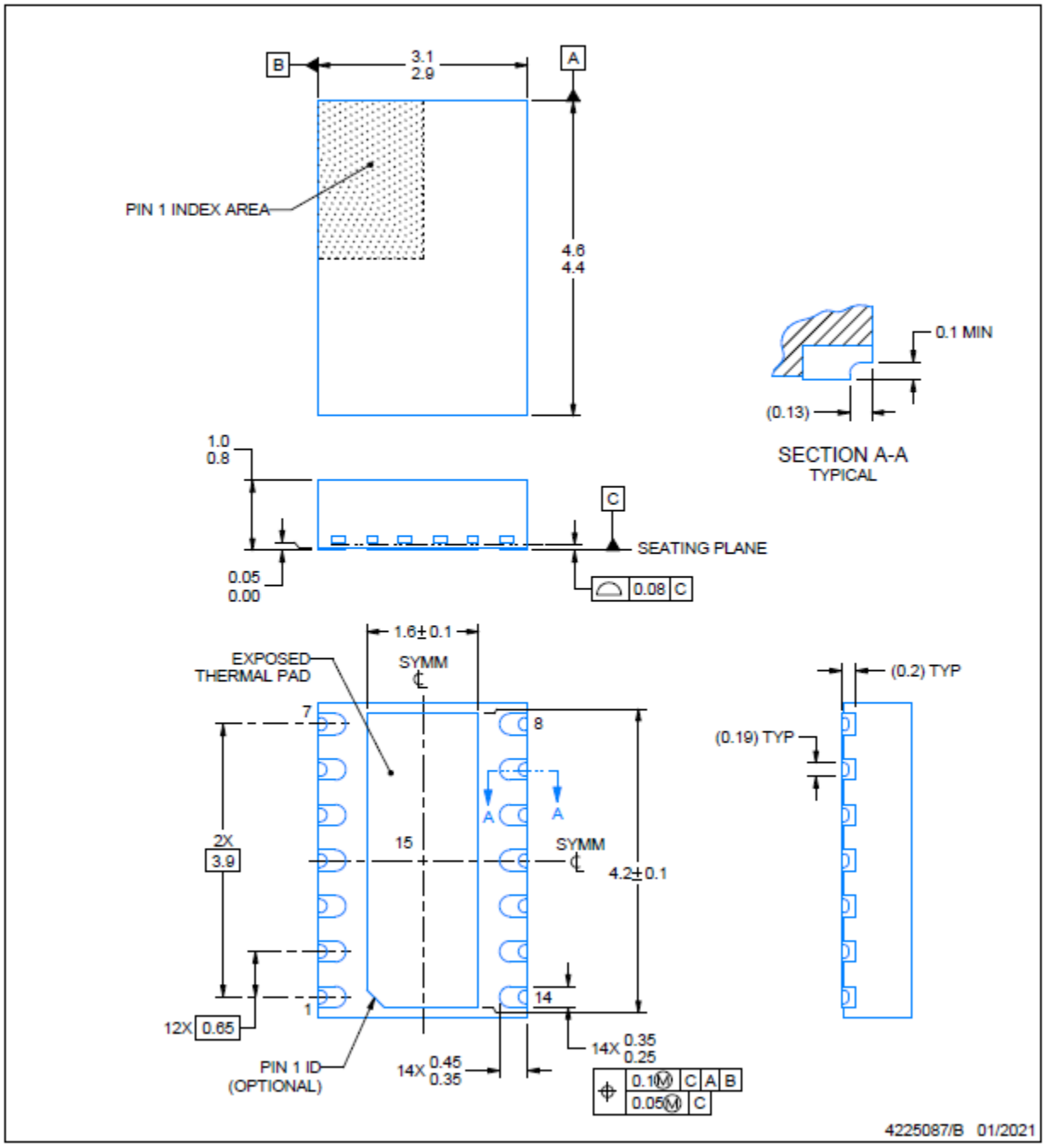
8.2 Mechanical Data

DMT0014B

PACKAGE OUTLINE

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



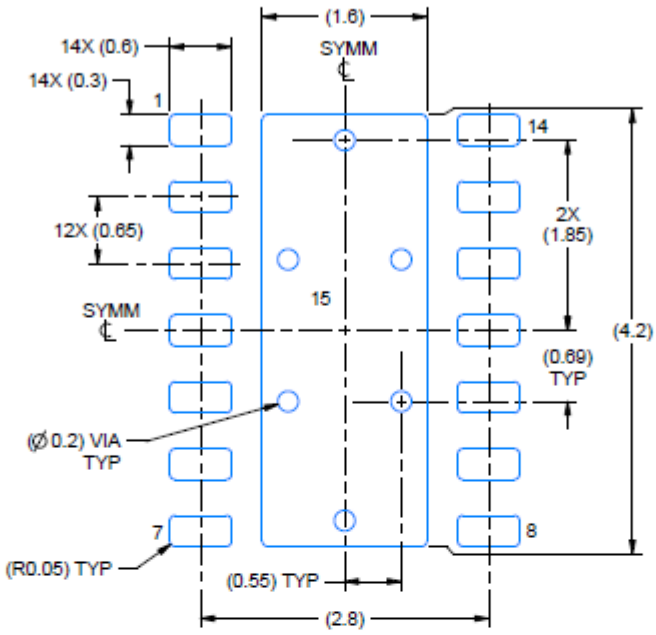
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

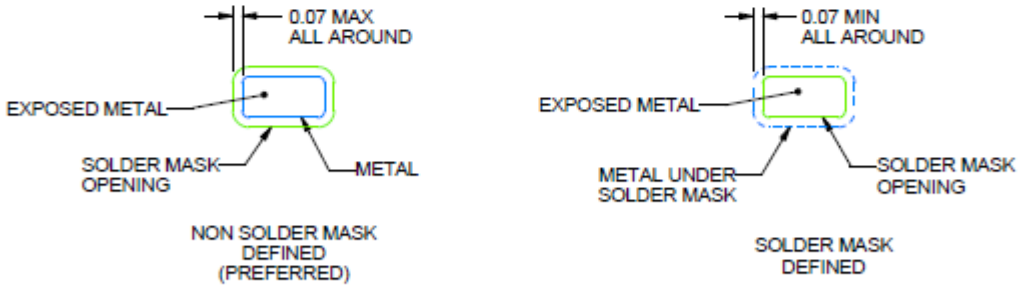
EXAMPLE BOARD LAYOUT

DMT0014B — **VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DMT0014B — **VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PDP83TD535DMTTC	Active	Preproduction	VSON (DMT) | 14	250 | SMALL T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

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GENERIC PACKAGE VIEW

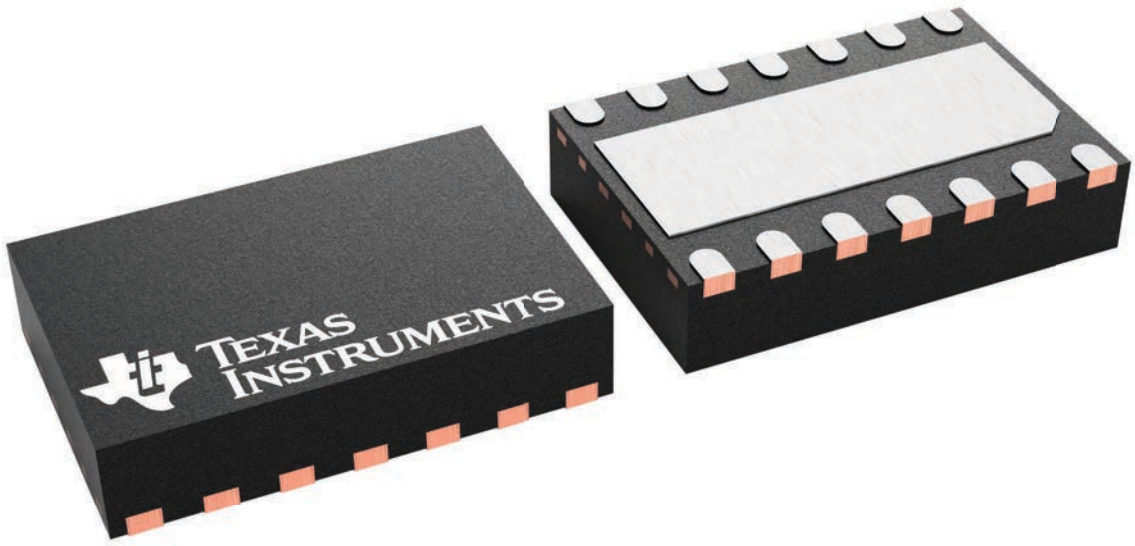
DMT 14

VSON - 0.9 mm max height

3 x 4.5, 0.65 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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