

## DRA821 Jacinto™ Processors

### 1 Features

#### Processor cores:

- Dual 64-bit Arm® Cortex®-A72 microprocessor subsystem at up to 2.0GHz
  - 1MB L2 shared cache per dual-core Cortex®-A72 cluster
  - 32KB L1 DCache and 48KB L1 ICache per A72 core
- 4× Arm® Cortex®-R5F MCUs at up to 1.0GHz with optional lockstep operation
  - 32K I-Cache, 32K D-Cache, 64K L2 TCM
  - 2× Arm® Cortex®-R5F MCUs in isolated MCU subsystem
  - 2× Arm® Cortex®-R5F MCUs in general compute partition

#### Memory subsystem:

- 1MB of On-Chip L3 RAM with ECC and coherency
  - ECC error protection
  - Shared coherent cache
  - Supports internal DMA engine
- External Memory Interface (EMIF) module with ECC
  - Supports LPDDR4 memory types that comply with the JESD209-4B specification. (No support for byte mode LPDDR4 memories, or memories with more than 17 row address bits)
  - Supports speeds up to 3200 MT/s
  - 32-bit and 16-bit data bus with inline ECC bus up to 12.8GB/s
- General-Purpose Memory Controller (GPMC)
- 512KB on-chip SRAM in MAIN domain, protected by ECC

#### Virtualization:

- Hypervisor support in Arm® Cortex®-A72
- Independent processing subsystems with Arm® Cortex®-A72, Arm® Cortex®-R5F with isolated safety MCU island
- IO virtualization support
  - Peripheral Virtualization Unit (PVU) for low latency high bandwidth peripheral traffic
- Multi-region firewall support for memory and peripheral isolation
- Virtualization support with Ethernet, PCIe, and DMA
- **Device security (on select part numbers):**
- Secure boot with secure runtime support
- Customer programmable root key, up to RSA-4K or ECC-512
- Embedded hardware security module

- Crypto hardware accelerators – PKA with ECC, AES, SHA, RNG, DES and 3DES

#### Functional Safety:

- **Functional Safety-Compliant** targeted (on select part numbers)
  - Developed for functional safety applications
  - Documentation will be available to aid ISO 26262 and IEC 61508 functional safety system design up to ASIL-D/SIL-3 targeted
  - Systematic capability up to ASIL-D/SIL-3 targeted
  - Hardware integrity up to ASIL-D/SIL-3 targeted for MCU Domain
  - Hardware integrity up to ASIL-D/SIL-3 targeted for Extended MCU (EMCU) portion of the Main Domain
  - Hardware integrity up to ASIL-B/SIL-2 targeted for remainder of the Main Domain
  - FFI isolation provided between EMCU and the remainder of the Main Domain
  - Safety-related certification
    - ISO 26262 and IEC 61508 planned
- AEC-Q100 qualified on part number variants ending in Q1
- **High-speed interfaces:**
  - Integrated Ethernet TSN/AVB switch supporting up to 4 (DRA821U4) or 2 (DRA821U2) external ports:
    - One port supports 5Gb, 10Gb USXGMII/XFI
    - All ports support 2.5Gb SGMII
    - All ports support 1Gb SGMII/RGMII
    - DRA821U4: Any single port can support QSGMII (using all 4 internal ports)
    - Non-blocking wire-rate store and forward switch
    - InterVLAN (Layer3) routing support
    - Time synchronization support with IEEE 1588(annex D,E,F)
    - TSN/AVB support for traffic scheduling, shaping
    - Port mirroring feature for debug and diagnostics
    - Policing and rate limiting support
  - One RGMII/RMII port in safety MCU island
- One PCI-Express® Gen3 controller
  - Gen1, Gen2, and Gen3 operation with auto-negotiation
  - 4× lanes
- One USB 3.1 Gen1 dual-role device subsystem
  - Supports type-C switching



- Independently configurable as USB host, USB peripheral, or USB dual-role device

**Automotive interfaces:**

- Twenty CAN-FD ports
- 12× Universal Asynchronous Receiver/Transmitter (UART)
- 11× Serial Peripheral Interfaces (SPI)
- One 8-channel ADC
- 10× Inter-Integrated Circuit ( I2C™)
- 2× Improved Inter-Integrated Circuit ( I3C®)

**Audio interfaces:**

- 3× Multichannel Audio Serial Port (McASP) modules

**Flash memory interfaces:**

- Embedded Multi Media Card ( eMMC™ 5.1) interface
  - Support speeds of up to HS400

- One Secure Digital® 3.0/Secure Digital Input Output 3.0 (SD3.0/SDIO3.0) interfaces
- One Octal SPI / Xccela™ / HyperBus™ Memory Controller (HBMC) interface
- 16-nm FinFET technology
- 17.2 mm x 17.2 mm, 0.8 mm pitch, IPC Class 3 PCB

## 2 Applications

- [Automotive gateway](#)
- [Vehicle compute](#)
- [Body control module](#)
- [Telematics control unit](#)
- [V2X/V2V](#)
- [Factory automation gateways](#)
- [Communications equipment](#)
- [Industrial transport](#)
- [Building Automation Gateway](#)

## 3 Description

Jacinto™ DRA821x processors, based on the Armv8 64-bit architecture, are optimized for gateway systems with cloud connectivity. The System-on-Chip (SoC) design reduces system-level costs and complexity through integration—notably, a system MCU, functional safety and security features, and an Ethernet switch for high-speed communication. Integrated diagnostics and functional safety features are targeted to ASIL-D and SIL 3 certification requirements. Real-time control and low-latency communication are enabled by a PCIe controller and a TSN capable Gigabit Ethernet switch.

Up to four general-purpose Arm® Cortex®-R5F subsystems can handle low-level, timing-critical processing tasks and leave the Arm® Cortex®-A72 core unencumbered for advanced and cloud-based applications.

Jacinto DRA821x processors also include the concept of the Extended MCU (eMCU) domain. This domain is a subset of the processors and peripherals on the main domain targeted at higher functional safety enablement, such as ASIL-D/SIL-3. The functional block diagram highlights which IP are included in the eMCU. For more details about eMCU and functional safety, see the ***DRA821 Safety Manual Processors Texas Instruments Jacinto™ 7 Family of Products (SPRUIX4)***.

### Package Information

| PART NUMBER             | PACKAGE <sup>(1)</sup> | PACKAGE SIZE <sup>(2)</sup> |
|-------------------------|------------------------|-----------------------------|
| DRA821U4-Q1<br>DRA821U4 | ALM (FCBGA, 433)       | 17.2 mm × 17.2 mm           |
| DRA821U2-Q1<br>DRA821U2 | ALM (FCBGA, 433)       | 17.2 mm × 17.2 mm           |
| XJ7200GB                | ALM (FCBGA, 433)       | 17.2 mm × 17.2 mm           |

(1) For more information, see [Mechanical, Packaging, and Orderable Information](#).

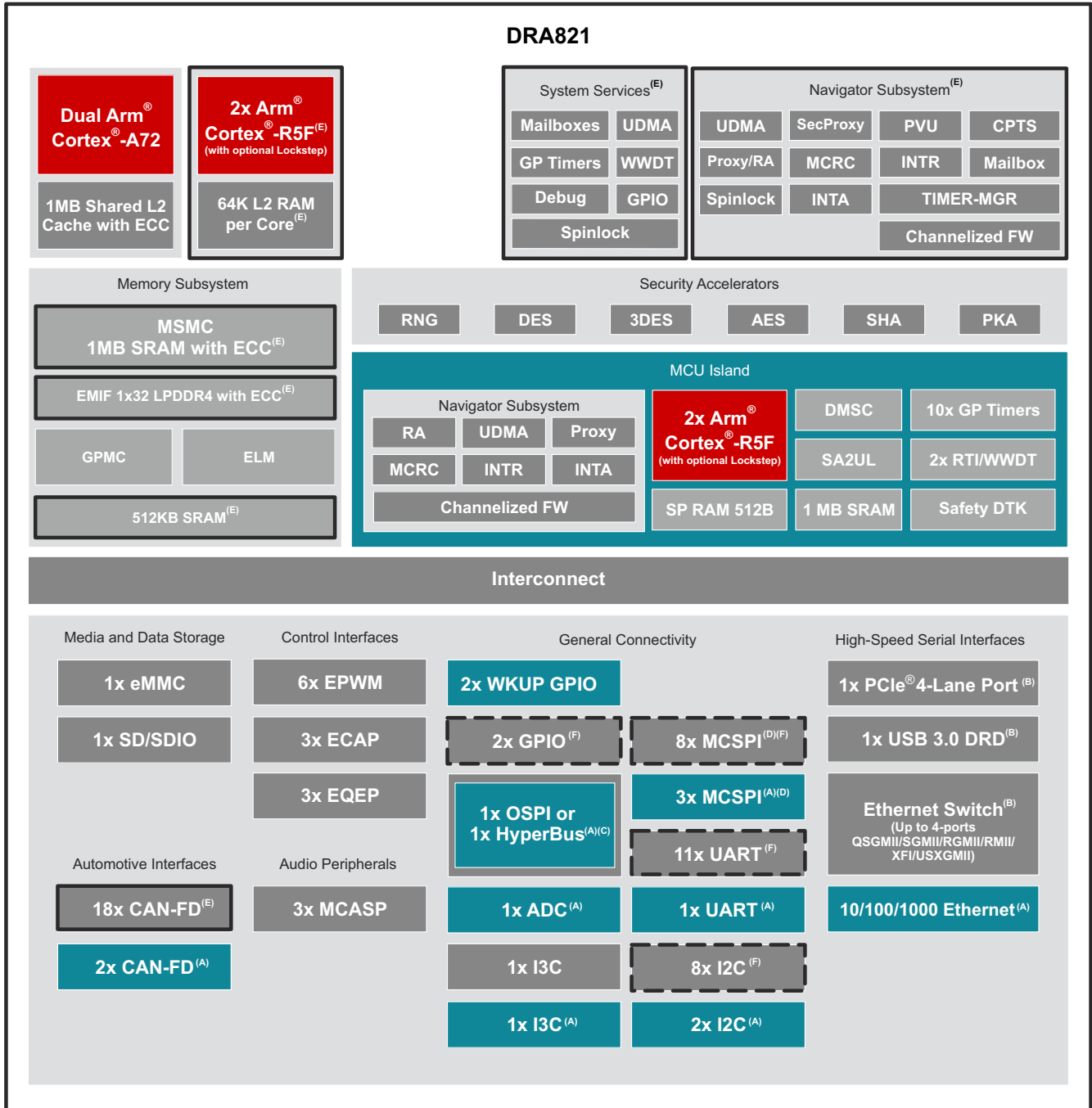
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

### 3.1 Functional Block Diagram

Figure 3-1 is functional block diagram for the device.

#### Note

To understand what device features are currently supported by TI Software Development Kits (SDKs), see the [DRA821 Software Build Sheet \( PROCESSOR-SDK-J7200 \)](#).



- A. Both WKUP and MCU domain instances are located on the MCU island but available for the full system to access.
- B. SGMII, USB3.0, and PCIE share total of four SerDes lanes. A maximum of two of the three IP (for example, SGMII and USB) can be used concurrently.
- C. Flash interface can be configured as OSPI0, or HyperBus.
- D. One port is internally connected only. Not connected to any pins.
- E. A solid black box indicates the IP is part of the Extended MCU (eMCU).
- F. A dashed black box indicates that some instances of the IP are present in the eMCU and some instances are present in the non-eMCU portion of the Main Domain.

**Figure 3-1. Functional Block Diagram**

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## 4 Device Comparison

Table 4-1 shows the features of the SoC, highlighting the differences.

### Note

To understand what device features are currently supported by TI Software Development Kits (SDKs), see the [DRA821 Software Build Sheet \( PROCESSOR-SDK-J7200 \)](#).

**Table 4-1. Device Comparison**

Same table as the unhidden one. Done to remove columns A4 and A2

| FEATURES <sup>(9)</sup>   | REFERENCE NAME | DRA821U4                                   | DRA821U2                                   |
|---|----------------|--|--|
| <b>Features</b>   |                |  |  |
| CTRLMMR_WKUP_JTAG_USER_ID[31:16]DEVICE_ID register bit field value <sup>(8) (9)</sup> |                | 0x1B90                                     | 0x1B91                                     |
| <b>PROCESSORS AND ACCELERATORS</b>  |                |  |  |
| Speed Grades (see Table 6-1)  |                | T, L, E                                    | E, C                                       |
| Arm Cortex-A72 Microprocessor Subsystem   | Arm A72        | Dual Core                                  | Dual Core                                  |
| Arm Cortex-R5F  | Arm R5F        | Quad Core                                  | Quad Core                                  |
|   | Lockstep       | Optional <sup>(5)</sup>                    | Optional <sup>(5)</sup>                    |
| Device Management Security Controller   | DMSC           | Yes  | Yes  |
| Security Accelerators   | SA             | Yes  | Yes  |
| <b>SAFETY AND SECURITY</b>  |                |  |  |
| Safety Targeted   | Safety         | Optional <sup>(5)</sup>                    | Optional <sup>(5)</sup>                    |
| Device Security   | Security       | Optional <sup>(6)</sup>                    | Optional <sup>(6)</sup>                    |
| AEC-Q100 Qualified  | Q1             | Optional <sup>(7)</sup>                    | Optional <sup>(7)</sup>                    |
| <b>PROGRAM AND DATA STORAGE</b>   |                |  |  |
| On-Chip Shared Memory (RAM) in MAIN Domain  | OCSRAM         | 512KB SRAM                                 | 512KB SRAM                                 |
| On-Chip Shared Memory (RAM) in MCU Domain   | MCU_MSRAM      | 1MB SRAM                                   | 1MB SRAM                                   |
| Multicore Shared Memory Controller  | MSMC           | 1MB (On-Chip SRAM with ECC)                | 1MB (On-Chip SRAM with ECC)                |
| LPDDR4 DDR Subsystem  | DDRSS          | Up to 8GB (16/32-bit data) with inline ECC | Up to 8GB (16/32-bit data) with inline ECC |
|   | SECDED         | 7-bit                                      | 7-bit                                      |
| General-Purpose Memory Controller   | GPMC           | Up to 1GB with ECC                         | Up to 1GB with ECC                         |
| <b>PERIPHERALS</b>  |                |  |  |
| Modular Controller Area Network Interface with Full CAN-FD Support                    | MCAN           | 20   | 20   |
| Navigator Subsystem   | NAVSS          | 2  | 2  |
| General-Purpose I/O   | GPIO           | Up to 141                                  | Up to 141                                  |
| Inter-Integrated Circuit Interface  | I2C            | 10   | 10   |
| Improved Inter-Integrated Circuit Interface   | I3C            | 2  | 2  |
| Analog-to-Digital Converter   | ADC            | 1  | 1  |
| Multichannel Serial Peripheral Interface  | MCSPi          | 11 <sup>(10)</sup>                         | 11 <sup>(10)</sup>                         |
| Multichannel Audio Serial Port  | MCASP0         | 16 Serializers                             | 16 Serializers                             |
|   | MCASP1         | 12 Serializers                             | 12 Serializers                             |
|   | MCASP2         | 6 Serializers                              | 6 Serializers                              |
| MultiMedia Card/ Secure Digital Interface   | MMCSd0         | eMMC (8-bits)                              | eMMC (8-bits)                              |
|   | MMCSd1         | SD/SDIO (4-bits)                           | SD/SDIO (4-bits)                           |
| Flash Subsystem (FSS)   | OSPI           | 8-bits <sup>(4)</sup>                      | 8-bits <sup>(4)</sup>                      |
|   | HyperBus       | Yes <sup>(4)</sup>                         | Yes <sup>(4)</sup>                         |

**Table 4-1. Device Comparison (continued)**

Same table as the unhidden one. Done to remove columns A4 and A2

| FEATURES <sup>(9)</sup>   | REFERENCE NAME | DRA821U4                        | DRA821U2                        |
|---|----------------|---------------------------------|---------------------------------|
| PCI Express Port with Integrated PHY  | PCIE           | Up to Four Lanes <sup>(1)</sup> | Up to Four Lanes <sup>(1)</sup> |
| Ethernet Interface  | CPSW2G         | 1 Port <sup>(3)</sup>           | 1 Port <sup>(3)</sup>           |
|   | CPSW5G         | 4 Ports <sup>(1) (2)</sup>      | 2 Ports <sup>(1) (2)</sup>      |
| General-Purpose Timers  | TIMER          | 30                              | 30                              |
| Enhanced Pulse-Width Modulator Module   | EPWM           | 6                               | 6                               |
| Enhanced Capture Module   | ECAP           | 3                               | 3                               |
| Enhanced Quadrature Encoder Pulse Module  | EQEP           | 3                               | 3                               |
| Universal Asynchronous Receiver and Transmitter                                   | UART           | 12                              | 12                              |
| Universal Serial Bus (USB3.1) SuperSpeed Dual-Role-Device (DRD) Ports with SS PHY | USB            | Yes <sup>(1)</sup>              | Yes <sup>(1)</sup>              |

- (1) SGMII, USB3.0, and PCIE share total of four SerDes lanes.
- (2) DRA821U4 CPSW5G supports the following instances, signals, and modes of operation:
- PORT1 **Signals:** RMII1/RGMII1/SGMII1, **Modes:** One of 5Gb, 10Gb USXGMII/XFI, 2.5 Gb SGMII/XAUI, 1Gb SGMII, 1Gb RGMII, 100Mb RMII, 5Gb QSGMII
  - PORT2 **Signals:** RMII2/RGMII2/SGMII2, **Modes:** One of 2.5 Gb SGMII/XAUI, 1Gb SGMII, 1Gb RGMII, 100Mb RMII, 5Gb QSGMII
  - PORT3 **Signals:** RMII3/RGMII3/SGMII3, **Modes:** One of 2.5 Gb SGMII/XAUI, 1Gb SGMII, 1Gb RGMII, 100Mb RMII, 5Gb QSGMII
  - PORT4 **Signals:** RMII4/RGMII4/SGMII4, **Modes:** One of 2.5 Gb SGMII/XAUI, 1Gb SGMII, 1Gb RGMII, 100Mb RMII, 5Gb QSGMII
  - QSGMII mode combines all four internal ports of the CPSW onto a single SERDES lane. Each port in this mode operates at 1-Gb full duplex
    - Any one of the port signals SGMII1:4 can be selected for this SERDES connectivity where upon the non-selected signals are unused by the CPSW

DRA821U2 CPSW5G supports a maximum of TWO RMIIn/RGMIIIn/SGMIIn ports to be used in a system. A system design can choose any TWO of the available ports between PORT1, PORT2, PORT3, or PORT4. QSGMII is not supported since QSGMII combines all four internal ports of the CPSW onto a single SERDES lane.

- (3) CPSW2G supports the following instances, signals, and modes of operation:
- PORT1 **Signals:** MCU\_RMII1/MCU\_RGMII1, **Modes:** One of 1Gb RGMII, 100Mb RMII
- (4) Flash interface can be configured as OSPI0, or HyperBus.
- (5) Safety features including R5F Lockstep and SIL/ASIL ratings are only applicable to select part number variants as indicated by the Device Type (Y) identifier in the [Section 9.1.2, Nomenclature Description Table](#).
- (6) Device security features including Secure Boot and Customer Programmable Keys are applicable to select part number variants as indicated by the Device Type (Y) identifier in the [Section 9.1.2, Nomenclature Description table](#).
- (7) AEC-Q100 qualification is applicable to select part number variants as indicated by the Automotive Designator (Q1) identifier in the [Section 9.1.2, Nomenclature Description table](#).
- (8) For more details about the CTRLMMR\_WKUP\_JTAG\_USER\_ID register and DEVICE\_ID bit field, see the device TRM.
- (9) J7200 is the base part number for the superset device. Software should constrain the features used to match the intended production device. (CTRLMMR\_WKUP\_JTAG\_USER\_ID[31:16] "DEVICE\_ID" register bit field value: **0x1B1D**.)
- (10) Two ports are internally connected only. Not connected to any pins.

## 4.1 Related Products

**Companion Products for DRA821U** Review products that are frequently purchased or used in conjunction with this product.

**Software Development Kit for DRA821 Jacinto™ Processors** Processor SDK RTOS (PSDK RTOS) can be used together with Processor SDK Linux (PSDK Linux) or Processor SDK QNX (PSDK QNX), to form a multi-processor software development platform for DRA821 SoCs within the TI's Jacinto™ Processors platform. The SDK provides a comprehensive set of software tools and components to help users develop and deploy their applications on supported J7 SoCs. PSDK RTOS and either PSDK Linux or PSDK QNX can be used together to implement various use-cases in factory and building automation, and gateway systems.

**DRA821 Evaluation Module** The J700XSOMXEVM paired with the [J721EXCP01EVM Common Processor Board](#) is an evaluation platform designed to speed up development efforts and reduce time to market for networking applications throughout automotive and industrial markets.

The EVM is supported by Processor SDK, which includes foundational drivers, compute and vision kernels, and example application frameworks and demonstrations that show you how to take advantage of the powerful, heterogeneous architecture of Jacinto 7 processors.

[Application Notes and White Paper](#) Gateway application processor with integrated system MCU.

## 5 Terminal Configuration and Functions

### 5.1 Pin Diagram

#### Note

The terms "ball", "pin", and "terminal" are used interchangeably throughout the document. An attempt is made to use "ball" only when referring to the physical package.

Figure 5-1 shows the ball locations for the 433-ball flip chip ball grid array (FCBGA) package that are used in conjunction with Table 5-1 through Table 5-107 to locate signal names and ball grid numbers.

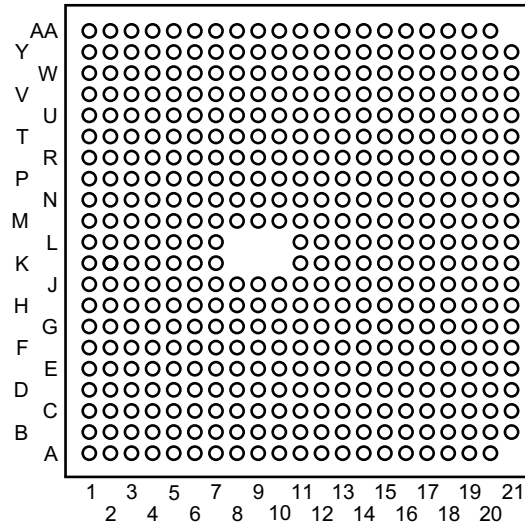


Figure 5-1. ALM FCBGA-N433 Pin Diagram (Bottom View)

## 5.2 Pin Attributes

Table 5-1. Pin Attributes

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | MUX MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUX MODE [7] | I/O VOLTAGE VALUE [8] | POWER [9]                           | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RX ACTIVE/ TX DISABLE [14] | IO RET [15] |
|-----------------|---------------|-----------------|--------------|----------|----------------------|------------------------------|-----------------------|-------------------------------------|----------|------------------|------------------------|-----------|----------------------------|-------------|
| M7              | CAP_VDDS0     | CAP_VDDS0       |              | PWR      |                      |                              |                       |                                     |          |                  |                        |           |                            |             |
| G14             | CAP_VDDS0_MCU | CAP_VDDS0_MCU   |              | PWR      |                      |                              |                       |                                     |          |                  |                        |           |                            |             |
| F9              | CAP_VDDS1_MCU | CAP_VDDS1_MCU   |              | PWR      |                      |                              |                       |                                     |          |                  |                        |           |                            |             |
| T12             | CAP_VDDS2     | CAP_VDDS2       |              | PWR      |                      |                              |                       |                                     |          |                  |                        |           |                            |             |
| F10             | CAP_VDDS2_MCU | CAP_VDDS2_MCU   |              | PWR      |                      |                              |                       |                                     |          |                  |                        |           |                            |             |
| L15             | CAP_VDDS5     | CAP_VDDS5       |              | PWR      |                      |                              |                       |                                     |          |                  |                        |           |                            |             |
| H1              | DDR0_CKN      | DDR0_CKN        |              | IO       |                      |                              | 1.1 V                 | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |          | DDR              |                        |           |                            |             |
| G1              | DDR0_CKP      | DDR0_CKP        |              | IO       |                      |                              | 1.1 V                 | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |          | DDR              |                        |           |                            |             |
| J5              | DDR0_RESETh   | DDR0_RESETh     |              | IO       |                      |                              | 1.1 V                 | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |          | DDR              |                        |           |                            |             |
| G4              | DDR0_CA0      | DDR0_CA0        |              | IO       |                      |                              | 1.1 V                 | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |          | DDR              |                        |           |                            |             |
| H3              | DDR0_CA1      | DDR0_CA1        |              | IO       |                      |                              | 1.1 V                 | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |          | DDR              |                        |           |                            |             |
| J4              | DDR0_CA2      | DDR0_CA2        |              | IO       |                      |                              | 1.1 V                 | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |          | DDR              |                        |           |                            |             |
| K1              | DDR0_CA3      | DDR0_CA3        |              | IO       |                      |                              | 1.1 V                 | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |          | DDR              |                        |           |                            |             |
| J2              | DDR0_CA4      | DDR0_CA4        |              | IO       |                      |                              | 1.1 V                 | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |          | DDR              |                        |           |                            |             |
| H5              | DDR0_CA5      | DDR0_CA5        |              | IO       |                      |                              | 1.1 V                 | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |          | DDR              |                        |           |                            |             |
| K5              | DDR0_CAL0     | DDR0_CAL0       |              | A        |                      |                              | 1.1 V                 | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |          | DDRCALR          |                        |           |                            |             |
| G2              | DDR0_CKE0     | DDR0_CKE0       |              | IO       |                      |                              | 1.1 V                 | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |          | DDR              |                        |           |                            |             |
| H2              | DDR0_CKE1     | DDR0_CKE1       |              | IO       |                      |                              | 1.1 V                 | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |          | DDR              |                        |           |                            |             |
| G3              | DDR0_CSn0_0   | DDR0_CSn0_0     |              | IO       |                      |                              | 1.1 V                 | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |          | DDR              |                        |           |                            |             |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER<br>[1] | BALL NAME<br>[2] | SIGNAL NAME<br>[3] | MUX MODE<br>[4] | TYPE<br>[5] | BALL RESET STATE<br>[6] | BALL RESET REL. MUX MODE<br>[7] | I/O VOLTAGE VALUE<br>[8] | POWER<br>[9]                              | HYS<br>[10] | BUFFER TYPE<br>[11] | PULL UP/DOWN TYPE<br>[12] | DSIS<br>[13] | RX ACTIVE/ TX DISABLE<br>[14] | IO RET<br>[15] |
|--------------------|------------------|--------------------|-----------------|-------------|-------------------------|---------------------------------|--------------------------|---|-------------|---------------------|---------------------------|--------------|-------------------------------|----------------|
| K2                 | DDR0_CSn0_1      | DDR0_CSn0_1        |                 | IO          |                         |                                 | 1.1 V                    | VDDS_DDR,<br>VDDS_DDR_C,<br>VDDS_DDR_BIAS |             | DDR                 |                           |              |                               |                |
| G5                 | DDR0_CSn1_0      | DDR0_CSn1_0        |                 | IO          |                         |                                 | 1.1 V                    | VDDS_DDR,<br>VDDS_DDR_C,<br>VDDS_DDR_BIAS |             | DDR                 |                           |              |                               |                |
| J3                 | DDR0_CSn1_1      | DDR0_CSn1_1        |                 | IO          |                         |                                 | 1.1 V                    | VDDS_DDR,<br>VDDS_DDR_C,<br>VDDS_DDR_BIAS |             | DDR                 |                           |              |                               |                |
| A3                 | DDR0_DM0         | DDR0_DM0           |                 | IO          |                         |                                 | 1.1 V                    | VDDS_DDR,<br>VDDS_DDR_C,<br>VDDS_DDR_BIAS |             | DDR                 |                           |              |                               |                |
| E4                 | DDR0_DM1         | DDR0_DM1           |                 | IO          |                         |                                 | 1.1 V                    | VDDS_DDR,<br>VDDS_DDR_C,<br>VDDS_DDR_BIAS |             | DDR                 |                           |              |                               |                |
| N1                 | DDR0_DM2         | DDR0_DM2           |                 | IO          |                         |                                 | 1.1 V                    | VDDS_DDR,<br>VDDS_DDR_C,<br>VDDS_DDR_BIAS |             | DDR                 |                           |              |                               |                |
| R4                 | DDR0_DM3         | DDR0_DM3           |                 | IO          |                         |                                 | 1.1 V                    | VDDS_DDR,<br>VDDS_DDR_C,<br>VDDS_DDR_BIAS |             | DDR                 |                           |              |                               |                |
| B4                 | DDR0_DQ0         | DDR0_DQ0           |                 | IO          |                         |                                 | 1.1 V                    | VDDS_DDR,<br>VDDS_DDR_C,<br>VDDS_DDR_BIAS |             | DDR                 |                           |              |                               |                |
| A4                 | DDR0_DQ1         | DDR0_DQ1           |                 | IO          |                         |                                 | 1.1 V                    | VDDS_DDR,<br>VDDS_DDR_C,<br>VDDS_DDR_BIAS |             | DDR                 |                           |              |                               |                |
| C4                 | DDR0_DQ2         | DDR0_DQ2           |                 | IO          |                         |                                 | 1.1 V                    | VDDS_DDR,<br>VDDS_DDR_C,<br>VDDS_DDR_BIAS |             | DDR                 |                           |              |                               |                |
| C1                 | DDR0_DQ3         | DDR0_DQ3           |                 | IO          |                         |                                 | 1.1 V                    | VDDS_DDR,<br>VDDS_DDR_C,<br>VDDS_DDR_BIAS |             | DDR                 |                           |              |                               |                |
| C3                 | DDR0_DQ4         | DDR0_DQ4           |                 | IO          |                         |                                 | 1.1 V                    | VDDS_DDR,<br>VDDS_DDR_C,<br>VDDS_DDR_BIAS |             | DDR                 |                           |              |                               |                |
| C2                 | DDR0_DQ5         | DDR0_DQ5           |                 | IO          |                         |                                 | 1.1 V                    | VDDS_DDR,<br>VDDS_DDR_C,<br>VDDS_DDR_BIAS |             | DDR                 |                           |              |                               |                |
| A2                 | DDR0_DQ6         | DDR0_DQ6           |                 | IO          |                         |                                 | 1.1 V                    | VDDS_DDR,<br>VDDS_DDR_C,<br>VDDS_DDR_BIAS |             | DDR                 |                           |              |                               |                |
| B3                 | DDR0_DQ7         | DDR0_DQ7           |                 | IO          |                         |                                 | 1.1 V                    | VDDS_DDR,<br>VDDS_DDR_C,<br>VDDS_DDR_BIAS |             | DDR                 |                           |              |                               |                |
| D1                 | DDR0_DQ8         | DDR0_DQ8           |                 | IO          |                         |                                 | 1.1 V                    | VDDS_DDR,<br>VDDS_DDR_C,<br>VDDS_DDR_BIAS |             | DDR                 |                           |              |                               |                |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | MUX MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUX MODE [7] | I/O VOLTAGE VALUE [8] | POWER [9]                           | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RX ACTIVE/ TX DISABLE [14] | IO RET [15] |
|-----------------|---------------|-----------------|--------------|----------|----------------------|------------------------------|-----------------------|-------------------------------------|----------|------------------|------------------------|-----------|----------------------------|-------------|
| D2              | DDR0_DQ9      | DDR0_DQ9        |              | IO       |                      |                              | 1.1 V                 | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |          | DDR              |                        |           |                            |             |
| F2              | DDR0_DQ10     | DDR0_DQ10       |              | IO       |                      |                              | 1.1 V                 | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |          | DDR              |                        |           |                            |             |
| E3              | DDR0_DQ11     | DDR0_DQ11       |              | IO       |                      |                              | 1.1 V                 | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |          | DDR              |                        |           |                            |             |
| F3              | DDR0_DQ12     | DDR0_DQ12       |              | IO       |                      |                              | 1.1 V                 | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |          | DDR              |                        |           |                            |             |
| F4              | DDR0_DQ13     | DDR0_DQ13       |              | IO       |                      |                              | 1.1 V                 | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |          | DDR              |                        |           |                            |             |
| D4              | DDR0_DQ14     | DDR0_DQ14       |              | IO       |                      |                              | 1.1 V                 | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |          | DDR              |                        |           |                            |             |
| F5              | DDR0_DQ15     | DDR0_DQ15       |              | IO       |                      |                              | 1.1 V                 | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |          | DDR              |                        |           |                            |             |
| K4              | DDR0_DQ16     | DDR0_DQ16       |              | IO       |                      |                              | 1.1 V                 | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |          | DDR              |                        |           |                            |             |
| L4              | DDR0_DQ17     | DDR0_DQ17       |              | IO       |                      |                              | 1.1 V                 | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |          | DDR              |                        |           |                            |             |
| M4              | DDR0_DQ18     | DDR0_DQ18       |              | IO       |                      |                              | 1.1 V                 | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |          | DDR              |                        |           |                            |             |
| L3              | DDR0_DQ19     | DDR0_DQ19       |              | IO       |                      |                              | 1.1 V                 | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |          | DDR              |                        |           |                            |             |
| L2              | DDR0_DQ20     | DDR0_DQ20       |              | IO       |                      |                              | 1.1 V                 | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |          | DDR              |                        |           |                            |             |
| L1              | DDR0_DQ21     | DDR0_DQ21       |              | IO       |                      |                              | 1.1 V                 | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |          | DDR              |                        |           |                            |             |
| M3              | DDR0_DQ22     | DDR0_DQ22       |              | IO       |                      |                              | 1.1 V                 | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |          | DDR              |                        |           |                            |             |
| N2              | DDR0_DQ23     | DDR0_DQ23       |              | IO       |                      |                              | 1.1 V                 | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |          | DDR              |                        |           |                            |             |
| R3              | DDR0_DQ24     | DDR0_DQ24       |              | IO       |                      |                              | 1.1 V                 | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |          | DDR              |                        |           |                            |             |

Table 5-1. Pin Attributes (continued)

| BALL NUMBER<br>[1] | BALL NAME<br>[2] | SIGNAL NAME<br>[3] | MUX MODE<br>[4] | TYPE<br>[5] | BALL RESET STATE<br>[6] | BALL RESET REL. MUX MODE<br>[7] | I/O VOLTAGE VALUE<br>[8] | POWER<br>[9]                        | HYS<br>[10] | BUFFER TYPE<br>[11] | PULL UP/DOWN TYPE<br>[12] | DSIS<br>[13] | RX ACTIVE/ TX DISABLE<br>[14] | IO RET<br>[15] |
|--------------------|------------------|--------------------|-----------------|-------------|-------------------------|---------------------------------|--------------------------|-------------------------------------|-------------|---------------------|---------------------------|--------------|-------------------------------|----------------|
| T1                 | DDR0_DQ25        | DDR0_DQ25          |                 | IO          |                         |                                 | 1.1 V                    | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |             | DDR                 |                           |              |                               |                |
| P1                 | DDR0_DQ26        | DDR0_DQ26          |                 | IO          |                         |                                 | 1.1 V                    | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |             | DDR                 |                           |              |                               |                |
| P2                 | DDR0_DQ27        | DDR0_DQ27          |                 | IO          |                         |                                 | 1.1 V                    | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |             | DDR                 |                           |              |                               |                |
| N4                 | DDR0_DQ28        | DDR0_DQ28          |                 | IO          |                         |                                 | 1.1 V                    | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |             | DDR                 |                           |              |                               |                |
| P3                 | DDR0_DQ29        | DDR0_DQ29          |                 | IO          |                         |                                 | 1.1 V                    | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |             | DDR                 |                           |              |                               |                |
| P4                 | DDR0_DQ30        | DDR0_DQ30          |                 | IO          |                         |                                 | 1.1 V                    | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |             | DDR                 |                           |              |                               |                |
| N5                 | DDR0_DQ31        | DDR0_DQ31          |                 | IO          |                         |                                 | 1.1 V                    | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |             | DDR                 |                           |              |                               |                |
| B1                 | DDR0_DQS0N       | DDR0_DQS0N         |                 | IO          |                         |                                 | 1.1 V                    | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |             | DDR                 |                           |              |                               |                |
| B2                 | DDR0_DQS0P       | DDR0_DQS0P         |                 | IO          |                         |                                 | 1.1 V                    | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |             | DDR                 |                           |              |                               |                |
| E1                 | DDR0_DQS1N       | DDR0_DQS1N         |                 | IO          |                         |                                 | 1.1 V                    | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |             | DDR                 |                           |              |                               |                |
| E2                 | DDR0_DQS1P       | DDR0_DQS1P         |                 | IO          |                         |                                 | 1.1 V                    | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |             | DDR                 |                           |              |                               |                |
| M1                 | DDR0_DQS2N       | DDR0_DQS2N         |                 | IO          |                         |                                 | 1.1 V                    | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |             | DDR                 |                           |              |                               |                |
| M2                 | DDR0_DQS2P       | DDR0_DQS2P         |                 | IO          |                         |                                 | 1.1 V                    | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |             | DDR                 |                           |              |                               |                |
| R1                 | DDR0_DQS3N       | DDR0_DQS3N         |                 | IO          |                         |                                 | 1.1 V                    | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |             | DDR                 |                           |              |                               |                |
| R2                 | DDR0_DQS3P       | DDR0_DQS3P         |                 | IO          |                         |                                 | 1.1 V                    | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |             | DDR                 |                           |              |                               |                |
| R5                 | DDR_RET          | DDR_RET            |                 | I           |                         |                                 | 1.1 V                    | VDDS_DDR, VDDS_DDR_C, VDDS_DDR_BIAS |             | DDR                 |                           |              |                               |                |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2]     | SIGNAL NAME [3]   | MUX MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUX MODE [7] | I/O VOLTAGE VALUE [8] | POWER [9]   | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RX ACTIVE/ TX DISABLE [14] | IO RET [15] |
|-----------------|-------------------|-------------------|--------------|----------|----------------------|------------------------------|-----------------------|-------------|----------|------------------|------------------------|-----------|----------------------------|-------------|
| U3              | ECAP0_IN_APWM_OUT | ECAP0_IN_APWM_OUT | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0     | Yes      | LVCMOS           | PU/PD                  | 0         |                            |             |
|                 |                   | SYNC0_OUT         | 1            | O        |                      |                              |                       |             |          |                  |                        |           |                            |             |
|                 |                   | CPTS0_RFT_CLK     | 2            | I        |                      |                              |                       |             |          |                  |                        |           |                            |             |
|                 |                   | I2C1_SCL          | 3            | IOD      |                      |                              |                       |             |          |                  |                        |           |                            |             |
|                 |                   | CPTS0_HW1TSPUSH   | 4            | I        |                      |                              |                       |             |          |                  |                        |           |                            |             |
|                 |                   | UART3_RXD         | 5            | I        |                      |                              |                       |             |          |                  |                        |           |                            |             |
|                 |                   | SPI7_CS0          | 6            | IO       |                      |                              |                       |             |          |                  |                        |           |                            |             |
|                 |                   | GPIO0_58          | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
| A13             | EMU0              | EMU0              | 0            | IO       | OFF                  | 0                            | 1.8 V/3.3 V           | VDDSHV0_MCU | Yes      | LVCMOS           | PU/PD                  |           | 0/0                        |             |
| D12             | EMU1              | EMU1              | 0            | IO       | OFF                  | 0                            | 1.8 V/3.3 V           | VDDSHV0_MCU | Yes      | LVCMOS           | PU/PD                  |           | 0/0                        |             |
| U6              | EXTINTn           | EXTINTn           | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0     | Yes      | I2C OD FS        |                        | 1         |                            |             |
|                 |                   | GPIO0_0           | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
| T3              | EXT_REFCLK1       | EXT_REFCLK1       | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0     | Yes      | LVCMOS           | PU/PD                  | 0         |                            |             |
|                 |                   | SYNC1_OUT         | 1            | O        |                      |                              |                       |             |          |                  |                        |           |                            |             |
|                 |                   | I2C1_SDA          | 3            | IOD      |                      |                              |                       |             |          |                  |                        |           |                            |             |
|                 |                   | CPTS0_HW2TSPUSH   | 4            | I        |                      |                              |                       |             |          |                  |                        |           |                            |             |
|                 |                   | UART3_TXD         | 5            | O        |                      |                              |                       |             |          |                  |                        |           |                            |             |
|                 |                   | SPI7_CLK          | 6            | IO       |                      |                              |                       |             |          |                  |                        |           |                            |             |
|                 |                   | GPIO0_59          | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
| U12             | GPIO0_41          | RGMI12_TX_CTL     | 4            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2     | Yes      | LVCMOS           | PU/PD                  |           |                            | Yes         |
|                 |                   | RMII2_TXD0        | 5            | O        |                      |                              |                       |             |          |                  |                        |           |                            |             |
|                 |                   | GPIO0_41          | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
|                 |                   | SPI6_D1           | 8            | IO       |                      |                              |                       |             |          |                  |                        | 0         |                            |             |
|                 |                   | UART4_RXD         | 11           | I        |                      |                              |                       |             |          |                  |                        | 1         |                            |             |
|                 |                   | MCASP2_ACLKX      | 12           | IO       |                      |                              |                       |             |          |                  |                        | 0         |                            |             |
|                 |                   | GPMC0_A13         | 13           | OZ       |                      |                              |                       |             |          |                  |                        |           |                            |             |
| U13             | GPMC0_CLK         | GPMC0_CLK         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2     | Yes      | LVCMOS           | PU/PD                  | 0         |                            | Yes         |
|                 |                   | USB0_DRVVBUS      | 1            | O        |                      |                              |                       |             |          |                  |                        |           |                            |             |
|                 |                   | RGMI14_RD3        | 4            | I        |                      |                              |                       |             |          |                  |                        | 0         |                            |             |
|                 |                   | GPIO0_44          | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
|                 |                   | SPI0_CS3          | 10           | IO       |                      |                              |                       |             |          |                  |                        | 1         |                            |             |
|                 |                   | UART9_RXD         | 11           | I        |                      |                              |                       |             |          |                  |                        | 1         |                            |             |
| V3              | I2C0_SCL          | I2C0_SCL          | 0            | IOD      | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0     | Yes      | I2C OD FS        |                        | 1         |                            |             |
|                 |                   | GPIO0_56          | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
| W2              | I2C0_SDA          | I2C0_SDA          | 0            | IOD      | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0     | Yes      | I2C OD FS        |                        | 1         |                            |             |
|                 |                   | GPIO0_57          | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1]   | BALL NAME [2] | SIGNAL NAME [3] | MUX MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUX MODE [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RX ACTIVE/ TX DISABLE [14] | IO RET [15] |
|-------------------|---------------|-----------------|--------------|----------|----------------------|------------------------------|-----------------------|-----------|----------|------------------|------------------------|-----------|----------------------------|-------------|
| V20               | MCAN0_RX      | MCAN0_RX        | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                  | 1         | 1/0                        | Yes         |
|                   |               | RGMI14_RD1      | 4            | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                   |               | MCAN0_RX        | 6            | I        |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                   |               | GPIO0_10        | 7            | IO       |                      |                              |                       |           |          |                  |                        | pad       |                            |             |
|                   |               | EQEP2_S         | 9            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                   |               | GPMC0_A2        | 11           | OZ       |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                   |               | MCASP0_AXR10    | 12           | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
| V18               | MCAN0_TX      | MCAN0_TX        | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                  |           | 1/0                        | Yes         |
|                   |               | RGMI14_RD0      | 4            | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                   |               | MCAN0_TX        | 6            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                   |               | GPIO0_9         | 7            | IO       |                      |                              |                       |           |          |                  |                        | pad       |                            |             |
|                   |               | EQEP2_B         | 9            | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                   |               | GPMC0_A1        | 11           | OZ       |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                   |               | MCASP0_AXR9     | 12           | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
| AUDIO_EXT_REFCLK0 | 14            | IO              | 0            |          |                      |                              |                       |           |          |                  |                        |           |                            |             |
| V16               | MCAN1_RX      | MCAN1_RX        | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                  | 1         | 1/0                        | Yes         |
|                   |               | RGMI14_RD2      | 4            | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                   |               | RMII2_TXD1      | 5            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                   |               | MCAN1_RX        | 6            | I        |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                   |               | GPIO0_12        | 7            | IO       |                      |                              |                       |           |          |                  |                        | pad       |                            |             |
|                   |               | SPI6_CS1        | 8            | IO       |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                   |               | EQEP2_I         | 9            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                   |               | GPMC0_AD7       | 10           | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                   |               | UART6_CTSn      | 11           | I        |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                   |               | MCASP0_AXR12    | 12           | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                   |               | OBSCLK1         | 14           | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
| W21               | MCAN1_TX      | MCAN1_TX        | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                  |           | 1/0                        | Yes         |
|                   |               | RGMI12_TXC      | 4            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                   |               | RMII2_TX_EN     | 5            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                   |               | MCAN1_TX        | 6            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                   |               | GPIO0_11        | 7            | IO       |                      |                              |                       |           |          |                  |                        | pad       |                            |             |
|                   |               | SPI6_CS0        | 8            | IO       |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                   |               | EHRPWM_SOCA     | 9            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                   |               | GPMC0_A3        | 11           | OZ       |                      |                              |                       |           |          |                  |                        |           |                            |             |
| MCASP0_AXR11      | 12            | IO              | 0            |          |                      |                              |                       |           |          |                  |                        |           |                            |             |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | MUX MODE [4] | TYPE [5]  | BALL RESET STATE [6] | BALL RESET REL. MUX MODE [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10]    | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RX ACTIVE/ TX DISABLE [14] | IO RET [15] |     |     |   |             |         |  |        |       |     |     |     |
|-----------------|---------------|-----------------|--------------|-----------|----------------------|------------------------------|-----------------------|-----------|-------------|------------------|------------------------|-----------|----------------------------|-------------|-----|-----|---|-------------|---------|--|--------|-------|-----|-----|-----|
| Y19             | MCAN2_RX      | MCAN2_RX        | 0            | I         | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   |             | LVCMOS           | PU/PD                  | 1         | 1/0                        | Yes         |     |     |   |             |         |  |        |       |     |     |     |
|                 |               | RGMI1_TD1       | 4            | O         |                      |                              |                       |           |             |                  |                        |           |                            |             |     |     |   |             |         |  |        |       |     |     |     |
|                 |               | RMII4_RXD1      | 5            | I         |                      |                              |                       |           |             |                  |                        | 0         |                            |             |     |     |   |             |         |  |        |       |     |     |     |
|                 |               | MCAN2_RX        | 6            | I         |                      |                              |                       |           |             |                  |                        | 1         |                            |             |     |     |   |             |         |  |        |       |     |     |     |
|                 |               | GPIO0_14        | 7            | IO        |                      |                              |                       |           |             |                  |                        | pad       |                            |             |     |     |   |             |         |  |        |       |     |     |     |
|                 |               | SPI5_CS2        | 8            | IO        |                      |                              |                       |           |             |                  |                        | 1         |                            |             |     |     |   |             |         |  |        |       |     |     |     |
|                 |               | EHRPWM0_B       | 9            | IO        |                      |                              |                       |           |             |                  |                        | 0         |                            |             |     |     |   |             |         |  |        |       |     |     |     |
|                 |               | TRC_DATA2       | 10           | O         |                      |                              |                       |           |             |                  |                        |           |                            |             |     |     |   |             |         |  |        |       |     |     |     |
|                 |               | UART3_TXD       | 11           | O         |                      |                              |                       |           |             |                  |                        |           |                            |             |     |     |   |             |         |  |        |       |     |     |     |
|                 |               | MCASP1_ACLKX    | 12           | IO        |                      |                              |                       |           |             |                  |                        | 0         |                            |             |     |     |   |             |         |  |        |       |     |     |     |
|                 |               | UART9_RTSn      | 13           | O         |                      |                              |                       |           |             |                  |                        |           |                            |             |     |     |   |             |         |  |        |       |     |     |     |
|                 |               | GPMC0_AD9       | 14           | IO        |                      |                              |                       |           |             |                  |                        | 0         |                            |             |     |     |   |             |         |  |        |       |     |     |     |
|                 |               | Y18             | MCAN2_TX     | MCAN2_TX  |                      |                              |                       |           |             |                  |                        | 0         |                            |             | O   | OFF | 7 | 1.8 V/3.3 V | VDDSHV2 |  | LVCMOS | PU/PD |     | 1/0 | Yes |
|                 |               |                 |              | RGMI1_TD0 |                      |                              |                       |           |             |                  |                        | 4         |                            |             | O   |     |   |             |         |  |        |       |     |     |     |
| RMII4_RXD0      | 5             |                 |              | I         | 0                    |                              |                       |           |             |                  |                        |           |                            |             |     |     |   |             |         |  |        |       |     |     |     |
| MCAN2_TX        | 6             |                 |              | O         |                      |                              |                       |           |             |                  |                        |           |                            |             |     |     |   |             |         |  |        |       |     |     |     |
| GPIO0_13        | 7             |                 |              | IO        | pad                  |                              |                       |           |             |                  |                        |           |                            |             |     |     |   |             |         |  |        |       |     |     |     |
| SPI5_CS3        | 8             |                 |              | IO        | 1                    |                              |                       |           |             |                  |                        |           |                            |             |     |     |   |             |         |  |        |       |     |     |     |
| EHRPWM1_A       | 9             |                 |              | IO        | 1                    |                              |                       |           |             |                  |                        |           |                            |             |     |     |   |             |         |  |        |       |     |     |     |
| TRC_DATA3       | 10            |                 |              | O         |                      |                              |                       |           |             |                  |                        |           |                            |             |     |     |   |             |         |  |        |       |     |     |     |
| UART3_RXD       | 11            |                 |              | I         | 1                    |                              |                       |           |             |                  |                        |           |                            |             |     |     |   |             |         |  |        |       |     |     |     |
| MCASP1_AFSX     | 12            |                 |              | IO        | 0                    |                              |                       |           |             |                  |                        |           |                            |             |     |     |   |             |         |  |        |       |     |     |     |
| UART9_CTSn      | 13            |                 |              | I         | 1                    |                              |                       |           |             |                  |                        |           |                            |             |     |     |   |             |         |  |        |       |     |     |     |
| GPMC0_AD8       | 14            |                 |              | IO        | 0                    |                              |                       |           |             |                  |                        |           |                            |             |     |     |   |             |         |  |        |       |     |     |     |
| W16             | MCAN3_RX      |                 |              | MCAN3_RX  | 0                    | I                            | OFF                   | 7         | 1.8 V/3.3 V | VDDSHV2          |                        | LVCMOS    | PU/PD                      | 1           | 1/0 |     |   |             |         |  |        |       | Yes |     |     |
|                 |               |                 |              | RGMI1_TD3 | 4                    | O                            |                       |           |             |                  |                        |           |                            |             |     |     |   |             |         |  |        |       |     |     |     |
|                 |               | RMII4_RX_ER     | 5            | I         | 0                    |                              |                       |           |             |                  |                        |           |                            |             |     |     |   |             |         |  |        |       |     |     |     |
|                 |               | MCAN3_RX        | 6            | I         | 1                    |                              |                       |           |             |                  |                        |           |                            |             |     |     |   |             |         |  |        |       |     |     |     |
|                 |               | GPIO0_16        | 7            | IO        | pad                  |                              |                       |           |             |                  |                        |           |                            |             |     |     |   |             |         |  |        |       |     |     |     |
|                 |               | SPI5_CS0        | 8            | IO        | 1                    |                              |                       |           |             |                  |                        |           |                            |             |     |     |   |             |         |  |        |       |     |     |     |
|                 |               | EHRPWM_TZn_IN0  | 9            | I         | 0                    |                              |                       |           |             |                  |                        |           |                            |             |     |     |   |             |         |  |        |       |     |     |     |
|                 |               | TRC_DATA0       | 10           | O         |                      |                              |                       |           |             |                  |                        |           |                            |             |     |     |   |             |         |  |        |       |     |     |     |
|                 |               | GPMC0_A4        | 11           | OZ        |                      |                              |                       |           |             |                  |                        |           |                            |             |     |     |   |             |         |  |        |       |     |     |     |
|                 |               | MCASP0_AXR0     | 12           | IO        | 0                    |                              |                       |           |             |                  |                        |           |                            |             |     |     |   |             |         |  |        |       |     |     |     |
|                 |               | SYNC2_OUT       | 14           | O         |                      |                              |                       |           |             |                  |                        |           |                            |             |     |     |   |             |         |  |        |       |     |     |     |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | MUX MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUX MODE [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RX ACTIVE/ TX DISABLE [14] | IO RET [15] |
|-----------------|---------------|-----------------|--------------|----------|----------------------|------------------------------|-----------------------|-----------|----------|------------------|------------------------|-----------|----------------------------|-------------|
| Y21             | MCAN3_TX      | MCAN3_TX        | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                  |           | 1/0                        | Yes         |
|                 |               | RGMI1_TD2       | 4            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | RMII4_CRS_DV    | 5            | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | MCAN3_TX        | 6            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | GPIO0_15        | 7            | IO       |                      |                              |                       |           |          |                  |                        | pad       |                            |             |
|                 |               | SPI5_D0         | 8            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | EHRPWM0_A       | 9            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | TRC_DATA1       | 10           | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | MCASP0_AXR1     | 12           | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | GPMC0_AD10      | 14           | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
| Y20             | MCAN4_RX      | MCAN4_RX        | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                  | 1         | 1/0                        | Yes         |
|                 |               | RGMI1_TXC       | 4            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | RMII4_TX_EN     | 5            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | MCAN4_RX        | 6            | I        |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | GPIO0_18        | 7            | IO       |                      |                              |                       |           |          |                  |                        | pad       |                            |             |
|                 |               | SPI5_D1         | 8            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | EHRPWM1_B       | 9            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | TRC_DATA4       | 10           | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | I2C2_SDA        | 11           | IOD      |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | MCASP0_AXR2     | 12           | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
| GPMC0_AD12      | 14            | IO              | 0            |          |                      |                              |                       |           |          |                  |                        |           |                            |             |
| W15             | MCAN4_TX      | MCAN4_TX        | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                  |           | 1/0                        | Yes         |
|                 |               | RGMI1_TX_CTL    | 4            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | RMII4_TXD0      | 5            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | MCAN4_TX        | 6            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | GPIO0_17        | 7            | IO       |                      |                              |                       |           |          |                  |                        | pad       |                            |             |
|                 |               | SPI5_CLK        | 8            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | EHRPWM0_SYNCI   | 9            | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | TRC_CLK         | 10           | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | I2C2_SCL        | 11           | IOD      |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | MCASP0_ACLKX    | 12           | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
| GPMC0_AD11      | 14            | IO              | 0            |          |                      |                              |                       |           |          |                  |                        |           |                            |             |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | MUX MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUX MODE [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RX ACTIVE/ TX DISABLE [14] | IO RET [15] |
|-----------------|---------------|-----------------|--------------|----------|----------------------|------------------------------|-----------------------|-----------|----------|------------------|------------------------|-----------|----------------------------|-------------|
| V19             | MCAN5_RX      | MCAN5_RX        | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                  | 1         | 1/0                        | Yes         |
|                 |               | RGMI3_RD0       | 4            | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | RMII3_RXD0      | 5            | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | MCAN5_RX        | 6            | I        |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | GPIO0_20        | 7            | IO       |                      |                              |                       |           |          |                  |                        | pad       |                            |             |
|                 |               | I2C3_SCL        | 8            | IOD      |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | EHRPWM_TZn_IN5  | 9            | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | TRC_DATA21      | 10           | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | GPMC0_A5        | 11           | OZ       |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | MCASP1_AXR7     | 12           | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
| V21             | MCAN5_TX      | MCAN5_TX        | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                  |           | 1/0                        | Yes         |
|                 |               | RGMI3_RXC       | 4            | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | RMII4_TXD1      | 5            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | MCAN5_TX        | 6            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | GPIO0_19        | 7            | IO       |                      |                              |                       |           |          |                  |                        | pad       |                            |             |
|                 |               | SPI5_CS1        | 8            | IO       |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | EHRPWM4_B       | 9            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | TRC_DATA17      | 10           | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | UART6_RTSn      | 11           | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | MCASP0_AXR7     | 12           | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
| GPMC0_DIR       | 13            | O               |              |          |                      |                              |                       |           |          |                  |                        |           |                            |             |
| SYNC3_OUT       | 14            | O               |              |          |                      |                              |                       |           |          |                  |                        |           |                            |             |
| U14             | MCAN6_RX      | MCAN6_RX        | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                  | 1         | 1/0                        | Yes         |
|                 |               | RGMI3_RD2       | 4            | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | RMII3_CRS_DV    | 5            | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | MCAN6_RX        | 6            | I        |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | GPIO0_22        | 7            | IO       |                      |                              |                       |           |          |                  |                        | pad       |                            |             |
|                 |               | EHRPWM5_A       | 9            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | TRC_DATA19      | 10           | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | MCASP1_AXR5     | 12           | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
| GPMC0_AD13      | 14            | IO              | 0            |          |                      |                              |                       |           |          |                  |                        |           |                            |             |

Table 5-1. Pin Attributes (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | MUX MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUX MODE [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RX ACTIVE/ TX DISABLE [14] | IO RET [15] |
|-----------------|---------------|-----------------|--------------|----------|----------------------|------------------------------|-----------------------|-----------|----------|------------------|------------------------|-----------|----------------------------|-------------|
| T13             | MCAN6_TX      | MCAN6_TX        | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                  |           | 1/0                        | Yes         |
|                 |               | RGMI13_RD1      | 4            | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | RMII3_RXD1      | 5            | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | MCAN6_TX        | 6            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | GPIO0_21        | 7            | IO       |                      |                              |                       |           |          |                  |                        | pad       |                            |             |
|                 |               | I2C3_SDA        | 8            | IOD      |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | EHRPWM5_B       | 9            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | TRC_DATA20      | 10           | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | GPMC0_A6        | 11           | OZ       |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | MCASP1_AXR6     | 12           | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
| U15             | MCAN7_RX      | MCAN7_RX        | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                  | 1         | 1/0                        | Yes         |
|                 |               | RGMI13_RX_CTL   | 4            | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | RMII3_TXD0      | 5            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | MCAN7_RX        | 6            | I        |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | GPIO0_24        | 7            | IO       |                      |                              |                       |           |          |                  |                        | pad       |                            |             |
|                 |               | SPI3_CS1        | 8            | IO       |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | EHRPWM3_A       | 9            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | TRC_DATA11      | 10           | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | MCASP0_AFSR     | 12           | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | GPMC0_AD15      | 14           | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
| U16             | MCAN7_TX      | MCAN7_TX        | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                  |           | 1/0                        | Yes         |
|                 |               | RGMI13_RD3      | 4            | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | RMII3_RX_ER     | 5            | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | MCAN7_TX        | 6            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | GPIO0_23        | 7            | IO       |                      |                              |                       |           |          |                  |                        | pad       |                            |             |
|                 |               | SPI3_CS0        | 8            | IO       |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | EHRPWM_TZn_IN4  | 9            | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | TRC_DATA18      | 10           | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | MCASP1_AXR4     | 12           | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | GPMC0_AD14      | 14           | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | MUX MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUX MODE [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10]    | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RX ACTIVE/ TX DISABLE [14] | IO RET [15] |
|-----------------|---------------|-----------------|--------------|----------|----------------------|------------------------------|-----------------------|-----------|-------------|------------------|------------------------|-----------|----------------------------|-------------|
| U19             | MCAN8_RX      | MCAN8_RX        | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   |             | LVCMOS           | PU/PD                  | 1         | 1/0                        | Yes         |
|                 |               | RGMI3_TD1       | 4            | O        |                      |                              |                       |           |             |                  |                        |           |                            |             |
|                 |               | RMI3_TXD1       | 5            | O        |                      |                              |                       |           |             |                  |                        |           |                            |             |
|                 |               | MCAN8_RX        | 6            | I        |                      |                              |                       |           |             |                  |                        | 1         |                            |             |
|                 |               | GPIO0_26        | 7            | IO       |                      |                              |                       |           |             |                  |                        | pad       |                            |             |
|                 |               | SPI3_CS3        | 8            | IO       |                      |                              |                       |           |             |                  |                        | 1         |                            |             |
|                 |               | EHRPWM3_SYNCO   | 9            | O        |                      |                              |                       |           |             |                  |                        |           |                            |             |
|                 |               | TRC_DATA14      | 10           | O        |                      |                              |                       |           |             |                  |                        |           |                            |             |
|                 |               | UART3_RTSn      | 11           | O        |                      |                              |                       |           |             |                  |                        |           |                            |             |
|                 |               | MCASP0_AXR4     | 12           | IO       |                      |                              |                       |           |             |                  |                        | 0         |                            |             |
|                 |               | GPMC0_A8        | 13           | OZ       |                      |                              |                       |           |             |                  |                        |           |                            |             |
|                 |               | UART0_DSRn      | 14           | I        |                      |                              |                       |           |             |                  |                        | 1         |                            |             |
|                 |               | T15             | MCAN8_TX     | MCAN8_TX |                      |                              |                       |           |             |                  |                        | 0         |                            |             |
| GPMC0_A7        | 3             |                 |              | OZ       |                      |                              |                       |           |             |                  |                        |           |                            |             |
| RGMI3_TD0       | 4             |                 |              | O        |                      |                              |                       |           |             |                  |                        |           |                            |             |
| RMI3_TX_EN      | 5             |                 |              | O        |                      |                              |                       |           |             |                  |                        |           |                            |             |
| MCAN8_TX        | 6             |                 |              | O        |                      |                              |                       |           |             |                  |                        |           |                            |             |
| GPIO0_25        | 7             |                 |              | IO       | pad                  |                              |                       |           |             |                  |                        |           |                            |             |
| SPI3_CS2        | 8             |                 |              | IO       | 1                    |                              |                       |           |             |                  |                        |           |                            |             |
| EHRPWM_TZn_IN3  | 9             |                 |              | I        | 0                    |                              |                       |           |             |                  |                        |           |                            |             |
| TRC_DATA15      | 10            |                 |              | O        |                      |                              |                       |           |             |                  |                        |           |                            |             |
| UART3_CTSn      | 11            |                 |              | I        | 1                    |                              |                       |           |             |                  |                        |           |                            |             |
| MCASP0_AXR5     | 12            |                 |              | IO       | 0                    |                              |                       |           |             |                  |                        |           |                            |             |
| UART0_DCDn      | 14            |                 |              | I        | 1                    |                              |                       |           |             |                  |                        |           |                            |             |
| U18             | MCAN9_RX      |                 |              | MCAN9_RX | 0                    | I                            | OFF                   | 7         | 1.8 V/3.3 V | VDDSHV2          |                        | LVCMOS    | PU/PD                      | 1           |
|                 |               | RGMI3_TD3       | 4            | O        |                      |                              |                       |           |             |                  |                        |           |                            |             |
|                 |               | MCAN9_RX        | 6            | I        | 1                    |                              |                       |           |             |                  |                        |           |                            |             |
|                 |               | GPIO0_28        | 7            | IO       | pad                  |                              |                       |           |             |                  |                        |           |                            |             |
|                 |               | SPI3_D0         | 8            | IO       | 0                    |                              |                       |           |             |                  |                        |           |                            |             |
|                 |               | EHRPWM3_B       | 9            | IO       | 0                    |                              |                       |           |             |                  |                        |           |                            |             |
|                 |               | TRC_DATA12      | 10           | O        |                      |                              |                       |           |             |                  |                        |           |                            |             |
|                 |               | MCASP1_ACLKR    | 12           | IO       | 0                    |                              |                       |           |             |                  |                        |           |                            |             |
|                 |               | GPMC0_A10       | 13           | OZ       |                      |                              |                       |           |             |                  |                        |           |                            |             |
|                 |               | MCASP1_AXR11    | 14           | IO       | 0                    |                              |                       |           |             |                  |                        |           |                            |             |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | MUX MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUX MODE [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RX ACTIVE/ TX DISABLE [14] | IO RET [15] |
|-----------------|---------------|-----------------|--------------|----------|----------------------|------------------------------|-----------------------|-----------|----------|------------------|------------------------|-----------|----------------------------|-------------|
| T14             | MCAN9_TX      | MCAN9_TX        | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                  |           | 1/0                        | Yes         |
|                 |               | RGMI3_TD2       | 4            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | MCAN9_TX        | 6            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | GPIO0_27        | 7            | IO       |                      |                              |                       |           |          |                  |                        | pad       |                            |             |
|                 |               | SPI3_CLK        | 8            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | EHRPWM3_SYNCI   | 9            | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | TRC_DATA13      | 10           | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | MCASP1_AFSR     | 12           | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | GPMC0_A9        | 13           | OZ       |                      |                              |                       |           |          |                  |                        |           |                            |             |
| MCASP1_AXR10    | 14            | IO              | 0            |          |                      |                              |                       |           |          |                  |                        |           |                            |             |
| U20             | MCAN10_RX     | MCAN10_RX       | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                  | 1         | 1/0                        | Yes         |
|                 |               | RGMI3_TXC       | 4            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | MCAN10_RX       | 6            | I        |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | GPIO0_30        | 7            | IO       |                      |                              |                       |           |          |                  |                        | pad       |                            |             |
|                 |               | SPI2_CLK        | 8            | IO       |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | EHRPWM4_A       | 9            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | TRC_DATA16      | 10           | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | UART2_RTSn      | 11           | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | MCASP0_AXR6     | 12           | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | GPMC0_BE0n_CLE  | 13           | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | GPMC0_A16       | 14           | OZ       |                      |                              |                       |           |          |                  |                        |           |                            |             |
| U17             | MCAN10_TX     | MCAN10_TX       | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                  |           | 1/0                        | Yes         |
|                 |               | RGMI3_TX_CTL    | 4            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | MCAN10_TX       | 6            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | GPIO0_29        | 7            | IO       |                      |                              |                       |           |          |                  |                        | pad       |                            |             |
|                 |               | SPI3_D1         | 8            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | EHRPWM_SOCB     | 9            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | TRC_DATA10      | 10           | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | UART2_CTSn      | 11           | I        |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | MCASP0_ACLKR    | 12           | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | GPMC0_WAIT1     | 13           | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
| GPMC0_A22       | 14            | OZ              |              |          |                      |                              |                       |           |          |                  |                        |           |                            |             |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | MUX MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUX MODE [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RX ACTIVE/ TX DISABLE [14] | IO RET [15] |
|-----------------|---------------|-----------------|--------------|----------|----------------------|------------------------------|-----------------------|-----------|----------|------------------|------------------------|-----------|----------------------------|-------------|
| Y13             | MCAN11_RX     | MCAN11_RX       | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                  | 1         | 1/0                        | Yes         |
|                 |               | RGMI2_RD0       | 4            | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | MCAN11_RX       | 6            | I        |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | GPIO0_32        | 7            | IO       |                      |                              |                       |           |          |                  |                        | pad       |                            |             |
|                 |               | SPI2_CS1        | 8            | IO       |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | EQEP0_B         | 9            | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | UART3_TXD       | 11           | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | MCASP0_AXR14    | 12           | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | GPMC0_A12       | 13           | OZ       |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | UART0_RIn       | 14           | I        |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
| Y14             | MCAN11_TX     | MCAN11_TX       | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                  |           | 1/0                        | Yes         |
|                 |               | RGMI2_RXC       | 4            | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | MCAN11_TX       | 6            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | GPIO0_31        | 7            | IO       |                      |                              |                       |           |          |                  |                        | pad       |                            |             |
|                 |               | SPI2_CS0        | 8            | IO       |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | EQEP0_A         | 9            | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | SPI0_CS2        | 10           | IO       |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | UART3_RXD       | 11           | I        |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | MCASP0_AXR13    | 12           | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | GPMC0_A11       | 13           | OZ       |                      |                              |                       |           |          |                  |                        |           |                            |             |
| UART0_DTRn      | 14            | O               |              |          |                      |                              |                       |           |          |                  |                        |           |                            |             |
| AA14            | MCAN12_RX     | MCAN12_RX       | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                  | 1         | 1/0                        | Yes         |
|                 |               | RGMI2_RD2       | 4            | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | MCAN12_RX       | 6            | I        |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | GPIO0_34        | 7            | IO       |                      |                              |                       |           |          |                  |                        | pad       |                            |             |
|                 |               | SPI2_CS3        | 8            | IO       |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | EQEP1_B         | 9            | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | I2C6_SDA        | 10           | IOD      |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | UART2_TXD       | 11           | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | MCASP1_AXR8     | 12           | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | I3C0_SDAPULLEN  | 13           | OD       |                      |                              |                       |           |          |                  |                        |           |                            |             |
| GPMC0_A18       | 14            | OZ              |              |          |                      |                              |                       |           |          |                  |                        |           |                            |             |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | MUX MODE [4] | TYPE [5]  | BALL RESET STATE [6] | BALL RESET REL. MUX MODE [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RX ACTIVE/ TX DISABLE [14] | IO RET [15] |   |     |   |             |         |  |        |       |   |     |     |
|-----------------|---------------|-----------------|--------------|-----------|----------------------|------------------------------|-----------------------|-----------|----------|------------------|------------------------|-----------|----------------------------|-------------|---|-----|---|-------------|---------|--|--------|-------|---|-----|-----|
| AA15            | MCAN12_TX     | MCAN12_TX       | 0            | O         | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   |          | LVCMOS           | PU/PD                  |           | 1/0                        | Yes         |   |     |   |             |         |  |        |       |   |     |     |
|                 |               | RGMI2_RD1       | 4            | I         |                      |                              |                       |           |          |                  |                        | 0         |                            |             |   |     |   |             |         |  |        |       |   |     |     |
|                 |               | MCAN12_TX       | 6            | O         |                      |                              |                       |           |          |                  |                        |           |                            |             |   |     |   |             |         |  |        |       |   |     |     |
|                 |               | GPIO0_33        | 7            | IO        |                      |                              |                       |           |          |                  |                        | pad       |                            |             |   |     |   |             |         |  |        |       |   |     |     |
|                 |               | SPI2_CS2        | 8            | IO        |                      |                              |                       |           |          |                  |                        | 1         |                            |             |   |     |   |             |         |  |        |       |   |     |     |
|                 |               | EQEP1_A         | 9            | I         |                      |                              |                       |           |          |                  |                        | 0         |                            |             |   |     |   |             |         |  |        |       |   |     |     |
|                 |               | I2C6_SCL        | 10           | IOD       |                      |                              |                       |           |          |                  |                        | 1         |                            |             |   |     |   |             |         |  |        |       |   |     |     |
|                 |               | UART2_RXD       | 11           | I         |                      |                              |                       |           |          |                  |                        | 1         |                            |             |   |     |   |             |         |  |        |       |   |     |     |
|                 |               | MCASP0_AXR15    | 12           | IO        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |   |     |   |             |         |  |        |       |   |     |     |
|                 |               | GPMC0_BE1n      | 13           | O         |                      |                              |                       |           |          |                  |                        |           |                            |             |   |     |   |             |         |  |        |       |   |     |     |
|                 |               | GPMC0_A17       | 14           | OZ        |                      |                              |                       |           |          |                  |                        |           |                            |             |   |     |   |             |         |  |        |       |   |     |     |
| AA16            | MCAN13_RX     | MCAN13_RX       | 0            | I         | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   |          | LVCMOS           | PU/PD                  | 1         | 1/0                        | Yes         |   |     |   |             |         |  |        |       |   |     |     |
|                 |               | RGMI2_RX_CTL    | 4            | I         |                      |                              |                       |           |          |                  |                        | 0         |                            |             |   |     |   |             |         |  |        |       |   |     |     |
|                 |               | GPMC0_CS3       | 5            | O         |                      |                              |                       |           |          |                  |                        |           |                            |             |   |     |   |             |         |  |        |       |   |     |     |
|                 |               | MCAN13_RX       | 6            | I         |                      |                              |                       |           |          |                  |                        | 1         |                            |             |   |     |   |             |         |  |        |       |   |     |     |
|                 |               | GPIO0_36        | 7            | IO        |                      |                              |                       |           |          |                  |                        | pad       |                            |             |   |     |   |             |         |  |        |       |   |     |     |
|                 |               | SPI2_D1         | 8            | IO        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |   |     |   |             |         |  |        |       |   |     |     |
|                 |               | EQEP0_I         | 9            | IO        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |   |     |   |             |         |  |        |       |   |     |     |
|                 |               | I2C5_SDA        | 10           | IOD       |                      |                              |                       |           |          |                  |                        | 1         |                            |             |   |     |   |             |         |  |        |       |   |     |     |
|                 |               | UART8_RTSn      | 11           | O         |                      |                              |                       |           |          |                  |                        |           |                            |             |   |     |   |             |         |  |        |       |   |     |     |
|                 |               | MCASP2_AXR0     | 12           | IO        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |   |     |   |             |         |  |        |       |   |     |     |
|                 |               | I3C0_SDA        | 13           | IO        |                      |                              |                       |           |          |                  |                        | 1         |                            |             |   |     |   |             |         |  |        |       |   |     |     |
|                 |               | GPMC0_A20       | 14           | OZ        |                      |                              |                       |           |          |                  |                        |           |                            |             |   |     |   |             |         |  |        |       |   |     |     |
|                 |               | AA18            | MCAN13_TX    | MCAN13_TX |                      |                              |                       |           |          |                  |                        | 0         |                            |             | O | OFF | 7 | 1.8 V/3.3 V | VDDSHV2 |  | LVCMOS | PU/PD |   | 1/0 | Yes |
|                 |               |                 |              | RGMI2_RD3 |                      |                              |                       |           |          |                  |                        | 4         |                            |             | I |     |   |             |         |  |        |       | 0 |     |     |
| GPMC0_WPn       | 5             |                 |              | O         |                      |                              |                       |           |          |                  |                        |           |                            |             |   |     |   |             |         |  |        |       |   |     |     |
| MCAN13_TX       | 6             |                 |              | O         |                      |                              |                       |           |          |                  |                        |           |                            |             |   |     |   |             |         |  |        |       |   |     |     |
| GPIO0_35        | 7             |                 |              | IO        | pad                  |                              |                       |           |          |                  |                        |           |                            |             |   |     |   |             |         |  |        |       |   |     |     |
| SPI2_D0         | 8             |                 |              | IO        | 0                    |                              |                       |           |          |                  |                        |           |                            |             |   |     |   |             |         |  |        |       |   |     |     |
| EQEP0_S         | 9             |                 |              | IO        | 0                    |                              |                       |           |          |                  |                        |           |                            |             |   |     |   |             |         |  |        |       |   |     |     |
| I2C5_SCL        | 10            |                 |              | IOD       | 1                    |                              |                       |           |          |                  |                        |           |                            |             |   |     |   |             |         |  |        |       |   |     |     |
| UART8_CTSn      | 11            |                 |              | I         | 1                    |                              |                       |           |          |                  |                        |           |                            |             |   |     |   |             |         |  |        |       |   |     |     |
| MCASP1_AXR9     | 12            |                 |              | IO        | 0                    |                              |                       |           |          |                  |                        |           |                            |             |   |     |   |             |         |  |        |       |   |     |     |
| I3C0_SCL        | 13            |                 |              | IO        | 1                    |                              |                       |           |          |                  |                        |           |                            |             |   |     |   |             |         |  |        |       |   |     |     |
| GPMC0_A19       | 14            |                 |              | OZ        |                      |                              |                       |           |          |                  |                        |           |                            |             |   |     |   |             |         |  |        |       |   |     |     |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1]   | BALL NAME [2] | SIGNAL NAME [3] | MUX MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUX MODE [7] | I/O VOLTAGE VALUE [8] | POWER [9]    | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RX ACTIVE/ TX DISABLE [14] | IO RET [15] |
|-------------------|---------------|-----------------|--------------|----------|----------------------|------------------------------|-----------------------|--------------|----------|------------------|------------------------|-----------|----------------------------|-------------|
| W20               | MCAN15_RX     | MCAN15_RX       | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2      | Yes      | LVCMOS           | PU/PD                  | 1         | 1/0                        | Yes         |
|                   |               | RGMI2_TD1       | 4            | O        |                      |                              |                       |              |          |                  |                        |           |                            |             |
|                   |               | RMII2_RXD1      | 5            | I        |                      |                              |                       |              |          |                  |                        | 0         |                            |             |
|                   |               | GPIO0_38        | 7            | IO       |                      |                              |                       |              |          |                  |                        | pad       |                            |             |
|                   |               | SPI6_CS3        | 8            | IO       |                      |                              |                       |              |          |                  |                        | 1         |                            |             |
|                   |               | EQEP1_I         | 9            | IO       |                      |                              |                       |              |          |                  |                        | 0         |                            |             |
|                   |               | MCAN15_RX       | 10           | I        |                      |                              |                       |              |          |                  |                        | 1         |                            |             |
|                   |               | MCASP2_AXR2     | 12           | IO       |                      |                              |                       |              |          |                  |                        | 0         |                            |             |
|                   |               | GPMC0_A15       | 13           | OZ       |                      |                              |                       |              |          |                  |                        |           |                            |             |
| GPMC0_ADVn_ALE    | 14            | O               |              |          |                      |                              |                       |              |          |                  |                        |           |                            |             |
| W17               | MCAN15_TX     | MCAN15_TX       | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2      | Yes      | LVCMOS           | PU/PD                  |           | 1/0                        | Yes         |
|                   |               | RGMI2_TD0       | 4            | O        |                      |                              |                       |              |          |                  |                        |           |                            |             |
|                   |               | RMII2_RXD0      | 5            | I        |                      |                              |                       |              |          |                  |                        | 0         |                            |             |
|                   |               | GPIO0_37        | 7            | IO       |                      |                              |                       |              |          |                  |                        | pad       |                            |             |
|                   |               | SPI6_CS2        | 8            | IO       |                      |                              |                       |              |          |                  |                        | 1         |                            |             |
|                   |               | EQEP1_S         | 9            | IO       |                      |                              |                       |              |          |                  |                        | 0         |                            |             |
|                   |               | MCAN15_TX       | 10           | O        |                      |                              |                       |              |          |                  |                        |           |                            |             |
|                   |               | GPMC0_CSn2      | 11           | O        |                      |                              |                       |              |          |                  |                        |           |                            |             |
|                   |               | MCASP2_AXR1     | 12           | IO       |                      |                              |                       |              |          |                  |                        | 0         |                            |             |
| GPMC0_A0          | 13            | OZ              |              |          |                      |                              |                       |              |          |                  |                        |           |                            |             |
| GPMC0_A21         | 14            | OZ              |              |          |                      |                              |                       |              |          |                  |                        |           |                            |             |
| U21               | MCAN16_RX     | MCAN16_RX       | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2      | Yes      | LVCMOS           | PU/PD                  | 1         | 1/0                        | Yes         |
|                   |               | CLKOUT          | 1            | OZ       |                      |                              |                       |              |          |                  |                        |           |                            |             |
|                   |               | RGMI4_TD0       | 4            | O        |                      |                              |                       |              |          |                  |                        |           |                            |             |
|                   |               | GPIO0_46        | 7            | IO       |                      |                              |                       |              |          |                  |                        | pad       |                            |             |
|                   |               | UART7_RXD       | 12           | I        |                      |                              |                       |              |          |                  |                        | 1         |                            |             |
|                   |               | GPMC0_CSn1      | 13           | O        |                      |                              |                       |              |          |                  |                        |           |                            |             |
| AUDIO_EXT_REFCLK1 | 14            | IO              | 0            |          |                      |                              |                       |              |          |                  |                        |           |                            |             |
| V15               | MCAN16_TX     | MCAN16_TX       | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2      | Yes      | LVCMOS           | PU/PD                  |           | 1/0                        | Yes         |
|                   |               | RMII_REF_CLK    | 1            | I        |                      |                              |                       |              |          |                  |                        | 0         |                            |             |
|                   |               | RGMI4_RX_CTL    | 4            | I        |                      |                              |                       |              |          |                  |                        | 0         |                            |             |
|                   |               | GPIO0_45        | 7            | IO       |                      |                              |                       |              |          |                  |                        | pad       |                            |             |
|                   |               | UART7_TXD       | 12           | O        |                      |                              |                       |              |          |                  |                        |           |                            |             |
| GPMC0_A14         | 13            | OZ              |              |          |                      |                              |                       |              |          |                  |                        |           |                            |             |
| H17               | MCU_ADC0_AIN0 | MCU_ADC0_AIN0   | 0            | A        |                      | 0                            | 1.8 V                 | VDDA_ADC_MCU |          | ADC12BT          |                        |           |                            |             |
| K18               | MCU_ADC0_AIN1 | MCU_ADC0_AIN1   | 0            | A        |                      | 0                            | 1.8 V                 | VDDA_ADC_MCU |          | ADC12BT          |                        |           |                            |             |
| M17               | MCU_ADC0_AIN2 | MCU_ADC0_AIN2   | 0            | A        |                      | 0                            | 1.8 V                 | VDDA_ADC_MCU |          | ADC12BT          |                        |           |                            |             |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2]              | SIGNAL NAME [3]                  | MUX MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUX MODE [7] | I/O VOLTAGE VALUE [8] | POWER [9]    | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RX ACTIVE/ TX DISABLE [14] | IO RET [15] |
|-----------------|----------------------------|----------------------------------|--------------|----------|----------------------|------------------------------|-----------------------|--------------|----------|------------------|------------------------|-----------|----------------------------|-------------|
| L18             | MCU_ADC0_AIN3              | MCU_ADC0_AIN3                    | 0            | A        |                      | 0                            | 1.8 V                 | VDDA_ADC_MCU |          | ADC12BT          |                        |           |                            |             |
| J18             | MCU_ADC0_AIN4              | MCU_ADC0_AIN4                    | 0            | A        |                      | 0                            | 1.8 V                 | VDDA_ADC_MCU |          | ADC12BT          |                        |           |                            |             |
| J17             | MCU_ADC0_AIN5              | MCU_ADC0_AIN5                    | 0            | A        |                      | 0                            | 1.8 V                 | VDDA_ADC_MCU |          | ADC12BT          |                        |           |                            |             |
| K17             | MCU_ADC0_AIN6              | MCU_ADC0_AIN6                    | 0            | A        |                      | 0                            | 1.8 V                 | VDDA_ADC_MCU |          | ADC12BT          |                        |           |                            |             |
| L17             | MCU_ADC0_AIN7              | MCU_ADC0_AIN7                    | 0            | A        |                      | 0                            | 1.8 V                 | VDDA_ADC_MCU |          | ADC12BT          |                        |           |                            |             |
| G21             | MCU_I2C0_SCL               | MCU_I2C0_SCL                     | 0            | IOD      | OFF                  | 0                            | 1.8 V/3.3 V           | VDDSHV0_MCU  | Yes      | I2C OD FS        |                        | 1         |                            | Yes         |
|                 |                            | WKUP_GPIO0_66                    | 7            | IO       | pad                  |                              |                       |              |          |                  |                        |           |                            |             |
| G20             | MCU_I2C0_SDA               | MCU_I2C0_SDA                     | 0            | IOD      | OFF                  | 0                            | 1.8 V/3.3 V           | VDDSHV0_MCU  | Yes      | I2C OD FS        |                        | 1         |                            | Yes         |
|                 |                            | WKUP_GPIO0_67                    | 7            | IO       | pad                  |                              |                       |              |          |                  |                        |           |                            |             |
| A17             | MCU_MCAN0_RX               | MCU_MCAN0_RX                     | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_MCU  | Yes      | LVCMOS           | PU/PD                  | 0         | 1/0                        | Yes         |
|                 |                            | WKUP_GPIO0_63                    | 7            | IO       | pad                  |                              |                       |              |          |                  |                        |           |                            |             |
| A16             | MCU_MCAN0_TX               | MCU_MCAN0_TX                     | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_MCU  | Yes      | LVCMOS           | PU/PD                  | pad       | 1/0                        | Yes         |
|                 |                            | WKUP_GPIO0_62                    | 7            | IO       |                      |                              |                       |              |          |                  |                        |           |                            |             |
| D9              | MCU_MDIO0_MDC              | MCU_MDIO0_MDC                    | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2_MCU  | Yes      | LVCMOS           | PU/PD                  | pad       | 1/0                        |             |
|                 |                            | WKUP_GPIO0_55                    | 7            | IO       |                      |                              |                       |              |          |                  |                        |           |                            |             |
| C9              | MCU_MDIO0_MDIO             | MCU_MDIO0_MDIO                   | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2_MCU  | Yes      | LVCMOS           | PU/PD                  | 0         | 1/0                        |             |
|                 |                            | WKUP_GPIO0_54                    | 7            | IO       | pad                  |                              |                       |              |          |                  |                        |           |                            |             |
| B6              | MCU_OSPI0_CLK              | MCU_OSPI0_CLK                    | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_MCU  | Yes      | LVCMOS           | PU/PD                  | pad       |                            |             |
|                 |                            | MCU_HYPERBUS0_CK                 | 1            | O        |                      |                              |                       |              |          |                  |                        |           |                            |             |
|                 |                            | WKUP_GPIO0_16                    | 7            | IO       |                      |                              |                       |              |          |                  |                        |           |                            |             |
| B7              | MCU_OSPI0_DQS              | MCU_OSPI0_DQS                    | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_MCU  | Yes      | LVCMOS           | PU/PD                  | 0         |                            |             |
|                 |                            | MCU_HYPERBUS0_RWDS               | 1            | IO       |                      |                              |                       |              |          |                  |                        |           |                            |             |
|                 |                            | WKUP_GPIO0_18                    | 7            | IO       | pad                  |                              |                       |              |          |                  |                        |           |                            |             |
| C8              | MCU_OSPI0_LBCLKO           | MCU_OSPI0_LBCLKO                 | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_MCU  | Yes      | LVCMOS           | PU/PD                  | 0         |                            |             |
|                 |                            | MCU_HYPERBUS0_CK <sub>n</sub>    | 1            | O        |                      |                              |                       |              |          |                  |                        |           |                            |             |
|                 |                            | WKUP_GPIO0_17                    | 7            | IO       | pad                  |                              |                       |              |          |                  |                        |           |                            |             |
| D6              | MCU_OSPI0_CS <sub>n0</sub> | MCU_OSPI0_CS <sub>n0</sub>       | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_MCU  | Yes      | LVCMOS           | PU/PD                  | pad       | 1/0                        |             |
|                 |                            | MCU_HYPERBUS0_CS <sub>n0</sub>   | 1            | O        |                      |                              |                       |              |          |                  |                        |           |                            |             |
|                 |                            | WKUP_GPIO0_27                    | 7            | IO       |                      |                              |                       |              |          |                  |                        |           |                            |             |
| D7              | MCU_OSPI0_CS <sub>n1</sub> | MCU_OSPI0_CS <sub>n1</sub>       | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_MCU  | Yes      | LVCMOS           | PU/PD                  | pad       | 1/0                        |             |
|                 |                            | MCU_HYPERBUS0_RESET <sub>n</sub> | 1            | O        |                      |                              |                       |              |          |                  |                        |           |                            |             |
|                 |                            | WKUP_GPIO0_28                    | 7            | IO       |                      |                              |                       |              |          |                  |                        |           |                            |             |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2]              | SIGNAL NAME [3]                   | MUX MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUX MODE [7] | I/O VOLTAGE VALUE [8] | POWER [9]   | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RX ACTIVE/ TX DISABLE [14] | IO RET [15] |
|-----------------|----------------------------|-----------------------------------|--------------|----------|----------------------|------------------------------|-----------------------|-------------|----------|------------------|------------------------|-----------|----------------------------|-------------|
| C6              | MCU_OSPI0_CSn2             | MCU_OSPI0_CSn2                    | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_MCU | Yes      | LVCMOS           | PU/PD                  |           |                            |             |
|                 |                            | MCU_OSPI0_CSn2                    | 1            | O        |                      |                              |                       |             |          |                  |                        |           |                            |             |
|                 |                            | MCU_HYPERBUS0_RESETO <sub>n</sub> | 2            | I        |                      |                              |                       |             |          |                  |                        | I         |                            |             |
|                 |                            | MCU_HYPERBUS0_WP <sub>n</sub>     | 3            | O        |                      |                              |                       |             |          |                  |                        |           |                            |             |
|                 |                            | MCU_HYPERBUS0_CS <sub>n1</sub>    | 4            | O        |                      |                              |                       |             |          |                  |                        |           |                            |             |
|                 |                            | MCU_OSPI0_RESET_OUT0              | 6            | O        |                      |                              |                       |             |          |                  |                        |           |                            |             |
|                 |                            | WKUP_GPIO0_30                     | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
| D5              | MCU_OSPI0_CS <sub>n3</sub> | MCU_OSPI0_CS <sub>n3</sub>        | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_MCU | Yes      | LVCMOS           | PU/PD                  |           |                            |             |
|                 |                            | MCU_OSPI0_CS <sub>n3</sub>        | 1            | O        |                      |                              |                       |             |          |                  |                        |           |                            |             |
|                 |                            | MCU_HYPERBUS0_INT <sub>n</sub>    | 2            | I        |                      |                              |                       |             |          |                  |                        | I         |                            |             |
|                 |                            | MCU_HYPERBUS0_WP <sub>n</sub>     | 3            | O        |                      |                              |                       |             |          |                  |                        |           |                            |             |
|                 |                            | MCU_OSPI0_RESET_OUT1              | 5            | O        |                      |                              |                       |             |          |                  |                        |           |                            |             |
|                 |                            | MCU_OSPI0_ECC_FAIL                | 6            | I        |                      |                              |                       |             |          |                  |                        | 1         |                            |             |
|                 |                            | WKUP_GPIO0_31                     | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
| D8              | MCU_OSPI0_D0               | MCU_OSPI0_D0                      | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_MCU | Yes      | LVCMOS           | PU/PD                  | 0         | 1/0                        |             |
|                 |                            | MCU_HYPERBUS0_DQ0                 | 1            | IO       |                      |                              |                       |             |          |                  |                        | 0         |                            |             |
|                 |                            | WKUP_GPIO0_19                     | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
|                 |                            | BOOTMODE00                        | Bootstrap    | I        |                      |                              |                       |             |          |                  |                        |           |                            |             |
| C7              | MCU_OSPI0_D1               | MCU_OSPI0_D1                      | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_MCU | Yes      | LVCMOS           | PU/PD                  | 0         | 1/0                        |             |
|                 |                            | MCU_HYPERBUS0_DQ1                 | 1            | IO       |                      |                              |                       |             |          |                  |                        | 0         |                            |             |
|                 |                            | WKUP_GPIO0_20                     | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
|                 |                            | BOOTMODE01                        | Bootstrap    | I        |                      |                              |                       |             |          |                  |                        |           |                            |             |
| C5              | MCU_OSPI0_D2               | MCU_OSPI0_D2                      | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_MCU | Yes      | LVCMOS           | PU/PD                  | 0         | 1/0                        |             |
|                 |                            | MCU_HYPERBUS0_DQ2                 | 1            | IO       |                      |                              |                       |             |          |                  |                        | 0         |                            |             |
|                 |                            | WKUP_GPIO0_21                     | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
| A5              | MCU_OSPI0_D3               | MCU_OSPI0_D3                      | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_MCU | Yes      | LVCMOS           | PU/PD                  | 0         | 1/0                        |             |
|                 |                            | MCU_HYPERBUS0_DQ3                 | 1            | IO       |                      |                              |                       |             |          |                  |                        | 0         |                            |             |
|                 |                            | WKUP_GPIO0_22                     | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
| A6              | MCU_OSPI0_D4               | MCU_OSPI0_D4                      | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_MCU | Yes      | LVCMOS           | PU/PD                  | 0         | 1/0                        |             |
|                 |                            | MCU_HYPERBUS0_DQ4                 | 1            | IO       |                      |                              |                       |             |          |                  |                        | 0         |                            |             |
|                 |                            | WKUP_GPIO0_23                     | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
|                 |                            | BOOTMODE02                        | Bootstrap    | I        |                      |                              |                       |             |          |                  |                        |           |                            |             |
| B8              | MCU_OSPI0_D5               | MCU_OSPI0_D5                      | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_MCU | Yes      | LVCMOS           | PU/PD                  | 0         | 1/0                        |             |
|                 |                            | MCU_HYPERBUS0_DQ5                 | 1            | IO       |                      |                              |                       |             |          |                  |                        | 0         |                            |             |
|                 |                            | WKUP_GPIO0_24                     | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
|                 |                            | BOOTMODE03                        | Bootstrap    | I        |                      |                              |                       |             |          |                  |                        |           |                            |             |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2]     | SIGNAL NAME [3]   | MUX MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUX MODE [7] | I/O VOLTAGE VALUE [8] | POWER [9]                | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RX ACTIVE/ TX DISABLE [14] | IO RET [15] |
|-----------------|-------------------|-------------------|--------------|----------|----------------------|------------------------------|-----------------------|--------------------------|----------|------------------|------------------------|-----------|----------------------------|-------------|
| A8              | MCU_OSPI0_D6      | MCU_OSPI0_D6      | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_MCU              | Yes      | LVCMOS           | PU/PD                  | 0         | 1/0                        |             |
|                 |                   | MCU_HYPERBUS0_DQ6 | 1            | IO       |                      |                              |                       |                          |          |                  |                        | 0         |                            |             |
|                 |                   | WKUP_GPIO0_25     | 7            | IO       |                      |                              |                       |                          |          |                  |                        | pad       |                            |             |
| A7              | MCU_OSPI0_D7      | MCU_OSPI0_D7      | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV1_MCU              | Yes      | LVCMOS           | PU/PD                  | 0         | 1/0                        |             |
|                 |                   | MCU_HYPERBUS0_DQ7 | 1            | IO       |                      |                              |                       |                          |          |                  |                        | 0         |                            |             |
|                 |                   | WKUP_GPIO0_26     | 7            | IO       |                      |                              |                       |                          |          |                  |                        | pad       |                            |             |
| G19             | MCU_PORz          | MCU_PORz          |              | I        |                      |                              | 1.8 V                 | VDDA_WKUP, VDDA_POR_WKUP | Yes      | FS RESET         |                        |           |                            |             |
| B13             | MCU_RESETSTATz    | MCU_RESETSTATz    | 0            | O        | PD                   | 0                            | 1.8 V/3.3 V           | VDDSHV0_MCU              | Yes      | LVCMOS           | PU/PD                  |           |                            |             |
|                 |                   | WKUP_GPIO0_79     | 7            | IO       |                      |                              |                       |                          |          |                  |                        | pad       |                            |             |
| A18             | MCU_RESETz        | MCU_RESETz        | 0            | I        |                      | 0                            | 1.8 V/3.3 V           | VDDSHV0_MCU              | Yes      | LVCMOS           | PU/PD                  |           |                            |             |
| B10             | MCU_RGMII1_RXC    | MCU_RGMII1_RXC    | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2_MCU              | Yes      | LVCMOS           | PU/PD                  | 0         | 1/0                        |             |
|                 |                   | MCU_RMII1_REF_CLK | 1            | I        |                      |                              |                       |                          |          |                  |                        | 0         |                            |             |
|                 |                   | WKUP_GPIO0_49     | 7            | IO       |                      |                              |                       |                          |          |                  |                        | pad       |                            |             |
| A11             | MCU_RGMII1_RX_CTL | MCU_RGMII1_RX_CTL | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2_MCU              | Yes      | LVCMOS           | PU/PD                  | 0         | 1/0                        |             |
|                 |                   | MCU_RMII1_RX_ER   | 1            | I        |                      |                              |                       |                          |          |                  |                        | 0         |                            |             |
|                 |                   | WKUP_GPIO0_43     | 7            | IO       |                      |                              |                       |                          |          |                  |                        | pad       |                            |             |
| A12             | MCU_RGMII1_TXC    | MCU_RGMII1_TXC    | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2_MCU              | Yes      | LVCMOS           | PU/PD                  |           | 1/0                        |             |
|                 |                   | MCU_RMII1_TX_EN   | 1            | O        |                      |                              |                       |                          |          |                  |                        |           |                            |             |
|                 |                   | WKUP_GPIO0_48     | 7            | IO       |                      |                              |                       |                          |          |                  |                        | pad       |                            |             |
| D11             | MCU_RGMII1_TX_CTL | MCU_RGMII1_TX_CTL | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2_MCU              | Yes      | LVCMOS           | PU/PD                  |           | 1/0                        |             |
|                 |                   | MCU_RMII1_CRD_DV  | 1            | I        |                      |                              |                       |                          |          |                  |                        | 0         |                            |             |
|                 |                   | WKUP_GPIO0_29     | 7            | IO       |                      |                              |                       |                          |          |                  |                        | pad       |                            |             |
| A9              | MCU_RGMII1_RD0    | MCU_RGMII1_RD0    | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2_MCU              | Yes      | LVCMOS           | PU/PD                  | 0         | 1/0                        |             |
|                 |                   | MCU_RMII1_RXD0    | 1            | I        |                      |                              |                       |                          |          |                  |                        | 0         |                            |             |
|                 |                   | WKUP_GPIO0_53     | 7            | IO       |                      |                              |                       |                          |          |                  |                        | pad       |                            |             |
| B9              | MCU_RGMII1_RD1    | MCU_RGMII1_RD1    | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2_MCU              | Yes      | LVCMOS           | PU/PD                  | 0         | 1/0                        |             |
|                 |                   | MCU_RMII1_RXD1    | 1            | I        |                      |                              |                       |                          |          |                  |                        | 0         |                            |             |
|                 |                   | WKUP_GPIO0_52     | 7            | IO       |                      |                              |                       |                          |          |                  |                        | pad       |                            |             |
| A10             | MCU_RGMII1_RD2    | MCU_RGMII1_RD2    | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2_MCU              | Yes      | LVCMOS           | PU/PD                  | 0         | 1/0                        |             |
|                 |                   | MCU_TIMER_IO5     | 1            | IO       |                      |                              |                       |                          |          |                  |                        | 0         |                            |             |
|                 |                   | WKUP_GPIO0_51     | 7            | IO       |                      |                              |                       |                          |          |                  |                        | pad       |                            |             |
| C10             | MCU_RGMII1_RD3    | MCU_RGMII1_RD3    | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2_MCU              | Yes      | LVCMOS           | PU/PD                  | 0         | 1/0                        |             |
|                 |                   | MCU_TIMER_IO4     | 1            | IO       |                      |                              |                       |                          |          |                  |                        | 0         |                            |             |
|                 |                   | WKUP_GPIO0_50     | 7            | IO       |                      |                              |                       |                          |          |                  |                        | pad       |                            |             |

Table 5-1. Pin Attributes (continued)

| BALL NUMBER [1] | BALL NAME [2]     | SIGNAL NAME [3]      | MUX MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUX MODE [7] | I/O VOLTAGE VALUE [8] | POWER [9]                     | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RX ACTIVE/ TX DISABLE [14] | IO RET [15] |
|-----------------|-------------------|----------------------|--------------|----------|----------------------|------------------------------|-----------------------|-------------------------------|----------|------------------|------------------------|-----------|----------------------------|-------------|
| D10             | MCU_RGMII1_TD0    | MCU_RGMII1_TD0       | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2_MCU                   | Yes      | LVCMOS           | PU/PD                  |           | 1/0                        |             |
|                 |                   | MCU_RMII1_TXD0       | 1            | O        |                      |                              |                       |                               |          |                  |                        |           |                            |             |
|                 |                   | WKUP_GPIO0_47        | 7            | IO       |                      |                              |                       |                               |          |                  |                        | pad       |                            |             |
| B11             | MCU_RGMII1_TD1    | MCU_RGMII1_TD1       | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2_MCU                   | Yes      | LVCMOS           | PU/PD                  |           | 1/0                        |             |
|                 |                   | MCU_RMII1_TXD1       | 1            | O        |                      |                              |                       |                               |          |                  |                        |           |                            |             |
|                 |                   | WKUP_GPIO0_46        | 7            | IO       |                      |                              |                       |                               |          |                  |                        | pad       |                            |             |
| B12             | MCU_RGMII1_TD2    | MCU_RGMII1_TD2       | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2_MCU                   | Yes      | LVCMOS           | PU/PD                  |           | 1/0                        |             |
|                 |                   | MCU_TIMER_IO3        | 1            | IO       |                      |                              |                       |                               |          |                  |                        | 0         |                            |             |
|                 |                   | MCU_ADC_EXT_TRIGGER1 | 3            | I        |                      |                              |                       |                               |          |                  |                        | 0         |                            |             |
|                 |                   | WKUP_GPIO0_45        | 7            | IO       |                      |                              |                       |                               |          |                  |                        | pad       |                            |             |
| C12             | MCU_RGMII1_TD3    | MCU_RGMII1_TD3       | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2_MCU                   | Yes      | LVCMOS           | PU/PD                  |           | 1/0                        |             |
|                 |                   | MCU_TIMER_IO2        | 1            | IO       |                      |                              |                       |                               |          |                  |                        | 0         |                            |             |
|                 |                   | MCU_ADC_EXT_TRIGGER0 | 3            | I        |                      |                              |                       |                               |          |                  |                        | 0         |                            |             |
|                 |                   | WKUP_GPIO0_44        | 7            | IO       |                      |                              |                       |                               |          |                  |                        | pad       |                            |             |
| G18             | MCU_SAFETY_ERRORn | MCU_SAFETY_ERRORn    | 0            | IO       | OFF                  | 0                            | 1.8 V                 | VDDA_WKUP, VDDA_POR_WKUP      | Yes      | LVCMOS           | PU/PD                  |           |                            |             |
| C13             | MCU_SPI0_CLK      | MCU_SPI0_CLK         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_MCU                   | Yes      | LVCMOS           | PU/PD                  | 0         | 1/0                        | Yes         |
|                 |                   | WKUP_GPIO0_56        | 7            | IO       |                      |                              |                       |                               |          |                  |                        | pad       |                            |             |
|                 |                   | MCU_BOOTMODE00       | Bootstrap    | I        |                      |                              |                       |                               |          |                  |                        |           |                            |             |
| A19             | MCU_SPI0_CS0      | MCU_SPI0_CS0         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_MCU                   | Yes      | LVCMOS           | PU/PD                  | 1         | 1/0                        | Yes         |
|                 |                   | MCU_TIMER_IO1        | 4            | IO       |                      |                              |                       |                               |          |                  |                        | 0         |                            |             |
|                 |                   | WKUP_GPIO0_59        | 7            | IO       |                      |                              |                       |                               |          |                  |                        | pad       |                            |             |
| A20             | MCU_SPI0_D0       | MCU_SPI0_D0          | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_MCU                   | Yes      | LVCMOS           | PU/PD                  | 0         | 1/0                        | Yes         |
|                 |                   | WKUP_GPIO0_57        | 7            | IO       |                      |                              |                       |                               |          |                  |                        | pad       |                            |             |
|                 |                   | MCU_BOOTMODE01       | Bootstrap    | I        |                      |                              |                       |                               |          |                  |                        |           |                            |             |
| B17             | MCU_SPI0_D1       | MCU_SPI0_D1          | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_MCU                   | Yes      | LVCMOS           | PU/PD                  | 0         | 1/0                        | Yes         |
|                 |                   | MCU_TIMER_IO0        | 4            | IO       |                      |                              |                       |                               |          |                  |                        | 0         |                            |             |
|                 |                   | WKUP_GPIO0_58        | 7            | IO       |                      |                              |                       |                               |          |                  |                        | pad       |                            |             |
|                 |                   | MCU_BOOTMODE02       | Bootstrap    | I        |                      |                              |                       |                               |          |                  |                        |           |                            |             |
| P20             | MMC0_CALPAD       | MMC0_CALPAD          |              | A        |                      |                              | 1.8 V                 | VDDS_MMC0, VDDA_0P8_DLL_MM C0 |          | eMMCPHY          | PU/PD                  |           |                            |             |
| P18             | MMC0_CLK          | MMC0_CLK             |              | O        | DRIVE 0 (OFF)        |                              | 1.8 V                 | VDDS_MMC0, VDDA_0P8_DLL_MM C0 |          | eMMCPHY          | PU/PD                  |           |                            |             |
| R17             | MMC0_CMD          | MMC0_CMD             |              | IO       | DRIVE 1 (OFF)        |                              | 1.8 V                 | VDDS_MMC0, VDDA_0P8_DLL_MM C0 |          | eMMCPHY          | PU/PD                  | 1         |                            |             |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | MUX MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUX MODE [7] | I/O VOLTAGE VALUE [8] | POWER [9]                     | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RX ACTIVE/ TX DISABLE [14] | IO RET [15] |
|-----------------|---------------|-----------------|--------------|----------|----------------------|------------------------------|-----------------------|-------------------------------|----------|------------------|------------------------|-----------|----------------------------|-------------|
| P19             | MMC0_DS       | MMC0_DS         |              | IO       | PD                   |                              | 1.8 V                 | VDDS_MMC0, VDDA_0P8_DLL_MM C0 |          | eMMCPHY          | PU/PD                  | 1         |                            |             |
| P21             | MMC1_CLK      | MMC1_CLK        | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV5                       | Yes      | SDIO             | PU/PD                  | 0         |                            |             |
|                 |               | UART8_RXD       | 1            | I        |                      |                              |                       |                               |          |                  |                        | 1         |                            |             |
|                 |               | TIMER_IO4       | 3            | IO       |                      |                              |                       |                               |          |                  |                        | 0         |                            |             |
|                 |               | UART4_CTSn      | 5            | I        |                      |                              |                       |                               |          |                  |                        | 1         |                            |             |
|                 |               | GPIO0_66        | 7            | IO       |                      |                              |                       |                               |          |                  |                        | pad       |                            |             |
|                 |               | SPI1_CLK        | 8            | IO       |                      |                              |                       |                               |          |                  |                        | 0         |                            |             |
|                 |               | UART0_RTSn      | 9            | O        |                      |                              |                       |                               |          |                  |                        |           |                            |             |
| I2C6_SDA        | 10            | IOD             | 1            |          |                      |                              |                       |                               |          |                  |                        |           |                            |             |
| M20             | MMC1_CMD      | MMC1_CMD        | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV5                       | Yes      | SDIO             | PU/PD                  | 1         |                            |             |
|                 |               | UART8_TXD       | 1            | O        |                      |                              |                       |                               |          |                  |                        |           |                            |             |
|                 |               | TIMER_IO5       | 3            | IO       |                      |                              |                       |                               |          |                  |                        | 0         |                            |             |
|                 |               | UART4_RTSn      | 5            | O        |                      |                              |                       |                               |          |                  |                        |           |                            |             |
|                 |               | GPIO0_67        | 7            | IO       |                      |                              |                       |                               |          |                  |                        | pad       |                            |             |
|                 |               | SPI1_D1         | 8            | IO       |                      |                              |                       |                               |          |                  |                        | 0         |                            |             |
|                 |               | I2C6_SCL        | 10           | IOD      |                      |                              |                       |                               |          |                  |                        | 1         |                            |             |
| R16             | MMC0_DAT0     | MMC0_DAT0       |              | IO       | PU                   |                              | 1.8 V                 | VDDS_MMC0, VDDA_0P8_DLL_MM C0 |          | eMMCPHY          | PU/PD                  | 1         |                            |             |
| P17             | MMC0_DAT1     | MMC0_DAT1       |              | IO       | PU                   |                              | 1.8 V                 | VDDS_MMC0, VDDA_0P8_DLL_MM C0 |          | eMMCPHY          | PU/PD                  | 1         |                            |             |
| R18             | MMC0_DAT2     | MMC0_DAT2       |              | IO       | PU                   |                              | 1.8 V                 | VDDS_MMC0, VDDA_0P8_DLL_MM C0 |          | eMMCPHY          | PU/PD                  | 1         |                            |             |
| R20             | MMC0_DAT3     | MMC0_DAT3       |              | IO       | PU                   |                              | 1.8 V                 | VDDS_MMC0, VDDA_0P8_DLL_MM C0 |          | eMMCPHY          | PU/PD                  | 1         |                            |             |
| R19             | MMC0_DAT4     | MMC0_DAT4       |              | IO       | PU                   |                              | 1.8 V                 | VDDS_MMC0, VDDA_0P8_DLL_MM C0 |          | eMMCPHY          | PU/PD                  | 1         |                            |             |
| P16             | MMC0_DAT5     | MMC0_DAT5       |              | IO       | PU                   |                              | 1.8 V                 | VDDS_MMC0, VDDA_0P8_DLL_MM C0 |          | eMMCPHY          | PU/PD                  | 1         |                            |             |
| R21             | MMC0_DAT6     | MMC0_DAT6       |              | IO       | PU                   |                              | 1.8 V                 | VDDS_MMC0, VDDA_0P8_DLL_MM C0 |          | eMMCPHY          | PU/PD                  | 1         |                            |             |
| T21             | MMC0_DAT7     | MMC0_DAT7       |              | IO       | PU                   |                              | 1.8 V                 | VDDS_MMC0, VDDA_0P8_DLL_MM C0 |          | eMMCPHY          | PU/PD                  | 1         |                            |             |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3]   | MUX MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUX MODE [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RX ACTIVE/ TX DISABLE [14] | IO RET [15] |
|-----------------|---------------|-------------------|--------------|----------|----------------------|------------------------------|-----------------------|-----------|----------|------------------|------------------------|-----------|----------------------------|-------------|
| M19             | MMC1_DAT0     | MMC1_DAT0         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV5   | Yes      | SDIO             | PU/PD                  | 1         |                            |             |
|                 |               | UART7_RTSn        | 1            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | ECAP1_IN_APWM_OUT | 2            | IO       |                      |                              |                       |           |          |                  |                        | IO        |                            |             |
|                 |               | TIMER_IO3         | 3            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | UART4_TXD         | 5            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | GPIO0_65          | 7            | IO       |                      |                              |                       |           |          |                  |                        | pad       |                            |             |
|                 |               | SPI1_D0           | 8            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | UART5_RTSn        | 9            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | I2C4_SCL          | 10           | IOD      |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | UART2_TXD         | 11           | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
| N21             | MMC1_DAT1     | MMC1_DAT1         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV5   | Yes      | SDIO             | PU/PD                  | 1         |                            |             |
|                 |               | UART7_CTSn        | 1            | I        |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | ECAP0_IN_APWM_OUT | 2            | IO       |                      |                              |                       |           |          |                  |                        | IO        |                            |             |
|                 |               | TIMER_IO2         | 3            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | UART4_RXD         | 5            | I        |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | GPIO0_64          | 7            | IO       |                      |                              |                       |           |          |                  |                        | pad       |                            |             |
|                 |               | SPI1_CS2          | 8            | IO       |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | UART5_CTSn        | 9            | I        |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | I2C4_SDA          | 10           | IOD      |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | UART2_RXD         | 11           | I        |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
| N20             | MMC1_DAT2     | MMC1_DAT2         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV5   | Yes      | SDIO             | PU/PD                  | 1         |                            |             |
|                 |               | UART7_TXD         | 1            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | TIMER_IO1         | 3            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | GPIO0_63          | 7            | IO       |                      |                              |                       |           |          |                  |                        | pad       |                            |             |
|                 |               | SPI1_CS1          | 8            | IO       |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | CPTS0_TS_SYNC     | 9            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | I2C3_SDA          | 10           | IOD      |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | UART5_TXD         | 11           | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
| N19             | MMC1_DAT3     | MMC1_DAT3         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV5   | Yes      | SDIO             | PU/PD                  | 1         |                            |             |
|                 |               | UART7_RXD         | 1            | I        |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | PCIE1_CLKREQn     | 2            | IO       |                      |                              |                       |           |          |                  |                        | IO        |                            |             |
|                 |               | TIMER_IO0         | 3            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | GPIO0_62          | 7            | IO       |                      |                              |                       |           |          |                  |                        | pad       |                            |             |
|                 |               | SPI1_CS0          | 8            | IO       |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | UART0_CTSn        | 9            | I        |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | I2C3_SCL          | 10           | IOD      |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | UART5_RXD         | 11           | I        |                      |                              |                       |           |          |                  |                        | 1         |                            |             |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2]  | SIGNAL NAME [3]    | MUX MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUX MODE [7] | I/O VOLTAGE VALUE [8] | POWER [9]                | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RX ACTIVE/ TX DISABLE [14] | IO RET [15] |
|-----------------|----------------|--------------------|--------------|----------|----------------------|------------------------------|-----------------------|--------------------------|----------|------------------|------------------------|-----------|----------------------------|-------------|
| K19             | OSC1_XI        | OSC1_XI            |              | I        |                      |                              | 1.8 V                 | VDDA_OSC1                | Yes      | HFOSC            |                        |           |                            |             |
| J19             | OSC1_XO        | OSC1_XO            |              | O        |                      |                              | 1.8 V                 | VDDA_OSC1                | Yes      | HFOSC            |                        |           |                            |             |
| C15             | PMIC_POWER_EN1 | PMIC_POWER_EN1     | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_MCU              | Yes      | LVCMOS           | PU/PD                  |           |                            | Yes         |
|                 |                | MCU_I3C0_SDAPULLEN | 5            | OD       |                      |                              |                       |                          |          |                  |                        |           |                            |             |
|                 |                | WKUP_GPIO0_68      | 7            | IO       |                      |                              |                       |                          |          |                  |                        | pad       |                            |             |
| T19             | PMIC_WAKE0n    | PMIC_WAKE0n        | 0            | OD       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2                  | Yes      | LVCMOS           | PU/PD                  |           |                            |             |
|                 |                | RGMI4_TD1          | 4            | O        |                      |                              |                       |                          |          |                  |                        |           |                            |             |
|                 |                | GPIO0_1            | 7            | IO       |                      |                              |                       |                          |          |                  |                        | pad       |                            |             |
| H20             | PORz           | PORz               | 0            | I        |                      | 0                            | 1.8 V                 | VDDA_WKUP, VDDA_POR_WKUP | Yes      | FS RESET         |                        |           |                            |             |
| U2              | RESETSTATz     | RESETSTATz         | 0            | O        | PD                   | 0                            | 1.8 V/3.3 V           | VDDSHV0                  | Yes      | LVCMOS           | PU/PD                  |           |                            |             |
| A15             | RESET_REQz     | RESET_REQz         | 0            | I        | OFF                  | 0                            | 1.8 V/3.3 V           | VDDSHV0_MCU              | Yes      | LVCMOS           | PU/PD                  |           |                            |             |
| AA20            | RMII1_CRS_DV   | RMII1_CRS_DV       | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2                  | Yes      | LVCMOS           | PU/PD                  | 0         | 1/0                        | Yes         |
|                 |                | RGMI1_RD2          | 4            | I        |                      |                              |                       |                          |          |                  |                        | 0         |                            |             |
|                 |                | RMII1_CRS_DV       | 5            | I        |                      |                              |                       |                          |          |                  |                        | 0         |                            |             |
|                 |                | GPIO0_4            | 7            | IO       |                      |                              |                       |                          |          |                  |                        | pad       |                            |             |
|                 |                | EHRPWM2_B          | 9            | IO       |                      |                              |                       |                          |          |                  |                        | 0         |                            |             |
|                 |                | TRC_DATA7          | 10           | O        |                      |                              |                       |                          |          |                  |                        |           |                            |             |
|                 |                | UART4_TXD          | 11           | O        |                      |                              |                       |                          |          |                  |                        |           |                            |             |
|                 |                | MCASP1_AXR1        | 12           | IO       |                      |                              |                       |                          |          |                  |                        | 0         |                            |             |
|                 |                | GPMC0_AD2          | 14           | IO       |                      |                              |                       |                          |          |                  |                        | 0         |                            |             |
| Y17             | RMII1_RX_ER    | RMII1_RX_ER        | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2                  | Yes      | LVCMOS           | PU/PD                  | 0         | 1/0                        | Yes         |
|                 |                | RGMI1_RD3          | 4            | I        |                      |                              |                       |                          |          |                  |                        | 0         |                            |             |
|                 |                | RMII1_RX_ER        | 5            | I        |                      |                              |                       |                          |          |                  |                        | 0         |                            |             |
|                 |                | GPIO0_5            | 7            | IO       |                      |                              |                       |                          |          |                  |                        | pad       |                            |             |
|                 |                | EHRPWM2_A          | 9            | IO       |                      |                              |                       |                          |          |                  |                        | 0         |                            |             |
|                 |                | TRC_DATA6          | 10           | O        |                      |                              |                       |                          |          |                  |                        |           |                            |             |
|                 |                | UART6_TXD          | 11           | O        |                      |                              |                       |                          |          |                  |                        |           |                            |             |
|                 |                | MCASP1_AXR0        | 12           | IO       |                      |                              |                       |                          |          |                  |                        | 0         |                            |             |
|                 |                | GPMC0_AD3          | 14           | IO       |                      |                              |                       |                          |          |                  |                        | 0         |                            |             |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | MUX MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUX MODE [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RX ACTIVE/ TX DISABLE [14] | IO RET [15] |
|-----------------|---------------|-----------------|--------------|----------|----------------------|------------------------------|-----------------------|-----------|----------|------------------|------------------------|-----------|----------------------------|-------------|
| V17             | RMII1_TX_EN   | RMII1_TX_EN     | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   |          | LVCMOS           | PU/PD                  |           | 1/0                        | Yes         |
|                 |               | RGMI14_RXC      | 4            | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | RMII1_TX_EN     | 5            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | GPIO0_7         | 7            | IO       |                      |                              |                       |           |          |                  |                        | pad       |                            |             |
|                 |               | EQEP2_A         | 9            | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | UART9_TXD       | 11           | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | MCASP0_AXR8     | 12           | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | I2C1_SCL        | 13           | IOD      |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
| GPMC0_AD5       | 14            | IO              | 0            |          |                      |                              |                       |           |          |                  |                        |           |                            |             |
| AA17            | RMII1_RXD0    | RMII1_RXD0      | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   |          | LVCMOS           | PU/PD                  | 0         | 1/0                        | Yes         |
|                 |               | RGMI1_RD0       | 4            | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | RMII1_RXD0      | 5            | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | MCAN14_TX       | 6            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | GPIO0_2         | 7            | IO       |                      |                              |                       |           |          |                  |                        | pad       |                            |             |
|                 |               | TRC_DATA9       | 10           | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | UART5_TXD       | 11           | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | MCASP1_AXR3     | 12           | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
| GPMC0_AD0       | 14            | IO              | 0            |          |                      |                              |                       |           |          |                  |                        |           |                            |             |
| Y15             | RMII1_RXD1    | RMII1_RXD1      | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   |          | LVCMOS           | PU/PD                  | 0         | 1/0                        | Yes         |
|                 |               | RGMI1_RD1       | 4            | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | RMII1_RXD1      | 5            | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | MCAN14_RX       | 6            | I        |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | GPIO0_3         | 7            | IO       |                      |                              |                       |           |          |                  |                        | pad       |                            |             |
|                 |               | EHRPWM_TZn_IN2  | 9            | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | TRC_DATA8       | 10           | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | UART5_RXD       | 11           | I        |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | MCASP1_AXR2     | 12           | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | GPMC0_AD1       | 14           | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
| Y16             | RMII1_TXD0    | RMII1_TXD0      | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   |          | LVCMOS           | PU/PD                  |           | 1/0                        | Yes         |
|                 |               | RGMI1_RX_CTL    | 4            | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | RMII1_TXD0      | 5            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | GPIO0_6         | 7            | IO       |                      |                              |                       |           |          |                  |                        | pad       |                            |             |
|                 |               | EHRPWM0_SYNCO   | 9            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | TRC_CTL         | 10           | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | UART6_RXD       | 11           | I        |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | MCASP0_AFSX     | 12           | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
| GPMC0_AD4       | 14            | IO              | 0            |          |                      |                              |                       |           |          |                  |                        |           |                            |             |

Table 5-1. Pin Attributes (continued)

| BALL NUMBER [1] | BALL NAME [2]    | SIGNAL NAME [3]  | MUX MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUX MODE [7] | I/O VOLTAGE VALUE [8] | POWER [9]  | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RX ACTIVE/ TX DISABLE [14] | IO RET [15] |  |
|-----------------|------------------|------------------|--------------|----------|----------------------|------------------------------|-----------------------|--|----------|------------------|------------------------|-----------|----------------------------|-------------|--|
| AA19            | RMII1_TXD1       | RMII1_TXD1       | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2  | Yes      | LVCMOS           | PU/PD                  |           | 1/0                        | Yes         |  |
|                 |                  | RGMI1_RXC        | 4            | I        |                      |                              |                       |  |          |                  |                        | 0         |                            |             |  |
|                 |                  | RMII1_TXD1       | 5            | O        |                      |                              |                       |  |          |                  |                        |           |                            |             |  |
|                 |                  | GPIO0_8          | 7            | IO       |                      |                              |                       |  |          |                  |                        | pad       |                            |             |  |
|                 |                  | EHRPWM_TZn_IN1   | 9            | I        |                      |                              |                       |  |          |                  |                        | 0         |                            |             |  |
|                 |                  | TRC_DATA5        | 10           | O        |                      |                              |                       |  |          |                  |                        |           |                            |             |  |
|                 |                  | UART9_RXD        | 11           | I        |                      |                              |                       |  |          |                  |                        | 1         |                            |             |  |
|                 |                  | MCASP0_AXR3      | 12           | IO       |                      |                              |                       |  |          |                  |                        | 0         |                            |             |  |
|                 |                  | I2C1_SDA         | 13           | IOD      |                      |                              |                       |  |          |                  |                        | 1         |                            |             |  |
| GPMC0_AD6       | 14               | IO               | 0            |          |                      |                              |                       |  |          |                  |                        |           |                            |             |  |
| V7              | SERDES0_REXT     | SERDES0_REXT     |              | A        |                      |                              | 0.8 V                 | VDDA_0P8_SERDES0<br>,<br>VDDA_1P8_SERDES0<br>,<br>VDDA_0P8_SERDES0<br>_C |          | SERDES           |                        |           |                            |             |  |
| AA8             | SERDES0_REFCLK_N | SERDES0_REFCLK_N |              | IO       |                      |                              | 0.8 V                 | VDDA_0P8_SERDES0<br>,<br>VDDA_1P8_SERDES0<br>,<br>VDDA_0P8_SERDES0<br>_C |          | SERDES           |                        |           |                            |             |  |
| AA9             | SERDES0_REFCLK_P | SERDES0_REFCLK_P |              | IO       |                      |                              | 0.8 V                 | VDDA_0P8_SERDES0<br>,<br>VDDA_1P8_SERDES0<br>,<br>VDDA_0P8_SERDES0<br>_C |          | SERDES           |                        |           |                            |             |  |
| AA11            | SERDES0_RX0_N    | SERDES0_RX0_N    |              | I        |                      |                              | 0.8 V                 | VDDA_0P8_SERDES0<br>,<br>VDDA_1P8_SERDES0<br>,<br>VDDA_0P8_SERDES0<br>_C |          | SERDES           |                        |           |                            |             |  |
|                 |                  | SGMII3_RX0_N     |              | I        |                      |                              |                       |  |          |                  |                        |           |                            |             |  |
|                 |                  | PCIE1_RX0_N      |              | I        |                      |                              |                       |  |          |                  |                        |           |                            |             |  |
|                 |                  | USB0_SSRX1N      |              | I        |                      |                              |                       |  |          |                  |                        |           |                            |             |  |
| AA12            | SERDES0_RX0_P    | SERDES0_RX0_P    |              | I        |                      |                              | 0.8 V                 | VDDA_0P8_SERDES0<br>,<br>VDDA_1P8_SERDES0<br>,<br>VDDA_0P8_SERDES0<br>_C |          | SERDES           |                        |           |                            |             |  |
|                 |                  | SGMII3_RX0_P     |              | I        |                      |                              |                       |  |          |                  |                        |           |                            |             |  |
|                 |                  | PCIE1_RX0_P      |              | I        |                      |                              |                       |  |          |                  |                        |           |                            |             |  |
|                 |                  | USB0_SSRX1P      |              | I        |                      |                              |                       |  |          |                  |                        |           |                            |             |  |
| W8              | SERDES0_RX1_N    | SERDES0_RX1_N    |              | I        |                      |                              | 0.8 V                 | VDDA_0P8_SERDES0<br>,<br>VDDA_1P8_SERDES0<br>,<br>VDDA_0P8_SERDES0<br>_C |          | SERDES           |                        |           |                            |             |  |
|                 |                  | SGMII4_RX0_N     |              | I        |                      |                              |                       |  |          |                  |                        |           |                            |             |  |
|                 |                  | PCIE1_RX1_N      |              | I        |                      |                              |                       |  |          |                  |                        |           |                            |             |  |
|                 |                  | USB0_SSRX2N      |              | I        |                      |                              |                       |  |          |                  |                        |           |                            |             |  |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | MUX MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUX MODE [7] | I/O VOLTAGE VALUE [8] | POWER [9]          | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RX ACTIVE/ TX DISABLE [14] | IO RET [15] |
|-----------------|---------------|-----------------|--------------|----------|----------------------|------------------------------|-----------------------|--------------------|----------|------------------|------------------------|-----------|----------------------------|-------------|
| W9              | SERDES0_RX1_P | SERDES0_RX1_P   |              | I        |                      |                              | 0.8 V                 | VDDA_0P8_SERDES0   |          | SERDES           |                        |           |                            |             |
|                 |               | SGMII4_RX0_P    |              | I        |                      |                              |                       | VDDA_1P8_SERDES0   |          |                  |                        |           |                            |             |
|                 |               | PCIE1_RX1_P     |              | I        |                      |                              |                       | VDDA_0P8_SERDES0_C |          |                  |                        |           |                            |             |
|                 |               | USB0_SSRX2P     |              | I        |                      |                              |                       |                    |          |                  |                        |           |                            |             |
| Y7              | SERDES0_RX2_N | SERDES0_RX2_N   |              | I        |                      |                              | 0.8 V                 | VDDA_0P8_SERDES0   |          | SERDES           |                        |           |                            |             |
|                 |               | SGMII1_RX0_N    |              | I        |                      |                              |                       | VDDA_1P8_SERDES0   |          |                  |                        |           |                            |             |
|                 |               | PCIE1_RX2_N     |              | I        |                      |                              |                       | VDDA_0P8_SERDES0_C |          |                  |                        |           |                            |             |
|                 |               | USB0_SSRX1N     |              | I        |                      |                              |                       |                    |          |                  |                        |           |                            |             |
| Y8              | SERDES0_RX2_P | SERDES0_RX2_P   |              | I        |                      |                              | 0.8 V                 | VDDA_0P8_SERDES0   |          | SERDES           |                        |           |                            |             |
|                 |               | SGMII1_RX0_P    |              | I        |                      |                              |                       | VDDA_1P8_SERDES0   |          |                  |                        |           |                            |             |
|                 |               | PCIE1_RX2_P     |              | I        |                      |                              |                       | VDDA_0P8_SERDES0_C |          |                  |                        |           |                            |             |
|                 |               | USB0_SSRX1P     |              | I        |                      |                              |                       |                    |          |                  |                        |           |                            |             |
| W5              | SERDES0_RX3_N | SERDES0_RX3_N   |              | I        |                      |                              | 0.8 V                 | VDDA_0P8_SERDES0   |          | SERDES           |                        |           |                            |             |
|                 |               | SGMII2_RX0_N    |              | I        |                      |                              |                       | VDDA_1P8_SERDES0   |          |                  |                        |           |                            |             |
|                 |               | PCIE1_RX3_N     |              | I        |                      |                              |                       | VDDA_0P8_SERDES0_C |          |                  |                        |           |                            |             |
|                 |               | USB0_SSRX2N     |              | I        |                      |                              |                       |                    |          |                  |                        |           |                            |             |
| W6              | SERDES0_RX3_P | SERDES0_RX3_P   |              | I        |                      |                              | 0.8 V                 | VDDA_0P8_SERDES0   |          | SERDES           |                        |           |                            |             |
|                 |               | SGMII2_RX0_P    |              | I        |                      |                              |                       | VDDA_1P8_SERDES0   |          |                  |                        |           |                            |             |
|                 |               | PCIE1_RX3_P     |              | I        |                      |                              |                       | VDDA_0P8_SERDES0_C |          |                  |                        |           |                            |             |
|                 |               | USB0_SSRX2P     |              | I        |                      |                              |                       |                    |          |                  |                        |           |                            |             |
| W11             | SERDES0_TX0_N | SERDES0_TX0_N   |              | O        |                      |                              | 0.8 V                 | VDDA_0P8_SERDES0   |          | SERDES           |                        |           |                            |             |
|                 |               | SGMII3_TX0_N    |              | O        |                      |                              |                       | VDDA_1P8_SERDES0   |          |                  |                        |           |                            |             |
|                 |               | PCIE1_TX0_N     |              | O        |                      |                              |                       | VDDA_0P8_SERDES0_C |          |                  |                        |           |                            |             |
|                 |               | USB0_SSTX1N     |              | O        |                      |                              |                       |                    |          |                  |                        |           |                            |             |
| W12             | SERDES0_TX0_P | SERDES0_TX0_P   |              | O        |                      |                              | 0.8 V                 | VDDA_0P8_SERDES0   |          | SERDES           |                        |           |                            |             |
|                 |               | SGMII3_TX0_P    |              | O        |                      |                              |                       | VDDA_1P8_SERDES0   |          |                  |                        |           |                            |             |
|                 |               | PCIE1_TX0_P     |              | O        |                      |                              |                       | VDDA_0P8_SERDES0_C |          |                  |                        |           |                            |             |
|                 |               | USB0_SSTX1P     |              | O        |                      |                              |                       |                    |          |                  |                        |           |                            |             |
| Y10             | SERDES0_TX1_N | SERDES0_TX1_N   |              | O        |                      |                              | 0.8 V                 | VDDA_0P8_SERDES0   |          | SERDES           |                        |           |                            |             |
|                 |               | SGMII4_TX0_N    |              | O        |                      |                              |                       | VDDA_1P8_SERDES0   |          |                  |                        |           |                            |             |
|                 |               | PCIE1_TX1_N     |              | O        |                      |                              |                       | VDDA_0P8_SERDES0_C |          |                  |                        |           |                            |             |
|                 |               | USB0_SSTX2N     |              | O        |                      |                              |                       |                    |          |                  |                        |           |                            |             |
| Y11             | SERDES0_TX1_P | SERDES0_TX1_P   |              | O        |                      |                              | 0.8 V                 | VDDA_0P8_SERDES0   |          | SERDES           |                        |           |                            |             |
|                 |               | SGMII4_TX0_P    |              | O        |                      |                              |                       | VDDA_1P8_SERDES0   |          |                  |                        |           |                            |             |
|                 |               | PCIE1_TX1_P     |              | O        |                      |                              |                       | VDDA_0P8_SERDES0_C |          |                  |                        |           |                            |             |
|                 |               | USB0_SSTX2P     |              | O        |                      |                              |                       |                    |          |                  |                        |           |                            |             |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2]     | SIGNAL NAME [3]   | MUX MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUX MODE [7] | I/O VOLTAGE VALUE [8] | POWER [9]        | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RX ACTIVE/ TX DISABLE [14] | IO RET [15] |
|-----------------|-------------------|-------------------|--------------|----------|----------------------|------------------------------|-----------------------|------------------|----------|------------------|------------------------|-----------|----------------------------|-------------|
| AA5             | SERDES0_TX2_N     | SERDES0_TX2_N     |              | O        |                      |                              | 0.8 V                 | VDDA_0P8_SERDES0 |          | SERDES           |                        |           |                            |             |
|                 |                   | SGMII1_TX0_N      |              | O        |                      | VDDA_1P8_SERDES0             |                       |                  |          |                  |                        |           |                            |             |
|                 |                   | PCIE1_TX2_N       |              | O        |                      | VDDA_0P8_SERDES0             |                       |                  |          |                  |                        |           |                            |             |
|                 |                   | USB0_SSTX1N       |              | O        |                      | _C                           |                       |                  |          |                  |                        |           |                            |             |
| AA6             | SERDES0_TX2_P     | SERDES0_TX2_P     |              | O        |                      |                              | 0.8 V                 | VDDA_0P8_SERDES0 |          | SERDES           |                        |           |                            |             |
|                 |                   | SGMII1_TX0_P      |              | O        |                      | VDDA_1P8_SERDES0             |                       |                  |          |                  |                        |           |                            |             |
|                 |                   | PCIE1_TX2_P       |              | O        |                      | VDDA_0P8_SERDES0             |                       |                  |          |                  |                        |           |                            |             |
|                 |                   | USB0_SSTX1P       |              | O        |                      | _C                           |                       |                  |          |                  |                        |           |                            |             |
| Y4              | SERDES0_TX3_N     | SERDES0_TX3_N     |              | O        |                      |                              | 0.8 V                 | VDDA_0P8_SERDES0 |          | SERDES           |                        |           |                            |             |
|                 |                   | SGMII2_TX0_N      |              | O        |                      | VDDA_1P8_SERDES0             |                       |                  |          |                  |                        |           |                            |             |
|                 |                   | PCIE1_TX3_N       |              | O        |                      | VDDA_0P8_SERDES0             |                       |                  |          |                  |                        |           |                            |             |
|                 |                   | USB0_SSTX2N       |              | O        |                      | _C                           |                       |                  |          |                  |                        |           |                            |             |
| Y5              | SERDES0_TX3_P     | SERDES0_TX3_P     |              | O        |                      |                              | 0.8 V                 | VDDA_0P8_SERDES0 |          | SERDES           |                        |           |                            |             |
|                 |                   | SGMII2_TX0_P      |              | O        |                      | VDDA_1P8_SERDES0             |                       |                  |          |                  |                        |           |                            |             |
|                 |                   | PCIE1_TX3_P       |              | O        |                      | VDDA_0P8_SERDES0             |                       |                  |          |                  |                        |           |                            |             |
|                 |                   | USB0_SSTX2P       |              | O        |                      | _C                           |                       |                  |          |                  |                        |           |                            |             |
| V2              | SOC_SAFETY_ERRORn | SOC_SAFETY_ERRORn | 0            | IO       | OFF                  | 0                            | 1.8 V/3.3 V           | VDDSHV0          | Yes      | LVCMOS           | PU/PD                  |           |                            |             |
| Y1              | SPI0_CLK          | SPI0_CLK          | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0          | Yes      | LVCMOS           | PU/PD                  | 0         |                            |             |
|                 |                   | UART1_CTSn        | 1            | I        |                      | 1                            |                       |                  |          |                  |                        |           |                            |             |
|                 |                   | I2C2_SCL          | 2            | IOD      |                      | IOD                          |                       |                  |          |                  |                        |           |                            |             |
|                 |                   | GPIO0_53          | 7            | IO       |                      | pad                          |                       |                  |          |                  |                        |           |                            |             |
| W3              | SPI0_CS0          | SPI0_CS0          | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0          | Yes      | LVCMOS           | PU/PD                  | 1         |                            |             |
|                 |                   | UART0_CTSn        | 2            | I        |                      | I                            |                       |                  |          |                  |                        |           |                            |             |
|                 |                   | GPIO0_51          | 7            | IO       |                      | pad                          |                       |                  |          |                  |                        |           |                            |             |
| U5              | SPI0_CS1          | SPI0_CS1          | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0          | Yes      | LVCMOS           | PU/PD                  | 1         |                            |             |
|                 |                   | CPTS0_TS_COMP     | 1            | O        |                      |                              |                       |                  |          |                  |                        |           |                            |             |
|                 |                   | UART0_RTSn        | 2            | O        |                      | O                            |                       |                  |          |                  |                        |           |                            |             |
|                 |                   | GPIO0_52          | 7            | IO       |                      | pad                          |                       |                  |          |                  |                        |           |                            |             |
| V4              | SPI0_D0           | SPI0_D0           | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0          | Yes      | LVCMOS           | PU/PD                  | 0         |                            |             |
|                 |                   | UART1_RTSn        | 1            | O        |                      |                              |                       |                  |          |                  |                        |           |                            |             |
|                 |                   | I2C2_SDA          | 2            | IOD      |                      | IOD                          |                       |                  |          |                  |                        |           |                            |             |
|                 |                   | GPIO0_54          | 7            | IO       |                      | pad                          |                       |                  |          |                  |                        |           |                            |             |
| T5              | SPI0_D1           | SPI0_D1           | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0          | Yes      | LVCMOS           | PU/PD                  | 0         |                            |             |
|                 |                   | GPIO0_55          | 7            | IO       |                      | pad                          |                       |                  |          |                  |                        |           |                            |             |
| B15             | TCK               | TCK               | 0            | I        |                      | 0                            | 1.8 V/3.3 V           | VDDSHV0_MCU      | Yes      | LVCMOS           | PU/PD                  |           |                            |             |
| F19             | TDI               | TDI               | 0            | I        | OFF                  | 0                            | 1.8 V/3.3 V           | VDDSHV0_MCU      | Yes      | LVCMOS           | PU/PD                  |           |                            |             |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3]   | MUX MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUX MODE [7] | I/O VOLTAGE VALUE [8] | POWER [9]   | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RX ACTIVE/ TX DISABLE [14] | IO RET [15] |
|-----------------|---------------|-------------------|--------------|----------|----------------------|------------------------------|-----------------------|-------------|----------|------------------|------------------------|-----------|----------------------------|-------------|
| F21             | TDO           | TDO               | 0            | OZ       | OFF                  | 0                            | 1.8 V/3.3 V           | VDDSHV0_MCU | Yes      | LVCMOS           | PU/PD                  |           |                            |             |
| V1              | TIMER_IO0     | TIMER_IO0         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0     | Yes      | LVCMOS           | PU/PD                  | 0         |                            |             |
|                 |               | ECAP1_IN_APWM_OUT | 1            | IO       |                      |                              |                       |             |          |                  |                        | 0         |                            |             |
|                 |               | SYSCLKOUT0        | 2            | O        |                      |                              |                       |             |          |                  |                        | O         |                            |             |
|                 |               | UART3_CTSn        | 5            | I        |                      |                              |                       |             |          |                  |                        | 1         |                            |             |
|                 |               | SPI7_D0           | 6            | IO       |                      |                              |                       |             |          |                  |                        | 0         |                            |             |
|                 |               | GPIO0_60          | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
|                 |               | MMC1_SDCD         | 8            | I        |                      |                              |                       |             |          |                  |                        | 1         |                            |             |
| W1              | TIMER_IO1     | TIMER_IO1         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0     | Yes      | LVCMOS           | PU/PD                  | 0         | 0/0                        |             |
|                 |               | ECAP2_IN_APWM_OUT | 1            | IO       |                      |                              |                       |             |          |                  |                        | 0         |                            |             |
|                 |               | OBSCLK0           | 2            | O        |                      |                              |                       |             |          |                  |                        | O         |                            |             |
|                 |               | UART3_RTSn        | 5            | O        |                      |                              |                       |             |          |                  |                        |           |                            |             |
|                 |               | SPI7_D1           | 6            | IO       |                      |                              |                       |             |          |                  |                        | 0         |                            |             |
|                 |               | GPIO0_61          | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
|                 |               | MMC1_SDWP         | 8            | I        |                      |                              |                       |             |          |                  |                        | 1         |                            |             |
|                 |               | PCIE1_CLKREQn     | 9            | IO       |                      |                              |                       |             |          |                  |                        | 0         |                            |             |
| U4              | TMS           | TMS               | 0            | I        | OFF                  | 0                            | 1.8 V/3.3 V           | VDDSHV0     | Yes      | LVCMOS           | PU/PD                  |           |                            |             |
| B20             | TRSTn         | TRSTn             | 0            | I        |                      | 0                            | 1.8 V/3.3 V           | VDDSHV0_MCU | Yes      | LVCMOS           | PU/PD                  |           |                            |             |
| T16             | UART0_RXD     | UART0_RXD         | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2     | Yes      | LVCMOS           | PU/PD                  | 1         | 0/0                        | Yes         |
|                 |               | RGMI4_TXC         | 4            | O        |                      |                              |                       |             |          |                  |                        |           |                            |             |
|                 |               | GPIO0_47          | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
|                 |               | GPMC0_WAIT0       | 14           | I        |                      |                              |                       |             |          |                  |                        | 0         |                            |             |
| T17             | UART0_TXD     | UART0_TXD         | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2     | Yes      | LVCMOS           | PU/PD                  |           |                            | Yes         |
|                 |               | RGMI4_TD2         | 4            | O        |                      |                              |                       |             |          |                  |                        |           |                            |             |
|                 |               | GPIO0_48          | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
|                 |               | GPMC0_WEn         | 14           | O        |                      |                              |                       |             |          |                  |                        |           |                            |             |
| T18             | UART1_RXD     | UART1_RXD         | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2     | Yes      | LVCMOS           | PU/PD                  | 1         |                            | Yes         |
|                 |               | MCAN17_TX         | 1            | O        |                      |                              |                       |             |          |                  |                        |           |                            |             |
|                 |               | TIMER_IO6         | 3            | IO       |                      |                              |                       |             |          |                  |                        | 0         |                            |             |
|                 |               | RGMI4_TD3         | 4            | O        |                      |                              |                       |             |          |                  |                        |           |                            |             |
|                 |               | GPIO0_49          | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
|                 |               | GPMC0_OEn_REn     | 14           | O        |                      |                              |                       |             |          |                  |                        |           |                            |             |

Table 5-1. Pin Attributes (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3] | MUX MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUX MODE [7] | I/O VOLTAGE VALUE [8] | POWER [9] | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RX ACTIVE/ TX DISABLE [14] | IO RET [15] |
|-----------------|---------------|-----------------|--------------|----------|----------------------|------------------------------|-----------------------|-----------|----------|------------------|------------------------|-----------|----------------------------|-------------|
| T20             | UART1_TXD     | UART1_TXD       | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                  |           |                            | Yes         |
|                 |               | MCAN17_RX       | 1            | I        |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | TIMER_I07       | 3            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | RGMI14_TX_CTL   | 4            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | GPIO0_50        | 7            | IO       |                      |                              |                       |           |          |                  |                        | pad       |                            |             |
|                 |               | GPMC0_CSn0      | 14           | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
| V14             | UART2_RXD     | UART2_RXD       | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                  | 1         | 0/0                        | Yes         |
|                 |               | RGMI12_TD2      | 4            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | RMII2_CRD_DV    | 5            | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | GPIO0_39        | 7            | IO       |                      |                              |                       |           |          |                  |                        | pad       |                            |             |
|                 |               | SPI6_CLK        | 8            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | GPMC0_CLKOUT    | 9            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | GPMC0_FCLK_MUX  | 10           | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | UART2_RXD       | 11           | I        |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | MCASP2_AXR3     | 12           | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | OBSCLK2         | 14           | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
| V13             | UART2_TXD     | UART2_TXD       | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                  |           |                            | Yes         |
|                 |               | RGMI12_TD3      | 4            | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | RMII2_RX_ER     | 5            | I        |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | GPIO0_40        | 7            | IO       |                      |                              |                       |           |          |                  |                        | pad       |                            |             |
|                 |               | SPI6_D0         | 8            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | UART2_TXD       | 11           | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | MCASP2_AFSX     | 12           | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
| W14             | UART8_RXD     | UART8_RXD       | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   | Yes      | LVCMOS           | PU/PD                  | 1         |                            | Yes         |
|                 |               | I2C4_SCL        | 2            | IOD      |                      |                              |                       |           |          |                  |                        | IOD       |                            |             |
|                 |               | MDIO0_MDIO      | 5            | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | GPIO0_42        | 7            | IO       |                      |                              |                       |           |          |                  |                        | pad       |                            |             |
|                 |               | TRC_DATA22      | 10           | O        |                      |                              |                       |           |          |                  |                        |           |                            |             |
|                 |               | UART8_RXD       | 11           | I        |                      |                              |                       |           |          |                  |                        | 1         |                            |             |
|                 |               | MCASP2_AFSR     | 12           | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |
|                 |               | MCASP2_AXR4     | 13           | IO       |                      |                              |                       |           |          |                  |                        | 0         |                            |             |

Table 5-1. Pin Attributes (continued)

| BALL NUMBER [1] | BALL NAME [2]      | SIGNAL NAME [3]    | MUX MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUX MODE [7] | I/O VOLTAGE VALUE [8] | POWER [9]                                       | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RX ACTIVE/ TX DISABLE [14] | IO RET [15] |
|-----------------|--------------------|--------------------|--------------|----------|----------------------|------------------------------|-----------------------|---|----------|------------------|------------------------|-----------|----------------------------|-------------|
| W19             | UART8_TXD          | UART8_TXD          | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV2   |          | LVCMOS           | PU/PD                  |           |                            | Yes         |
|                 |                    | SPI1_CS3           | 1            | IO       |                      |                              |                       |   |          |                  |                        | 1         |                            |             |
|                 |                    | I2C4_SDA           | 2            | IOD      |                      |                              |                       |   |          |                  |                        | IOD       |                            |             |
|                 |                    | MDIO0_MDC          | 5            | O        |                      |                              |                       |   |          |                  |                        |           |                            |             |
|                 |                    | GPIO0_43           | 7            | IO       |                      |                              |                       |   |          |                  |                        | pad       |                            |             |
|                 |                    | TRC_DATA23         | 10           | O        |                      |                              |                       |   |          |                  |                        |           |                            |             |
|                 |                    | UART8_TXD          | 11           | O        |                      |                              |                       |   |          |                  |                        |           |                            |             |
|                 |                    | MCASP2_ACLKR       | 12           | IO       |                      |                              |                       |   |          |                  |                        | 0         |                            |             |
|                 |                    | MCASP2_AXR5        | 13           | IO       |                      |                              |                       |   |          |                  |                        | 0         |                            |             |
| AA3             | USB0_DM            | USB0_DM            |              | IO       |                      |                              | 3.3 V                 | VDDA_0P8_USB ,VD<br>DA_1P8_USB,<br>VDDA_3P3_USB |          | USB2PHY          |                        |           |                            |             |
| AA2             | USB0_DP            | USB0_DP            |              | IO       |                      |                              | 3.3 V                 | VDDA_0P8_USB ,VD<br>DA_1P8_USB,<br>VDDA_3P3_USB |          | USB2PHY          |                        |           |                            |             |
| T4              | USB0_DRVVBUS       | USB0_DRVVBUS       | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0   | Yes      | LVCMOS           | PU/PD                  |           |                            |             |
|                 |                    | GPIO0_68           | 7            | IO       |                      |                              |                       |   |          |                  |                        | pad       |                            |             |
| V6              | USB0_ID            | USB0_ID            |              | A        |                      |                              | 3.3 V                 | VDDA_0P8_USB ,VD<br>DA_1P8_USB,<br>VDDA_3P3_USB |          | USB2PHY          |                        |           |                            |             |
| V5              | USB0_RCALIB        | USB0_RCALIB        |              | IO       |                      |                              | 3.3 V                 | VDDA_0P8_USB ,VD<br>DA_1P8_USB,<br>VDDA_3P3_USB |          | USB2PHY          |                        |           |                            |             |
| Y2              | USB0_VBUS          | USB0_VBUS          |              | A        |                      |                              | 5.0 V                 | VDDA_0P8_USB ,VD<br>DA_1P8_USB,<br>VDDA_3P3_USB |          | USB2PHY          |                        |           |                            |             |
| K14, P14        | VDDAR_CORE         | VDDAR_CORE         |              | PWR      |                      |                              |                       |   |          |                  |                        |           |                            |             |
| J11, M10        | VDDAR_CPU          | VDDAR_CPU          |              | PWR      |                      |                              |                       |   |          |                  |                        |           |                            |             |
| H12, J14        | VDDAR_MCU          | VDDAR_MCU          |              | PWR      |                      |                              |                       |   |          |                  |                        |           |                            |             |
| K7              | VDDA_0P8_PLL_DDR   | VDDA_0P8_PLL_DDR   |              | PWR      |                      |                              |                       |   |          |                  |                        |           |                            |             |
| P7              | VDDA_0P8_USB       | VDDA_0P8_USB       |              | PWR      |                      |                              |                       |   |          |                  |                        |           |                            |             |
| M18             | VDDA_0P8_DLL_MMC0  | VDDA_0P8_DLL_MMC0  |              | PWR      |                      |                              |                       |   |          |                  |                        |           |                            |             |
| R8, T7, U8      | VDDA_0P8_SERDES0   | VDDA_0P8_SERDES0   |              | PWR      |                      |                              |                       |   |          |                  |                        |           |                            |             |
| R9              | VDDA_0P8_SERDES0_C | VDDA_0P8_SERDES0_C |              | PWR      |                      |                              |                       |   |          |                  |                        |           |                            |             |
| R6              | VDDA_1P8_USB       | VDDA_1P8_USB       |              | PWR      |                      |                              |                       |   |          |                  |                        |           |                            |             |
| P8              | VDDA_1P8_SERDES0   | VDDA_1P8_SERDES0   |              | PWR      |                      |                              |                       |   |          |                  |                        |           |                            |             |
| R7              | VDDA_3P3_USB       | VDDA_3P3_USB       |              | PWR      |                      |                              |                       |   |          |                  |                        |           |                            |             |
| J16             | VDDA_ADC_MCU       | VDDA_ADC_MCU       |              | PWR      |                      |                              |                       |   |          |                  |                        |           |                            |             |
| F15             | VDDA_MCU_PLLGRP0   | VDDA_MCU_PLLGRP0   |              | PWR      |                      |                              |                       |   |          |                  |                        |           |                            |             |
| F16             | VDDA_MCU_TEMP      | VDDA_MCU_TEMP      |              | PWR      |                      |                              |                       |   |          |                  |                        |           |                            |             |
| G17             | VDDA_OSC1          | VDDA_OSC1          |              | PWR      |                      |                              |                       |   |          |                  |                        |           |                            |             |

Table 5-1. Pin Attributes (continued)

| BALL NUMBER<br>[1]  | BALL NAME<br>[2] | SIGNAL NAME<br>[3] | MUX MODE<br>[4] | TYPE<br>[5] | BALL RESET STATE<br>[6] | BALL RESET REL. MUX MODE<br>[7] | I/O VOLTAGE VALUE<br>[8] | POWER<br>[9] | HYS<br>[10] | BUFFER TYPE<br>[11] | PULL UP/DOWN TYPE<br>[12] | DSIS<br>[13] | RX ACTIVE/ TX DISABLE<br>[14] | IO RET<br>[15] |
|---|------------------|--------------------|-----------------|-------------|-------------------------|---------------------------------|--------------------------|--------------|-------------|---------------------|---------------------------|--------------|-------------------------------|----------------|
| N14   | VDDA_PLLGRP0     | VDDA_PLLGRP0       |                 | PWR         |                         |                                 |                          |              |             |                     |                           |              |                               |                |
| N9  | VDDA_PLLGRP4     | VDDA_PLLGRP4       |                 | PWR         |                         |                                 |                          |              |             |                     |                           |              |                               |                |
| J9  | VDDA_PLLGRP6     | VDDA_PLLGRP6       |                 | PWR         |                         |                                 |                          |              |             |                     |                           |              |                               |                |
| L7  | VDDA_PLLGRP8     | VDDA_PLLGRP8       |                 | PWR         |                         |                                 |                          |              |             |                     |                           |              |                               |                |
| J15   | VDDA_POR_WKUP    | VDDA_POR_WKUP      |                 | PWR         |                         |                                 |                          |              |             |                     |                           |              |                               |                |
| J8  | VDDA_TEMP0       | VDDA_TEMP0         |                 | PWR         |                         |                                 |                          |              |             |                     |                           |              |                               |                |
| P15   | VDDA_TEMP1       | VDDA_TEMP1         |                 | PWR         |                         |                                 |                          |              |             |                     |                           |              |                               |                |
| H16   | VDDA_WKUP        | VDDA_WKUP          |                 | PWR         |                         |                                 |                          |              |             |                     |                           |              |                               |                |
| N6, P6  | VDDSHV0          | VDDSHV0            |                 | PWR         |                         |                                 |                          |              |             |                     |                           |              |                               |                |
| E13, E14, F13, F14  | VDDSHV0_MCU      | VDDSHV0_MCU        |                 | PWR         |                         |                                 |                          |              |             |                     |                           |              |                               |                |
| E7, E8, F8  | VDDSHV1_MCU      | VDDSHV1_MCU        |                 | PWR         |                         |                                 |                          |              |             |                     |                           |              |                               |                |
| T10, U11, U9  | VDDSHV2          | VDDSHV2            |                 | PWR         |                         |                                 |                          |              |             |                     |                           |              |                               |                |
| F11, F12, G11   | VDDSHV2_MCU      | VDDSHV2_MCU        |                 | PWR         |                         |                                 |                          |              |             |                     |                           |              |                               |                |
| K16, L16  | VDDSHV5          | VDDSHV5            |                 | PWR         |                         |                                 |                          |              |             |                     |                           |              |                               |                |
| A1, G7, H6, J7, K6, M5, U1                                    | VDDS_DDR         | VDDS_DDR           |                 | PWR         |                         |                                 |                          |              |             |                     |                           |              |                               |                |
| F7, L6  | VDDS_DDR_BIAS    | VDDS_DDR_BIAS      |                 | PWR         |                         |                                 |                          |              |             |                     |                           |              |                               |                |
| J6  | VDDS_DDR_C       | VDDS_DDR_C         |                 | PWR         |                         |                                 |                          |              |             |                     |                           |              |                               |                |
| M16, N16  | VDDS_MMC0        | VDDS_MMC0          |                 | PWR         |                         |                                 |                          |              |             |                     |                           |              |                               |                |
| H8, K12, L13, M12, M14, N13, N15, N7, P10, P12, R11, R13, R15 | VDD_CORE         | VDD_CORE           |                 | PWR         |                         |                                 |                          |              |             |                     |                           |              |                               |                |
| J10, L11, M9, N11, N8   | VDD_CPU          | VDD_CPU            |                 | PWR         |                         |                                 |                          |              |             |                     |                           |              |                               |                |
| G9, H10, H14, J13, K15  | VDD_MCU          | VDD_MCU            |                 | PWR         |                         |                                 |                          |              |             |                     |                           |              |                               |                |
| G13   | VDD_MCU_WAKE1    | VDD_MCU_WAKE1      |                 | PWR         |                         |                                 |                          |              |             |                     |                           |              |                               |                |
| P11   | VDD_WAKE0        | VDD_WAKE0          |                 | PWR         |                         |                                 |                          |              |             |                     |                           |              |                               |                |
| G15   | VMON1_ER_VSYS    | VMON1_ER_VSYS      |                 | PWR         |                         |                                 |                          |              |             |                     |                           |              |                               |                |
| D16   | VMON2_IR_VCPU    | VMON2_IR_VCPU      |                 | PWR         |                         |                                 |                          |              |             |                     |                           |              |                               |                |
| E17   | VMON3_IR_VEXT1P8 | VMON3_IR_VEXT1P8   |                 | PWR         |                         |                                 |                          |              |             |                     |                           |              |                               |                |
| F17   | VMON4_IR_VEXT1P8 | VMON4_IR_VEXT1P8   |                 | PWR         |                         |                                 |                          |              |             |                     |                           |              |                               |                |
| L14   | VMON5_IR_VEXT3P3 | VMON5_IR_VEXT3P3   |                 | PWR         |                         |                                 |                          |              |             |                     |                           |              |                               |                |
| N17   | VPP_CORE         | VPP_CORE           |                 | PWR         |                         |                                 |                          |              |             |                     |                           |              |                               |                |
| E11   | VPP_MCU          | VPP_MCU            |                 | PWR         |                         |                                 |                          |              |             |                     |                           |              |                               |                |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1]  | BALL NAME [2] | SIGNAL NAME [3]      | MUX MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUX MODE [7] | I/O VOLTAGE VALUE [8] | POWER [9]   | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RX ACTIVE/ TX DISABLE [14] | IO RET [15] |
|--|---------------|----------------------|--------------|----------|----------------------|------------------------------|-----------------------|-------------|----------|------------------|------------------------|-----------|----------------------------|-------------|
| B5,AA1, AA10, AA13, AA4, AA7, C11, D15, D17, D3, E10, E12, E15, E16, E6, E9, F1, G10, G12, G16, G6, G8, H11, H13, H15, H19, H4, H7, H9, J1, J12, J21, K11, K13, K3, L12, L19, L5, M11, M13, M15, M21, M6, M8, N10, N12, N3, P13, P5, P9, R10, R12, R14, T11, T2, T6, T8, T9, U10, U7, V11, V12, V9, W10, W13, W18, W4, W7, Y12, Y3, Y6, Y9 | VSS           | VSS                  |              | GND      |                      |                              |                       |             |          |                  |                        |           |                            |             |
| B18  | WKUP_GPIO0_0  | MCU_SPI1_CLK         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_MCU | Yes      | LVCMOS           | PU/PD                  | 0         |                            | Yes         |
|  |               | MCU_SPI1_CLK         | 1            | IO       |                      |                              |                       |             |          |                  |                        | 0         |                            |             |
|  |               | WKUP_GPIO0_0         | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
|  |               | MCU_BOOTMODE03       | Bootstrap    | I        |                      |                              |                       |             |          |                  |                        |           |                            |             |
| B19  | WKUP_GPIO0_1  | MCU_SPI1_D0          | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_MCU | Yes      | LVCMOS           | PU/PD                  | 0         | 1/0                        | Yes         |
|  |               | MCU_SPI1_D0          | 1            | IO       |                      |                              |                       |             |          |                  |                        | 0         |                            |             |
|  |               | WKUP_GPIO0_1         | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
|  |               | MCU_BOOTMODE04       | Bootstrap    | I        |                      |                              |                       |             |          |                  |                        |           |                            |             |
| D14  | WKUP_GPIO0_2  | MCU_SPI1_D1          | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_MCU | Yes      | LVCMOS           | PU/PD                  | 0         | 1/0                        | Yes         |
|  |               | MCU_SPI1_D1          | 1            | IO       |                      |                              |                       |             |          |                  |                        | 0         |                            |             |
|  |               | WKUP_GPIO0_2         | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
|  |               | MCU_BOOTMODE05       | Bootstrap    | I        |                      |                              |                       |             |          |                  |                        |           |                            |             |
| B21  | WKUP_GPIO0_3  | MCU_SPI1_CS0         | 0            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_MCU | Yes      | LVCMOS           | PU/PD                  | 1         |                            | Yes         |
|  |               | MCU_SPI1_CS0         | 1            | IO       |                      |                              |                       |             |          |                  |                        | 1         |                            |             |
|  |               | WKUP_GPIO0_3         | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
| D13  | WKUP_GPIO0_4  | MCU_MCAN1_TX         | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_MCU | Yes      | LVCMOS           | PU/PD                  |           |                            | Yes         |
|  |               | MCU_MCAN1_TX         | 1            | O        |                      |                              |                       |             |          |                  |                        |           |                            |             |
|  |               | MCU_SPI0_CS3         | 2            | IO       |                      |                              |                       |             |          |                  |                        | IO        |                            |             |
|  |               | MCU_ADC_EXT_TRIGGER0 | 3            | I        |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
|  |               | WKUP_GPIO0_4         | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |

Table 5-1. Pin Attributes (continued)

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3]      | MUX MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUX MODE [7] | I/O VOLTAGE VALUE [8] | POWER [9]   | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RX ACTIVE/ TX DISABLE [14] | IO RET [15] |
|-----------------|---------------|----------------------|--------------|----------|----------------------|------------------------------|-----------------------|-------------|----------|------------------|------------------------|-----------|----------------------------|-------------|
| B16             | WKUP_GPIO0_5  | MCU_MCAN1_RX         | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_MCU | Yes      | LVCMOS           | PU/PD                  | 1         |                            | Yes         |
|                 |               | MCU_MCAN1_RX         | 1            | I        |                      |                              |                       |             |          |                  |                        | 1         |                            |             |
|                 |               | MCU_SPI1_CS3         | 2            | IO       |                      |                              |                       |             |          |                  |                        | IO        |                            |             |
|                 |               | MCU_ADC_EXT_TRIGGER1 | 3            | I        |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
|                 |               | WKUP_GPIO0_5         | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
| C14             | WKUP_GPIO0_6  | WKUP_UART0_CTSn      | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_MCU | Yes      | LVCMOS           | PU/PD                  | 1         |                            | Yes         |
|                 |               | WKUP_UART0_CTSn      | 1            | I        |                      |                              |                       |             |          |                  |                        | 1         |                            |             |
|                 |               | MCU_CPTS0_HW1TSPUSH  | 2            | I        |                      |                              |                       |             |          |                  |                        | I         |                            |             |
|                 |               | MCU_I2C1_SCL         | 3            | IOD      |                      |                              |                       |             |          |                  |                        | 1         |                            |             |
|                 |               | WKUP_GPIO0_6         | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
| C18             | WKUP_GPIO0_7  | WKUP_UART0_RTSn      | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_MCU | Yes      | LVCMOS           | PU/PD                  |           |                            | Yes         |
|                 |               | WKUP_UART0_RTSn      | 1            | O        |                      |                              |                       |             |          |                  |                        |           |                            |             |
|                 |               | MCU_CPTS0_HW2TSPUSH  | 2            | I        |                      |                              |                       |             |          |                  |                        | I         |                            |             |
|                 |               | MCU_I2C1_SDA         | 3            | IOD      |                      |                              |                       |             |          |                  |                        | 1         |                            |             |
|                 |               | WKUP_GPIO0_7         | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
| C21             | WKUP_GPIO0_8  | MCU_I2C1_SCL         | 0            | IOD      | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_MCU | Yes      | LVCMOS           | PU/PD                  | 1         |                            | Yes         |
|                 |               | MCU_I2C1_SCL         | 1            | IOD      |                      |                              |                       |             |          |                  |                        | 1         |                            |             |
|                 |               | MCU_CPTS0_TS_SYNC    | 2            | O        |                      |                              |                       |             |          |                  |                        | O         |                            |             |
|                 |               | MCU_I3C0_SCL         | 3            | IO       |                      |                              |                       |             |          |                  |                        | 1         |                            |             |
|                 |               | MCU_TIMER_IO6        | 4            | IO       |                      |                              |                       |             |          |                  |                        | 0         |                            |             |
|                 |               | WKUP_GPIO0_8         | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
| C19             | WKUP_GPIO0_9  | MCU_I2C1_SDA         | 0            | IOD      | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_MCU | Yes      | LVCMOS           | PU/PD                  | 1         |                            | Yes         |
|                 |               | MCU_I2C1_SDA         | 1            | IOD      |                      |                              |                       |             |          |                  |                        | 1         |                            |             |
|                 |               | MCU_CPTS0_TS_COMP    | 2            | O        |                      |                              |                       |             |          |                  |                        | O         |                            |             |
|                 |               | MCU_I3C0_SDA         | 3            | IO       |                      |                              |                       |             |          |                  |                        | 1         |                            |             |
|                 |               | MCU_TIMER_IO7        | 4            | IO       |                      |                              |                       |             |          |                  |                        | 0         |                            |             |
|                 |               | WKUP_GPIO0_9         | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
| C20             | WKUP_GPIO0_10 | MCU_EXT_REFCLK0      | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_MCU | Yes      | LVCMOS           | PU/PD                  | 0         |                            | Yes         |
|                 |               | MCU_EXT_REFCLK0      | 1            | I        |                      |                              |                       |             |          |                  |                        | 0         |                            |             |
|                 |               | MCU_UART0_TXD        | 2            | O        |                      |                              |                       |             |          |                  |                        | O         |                            |             |
|                 |               | MCU_ADC_EXT_TRIGGER0 | 3            | I        |                      |                              |                       |             |          |                  |                        | 0         |                            |             |
|                 |               | MCU_CPTS0_RFT_CLK    | 4            | I        |                      |                              |                       |             |          |                  |                        | 0         |                            |             |
|                 |               | MCU_SYSCLKOUT0       | 5            | O        |                      |                              |                       |             |          |                  |                        |           |                            |             |
|                 |               | WKUP_GPIO0_10        | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2] | SIGNAL NAME [3]      | MUX MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUX MODE [7] | I/O VOLTAGE VALUE [8] | POWER [9]   | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RX ACTIVE/ TX DISABLE [14] | IO RET [15] |
|-----------------|---------------|----------------------|--------------|----------|----------------------|------------------------------|-----------------------|-------------|----------|------------------|------------------------|-----------|----------------------------|-------------|
| C16             | WKUP_GPIO0_11 | MCU_OBSCLK0          | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_MCU | Yes      | LVCMOS           | PU/PD                  |           |                            | Yes         |
|                 |               | MCU_OBSCLK0          | 1            | O        |                      |                              |                       |             |          |                  |                        |           |                            |             |
|                 |               | MCU_UART0_RXD        | 2            | I        |                      |                              |                       |             |          |                  |                        | I         |                            |             |
|                 |               | MCU_ADC_EXT_TRIGGER1 | 3            | I        |                      |                              |                       |             |          |                  |                        | 0         |                            |             |
|                 |               | MCU_TIMER_IO1        | 4            | IO       |                      |                              |                       |             |          |                  |                        | 0         |                            |             |
|                 |               | MCU_I3C0_SDAPULLEN   | 5            | OD       |                      |                              |                       |             |          |                  |                        |           |                            |             |
|                 |               | MCU_CLKOUT0          | 6            | OZ       |                      |                              |                       |             |          |                  |                        |           |                            |             |
| WKUP_GPIO0_11   | 7             | IO                   | pad          |          |                      |                              |                       |             |          |                  |                        |           |                            |             |
| D19             | WKUP_GPIO0_12 | MCU_UART0_TXD        | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_MCU | Yes      | LVCMOS           | PU/PD                  |           |                            | Yes         |
|                 |               | MCU_SPI0_CS1         | 1            | IO       |                      |                              |                       |             |          |                  |                        |           |                            |             |
|                 |               | WKUP_GPIO0_12        | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
|                 |               | MCU_BOOTMODE08       | Bootstrap    | I        |                      |                              |                       |             |          |                  |                        |           |                            |             |
| D20             | WKUP_GPIO0_13 | MCU_UART0_RXD        | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_MCU | Yes      | LVCMOS           | PU/PD                  | 1         |                            | Yes         |
|                 |               | MCU_SPI1_CS1         | 1            | IO       |                      |                              |                       |             |          |                  |                        |           |                            |             |
|                 |               | WKUP_GPIO0_13        | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
|                 |               | MCU_BOOTMODE09       | Bootstrap    | I        |                      |                              |                       |             |          |                  |                        |           |                            |             |
| E20             | WKUP_GPIO0_14 | MCU_UART0_CTSn       | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_MCU | Yes      | LVCMOS           | PU/PD                  | 1         |                            | Yes         |
|                 |               | MCU_SPI0_CS2         | 1            | IO       |                      |                              |                       |             |          |                  |                        |           |                            |             |
|                 |               | MCU_TIMER_IO8        | 4            | IO       |                      |                              |                       |             |          |                  |                        | 0         |                            |             |
|                 |               | WKUP_GPIO0_14        | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
|                 |               | MCU_BOOTMODE06       | Bootstrap    | I        |                      |                              |                       |             |          |                  |                        |           |                            |             |
| E21             | WKUP_GPIO0_15 | MCU_UART0_RTSn       | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_MCU | Yes      | LVCMOS           | PU/PD                  |           |                            | Yes         |
|                 |               | MCU_SPH1_CS2         | 1            | IO       |                      |                              |                       |             |          |                  |                        |           |                            |             |
|                 |               | MCU_TIMER_IO9        | 4            | IO       |                      |                              |                       |             |          |                  |                        | 0         |                            |             |
|                 |               | WKUP_GPIO0_15        | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
|                 |               | MCU_BOOTMODE07       | Bootstrap    | I        |                      |                              |                       |             |          |                  |                        |           |                            |             |
| D21             | WKUP_GPIO0_77 | MCU_TIMER_IO6        | 4            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_MCU | Yes      | LVCMOS           | PU/PD                  | 0         |                            | Yes         |
|                 |               | WKUP_GPIO0_77        | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
|                 |               | BOOTMODE04           | Bootstrap    | I        |                      |                              |                       |             |          |                  |                        |           |                            |             |
| E19             | WKUP_GPIO0_78 | MCU_TIMER_IO7        | 4            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_MCU | Yes      | LVCMOS           | PU/PD                  | 0         |                            | Yes         |
|                 |               | WKUP_GPIO0_78        | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
|                 |               | BOOTMODE05           | Bootstrap    | I        |                      |                              |                       |             |          |                  |                        |           |                            |             |
| D18             | WKUP_GPIO0_80 | WKUP_GPIO0_80        | 7            | IO       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_MCU | Yes      | LVCMOS           | PU/PD                  | pad       |                            | Yes         |
|                 |               | BOOTMODE06           | Bootstrap    | I        |                      |                              |                       |             |          |                  |                        |           |                            |             |
| C17             | WKUP_GPIO0_81 | WKUP_LF_CLKIN        | 1            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_MCU | Yes      | LVCMOS           | PU/PD                  | pad       |                            | Yes         |
|                 |               | WKUP_GPIO0_81        | 7            | IO       |                      |                              |                       |             |          |                  |                        | pad       |                            |             |
|                 |               | BOOTMODE07           | Bootstrap    | I        |                      |                              |                       |             |          |                  |                        |           |                            |             |

**Table 5-1. Pin Attributes (continued)**

| BALL NUMBER [1] | BALL NAME [2]  | SIGNAL NAME [3]   | MUX MODE [4] | TYPE [5] | BALL RESET STATE [6] | BALL RESET REL. MUX MODE [7] | I/O VOLTAGE VALUE [8] | POWER [9]                | HYS [10] | BUFFER TYPE [11] | PULL UP/DOWN TYPE [12] | DSIS [13] | RX ACTIVE/ TX DISABLE [14] | IO RET [15] |
|-----------------|----------------|-------------------|--------------|----------|----------------------|------------------------------|-----------------------|--------------------------|----------|------------------|------------------------|-----------|----------------------------|-------------|
| E18             | WKUP_GPIO0_84  | PMIC_WAKE1n       | 0            | OD       | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_MCU              | Yes      | LVCMOS           | PU/PD                  |           |                            |             |
|                 |                | MCU_EXT_REFCLK0   | 1            | I        |                      |                              |                       |                          |          |                  |                        | 0         |                            |             |
|                 |                | MCU_CPTS0_RFT_CLK | 2            | I        |                      |                              |                       |                          |          |                  |                        | I         |                            |             |
|                 |                | WKUP_GPIO0_84     | 7            | IO       |                      |                              |                       |                          |          |                  |                        | pad       |                            |             |
| F20             | WKUP_I2C0_SCL  | WKUP_I2C0_SCL     | 0            | IOD      | OFF                  | 0                            | 1.8 V/3.3 V           | VDDSHV0_MCU              | Yes      | I2C OD FS        |                        | 1         |                            | Yes         |
|                 |                | WKUP_GPIO0_64     | 7            | IO       |                      |                              |                       |                          |          |                  |                        | pad       |                            |             |
| H21             | WKUP_I2C0_SDA  | WKUP_I2C0_SDA     | 0            | IOD      | OFF                  | 0                            | 1.8 V/3.3 V           | VDDSHV0_MCU              | Yes      | I2C OD FS        |                        | 1         |                            | Yes         |
|                 |                | WKUP_GPIO0_65     | 7            | IO       |                      |                              |                       |                          |          |                  |                        | pad       |                            |             |
| K21             | WKUP_OSC0_XI   | WKUP_OSC0_XI      |              | I        |                      |                              | 1.8 V                 | VDDA_WKUP, VDDA_POR_WKUP | Yes      | HFOSC            |                        |           |                            |             |
| L21             | WKUP_OSC0_XO   | WKUP_OSC0_XO      |              | O        |                      |                              | 1.8 V                 | VDDA_WKUP, VDDA_POR_WKUP | Yes      | HFOSC            |                        |           |                            |             |
| B14             | WKUP_UART0_RXD | WKUP_UART0_RXD    | 0            | I        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_MCU              | Yes      | LVCMOS           | PU/PD                  | 1         | 1/0                        | Yes         |
|                 |                | WKUP_GPIO0_60     | 7            | IO       |                      |                              |                       |                          |          |                  |                        | pad       |                            |             |
| A14             | WKUP_UART0_TXD | WKUP_UART0_TXD    | 0            | O        | OFF                  | 7                            | 1.8 V/3.3 V           | VDDSHV0_MCU              | Yes      | LVCMOS           | PU/PD                  |           | 1/0                        | Yes         |
|                 |                | WKUP_GPIO0_61     | 7            | IO       |                      |                              |                       |                          |          |                  |                        | pad       |                            |             |

The following list describes the table column headers:

- BALL NUMBER:** Ball numbers on the bottom side associated with each signal on the bottom.
- BALL NAME:** Mechanical name from package device (name is taken from muxmode 0).
- SIGNAL NAME:** Names of signals multiplexed on each ball (also notice that the name of the ball is the signal name in muxmode 0).

**Note**

Table 5-1, *Pin Attributes*, does not take into account the subsystem multiplexing signals. Subsystem multiplexing signals are described in Section 5.3, *Signal Descriptions*.

- MUXMODE:** Multiplexing mode number:
  - MUXMODE 0 is the primary muxmode. The primary muxmode is not necessarily the default muxmode.

**Note**

The default muxmode is the mode at the release of the reset; also see the BALL RESET REL. MUXMODE column.

- MUXMODE 1 through 7 are possible muxmodes for alternate functions. On each pin, some muxmodes are effectively used for alternate functions, while some muxmodes are not used. Only MUXMODE values which correspond to defined functions should be used.
  - An empty box means Not Applicable.
- TYPE:** Signal type and direction:

- I = Input
  - O = Output
  - OD = Open drain terminal - Output
  - IO = Input or Output
  - IOD = Open drain terminal - Input or Output
  - IOZ = Input, Output or Three-state terminal
  - OZ = Output or Three-state terminal
  - A = Analog
  - PWR = Power
  - GND = Ground
  - CAP = LDO Capacitor.
6. **BALL RESET STATE:** The state of the terminal at power-on reset:
- DRIVE 0 (OFF): The buffer drives  $V_{OL}$  (pulldown or pullup resistor not activated).
  - DRIVE 1 (OFF): The buffer drives  $V_{OH}$  (pulldown or pullup resistor not activated).
  - OFF: High-impedance
  - PD: High-impedance with an active pulldown resistor
  - PU: High-impedance with an active pullup resistor
  - An empty box means Not Applicable.
7. **BALL RESET REL. MUXMODE:** This muxmode is automatically configured at the release of the RESETSTATz and MCU\_RESETSTATz signals.  
An empty box means Not Applicable.
8. **I/O VOLTAGE VALUE:** This column describes the IO voltage value (the corresponding power supply).  
An empty box means Not Applicable.
9. **POWER:** The voltage supply that powers the terminal IO buffers.  
An empty box means Not Applicable.
10. **HYS:** Indicates if the input buffer has hysteresis:
- Yes: With hysteresis
  - No: Without hysteresis
- An empty box means No.
- For more information, see the hysteresis values in [Section 6.6, Electrical Characteristics](#).
11. **BUFFER TYPE:** This column describes the associated output buffer type  
An empty box means Not Applicable.
- For drive strength of the associated output buffer, refer to [Section 6.6, Electrical Characteristics](#).
12. **PULL UP/DOWN TYPE:** Indicates the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.
- PU: Internal pullup
  - PD: Internal pulldown
  - PU/PD: Internal pullup and pulldown

- An empty box means No pull.
13. **DSIS:** The deselected input state (DSIS) indicates the state driven on the peripheral input (logic "0", logic "1", or "pad" level) when the peripheral pin function is not selected by any of the PINCTLx registers.
- 0: Logic 0 driven on the input signal port of the peripheral.
  - 1: Logic 1 driven on the input signal port of the peripheral.
  - pad: Logic state of the pad is driven on the input signal port of the peripheral.
  - An empty box means Not Applicable.
14. **RXACTIVE / TXDISABLE:** This column indicates the default value of the RXACTIVE / TXDISABLE bits in the PADCONFIG register.
- RXACTIVE: 0 = receiver disabled, 1 = receiver enabled.
  - TXDISABLE: 0 = driver enabled, 1 = driver disabled.
  - An empty box means Not Applicable.

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**Note**

Configuring two pins to the same input signal is not supported as it can yield unexpected results. This can be easily prevented with the proper software configuration (HiZ mode is not an input signal).

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**Note**

When a pad is set into a multiplexing mode which is not defined by pin multiplexing, that pad's behavior is undefined. This should be avoided.

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15. **IO RET:** Indicates if wakeup and IO retention are supported.

## 5.3 Signal Descriptions

Many signals are available on multiple pins, according to the software configuration of the pin multiplexing options.

The following list describes the column headers:

1. **SIGNAL NAME:** The name of the signal passing through the pin.

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### Note

Signal names provided in each Signal Descriptions table, ([Table 5-1](#) through [Table 5-106](#)) represent the pin layer multiplexed signal function which is selected via the PADCONFIG registers. Device subsystems may provide an additional layer of signal multiplexing, which means the signal names described in these tables may have additional signal functions. For more information, see the respective peripheral chapter of the device TRM.

2. **DESCRIPTION:** Description of the signal
3. **PIN TYPE:** Signal direction and type:
  - I = Input
  - O = Output
  - OD = Opent drain terminal - Output
  - IO = Input or Output
  - IOD = Open drain terminal - Input or Output
  - IOZ = Input, Output or Three-state terminal
  - OZ = Output or Three-state terminal
  - A = Analog
  - PWR = Power
  - GND = Ground
  - CAP = LDO Capacitor
4. **BALL:** Associated balls bottom

For more information on the I/O cell configurations, see *Pad Configuration Registers* section in *Device Configuration* chapter of the device TRM.

### 5.3.1 ADC

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### Note

The ADC can be configured to be used as a GPI. For more information, see *Analog-to-Digital Converter (ADC)* section in *Peripherals* chapter in the device TRM.

#### 5.3.1.1 MCU Domain

**Table 5-2. ADC0 Signal Descriptions**

| SIGNAL NAME [1]      | DESCRIPTION [2]    | PIN TYPE [3] | BALL [4]      |
|----------------------|--------------------|--------------|---------------|
| MCU_ADC0_AIN0        | ADC Analog Input 0 | A            | H17           |
| MCU_ADC0_AIN1        | ADC Analog Input 1 | A            | K18           |
| MCU_ADC0_AIN2        | ADC Analog Input 2 | A            | M17           |
| MCU_ADC0_AIN3        | ADC Analog Input 3 | A            | L18           |
| MCU_ADC0_AIN4        | ADC Analog Input 4 | A            | J18           |
| MCU_ADC0_AIN5        | ADC Analog Input 5 | A            | J17           |
| MCU_ADC0_AIN6        | ADC Analog Input 6 | A            | K17           |
| MCU_ADC0_AIN7        | ADC Analog Input 7 | A            | L17           |
| MCU_ADC_EXT_TRIGGER0 | ADC Trigger Input  | I            | C12, C20, D13 |

**Table 5-2. ADC0 Signal Descriptions (continued)**

| SIGNAL NAME [1]      | DESCRIPTION [2]   | PIN TYPE [3] | BALL [4]      |
|----------------------|-------------------|--------------|---------------|
| MCU_ADC_EXT_TRIGGER1 | ADC Trigger Input | I            | B12, B16, C16 |

**5.3.2 DDRSS****5.3.2.1 MAIN Domain****Table 5-3. DDRSS0 Signal Descriptions**

| SIGNAL NAME [1]          | DESCRIPTION [2]                     | PIN TYPE [3] | BALL [4] |
|--------------------------|-------------------------------------|--------------|----------|
| DDR_RET                  | External IO Retention Enable        | I            | R5       |
| DDR0_CKN                 | DDRSS Differential Clock (negative) | IO           | H1       |
| DDR0_CKP                 | DDRSS Differential Clock (positive) | IO           | G1       |
| DDR0_RESETh              | DDRSS Reset                         | IO           | J5       |
| DDR0_CA0                 | DDRSS Command Address               | IO           | G4       |
| DDR0_CA1                 | DDRSS Command Address               | IO           | H3       |
| DDR0_CA2                 | DDRSS Command Address               | IO           | J4       |
| DDR0_CA3                 | DDRSS Command Address               | IO           | K1       |
| DDR0_CA4                 | DDRSS Command Address               | IO           | J2       |
| DDR0_CA5                 | DDRSS Command Address               | IO           | H5       |
| DDR0_CAL0 <sup>(1)</sup> | IO Pad Calibration Resistor         | A            | K5       |
| DDR0_CKE0                | DDRSS Clock Enable                  | IO           | G2       |
| DDR0_CKE1                | DDRSS Clock Enable                  | IO           | H2       |
| DDR0_CSn0_0              | DDRSS Chip Select                   | IO           | G3       |
| DDR0_CSn0_1              | DDRSS Chip Select                   | IO           | K2       |
| DDR0_CSn1_0              | DDRSS Chip Select                   | IO           | G5       |
| DDR0_CSn1_1              | DDRSS Chip Select                   | IO           | J3       |
| DDR0_DM0                 | DDRSS Data Mask                     | IO           | A3       |
| DDR0_DM1                 | DDRSS Data Mask                     | IO           | E4       |
| DDR0_DM2                 | DDRSS Data Mask                     | IO           | N1       |
| DDR0_DM3                 | DDRSS Data Mask                     | IO           | R4       |
| DDR0_DQ0                 | DDRSS Data                          | IO           | B4       |
| DDR0_DQ1                 | DDRSS Data                          | IO           | A4       |
| DDR0_DQ2                 | DDRSS Data                          | IO           | C4       |
| DDR0_DQ3                 | DDRSS Data                          | IO           | C1       |
| DDR0_DQ4                 | DDRSS Data                          | IO           | C3       |
| DDR0_DQ5                 | DDRSS Data                          | IO           | C2       |
| DDR0_DQ6                 | DDRSS Data                          | IO           | A2       |
| DDR0_DQ7                 | DDRSS Data                          | IO           | B3       |
| DDR0_DQ8                 | DDRSS Data                          | IO           | D1       |
| DDR0_DQ9                 | DDRSS Data                          | IO           | D2       |
| DDR0_DQ10                | DDRSS Data                          | IO           | F2       |
| DDR0_DQ11                | DDRSS Data                          | IO           | E3       |
| DDR0_DQ12                | DDRSS Data                          | IO           | F3       |
| DDR0_DQ13                | DDRSS Data                          | IO           | F4       |
| DDR0_DQ14                | DDRSS Data                          | IO           | D4       |
| DDR0_DQ15                | DDRSS Data                          | IO           | F5       |
| DDR0_DQ16                | DDRSS Data                          | IO           | K4       |

**Table 5-3. DDRSS0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]                 | PIN TYPE [3] | BALL [4] |
|-----------------|---------------------------------|--------------|----------|
| DDR0_DQ17       | DDRSS Data                      | IO           | L4       |
| DDR0_DQ18       | DDRSS Data                      | IO           | M4       |
| DDR0_DQ19       | DDRSS Data                      | IO           | L3       |
| DDR0_DQ20       | DDRSS Data                      | IO           | L2       |
| DDR0_DQ21       | DDRSS Data                      | IO           | L1       |
| DDR0_DQ22       | DDRSS Data                      | IO           | M3       |
| DDR0_DQ23       | DDRSS Data                      | IO           | N2       |
| DDR0_DQ24       | DDRSS Data                      | IO           | R3       |
| DDR0_DQ25       | DDRSS Data                      | IO           | T1       |
| DDR0_DQ26       | DDRSS Data                      | IO           | P1       |
| DDR0_DQ27       | DDRSS Data                      | IO           | P2       |
| DDR0_DQ28       | DDRSS Data                      | IO           | N4       |
| DDR0_DQ29       | DDRSS Data                      | IO           | P3       |
| DDR0_DQ30       | DDRSS Data                      | IO           | P4       |
| DDR0_DQ31       | DDRSS Data                      | IO           | N5       |
| DDR0_DQS0N      | DDRSS Complimentary Data Strobe | IO           | B1       |
| DDR0_DQS0P      | DDRSS Data Strobe               | IO           | B2       |
| DDR0_DQS1N      | DDRSS Complimentary Data Strobe | IO           | E1       |
| DDR0_DQS1P      | DDRSS Data Strobe               | IO           | E2       |
| DDR0_DQS2N      | DDRSS Complimentary Data Strobe | IO           | M1       |
| DDR0_DQS2P      | DDRSS Data Strobe               | IO           | M2       |
| DDR0_DQS3N      | DDRSS Complimentary Data Strobe | IO           | R1       |
| DDR0_DQS3P      | DDRSS Data Strobe               | IO           | R2       |

(1) An external 240 Ω ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.

### 5.3.2.2 DDRSS Mapping

Table 5-4 presents DDRSS interface signal mapping.

**Table 5-4. DDRSS Signal Mapping**

| SIGNAL NAME [1] | MEMORY TYPE | PIN TYPE [3] | BALL [4] |
|-----------------|-------------|--------------|----------|
|                 | LPDDR4      |              |          |
| DDR0_CA0        | CA0_A       | IO           | G4       |
| DDR0_CA1        | CA1_A       | IO           | H3       |
| DDR0_CA2        | CA2_A       | IO           | J4       |
| DDR0_CA3        | CA3_A       | IO           | K1       |
| DDR0_CA4        | CA4_A       | IO           | J2       |
| DDR0_CA5        | CA5_A       | IO           | H5       |
| DDR0_CKP        | CK_t_A      | IO           | H1       |
| DDR0_CKN        | CK_c_A      | IO           | G1       |
| DDR0_DQ0        | DQ0         | IO           | B4       |
| DDR0_DQ1        | DQ1         | IO           | A4       |
| DDR0_DQ2        | DQ2         | IO           | C4       |
| DDR0_DQ3        | DQ3         | IO           | C1       |
| DDR0_DQ4        | DQ4         | IO           | C3       |
| DDR0_DQ5        | DQ5         | IO           | C2       |

Table 5-4. DDRSS Signal Mapping (continued)

| SIGNAL NAME [1] | MEMORY TYPE | PIN TYPE [3] | BALL [4] |
|-----------------|-------------|--------------|----------|
|                 | LPDDR4      |              |          |
| DDR0_DQ6        | DQ6         | IO           | A2       |
| DDR0_DQ7        | DQ7         | IO           | B3       |
| DDR0_DQ8        | DQ8         | IO           | D1       |
| DDR0_DQ9        | DQ9         | IO           | D2       |
| DDR0_DQ10       | DQ10        | IO           | F2       |
| DDR0_DQ11       | DQ11        | IO           | E3       |
| DDR0_DQ12       | DQ12        | IO           | F3       |
| DDR0_DQ13       | DQ13        | IO           | F4       |
| DDR0_DQ14       | DQ14        | IO           | D4       |
| DDR0_DQ15       | DQ15        | IO           | F5       |
| DDR0_DQ16       | DQ16        | IO           | K4       |
| DDR0_DQ17       | DQ17        | IO           | L4       |
| DDR0_DQ18       | DQ18        | IO           | M4       |
| DDR0_DQ19       | DQ19        | IO           | L3       |
| DDR0_DQ20       | DQ20        | IO           | L2       |
| DDR0_DQ21       | DQ21        | IO           | L1       |
| DDR0_DQ22       | DQ22        | IO           | M3       |
| DDR0_DQ23       | DQ23        | IO           | N2       |
| DDR0_DQ24       | DQ24        | IO           | R3       |
| DDR0_DQ25       | DQ25        | IO           | T1       |
| DDR0_DQ26       | DQ26        | IO           | P1       |
| DDR0_DQ27       | DQ27        | IO           | P2       |
| DDR0_DQ28       | DQ28        | IO           | N4       |
| DDR0_DQ29       | DQ29        | IO           | P3       |
| DDR0_DQ30       | DQ30        | IO           | P4       |
| DDR0_DQ31       | DQ31        | IO           | N5       |
| DDR0_DM0        | DMI0        | IO           | A3       |
| DDR0_DM1        | DMI1        | IO           | E4       |
| DDR0_DM2        | DMI2        | IO           | N1       |
| DDR0_DM3        | DMI3        | IO           | R4       |
| DDR0_DQS0N      | DQS0        | IO           | B1       |
| DDR0_DQS0P      | DQS0_n      | IO           | B2       |
| DDR0_DQS1N      | DQS1        | IO           | E1       |
| DDR0_DQS1P      | DQS1_n      | IO           | E2       |
| DDR0_DQS2N      | DQS2        | IO           | M1       |
| DDR0_DQS2P      | DQS2_n      | IO           | M2       |
| DDR0_DQS3N      | DQS3        | IO           | R1       |
| DDR0_DQS3P      | DQS3_n      | IO           | R2       |
| DDR0_RESETn     | RESET_n     | IO           | J5       |
| DDR0_CAL0       | VTP         | A            | K5       |
| DDR0_CKE0       |             | IO           | G2       |
| DDR0_CKE1       |             | IO           | H2       |
| DDR0_CSn0_0     |             | IO           | G3       |
| DDR0_CSn0_1     |             | IO           | K2       |

**Table 5-4. DDRSS Signal Mapping (continued)**

| SIGNAL NAME [1] | MEMORY TYPE | PIN TYPE [3] | BALL [4] |
|-----------------|-------------|--------------|----------|
|                 | LPDDR4      |              |          |
| DDR0_CSn1_0     |             | IO           | G5       |
| DDR0_CSn1_1     |             | IO           | J3       |

### 5.3.3 GPIO

#### 5.3.3.1 MAIN Domain

**Table 5-5. GPIO0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]              | PIN TYPE [3] | BALL [4] |
|-----------------|------------------------------|--------------|----------|
| GPIO0_0         | General Purpose Input/Output | IO           | U6       |
| GPIO0_1         | General Purpose Input/Output | IO           | T19      |
| GPIO0_2         | General Purpose Input/Output | IO           | AA17     |
| GPIO0_3         | General Purpose Input/Output | IO           | Y15      |
| GPIO0_4         | General Purpose Input/Output | IO           | AA20     |
| GPIO0_5         | General Purpose Input/Output | IO           | Y17      |
| GPIO0_6         | General Purpose Input/Output | IO           | Y16      |
| GPIO0_7         | General Purpose Input/Output | IO           | V17      |
| GPIO0_8         | General Purpose Input/Output | IO           | AA19     |
| GPIO0_9         | General Purpose Input/Output | IO           | V18      |
| GPIO0_10        | General Purpose Input/Output | IO           | V20      |
| GPIO0_11        | General Purpose Input/Output | IO           | W21      |
| GPIO0_12        | General Purpose Input/Output | IO           | V16      |
| GPIO0_13        | General Purpose Input/Output | IO           | Y18      |
| GPIO0_14        | General Purpose Input/Output | IO           | Y19      |
| GPIO0_15        | General Purpose Input/Output | IO           | Y21      |
| GPIO0_16        | General Purpose Input/Output | IO           | W16      |
| GPIO0_17        | General Purpose Input/Output | IO           | W15      |
| GPIO0_18        | General Purpose Input/Output | IO           | Y20      |
| GPIO0_19        | General Purpose Input/Output | IO           | V21      |
| GPIO0_20        | General Purpose Input/Output | IO           | V19      |
| GPIO0_21        | General Purpose Input/Output | IO           | T13      |
| GPIO0_22        | General Purpose Input/Output | IO           | U14      |
| GPIO0_23        | General Purpose Input/Output | IO           | U16      |
| GPIO0_24        | General Purpose Input/Output | IO           | U15      |
| GPIO0_25        | General Purpose Input/Output | IO           | T15      |
| GPIO0_26        | General Purpose Input/Output | IO           | U19      |
| GPIO0_27        | General Purpose Input/Output | IO           | T14      |
| GPIO0_28        | General Purpose Input/Output | IO           | U18      |
| GPIO0_29        | General Purpose Input/Output | IO           | U17      |
| GPIO0_30        | General Purpose Input/Output | IO           | U20      |
| GPIO0_31        | General Purpose Input/Output | IO           | Y14      |
| GPIO0_32        | General Purpose Input/Output | IO           | Y13      |
| GPIO0_33        | General Purpose Input/Output | IO           | AA15     |
| GPIO0_34        | General Purpose Input/Output | IO           | AA14     |
| GPIO0_35        | General Purpose Input/Output | IO           | AA18     |

**Table 5-5. GPIO0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]              | PIN TYPE [3] | BALL [4] |
|-----------------|------------------------------|--------------|----------|
| GPIO0_36        | General Purpose Input/Output | IO           | AA16     |
| GPIO0_37        | General Purpose Input/Output | IO           | W17      |
| GPIO0_38        | General Purpose Input/Output | IO           | W20      |
| GPIO0_39        | General Purpose Input/Output | IO           | V14      |
| GPIO0_40        | General Purpose Input/Output | IO           | V13      |
| GPIO0_41        | General Purpose Input/Output | IO           | U12      |
| GPIO0_42        | General Purpose Input/Output | IO           | W14      |
| GPIO0_43        | General Purpose Input/Output | IO           | W19      |
| GPIO0_44        | General Purpose Input/Output | IO           | U13      |
| GPIO0_45        | General Purpose Input/Output | IO           | V15      |
| GPIO0_46        | General Purpose Input/Output | IO           | U21      |
| GPIO0_47        | General Purpose Input/Output | IO           | T16      |
| GPIO0_48        | General Purpose Input/Output | IO           | T17      |
| GPIO0_49        | General Purpose Input/Output | IO           | T18      |
| GPIO0_50        | General Purpose Input/Output | IO           | T20      |
| GPIO0_51        | General Purpose Input/Output | IO           | W3       |
| GPIO0_52        | General Purpose Input/Output | IO           | U5       |
| GPIO0_53        | General Purpose Input/Output | IO           | Y1       |
| GPIO0_54        | General Purpose Input/Output | IO           | V4       |
| GPIO0_55        | General Purpose Input/Output | IO           | T5       |
| GPIO0_56        | General Purpose Input/Output | IO           | V3       |
| GPIO0_57        | General Purpose Input/Output | IO           | W2       |
| GPIO0_58        | General Purpose Input/Output | IO           | U3       |
| GPIO0_59        | General Purpose Input/Output | IO           | T3       |
| GPIO0_60        | General Purpose Input/Output | IO           | V1       |
| GPIO0_61        | General Purpose Input/Output | IO           | W1       |
| GPIO0_62        | General Purpose Input/Output | IO           | N19      |
| GPIO0_63        | General Purpose Input/Output | IO           | N20      |
| GPIO0_64        | General Purpose Input/Output | IO           | N21      |
| GPIO0_65        | General Purpose Input/Output | IO           | M19      |
| GPIO0_66        | General Purpose Input/Output | IO           | P21      |
| GPIO0_67        | General Purpose Input/Output | IO           | M20      |
| GPIO0_68        | General Purpose Input/Output | IO           | T4       |

**5.3.3.2 WKUP Domain****Table 5-6. GPIO0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]              | PIN TYPE [3] | ALF [4] |
|-----------------|------------------------------|--------------|---------|
| WKUP_GPIO0_0    | General Purpose Input/Output | IO           | B18     |
| WKUP_GPIO0_1    | General Purpose Input/Output | IO           | B19     |
| WKUP_GPIO0_2    | General Purpose Input/Output | IO           | D14     |
| WKUP_GPIO0_3    | General Purpose Input/Output | IO           | B21     |
| WKUP_GPIO0_4    | General Purpose Input/Output | IO           | D13     |
| WKUP_GPIO0_5    | General Purpose Input/Output | IO           | B16     |
| WKUP_GPIO0_6    | General Purpose Input/Output | IO           | C14     |

**Table 5-6. GPIO0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]              | PIN TYPE [3] | ALF [4] |
|-----------------|------------------------------|--------------|---------|
| WKUP_GPIO0_7    | General Purpose Input/Output | IO           | C18     |
| WKUP_GPIO0_8    | General Purpose Input/Output | IO           | C21     |
| WKUP_GPIO0_9    | General Purpose Input/Output | IO           | C19     |
| WKUP_GPIO0_10   | General Purpose Input/Output | IO           | C20     |
| WKUP_GPIO0_11   | General Purpose Input/Output | IO           | C16     |
| WKUP_GPIO0_12   | General Purpose Input/Output | IO           | D19     |
| WKUP_GPIO0_13   | General Purpose Input/Output | IO           | D20     |
| WKUP_GPIO0_14   | General Purpose Input/Output | IO           | E20     |
| WKUP_GPIO0_15   | General Purpose Input/Output | IO           | E21     |
| WKUP_GPIO0_16   | General Purpose Input/Output | IO           | B6      |
| WKUP_GPIO0_17   | General Purpose Input/Output | IO           | C8      |
| WKUP_GPIO0_18   | General Purpose Input/Output | IO           | B7      |
| WKUP_GPIO0_19   | General Purpose Input/Output | IO           | D8      |
| WKUP_GPIO0_20   | General Purpose Input/Output | IO           | C7      |
| WKUP_GPIO0_21   | General Purpose Input/Output | IO           | C5      |
| WKUP_GPIO0_22   | General Purpose Input/Output | IO           | A5      |
| WKUP_GPIO0_23   | General Purpose Input/Output | IO           | A6      |
| WKUP_GPIO0_24   | General Purpose Input/Output | IO           | B8      |
| WKUP_GPIO0_25   | General Purpose Input/Output | IO           | A8      |
| WKUP_GPIO0_26   | General Purpose Input/Output | IO           | A7      |
| WKUP_GPIO0_27   | General Purpose Input/Output | IO           | D6      |
| WKUP_GPIO0_28   | General Purpose Input/Output | IO           | D7      |
| WKUP_GPIO0_29   | General Purpose Input/Output | IO           | D11     |
| WKUP_GPIO0_30   | General Purpose Input/Output | IO           | C6      |
| WKUP_GPIO0_31   | General Purpose Input/Output | IO           | D5      |
| WKUP_GPIO0_43   | General Purpose Input/Output | IO           | A11     |
| WKUP_GPIO0_44   | General Purpose Input/Output | IO           | C12     |
| WKUP_GPIO0_45   | General Purpose Input/Output | IO           | B12     |
| WKUP_GPIO0_46   | General Purpose Input/Output | IO           | B11     |
| WKUP_GPIO0_47   | General Purpose Input/Output | IO           | D10     |
| WKUP_GPIO0_48   | General Purpose Input/Output | IO           | A12     |
| WKUP_GPIO0_49   | General Purpose Input/Output | IO           | B10     |
| WKUP_GPIO0_50   | General Purpose Input/Output | IO           | C10     |
| WKUP_GPIO0_51   | General Purpose Input/Output | IO           | A10     |
| WKUP_GPIO0_52   | General Purpose Input/Output | IO           | B9      |
| WKUP_GPIO0_53   | General Purpose Input/Output | IO           | A9      |
| WKUP_GPIO0_54   | General Purpose Input/Output | IO           | C9      |
| WKUP_GPIO0_55   | General Purpose Input/Output | IO           | D9      |
| WKUP_GPIO0_56   | General Purpose Input/Output | IO           | C13     |
| WKUP_GPIO0_57   | General Purpose Input/Output | IO           | A20     |
| WKUP_GPIO0_58   | General Purpose Input/Output | IO           | B17     |
| WKUP_GPIO0_59   | General Purpose Input/Output | IO           | A19     |
| WKUP_GPIO0_60   | General Purpose Input/Output | IO           | B14     |
| WKUP_GPIO0_61   | General Purpose Input/Output | IO           | A14     |

**Table 5-6. GPIO0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]              | PIN TYPE [3] | ALF [4] |
|-----------------|------------------------------|--------------|---------|
| WKUP_GPIO0_62   | General Purpose Input/Output | IO           | A16     |
| WKUP_GPIO0_63   | General Purpose Input/Output | IO           | A17     |
| WKUP_GPIO0_64   | General Purpose Input/Output | IO           | F20     |
| WKUP_GPIO0_65   | General Purpose Input/Output | IO           | H21     |
| WKUP_GPIO0_66   | General Purpose Input/Output | IO           | G21     |
| WKUP_GPIO0_67   | General Purpose Input/Output | IO           | G20     |
| WKUP_GPIO0_68   | General Purpose Input/Output | IO           | C15     |
| WKUP_GPIO0_77   | General Purpose Input/Output | IO           | D21     |
| WKUP_GPIO0_78   | General Purpose Input/Output | IO           | E19     |
| WKUP_GPIO0_79   | General Purpose Input/Output | IO           | B13     |
| WKUP_GPIO0_80   | General Purpose Input/Output | IO           | D18     |
| WKUP_GPIO0_81   | General Purpose Input/Output | IO           | C17     |
| WKUP_GPIO0_84   | General Purpose Input/Output | IO           | E18     |

**5.3.4 I2C****5.3.4.1 MAIN Domain****Table 5-7. I2C0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------|--------------|----------|
| I2C0_SCL        | I2C Clock       | IOD          | V3       |
| I2C0_SDA        | I2C Data        | IOD          | W2       |

**Table 5-8. I2C1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------|--------------|----------|
| I2C1_SCL        | I2C Clock       | IOD          | U3, V17  |
| I2C1_SDA        | I2C Data        | IOD          | AA19, T3 |

**Table 5-9. I2C2 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------|--------------|----------|
| I2C2_SCL        | I2C Clock       | IOD          | W15, Y1  |
| I2C2_SDA        | I2C Data        | IOD          | V4, Y20  |

**Table 5-10. I2C3 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------|--------------|----------|
| I2C3_SCL        | I2C Clock       | IOD          | N19, V19 |
| I2C3_SDA        | I2C Data        | IOD          | N20, T13 |

**Table 5-11. I2C4 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------|--------------|----------|
| I2C4_SCL        | I2C Clock       | IOD          | M19, W14 |
| I2C4_SDA        | I2C Data        | IOD          | N21, W19 |

**Table 5-12. I2C5 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------|--------------|----------|
| I2C5_SCL        | I2C Clock       | IOD          | AA18     |
| I2C5_SDA        | I2C Data        | IOD          | AA16     |

**Table 5-13. I2C6 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | PIN TYPE [3] | BALL [4]  |
|-----------------|-----------------|--------------|-----------|
| I2C6_SCL        | I2C Clock       | IOD          | AA15, M20 |
| I2C6_SDA        | I2C Data        | IOD          | AA14, P21 |

#### 5.3.4.2 MCU Domain

**Table 5-14. I2C0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------|--------------|----------|
| MCU_I2C0_SCL    | I2C Clock       | IOD          | G21      |
| MCU_I2C0_SDA    | I2C Data        | IOD          | G20      |

**Table 5-15. I2C1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------|--------------|----------|
| MCU_I2C1_SCL    | I2C Clock       | IOD          | C14, C21 |
| MCU_I2C1_SDA    | I2C Data        | IOD          | C18, C19 |

#### 5.3.4.3 WKUP Domain

**Table 5-16. I2C0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------|--------------|----------|
| WKUP_I2C0_SCL   | I2C Clock       | IOD          | F20      |
| WKUP_I2C0_SDA   | I2C Data        | IOD          | H21      |

### 5.3.5 I3C

#### 5.3.5.1 MAIN Domain

**Table 5-17. I3C0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                  | PIN TYPE [3] | BALL [4] |
|-----------------|----------------------------------|--------------|----------|
| I3C0_SCL        | I3C Clock                        | IO           | AA18     |
| I3C0_SDA        | I3C Data                         | IO           | AA16     |
| I3C0_SDAPULLEN  | MAIN domain I3C Data Pull Enable | O            | AA14     |

#### 5.3.5.2 MCU Domain

**Table 5-18. I3C0 Signal Descriptions**

| SIGNAL NAME [1]    | DESCRIPTION [2]                 | PIN TYPE [3] | BALL [4] |
|--------------------|---------------------------------|--------------|----------|
| MCU_I3C0_SCL       | I3C Clock                       | IO           | C21      |
| MCU_I3C0_SDA       | I3C Data                        | IO           | C19      |
| MCU_I3C0_SDAPULLEN | MCU domain I3C Data Pull Enable | O            | C15, C16 |

### 5.3.6 MCAN

#### 5.3.6.1 MAIN Domain

**Table 5-19. MCAN0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]    | PIN TYPE [3] | BALL [4] |
|-----------------|--------------------|--------------|----------|
| MCAN0_RX        | MCAN Receive Data  | I            | V20      |
| MCAN0_TX        | MCAN Transmit Data | O            | V18      |

**Table 5-20. MCAN1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]    | PIN TYPE [3] | BALL [4] |
|-----------------|--------------------|--------------|----------|
| MCAN1_RX        | MCAN Receive Data  | I            | V16      |
| MCAN1_TX        | MCAN Transmit Data | O            | W21      |

**Table 5-21. MCAN2 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]    | PIN TYPE [3] | BALL [4] |
|-----------------|--------------------|--------------|----------|
| MCAN2_RX        | MCAN Receive Data  | I            | Y19      |
| MCAN2_TX        | MCAN Transmit Data | O            | Y18      |

**Table 5-22. MCAN3 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]    | PIN TYPE [3] | BALL [4] |
|-----------------|--------------------|--------------|----------|
| MCAN3_RX        | MCAN Receive Data  | I            | W16      |
| MCAN3_TX        | MCAN Transmit Data | O            | Y21      |

**Table 5-23. MCAN4 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]    | PIN TYPE [3] | BALL [4] |
|-----------------|--------------------|--------------|----------|
| MCAN4_RX        | MCAN Receive Data  | I            | Y20      |
| MCAN4_TX        | MCAN Transmit Data | O            | W15      |

**Table 5-24. MCAN5 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]    | PIN TYPE [3] | BALL [4] |
|-----------------|--------------------|--------------|----------|
| MCAN5_RX        | MCAN Receive Data  | I            | V19      |
| MCAN5_TX        | MCAN Transmit Data | O            | V21      |

**Table 5-25. MCAN6 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]    | PIN TYPE [3] | BALL [4] |
|-----------------|--------------------|--------------|----------|
| MCAN6_RX        | MCAN Receive Data  | I            | U14      |
| MCAN6_TX        | MCAN Transmit Data | O            | T13      |

**Table 5-26. MCAN7 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]    | PIN TYPE [3] | BALL [4] |
|-----------------|--------------------|--------------|----------|
| MCAN7_RX        | MCAN Receive Data  | I            | U15      |
| MCAN7_TX        | MCAN Transmit Data | O            | U16      |

**Table 5-27. MCAN8 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]    | PIN TYPE [3] | BALL [4] |
|-----------------|--------------------|--------------|----------|
| MCAN8_RX        | MCAN Receive Data  | I            | U19      |
| MCAN8_TX        | MCAN Transmit Data | O            | T15      |

**Table 5-28. MCAN9 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]    | PIN TYPE [3] | BALL [4] |
|-----------------|--------------------|--------------|----------|
| MCAN9_RX        | MCAN Receive Data  | I            | U18      |
| MCAN9_TX        | MCAN Transmit Data | O            | T14      |

**Table 5-29. MCAN10 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]    | PIN TYPE [3] | BALL [4] |
|-----------------|--------------------|--------------|----------|
| MCAN10_RX       | MCAN Receive Data  | I            | U20      |
| MCAN10_TX       | MCAN Transmit Data | O            | U17      |

**Table 5-30. MCAN11 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]    | PIN TYPE [3] | BALL [4] |
|-----------------|--------------------|--------------|----------|
| MCAN11_RX       | MCAN Receive Data  | I            | Y13      |
| MCAN11_TX       | MCAN Transmit Data | O            | Y14      |

**Table 5-31. MCAN12 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]    | PIN TYPE [3] | BALL [4] |
|-----------------|--------------------|--------------|----------|
| MCAN12_RX       | MCAN Receive Data  | I            | AA14     |
| MCAN12_TX       | MCAN Transmit Data | O            | AA15     |

**Table 5-32. MCAN13 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]    | PIN TYPE [3] | BALL [4] |
|-----------------|--------------------|--------------|----------|
| MCAN13_RX       | MCAN Receive Data  | I            | AA16     |
| MCAN13_TX       | MCAN Transmit Data | O            | AA18     |

**Table 5-33. MCAN14 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]    | PIN TYPE [3] | BALL [4] |
|-----------------|--------------------|--------------|----------|
| MCAN14_RX       | MCAN Receive Data  | I            | Y15      |
| MCAN14_TX       | MCAN Transmit Data | O            | AA17     |

**Table 5-34. MCAN15 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]    | PIN TYPE [3] | BALL [4] |
|-----------------|--------------------|--------------|----------|
| MCAN15_RX       | MCAN Receive Data  | I            | W20      |
| MCAN15_TX       | MCAN Transmit Data | O            | W17      |

**Table 5-35. MCAN16 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]    | PIN TYPE [3] | BALL [4] |
|-----------------|--------------------|--------------|----------|
| MCAN16_RX       | MCAN Receive Data  | I            | U21      |
| MCAN16_TX       | MCAN Transmit Data | O            | V15      |

**Table 5-36. MCAN17 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]    | PIN TYPE [3] | BALL [4] |
|-----------------|--------------------|--------------|----------|
| MCAN17_RX       | MCAN Receive Data  | I            | T20      |
| MCAN17_TX       | MCAN Transmit Data | O            | T18      |

**5.3.6.2 MCU Domain****Table 5-37. MCAN0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]    | PIN TYPE [3] | BALL [4] |
|-----------------|--------------------|--------------|----------|
| MCU_MCAN0_RX    | MCAN Receive Data  | I            | A17      |
| MCU_MCAN0_TX    | MCAN Transmit Data | O            | A16      |

**Table 5-38. MCAN1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]    | PIN TYPE [3] | BALL [4] |
|-----------------|--------------------|--------------|----------|
| MCU_MCAN1_RX    | MCAN Receive Data  | I            | B16      |
| MCU_MCAN1_TX    | MCAN Transmit Data | O            | D13      |

**5.3.7 MCSPI****5.3.7.1 MAIN Domain****Table 5-39. MCSPI0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]   | PIN TYPE [3] | BALL [4] |
|-----------------|-------------------|--------------|----------|
| SPI0_CLK        | SPI Clock         | IO           | Y1       |
| SPI0_CS0        | SPI Chip Select 0 | IO           | W3       |
| SPI0_CS1        | SPI Chip Select 1 | IO           | U5       |
| SPI0_CS2        | SPI Chip Select 2 | IO           | Y14      |
| SPI0_CS3        | SPI Chip Select 3 | IO           | U13      |
| SPI0_D0         | SPI Data 0        | IO           | V4       |
| SPI0_D1         | SPI Data 1        | IO           | T5       |

**Table 5-40. MCSPI1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]   | PIN TYPE [3] | BALL [4] |
|-----------------|-------------------|--------------|----------|
| SPI1_CLK        | SPI Clock         | IO           | P21      |
| SPI1_CS0        | SPI Chip Select 0 | IO           | N19      |
| SPI1_CS1        | SPI Chip Select 1 | IO           | N20      |
| SPI1_CS2        | SPI Chip Select 2 | IO           | N21      |
| SPI1_CS3        | SPI Chip Select 3 | IO           | W19      |
| SPI1_D0         | SPI Data 0        | IO           | M19      |
| SPI1_D1         | SPI Data 1        | IO           | M20      |

**Table 5-41. MCSPI2 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]   | PIN TYPE [3] | BALL [4] |
|-----------------|-------------------|--------------|----------|
| SPI2_CLK        | SPI Clock         | IO           | U20      |
| SPI2_CS0        | SPI Chip Select 0 | IO           | Y14      |
| SPI2_CS1        | SPI Chip Select 1 | IO           | Y13      |
| SPI2_CS2        | SPI Chip Select 2 | IO           | AA15     |
| SPI2_CS3        | SPI Chip Select 3 | IO           | AA14     |

**Table 5-41. MCSPI2 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2] | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------|--------------|----------|
| SPI2_D0         | SPI Data 0      | IO           | AA18     |
| SPI2_D1         | SPI Data 1      | IO           | AA16     |

**Table 5-42. MCSPI3 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]   | PIN TYPE [3] | BALL [4] |
|-----------------|-------------------|--------------|----------|
| SPI3_CLK        | SPI Clock         | IO           | T14      |
| SPI3_CS0        | SPI Chip Select 0 | IO           | U16      |
| SPI3_CS1        | SPI Chip Select 1 | IO           | U15      |
| SPI3_CS2        | SPI Chip Select 2 | IO           | T15      |
| SPI3_CS3        | SPI Chip Select 3 | IO           | U19      |
| SPI3_D0         | SPI Data 0        | IO           | U18      |
| SPI3_D1         | SPI Data 1        | IO           | U17      |

**Table 5-43. MCSPI5 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]   | PIN TYPE [3] | BALL [4] |
|-----------------|-------------------|--------------|----------|
| SPI5_CLK        | SPI Clock         | IO           | W15      |
| SPI5_CS0        | SPI Chip Select 0 | IO           | W16      |
| SPI5_CS1        | SPI Chip Select 1 | IO           | V21      |
| SPI5_CS2        | SPI Chip Select 2 | IO           | Y19      |
| SPI5_CS3        | SPI Chip Select 3 | IO           | Y18      |
| SPI5_D0         | SPI Data 0        | IO           | Y21      |
| SPI5_D1         | SPI Data 1        | IO           | Y20      |

**Table 5-44. MCSPI6 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]   | PIN TYPE [3] | BALL [4] |
|-----------------|-------------------|--------------|----------|
| SPI6_CLK        | SPI Clock         | IO           | V14      |
| SPI6_CS0        | SPI Chip Select 0 | IO           | W21      |
| SPI6_CS1        | SPI Chip Select 1 | IO           | V16      |
| SPI6_CS2        | SPI Chip Select 2 | IO           | W17      |
| SPI6_CS3        | SPI Chip Select 3 | IO           | W20      |
| SPI6_D0         | SPI Data 0        | IO           | V13      |
| SPI6_D1         | SPI Data 1        | IO           | U12      |

**Table 5-45. MCSPI7 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]   | PIN TYPE [3] | BALL [4] |
|-----------------|-------------------|--------------|----------|
| SPI7_CLK        | SPI Clock         | IO           | T3       |
| SPI7_CS0        | SPI Chip Select 0 | IO           | U3       |
| SPI7_D0         | SPI Data 0        | IO           | V1       |
| SPI7_D1         | SPI Data 1        | IO           | W1       |

### 5.3.7.2 MCU Domain

**Table 5-46. MCSPI0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]   | PIN TYPE [3] | BALL [4] |
|-----------------|-------------------|--------------|----------|
| MCU_SPI0_CLK    | SPI Clock         | IO           | C13      |
| MCU_SPI0_CS0    | SPI Chip Select 0 | IO           | A19      |
| MCU_SPI0_CS1    | SPI Chip Select 1 | IO           | D19      |
| MCU_SPI0_CS2    | SPI Chip Select 2 | IO           | E20      |
| MCU_SPI0_CS3    | SPI Chip Select 3 | IO           | D13      |
| MCU_SPI0_D0     | SPI Data 0        | IO           | A20      |
| MCU_SPI0_D1     | SPI Data 1        | IO           | B17      |

**Table 5-47. MCSPI1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]   | PIN TYPE [3] | BALL [4] |
|-----------------|-------------------|--------------|----------|
| MCU_SPI1_CLK    | SPI Clock         | IO           | B18      |
| MCU_SPI1_CS0    | SPI Chip Select 0 | IO           | B21      |
| MCU_SPI1_CS1    | SPI Chip Select 1 | IO           | D20      |
| MCU_SPI1_CS2    | SPI Chip Select 2 | IO           | E21      |
| MCU_SPI1_CS3    | SPI Chip Select 3 | IO           | B16      |
| MCU_SPI1_D0     | SPI Data 0        | IO           | B19      |
| MCU_SPI1_D1     | SPI Data 1        | IO           | D14      |

### 5.3.8 UART

#### 5.3.8.1 MAIN Domain

**Table 5-48. UART0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                       | PIN TYPE [3] | BALL [4] |
|-----------------|---------------------------------------|--------------|----------|
| UART0_CTSn      | UART Clear to Send (active low)       | I            | N19, W3  |
| UART0_DCDn      | UART Data Carrier Detect (active low) | I            | T15      |
| UART0_DSRn      | UART Data Set Ready (active low)      | I            | U19      |
| UART0_DTRn      | UART Data Terminal Ready (active low) | O            | Y14      |
| UART0_RIn       | UART Ring Indicator                   | I            | Y13      |
| UART0_RTSn      | UART Request to Send (active low)     | O            | P21, U5  |
| UART0_RXD       | UART Receive Data                     | I            | T16      |
| UART0_TXD       | UART Transmit Data                    | O            | T17      |

**Table 5-49. UART1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                   | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------------------------|--------------|----------|
| UART1_CTSn      | UART Clear to Send (active low)   | I            | Y1       |
| UART1_RTSn      | UART Request to Send (active low) | O            | V4       |
| UART1_RXD       | UART Receive Data                 | I            | T18      |
| UART1_TXD       | UART Transmit Data                | O            | T20      |

**Table 5-50. UART2 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                   | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------------------------|--------------|----------|
| UART2_CTSn      | UART Clear to Send (active low)   | I            | U17      |
| UART2_RTSn      | UART Request to Send (active low) | O            | U20      |

**Table 5-50. UART2 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]    | PIN TYPE [3] | BALL [4]       |
|-----------------|--------------------|--------------|----------------|
| UART2_RXD       | UART Receive Data  | I            | AA15, N21, V14 |
| UART2_TXD       | UART Transmit Data | O            | AA14, M19, V13 |

**Table 5-51. UART3 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                   | PIN TYPE [3] | BALL [4]     |
|-----------------|-----------------------------------|--------------|--------------|
| UART3_CTSn      | UART Clear to Send (active low)   | I            | T15, V1      |
| UART3_RTSn      | UART Request to Send (active low) | O            | U19, W1      |
| UART3_RXD       | UART Receive Data                 | I            | U3, Y14, Y18 |
| UART3_TXD       | UART Transmit Data                | O            | T3, Y13, Y19 |

**Table 5-52. UART4 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                   | PIN TYPE [3] | BALL [4]  |
|-----------------|-----------------------------------|--------------|-----------|
| UART4_CTSn      | UART Clear to Send (active low)   | I            | P21       |
| UART4_RTSn      | UART Request to Send (active low) | O            | M20       |
| UART4_RXD       | UART Receive Data                 | I            | N21, U12  |
| UART4_TXD       | UART Transmit Data                | O            | AA20, M19 |

**Table 5-53. UART5 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                   | PIN TYPE [3] | BALL [4]  |
|-----------------|-----------------------------------|--------------|-----------|
| UART5_CTSn      | UART Clear to Send (active low)   | I            | N21       |
| UART5_RTSn      | UART Request to Send (active low) | O            | M19       |
| UART5_RXD       | UART Receive Data                 | I            | N19, Y15  |
| UART5_TXD       | UART Transmit Data                | O            | AA17, N20 |

**Table 5-54. UART6 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                   | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------------------------|--------------|----------|
| UART6_CTSn      | UART Clear to Send (active low)   | I            | V16      |
| UART6_RTSn      | UART Request to Send (active low) | O            | V21      |
| UART6_RXD       | UART Receive Data                 | I            | Y16      |
| UART6_TXD       | UART Transmit Data                | O            | Y17      |

**Table 5-55. UART7 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                   | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------------------------|--------------|----------|
| UART7_CTSn      | UART Clear to Send (active low)   | I            | N21      |
| UART7_RTSn      | UART Request to Send (active low) | O            | M19      |
| UART7_RXD       | UART Receive Data                 | I            | N19, U21 |
| UART7_TXD       | UART Transmit Data                | O            | N20, V15 |

**Table 5-56. UART8 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                   | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------------------------|--------------|----------|
| UART8_CTSn      | UART Clear to Send (active low)   | I            | AA18     |
| UART8_RTSn      | UART Request to Send (active low) | O            | AA16     |
| UART8_RXD       | UART Receive Data                 | I            | P21, W14 |

**Table 5-56. UART8 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]    | PIN TYPE [3] | BALL [4] |
|-----------------|--------------------|--------------|----------|
| UART8_TXD       | UART Transmit Data | O            | M20, W19 |

**Table 5-57. UART9 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                   | PIN TYPE [3] | BALL [4]  |
|-----------------|-----------------------------------|--------------|-----------|
| UART9_CTSn      | UART Clear to Send (active low)   | I            | Y18       |
| UART9_RTSn      | UART Request to Send (active low) | O            | Y19       |
| UART9_RXD       | UART Receive Data                 | I            | AA19, U13 |
| UART9_TXD       | UART Transmit Data                | O            | V17       |

**5.3.8.2 MCU Domain**

**Table 5-58. UART0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                   | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------------------------|--------------|----------|
| MCU_UART0_CTSn  | UART Clear to Send (active low)   | I            | E20      |
| MCU_UART0_RTSn  | UART Request to Send (active low) | O            | E21      |
| MCU_UART0_RXD   | UART Receive Data                 | I            | C16, D20 |
| MCU_UART0_TXD   | UART Transmit Data                | O            | C20, D19 |

**5.3.8.3 WKUP Domain**

**Table 5-59. UART0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                   | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------------------------|--------------|----------|
| WKUP_UART0_CTSn | UART Clear to Send (active low)   | I            | C14      |
| WKUP_UART0_RTSn | UART Request to Send (active low) | O            | C18      |
| WKUP_UART0_RXD  | UART Receive Data                 | I            | B14      |
| WKUP_UART0_TXD  | UART Transmit Data                | O            | A14      |

**5.3.9 MDIO**

**5.3.9.1 MCU Domain**

**Table 5-60. MDIO0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------|--------------|----------|
| MCU_MDIO0_MDC   | MDIO Clock      | O            | D9       |
| MCU_MDIO0_MDIO  | MDIO Data       | IO           | C9       |

**5.3.9.2 MAIN Domain**

**Table 5-61. MDIO0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------|--------------|----------|
| MDIO0_MDC       | MDIO Clock      | O            | W19      |
| MDIO0_MDIO      | MDIO Data       | IO           | W14      |

### 5.3.10 CPSW2G

#### 5.3.10.1 MCU Domain

**Table 5-62. CPSW2G0 Signal Descriptions**

| SIGNAL NAME [1]   | DESCRIPTION [2]                 | PIN TYPE [3] | BALL [4] |
|-------------------|---------------------------------|--------------|----------|
| MCU_RGMII1_RXC    | RGMII Receive Clock             | I            | B10      |
| MCU_RGMII1_TXC    | RGMII Transmit Clock            | O            | A12      |
| MCU_RGMII1_RX_CTL | RGMII Receive Control           | I            | A11      |
| MCU_RGMII1_TX_CTL | RGMII Transmit Control          | O            | D11      |
| MCU_RGMII1_RD0    | RGMII Receive Data 0            | I            | A9       |
| MCU_RGMII1_RD1    | RGMII Receive Data 1            | I            | B9       |
| MCU_RGMII1_RD2    | RGMII Receive Data 2            | I            | A10      |
| MCU_RGMII1_RD3    | RGMII Receive Data 3            | I            | C10      |
| MCU_RGMII1_TD0    | RGMII Transmit Data 0           | O            | D10      |
| MCU_RGMII1_TD1    | RGMII Transmit Data 1           | O            | B11      |
| MCU_RGMII1_TD2    | RGMII Transmit Data 2           | O            | B12      |
| MCU_RGMII1_TD3    | RGMII Transmit Data 3           | O            | C12      |
| MCU_RMII1_CRD_V   | RMII Carrier Sense / Data Valid | I            | D11      |
| MCU_RMII1_REF_CLK | RMII Reference Clock            | I            | B10      |
| MCU_RMII1_RX_ER   | RMII Receive Data Error         | I            | A11      |
| MCU_RMII1_TX_EN   | RMII Transmit Enable            | O            | A12      |
| MCU_RMII1_RXD0    | RMII Receive Data 0             | I            | A9       |
| MCU_RMII1_RXD1    | RMII Receive Data 1             | I            | B9       |
| MCU_RMII1_TXD0    | RMII Transmit Data 0            | O            | D10      |
| MCU_RMII1_TXD1    | RMII Transmit Data 1            | O            | B11      |

### 5.3.11 CPSW5G

#### 5.3.11.1 MAIN Domain

**Table 5-63. CPSW5G0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]  | PIN TYPE [3] | BALL [4] |
|-----------------|--|--------------|----------|
| CLKOUT          | RMII Clock Output (50 MHz). This pin is used for clock source to the external PHY and must be routed back to the RMII_REF_CLK pin for proper device operation. | OZ           | U21      |
| RGMII1_RXC      | RGMII Receive Clock  | I            | AA19     |
| RGMII1_TXC      | RGMII Transmit Clock   | O            | Y20      |
| RGMII1_RX_CTL   | RGMII Receive Control  | I            | Y16      |
| RGMII1_TX_CTL   | RGMII Transmit Control   | O            | W15      |
| RGMII1_RD0      | RGMII Receive Data 0   | I            | AA17     |
| RGMII1_RD1      | RGMII Receive Data 1   | I            | Y15      |
| RGMII1_RD2      | RGMII Receive Data 2   | I            | AA20     |
| RGMII1_RD3      | RGMII Receive Data 3   | I            | Y17      |
| RGMII1_TD0      | RGMII Transmit Data 0  | O            | Y18      |
| RGMII1_TD1      | RGMII Transmit Data 1  | O            | Y19      |
| RGMII1_TD2      | RGMII Transmit Data 2  | O            | Y21      |
| RGMII1_TD3      | RGMII Transmit Data 3  | O            | W16      |
| RGMII2_RXC      | RGMII Receive Clock  | I            | Y14      |
| RGMII2_TXC      | RGMII Transmit Clock   | O            | W21      |

**Table 5-63. CPSW5G0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]                  | PIN TYPE [3] | BALL [4] |
|-----------------|----------------------------------|--------------|----------|
| RGMI2_RX_CTL    | RGMI2 Receive Control            | I            | AA16     |
| RGMI2_TX_CTL    | RGMI2 Transmit Control           | O            | U12      |
| RGMI2_RD0       | RGMI2 Receive Data 0             | I            | Y13      |
| RGMI2_RD1       | RGMI2 Receive Data 1             | I            | AA15     |
| RGMI2_RD2       | RGMI2 Receive Data 2             | I            | AA14     |
| RGMI2_RD3       | RGMI2 Receive Data 3             | I            | AA18     |
| RGMI2_TD0       | RGMI2 Transmit Data 0            | O            | W17      |
| RGMI2_TD1       | RGMI2 Transmit Data 1            | O            | W20      |
| RGMI2_TD2       | RGMI2 Transmit Data 2            | O            | V14      |
| RGMI2_TD3       | RGMI2 Transmit Data 3            | O            | V13      |
| RGMI3_RXC       | RGMI3 Receive Clock              | I            | V21      |
| RGMI3_TXC       | RGMI3 Transmit Clock             | O            | U20      |
| RGMI3_RX_CTL    | RGMI3 Receive Control            | I            | U15      |
| RGMI3_TX_CTL    | RGMI3 Transmit Control           | O            | U17      |
| RGMI3_RD0       | RGMI3 Receive Data 0             | I            | V19      |
| RGMI3_RD1       | RGMI3 Receive Data 1             | I            | T13      |
| RGMI3_RD2       | RGMI3 Receive Data 2             | I            | U14      |
| RGMI3_RD3       | RGMI3 Receive Data 3             | I            | U16      |
| RGMI3_TD0       | RGMI3 Transmit Data 0            | O            | T15      |
| RGMI3_TD1       | RGMI3 Transmit Data 1            | O            | U19      |
| RGMI3_TD2       | RGMI3 Transmit Data 2            | O            | T14      |
| RGMI3_TD3       | RGMI3 Transmit Data 3            | O            | U18      |
| RGMI4_RXC       | RGMI4 Receive Clock              | I            | V17      |
| RGMI4_TXC       | RGMI4 Transmit Clock             | O            | T16      |
| RGMI4_RX_CTL    | RGMI4 Receive Control            | I            | V15      |
| RGMI4_TX_CTL    | RGMI4 Transmit Control           | O            | T20      |
| RGMI4_RD0       | RGMI4 Receive Data 0             | I            | V18      |
| RGMI4_RD1       | RGMI4 Receive Data 1             | I            | V20      |
| RGMI4_RD2       | RGMI4 Receive Data 2             | I            | V16      |
| RGMI4_RD3       | RGMI4 Receive Data 3             | I            | U13      |
| RGMI4_TD0       | RGMI4 Transmit Data 0            | O            | U21      |
| RGMI4_TD1       | RGMI4 Transmit Data 1            | O            | T19      |
| RGMI4_TD2       | RGMI4 Transmit Data 2            | O            | T17      |
| RGMI4_TD3       | RGMI4 Transmit Data 3            | O            | T18      |
| RMII1_CRSDV     | RMII1 Carrier Sense / Data Valid | I            | AA20     |
| RMII1_RX_ER     | RMII1 Receive Data Error         | I            | Y17      |
| RMII1_TX_EN     | RMII1 Transmit Enable            | O            | V17      |
| RMII1_RXD0      | RMII1 Receive Data 0             | I            | AA17     |
| RMII1_RXD1      | RMII1 Receive Data 1             | I            | Y15      |
| RMII1_TXD0      | RMII1 Transmit Data 0            | O            | Y16      |
| RMII1_TXD1      | RMII1 Transmit Data 1            | O            | AA19     |
| RMII2_CRSDV     | RMII2 Carrier Sense / Data Valid | I            | V14      |
| RMII2_RX_ER     | RMII2 Receive Data Error         | I            | V13      |
| RMII2_TX_EN     | RMII2 Transmit Enable            | O            | W21      |

**Table 5-63. CPSW5G0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]                 | PIN TYPE [3] | BALL [4] |
|-----------------|---------------------------------|--------------|----------|
| RMII2_RXD0      | RMII Receive Data 0             | I            | W17      |
| RMII2_RXD1      | RMII Receive Data 1             | I            | W20      |
| RMII2_TXD0      | RMII Transmit Data 0            | O            | U12      |
| RMII2_TXD1      | RMII Transmit Data 1            | O            | V16      |
| RMII3_CRS_DV    | RMII Carrier Sense / Data Valid | I            | U14      |
| RMII3_RX_ER     | RMII Receive Data Error         | I            | U16      |
| RMII3_TX_EN     | RMII Transmit Enable            | O            | T15      |
| RMII3_RXD0      | RMII Receive Data 0             | I            | V19      |
| RMII3_RXD1      | RMII Receive Data 1             | I            | T13      |
| RMII3_TXD0      | RMII Transmit Data 0            | O            | U15      |
| RMII3_TXD1      | RMII Transmit Data 1            | O            | U19      |
| RMII4_CRS_DV    | RMII Carrier Sense / Data Valid | I            | Y21      |
| RMII4_RX_ER     | RMII Receive Data Error         | I            | W16      |
| RMII4_TX_EN     | RMII Transmit Enable            | O            | Y20      |
| RMII4_RXD0      | RMII Receive Data 0             | I            | Y18      |
| RMII4_RXD1      | RMII Receive Data 1             | I            | Y19      |
| RMII4_TXD0      | RMII Transmit Data 0            | O            | W15      |
| RMII4_TXD1      | RMII Transmit Data 1            | O            | V21      |
| RMII_REF_CLK    | RMII Reference Clock            | I            | V15      |

### 5.3.12 ECAP

#### 5.3.12.1 MAIN Domain

**Table 5-64. ECAP0 Signal Descriptions**

| SIGNAL NAME [1]   | DESCRIPTION [2]  | PIN TYPE [3] | BALL [4] |
|-------------------|--|--------------|----------|
| ECAP0_IN_APWM_OUT | Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output | IO           | N21, U3  |

**Table 5-65. ECAP1 Signal Descriptions**

| SIGNAL NAME [1]   | DESCRIPTION [2]  | PIN TYPE [3] | BALL [4] |
|-------------------|--|--------------|----------|
| ECAP1_IN_APWM_OUT | Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output | IO           | M19, V1  |

**Table 5-66. ECAP2 Signal Descriptions**

| SIGNAL NAME [1]   | DESCRIPTION [2]  | PIN TYPE [3] | BALL [4] |
|-------------------|--|--------------|----------|
| ECAP2_IN_APWM_OUT | Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output | IO           | W1       |

### 5.3.13 EQEP

#### 5.3.13.1 MAIN Domain

**Table 5-67. EQEP0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]         | PIN TYPE [3] | BALL [4] |
|-----------------|-------------------------|--------------|----------|
| EQEP0_A         | EQEP Quadrature Input A | I            | Y14      |
| EQEP0_B         | EQEP Quadrature Input B | I            | Y13      |
| EQEP0_I         | EQEP Index              | IO           | AA16     |

**Table 5-67. EQEP0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2] | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------|--------------|----------|
| EQEP0_S         | EQEP Strobe     | IO           | AA18     |

**Table 5-68. EQEP1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]         | PIN TYPE [3] | BALL [4] |
|-----------------|-------------------------|--------------|----------|
| EQEP1_A         | EQEP Quadrature Input A | I            | AA15     |
| EQEP1_B         | EQEP Quadrature Input B | I            | AA14     |
| EQEP1_I         | EQEP Index              | IO           | W20      |
| EQEP1_S         | EQEP Strobe             | IO           | W17      |

**Table 5-69. EQEP2 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]         | PIN TYPE [3] | BALL [4] |
|-----------------|-------------------------|--------------|----------|
| EQEP2_A         | EQEP Quadrature Input A | I            | V17      |
| EQEP2_B         | EQEP Quadrature Input B | I            | V18      |
| EQEP2_I         | EQEP Index              | IO           | V16      |
| EQEP2_S         | EQEP Strobe             | IO           | V20      |

**5.3.14 EPWM****5.3.14.1 MAIN Domain****Table 5-70. EPWM Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]              | PIN TYPE [3] | BALL [4] |
|-----------------|------------------------------|--------------|----------|
| EHRPWM_SOCA     | EHRPWM Start of Conversion A | O            | W21      |
| EHRPWM_SOCB     | EHRPWM Start of Conversion B | O            | U17      |

**Table 5-71. EPWM0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                                  | PIN TYPE [3] | BALL [4] |
|-----------------|--|--------------|----------|
| EHRPWM0_A       | EHRPWM Output A                                  | IO           | Y21      |
| EHRPWM0_B       | EHRPWM Output B                                  | IO           | Y19      |
| EHRPWM0_SYNCI   | Sync Input to EHRPWM module from an external pin | I            | W15      |
| EHRPWM0_SYNCO   | Sync Output to EHRPWM module to an external pin  | O            | Y16      |
| EHRPWM_TZn_IN0  | EHRPWM Trip Zone Input 0 (active low)            | I            | W16      |

**Table 5-72. EPWM1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                       | PIN TYPE [3] | BALL [4] |
|-----------------|---------------------------------------|--------------|----------|
| EHRPWM1_A       | EHRPWM Output A                       | IO           | Y18      |
| EHRPWM1_B       | EHRPWM Output B                       | IO           | Y20      |
| EHRPWM_TZn_IN1  | EHRPWM Trip Zone Input 1 (active low) | I            | AA19     |

**Table 5-73. EPWM2 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                       | PIN TYPE [3] | BALL [4] |
|-----------------|---------------------------------------|--------------|----------|
| EHRPWM2_A       | EHRPWM Output A                       | IO           | Y17      |
| EHRPWM2_B       | EHRPWM Output B                       | IO           | AA20     |
| EHRPWM_TZn_IN2  | EHRPWM Trip Zone Input 2 (active low) | I            | Y15      |

**Table 5-74. EPWM3 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                                  | PIN TYPE [3] | BALL [4] |
|-----------------|--|--------------|----------|
| EHRPWM3_A       | EHRPWM Output A                                  | IO           | U15      |
| EHRPWM3_B       | EHRPWM Output B                                  | IO           | U18      |
| EHRPWM3_SYNCI   | Sync Input to EHRPWM module from an external pin | I            | T14      |
| EHRPWM3_SYNCO   | Sync Output to EHRPWM module to an external pin  | O            | U19      |
| EHRPWM_TZn_IN3  | EHRPWM Trip Zone Input 3 (active low)            | I            | T15      |

**Table 5-75. EPWM4 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                       | PIN TYPE [3] | BALL [4] |
|-----------------|---------------------------------------|--------------|----------|
| EHRPWM4_A       | EHRPWM Output A                       | IO           | U20      |
| EHRPWM4_B       | EHRPWM Output B                       | IO           | V21      |
| EHRPWM_TZn_IN4  | EHRPWM Trip Zone Input 4 (active low) | I            | U16      |

**Table 5-76. EPWM5 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                       | PIN TYPE [3] | BALL [4] |
|-----------------|---------------------------------------|--------------|----------|
| EHRPWM5_A       | EHRPWM Output A                       | IO           | U14      |
| EHRPWM5_B       | EHRPWM Output B                       | IO           | T13      |
| EHRPWM_TZn_IN5  | EHRPWM Trip Zone Input 5 (active low) | I            | V19      |

### 5.3.15 USB

#### 5.3.15.1 MAIN Domain

**Note**

USB3 functionality is available on the SERDES pins. For more information, refer to [Section 5.3.16, SERDES](#).

**Table 5-77. USB0 Signal Descriptions**

| SIGNAL NAME [1]            | DESCRIPTION [2]                        | PIN TYPE [3] | BALL [4] |
|----------------------------|--|--------------|----------|
| USB0_DM                    | USB 2.0 Differential Data (negative)   | IO           | AA3      |
| USB0_DP                    | USB 2.0 Differential Data (positive)   | IO           | AA2      |
| USB0_DRVVBUS               | USB VBUS control output (active high)  | O            | T4, U13  |
| USB0_ID                    | USB 2.0 Dual-Role Device Role Select   | A            | V6       |
| USB0_RCALIB <sup>(2)</sup> | Pin to connect to calibration resistor | IO           | V5       |
| USB0_VBUS <sup>(1)</sup>   | USB Level-shifted VBUS Input           | A            | Y2       |

(1) An external resistor divider is required to limit the voltage applied to the device pin. For more information, see [Section 8.3.3, USB Design Guidelines](#).

(2) An external 500 Ω ±1% resistor must be connected between this pin and VSS, even when the pin is unused.

### 5.3.16 SERDES

**Note**

The functionality of these pins is controlled by SERDES0\_LN[4:0]\_CTRL\_LANE\_FUNC\_SEL.

## 5.3.16.1 MAIN Domain

Table 5-78. SERDES0 Lane0 Signal Descriptions

| SIGNAL NAME [1] | DESCRIPTION [2]                              | PIN TYPE [3] | BALL [4] |
|-----------------|--|--------------|----------|
| SERDES0_RX0_N   | SERDES Differential Receive Data (negative)  | I            | AA11     |
| SERDES0_RX0_P   | SERDES Differential Receive Data (positive)  | I            | AA12     |
| SERDES0_TX0_N   | SERDES Differential Transmit Data (negative) | O            | W11      |
| SERDES0_TX0_P   | SERDES Differential Transmit Data (positive) | O            | W12      |

Table 5-79. SERDES0 Lane1 Signal Descriptions

| SIGNAL NAME [1] | DESCRIPTION [2]                              | PIN TYPE [3] | BALL [4] |
|-----------------|--|--------------|----------|
| SERDES0_RX1_N   | SERDES Differential Receive Data (negative)  | I            | W8       |
| SERDES0_RX1_P   | SERDES Differential Receive Data (positive)  | I            | W9       |
| SERDES0_TX1_N   | SERDES Differential Transmit Data (negative) | O            | Y10      |
| SERDES0_TX1_P   | SERDES Differential Transmit Data (positive) | O            | Y11      |

Table 5-80. SERDES0 Lane2 Signal Descriptions

| SIGNAL NAME [1] | DESCRIPTION [2]                              | PIN TYPE [3] | BALL [4] |
|-----------------|--|--------------|----------|
| SERDES0_RX2_N   | SERDES Differential Receive Data (negative)  | I            | Y7       |
| SERDES0_RX2_P   | SERDES Differential Receive Data (positive)  | I            | Y8       |
| SERDES0_TX2_N   | SERDES Differential Transmit Data (negative) | O            | AA5      |
| SERDES0_TX2_P   | SERDES Differential Transmit Data (positive) | O            | AA6      |

Table 5-81. SERDES0 Lane3 Signal Descriptions

| SIGNAL NAME [1] | DESCRIPTION [2]                              | PIN TYPE [3] | BALL [4] |
|-----------------|--|--------------|----------|
| SERDES0_RX3_N   | SERDES Differential Receive Data (negative)  | I            | W5       |
| SERDES0_RX3_P   | SERDES Differential Receive Data (positive)  | I            | W6       |
| SERDES0_TX3_N   | SERDES Differential Transmit Data (negative) | O            | Y4       |
| SERDES0_TX3_P   | SERDES Differential Transmit Data (positive) | O            | Y5       |

Table 5-82. SERDES0 Signal Descriptions

| SIGNAL NAME [1]             | DESCRIPTION [2]                                | PIN TYPE [3] | BALL [4] |
|-----------------------------|--|--------------|----------|
| PCIE1_CLKREQn               | PCIE Clock Request Signal                      | IO           | N19, W1  |
| SERDES0_REXT <sup>(1)</sup> | External Calibration Resistor                  | A            | V7       |
| SERDES0_REFCLK_N            | Serdes Reference Clock Input/Output (negative) | IO           | AA8      |
| SERDES0_REFCLK_P            | Serdes Reference Clock Input/Output (positive) | IO           | AA9      |

(1) An external 3.01 kΩ ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.

## 5.3.17 OSPI

## 5.3.17.1 MCU Domain

Table 5-83. OSPI0 Signal Descriptions

| SIGNAL NAME [1]    | DESCRIPTION [2]                                | PIN TYPE [3] | BALL [4] |
|--------------------|--|--------------|----------|
| MCU_OSPI0_CLK      | OSPI Clock                                     | O            | B6       |
| MCU_OSPI0_DQS      | OSPI Data Strobe (DQS) or Loopback Clock Input | I            | B7       |
| MCU_OSPI0_ECC_FAIL | OSPI ECC Status                                | I            | D5       |
| MCU_OSPI0_LBCLKO   | OSPI Loopback Clock Output                     | IO           | C8       |

**Table 5-83. OSPI0 Signal Descriptions (continued)**

| SIGNAL NAME [1]      | DESCRIPTION [2]                 | PIN TYPE [3] | BALL [4] |
|----------------------|---------------------------------|--------------|----------|
| MCU_OSPI0_CSn0       | OSPI Chip Select 0 (active low) | O            | D6       |
| MCU_OSPI0_CSn1       | OSPI Chip Select 1 (active low) | O            | D7       |
| MCU_OSPI0_CSn2       | OSPI Chip Select 2 (active low) | O            | C6       |
| MCU_OSPI0_CSn3       | OSPI Chip Select 3 (active low) | O            | D5       |
| MCU_OSPI0_D0         | OSPI Data 0                     | IO           | D8       |
| MCU_OSPI0_D1         | OSPI Data 1                     | IO           | C7       |
| MCU_OSPI0_D2         | OSPI Data 2                     | IO           | C5       |
| MCU_OSPI0_D3         | OSPI Data 3                     | IO           | A5       |
| MCU_OSPI0_D4         | OSPI Data 4                     | IO           | A6       |
| MCU_OSPI0_D5         | OSPI Data 5                     | IO           | B8       |
| MCU_OSPI0_D6         | OSPI Data 6                     | IO           | A8       |
| MCU_OSPI0_D7         | OSPI Data 7                     | IO           | A7       |
| MCU_OSPI0_RESET_OUT0 | OSPI Reset                      | O            | C6       |
| MCU_OSPI0_RESET_OUT1 | OSPI Reset                      | O            | D5       |

### 5.3.18 Hyperbus

#### 5.3.18.1 MCU Domain

**Table 5-84. HYPERBUS0 Signal Descriptions**

| SIGNAL NAME [1]       | DESCRIPTION [2]   | PIN TYPE [3] | BALL [4] |
|-----------------------|---|--------------|----------|
| MCU_HYPERBUS0_CK      | Hyperbus Differential Clock (positive)                            | O            | B6       |
| MCU_HYPERBUS0_CKn     | Hyperbus Differential Clock (negative)                            | O            | C8       |
| MCU_HYPERBUS0_INTn    | Hyperbus Interrupt (active low)                                   | I            | D5       |
| MCU_HYPERBUS0_RESETn  | Hyperbus Reset (active low) Output                                | O            | D7       |
| MCU_HYPERBUS0_RESETOn | Hyperbus Reset Status Indicator (active low) from Hyperbus Memory | I            | C6       |
| MCU_HYPERBUS0_RWDS    | Hyperbus Read-Write Data Strobe                                   | IO           | B7       |
| MCU_HYPERBUS0_WPn     | Hyperbus Write Protect (Not in use)                               | O            | C6, D5   |
| MCU_HYPERBUS0_CSn0    | Hyperbus Chip Select 0  | O            | D6       |
| MCU_HYPERBUS0_CSn1    | Hyperbus Chip Select 1  | O            | C6       |
| MCU_HYPERBUS0_DQ0     | Hyperbus Data 0   | IO           | D8       |
| MCU_HYPERBUS0_DQ1     | Hyperbus Data 1   | IO           | C7       |
| MCU_HYPERBUS0_DQ2     | Hyperbus Data 2   | IO           | C5       |
| MCU_HYPERBUS0_DQ3     | Hyperbus Data 3   | IO           | A5       |
| MCU_HYPERBUS0_DQ4     | Hyperbus Data 4   | IO           | A6       |
| MCU_HYPERBUS0_DQ5     | Hyperbus Data 5   | IO           | B8       |
| MCU_HYPERBUS0_DQ6     | Hyperbus Data 6   | IO           | A8       |
| MCU_HYPERBUS0_DQ7     | Hyperbus Data 7   | IO           | A7       |

### 5.3.19 GPMC

#### 5.3.19.1 MAIN Domain

**Table 5-85. GPMC0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------|--------------|----------|
| GPMC0_CLK       | GPMC clock      | IO           | U13      |

**Table 5-85. GPMC0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]   | PIN TYPE [3] | BALL [4] |
|-----------------|---|--------------|----------|
| GPMC0_ADVn_ALE  | GPMC Address Valid (active low) or Address Latch Enable                                     | O            | W20      |
| GPMC0_CLKOUT    | GPMC clock generated for external synchronization   | O            | V14      |
| GPMC0_DIR       | GPMC Data Bus Signal Direction Control  | O            | V21      |
| GPMC0_OEn_REn   | GPMC Output Enable (active low) or Read Enable (active low)                                 | O            | T18      |
| GPMC0_WEn       | GPMC Write Enable (active low)  | O            | T17      |
| GPMC0_WPn       | GPMC Flash Write Protect (active low)   | O            | AA18     |
| GPMC0_A0        | GPMC Address 0 Output. Only used to effectively address 8-bit data non-multiplexed memories | OZ           | W17      |
| GPMC0_A1        | GPMC address 1 Output in A/D non-multiplexed mode and Address 17 in A/D multiplexed mode    | OZ           | V18      |
| GPMC0_A2        | GPMC address 2 Output in A/D non-multiplexed mode and Address 18 in A/D multiplexed mode    | OZ           | V20      |
| GPMC0_A3        | GPMC address 3 Output in A/D non-multiplexed mode and Address 19 in A/D multiplexed mode    | OZ           | W21      |
| GPMC0_A4        | GPMC address 4 Output in A/D non-multiplexed mode and Address 20 in A/D multiplexed mode    | OZ           | W16      |
| GPMC0_A5        | GPMC address 5 Output in A/D non-multiplexed mode and Address 21 in A/D multiplexed mode    | OZ           | V19      |
| GPMC0_A6        | GPMC address 6 Output in A/D non-multiplexed mode and Address 22 in A/D multiplexed mode    | OZ           | T13      |
| GPMC0_A7        | GPMC address 7 Output in A/D non-multiplexed mode and Address 23 in A/D multiplexed mode    | OZ           | T15      |
| GPMC0_A8        | GPMC address 8 Output in A/D non-multiplexed mode and Address 24 in A/D multiplexed mode    | OZ           | U19      |
| GPMC0_A9        | GPMC address 9 Output in A/D non-multiplexed mode and Address 25 in A/D multiplexed mode    | OZ           | T14      |
| GPMC0_A10       | GPMC address 10 Output in A/D non-multiplexed mode and Address 26 in A/D multiplexed mode   | OZ           | U18      |
| GPMC0_A11       | GPMC address 11 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode       | OZ           | Y14      |
| GPMC0_A12       | GPMC address 12 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode       | OZ           | Y13      |
| GPMC0_A13       | GPMC address 13 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode       | OZ           | U12      |
| GPMC0_A14       | GPMC address 14 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode       | OZ           | V15      |
| GPMC0_A15       | GPMC address 15 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode       | OZ           | W20      |
| GPMC0_A16       | GPMC address 16 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode       | OZ           | U20      |
| GPMC0_A17       | GPMC address 17 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode       | OZ           | AA15     |
| GPMC0_A18       | GPMC address 18 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode       | OZ           | AA14     |
| GPMC0_A19       | GPMC address 19 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode       | OZ           | AA18     |
| GPMC0_A20       | GPMC address 20 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode       | OZ           | AA16     |
| GPMC0_A21       | GPMC address 21 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode       | OZ           | W17      |

**Table 5-85. GPMC0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]  | PIN TYPE [3] | BALL [4] |
|-----------------|--|--------------|----------|
| GPMC0_A22       | GPMC address 22 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode                            | OZ           | U17      |
| GPMC0_AD0       | GPMC Data 0 Input/Output in A/D non-multiplexed mode and additionally Address 1 Output in A/D multiplexed mode   | IO           | AA17     |
| GPMC0_AD1       | GPMC Data 1 Input/Output in A/D non-multiplexed mode and additionally Address 2 Output in A/D multiplexed mode   | IO           | Y15      |
| GPMC0_AD2       | GPMC Data 2 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode   | IO           | AA20     |
| GPMC0_AD3       | GPMC Data 3 Input/Output in A/D non-multiplexed mode and additionally Address 4 Output in A/D multiplexed mode   | IO           | Y17      |
| GPMC0_AD4       | GPMC Data 4 Input/Output in A/D non-multiplexed mode and additionally Address 5 Output in A/D multiplexed mode   | IO           | Y16      |
| GPMC0_AD5       | GPMC Data 5 Input/Output in A/D non-multiplexed mode and additionally Address 6 Output in A/D multiplexed mode   | IO           | V17      |
| GPMC0_AD6       | GPMC Data 6 Input/Output in A/D non-multiplexed mode and additionally Address 7 Output in A/D multiplexed mode   | IO           | AA19     |
| GPMC0_AD7       | GPMC Data 7 Input/Output in A/D non-multiplexed mode and additionally Address 8 Output in A/D multiplexed mode   | IO           | V16      |
| GPMC0_AD8       | GPMC Data 8 Input/Output in A/D non-multiplexed mode and additionally Address 9 Output in A/D multiplexed mode   | IO           | Y18      |
| GPMC0_AD9       | GPMC Data 9 Input/Output in A/D non-multiplexed mode and additionally Address 10 Output in A/D multiplexed mode  | IO           | Y19      |
| GPMC0_AD10      | GPMC Data 10 Input/Output in A/D non-multiplexed mode and additionally Address 11 Output in A/D multiplexed mode | IO           | Y21      |
| GPMC0_AD11      | GPMC Data 11 Input/Output in A/D non-multiplexed mode and additionally Address 12 Output in A/D multiplexed mode | IO           | W15      |
| GPMC0_AD12      | GPMC Data 12 Input/Output in A/D non-multiplexed mode and additionally Address 13 Output in A/D multiplexed mode | IO           | Y20      |
| GPMC0_AD13      | GPMC Data 13 Input/Output in A/D non-multiplexed mode and additionally Address 14 Output in A/D multiplexed mode | IO           | U14      |
| GPMC0_AD14      | GPMC Data 14 Input/Output in A/D non-multiplexed mode and additionally Address 15 Output in A/D multiplexed mode | IO           | U16      |
| GPMC0_AD15      | GPMC Data 15 Input/Output in A/D non-multiplexed mode and additionally Address 16 Output in A/D multiplexed mode | IO           | U15      |
| GPMC0_BE0n_CLE  | GPMC Lower-Byte Enable (active low) or Command Latch Enable  | O            | U20      |
| GPMC0_BE1n      | GPMC Upper-Byte Enable (active low)  | O            | AA15     |
| GPMC0_CSn0      | GPMC Chip Select 0 (active low)  | O            | T20      |
| GPMC0_CSn1      | GPMC Chip Select 1 (active low)  | O            | U21      |

**Table 5-85. GPMC0 Signal Descriptions (continued)**

| SIGNAL NAME [1]         | DESCRIPTION [2]                  | PIN TYPE [3] | BALL [4] |
|-------------------------|----------------------------------|--------------|----------|
| GPMC0_CS <sub>n</sub> 2 | GPMC Chip Select 2 (active low)  | O            | W17      |
| GPMC0_CS <sub>n</sub> 3 | GPMC Chip Select 3 (active low)  | O            | AA16     |
| GPMC0_WAIT0             | GPMC External Indication of Wait | I            | T16      |
| GPMC0_WAIT1             | GPMC External Indication of Wait | I            | U17      |

**5.3.20 MMC****5.3.20.1 MAIN Domain****Table 5-86. MMC0 Signal Descriptions**

| SIGNAL NAME [1]            | DESCRIPTION [2]                  | PIN TYPE [3] | BALL [4] |
|----------------------------|----------------------------------|--------------|----------|
| MMC0_CALPAD <sup>(1)</sup> | MMC/SD/SDIO Calibration Resistor | A            | P20      |
| MMC0_CLK                   | MMC/SD/SDIO Clock                | O            | P18      |
| MMC0_CMD                   | MMC/SD/SDIO Command              | IO           | R17      |
| MMC0_DS                    | MMC Data Strobe                  | IO           | P19      |
| MMC0_DAT0                  | MMC/SD/SDIO Data                 | IO           | R16      |
| MMC0_DAT1                  | MMC/SD/SDIO Data                 | IO           | P17      |
| MMC0_DAT2                  | MMC/SD/SDIO Data                 | IO           | R18      |
| MMC0_DAT3                  | MMC/SD/SDIO Data                 | IO           | R20      |
| MMC0_DAT4                  | MMC/SD/SDIO Data                 | IO           | R19      |
| MMC0_DAT5                  | MMC/SD/SDIO Data                 | IO           | P16      |
| MMC0_DAT6                  | MMC/SD/SDIO Data                 | IO           | R21      |
| MMC0_DAT7                  | MMC/SD/SDIO Data                 | IO           | T21      |

(1) An external 10 kΩ ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.

**Table 5-87. MMC1 Signal Descriptions**

| SIGNAL NAME [1]          | DESCRIPTION [2]     | PIN TYPE [3] | BALL [4] |
|--------------------------|---------------------|--------------|----------|
| MMC1_CLK <sup>(1)</sup>  | MMC/SD/SDIO Clock   | IO           | P21      |
| MMC1_CMD                 | MMC/SD/SDIO Command | IO           | M20      |
| MMC1_SDCD <sup>(2)</sup> | SD Card Detect      | I            | V1       |
| MMC1_SDWP                | SD Write Protect    | I            | W1       |
| MMC1_DAT0                | MMC/SD/SDIO Data    | IO           | M19      |
| MMC1_DAT1                | MMC/SD/SDIO Data    | IO           | N21      |
| MMC1_DAT2                | MMC/SD/SDIO Data    | IO           | N20      |
| MMC1_DAT3                | MMC/SD/SDIO Data    | IO           | N19      |

(1) For MMC1\_CLK signal to work properly, the RXACTIVE bit of the CTRLMMR\_PADCONFIG63 register should be set to 0x1 because of retiming purposes.

(2) For ROM boot to work properly, the MMC1\_SDCD pin should be pulled low externally with a resistor.

**5.3.21 CPTS****5.3.21.1 MAIN Domain****Table 5-88. CPTS0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                 | PIN TYPE [3] | BALL [4] |
|-----------------|---------------------------------|--------------|----------|
| CPTS0_RFT_CLK   | CPTS Reference Clock            | I            | U3       |
| CPTS0_TS_COMP   | CPTS Time Stamp Counter Compare | O            | U5       |

**Table 5-88. CPTS0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]                 | PIN TYPE [3] | BALL [4] |
|-----------------|---------------------------------|--------------|----------|
| CPTS0_TS_SYNC   | CPTS Time Stamp Counter Bit     | O            | N20      |
| CPTS0_HW1TSPUSH | CPTS Hardware Time Stamp Push 1 | I            | U3       |
| CPTS0_HW2TSPUSH | CPTS Hardware Time Stamp Push 2 | I            | T3       |

### 5.3.21.2 MCU Domain

**Table 5-89. CPTS0 Signal Descriptions**

| SIGNAL NAME [1]     | DESCRIPTION [2]                 | PIN TYPE [3] | BALL [4] |
|---------------------|---------------------------------|--------------|----------|
| MCU_CPTS0_RFT_CLK   | CPTS Reference Clock            | I            | C20, E18 |
| MCU_CPTS0_TS_COMP   | CPTS Time Stamp Counter Compare | O            | C19      |
| MCU_CPTS0_TS_SYNC   | CPTS Time Stamp Counter Bit     | O            | C21      |
| MCU_CPTS0_HW1TSPUSH | CPTS Hardware Time Stamp Push 1 | I            | C14      |
| MCU_CPTS0_HW2TSPUSH | CPTS Hardware Time Stamp Push 2 | I            | C18      |

### 5.3.22 MCASP

#### 5.3.22.1 MAIN Domain

**Table 5-90. MCASP0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                  | PIN TYPE [3] | BALL [4] |
|-----------------|----------------------------------|--------------|----------|
| MCASP0_ACLKR    | MCASP Receive Bit Clock          | IO           | U17      |
| MCASP0_ACLKX    | MCASP Transmit Bit Clock         | IO           | W15      |
| MCASP0_AFSR     | MCASP Receive Frame Sync         | IO           | U15      |
| MCASP0_AFSX     | MCASP Transmit Frame Sync        | IO           | Y16      |
| MCASP0_AXR0     | MCASP Serial Data (Input/Output) | IO           | W16      |
| MCASP0_AXR1     | MCASP Serial Data (Input/Output) | IO           | Y21      |
| MCASP0_AXR2     | MCASP Serial Data (Input/Output) | IO           | Y20      |
| MCASP0_AXR3     | MCASP Serial Data (Input/Output) | IO           | AA19     |
| MCASP0_AXR4     | MCASP Serial Data (Input/Output) | IO           | U19      |
| MCASP0_AXR5     | MCASP Serial Data (Input/Output) | IO           | T15      |
| MCASP0_AXR6     | MCASP Serial Data (Input/Output) | IO           | U20      |
| MCASP0_AXR7     | MCASP Serial Data (Input/Output) | IO           | V21      |
| MCASP0_AXR8     | MCASP Serial Data (Input/Output) | IO           | V17      |
| MCASP0_AXR9     | MCASP Serial Data (Input/Output) | IO           | V18      |
| MCASP0_AXR10    | MCASP Serial Data (Input/Output) | IO           | V20      |
| MCASP0_AXR11    | MCASP Serial Data (Input/Output) | IO           | W21      |
| MCASP0_AXR12    | MCASP Serial Data (Input/Output) | IO           | V16      |
| MCASP0_AXR13    | MCASP Serial Data (Input/Output) | IO           | Y14      |
| MCASP0_AXR14    | MCASP Serial Data (Input/Output) | IO           | Y13      |
| MCASP0_AXR15    | MCASP Serial Data (Input/Output) | IO           | AA15     |

**Table 5-91. MCASP1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]          | PIN TYPE [3] | BALL [4] |
|-----------------|--------------------------|--------------|----------|
| MCASP1_ACLKR    | MCASP Receive Bit Clock  | IO           | U18      |
| MCASP1_ACLKX    | MCASP Transmit Bit Clock | IO           | Y19      |
| MCASP1_AFSR     | MCASP Receive Frame Sync | IO           | T14      |

**Table 5-91. MCASP1 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]                  | PIN TYPE [3] | BALL [4] |
|-----------------|----------------------------------|--------------|----------|
| MCASP1_AFSX     | MCASP Transmit Frame Sync        | IO           | Y18      |
| MCASP1_AXR0     | MCASP Serial Data (Input/Output) | IO           | Y17      |
| MCASP1_AXR1     | MCASP Serial Data (Input/Output) | IO           | AA20     |
| MCASP1_AXR2     | MCASP Serial Data (Input/Output) | IO           | Y15      |
| MCASP1_AXR3     | MCASP Serial Data (Input/Output) | IO           | AA17     |
| MCASP1_AXR4     | MCASP Serial Data (Input/Output) | IO           | U16      |
| MCASP1_AXR5     | MCASP Serial Data (Input/Output) | IO           | U14      |
| MCASP1_AXR6     | MCASP Serial Data (Input/Output) | IO           | T13      |
| MCASP1_AXR7     | MCASP Serial Data (Input/Output) | IO           | V19      |
| MCASP1_AXR8     | MCASP Serial Data (Input/Output) | IO           | AA14     |
| MCASP1_AXR9     | MCASP Serial Data (Input/Output) | IO           | AA18     |
| MCASP1_AXR10    | MCASP Serial Data (Input/Output) | IO           | T14      |
| MCASP1_AXR11    | MCASP Serial Data (Input/Output) | IO           | U18      |

**Table 5-92. MCASP2 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                  | PIN TYPE [3] | BALL [4] |
|-----------------|----------------------------------|--------------|----------|
| MCASP2_ACLKR    | MCASP Receive Bit Clock          | IO           | W19      |
| MCASP2_ACLKX    | MCASP Transmit Bit Clock         | IO           | U12      |
| MCASP2_AFSR     | MCASP Receive Frame Sync         | IO           | W14      |
| MCASP2_AFSX     | MCASP Transmit Frame Sync        | IO           | V13      |
| MCASP2_AXR0     | MCASP Serial Data (Input/Output) | IO           | AA16     |
| MCASP2_AXR1     | MCASP Serial Data (Input/Output) | IO           | W17      |
| MCASP2_AXR2     | MCASP Serial Data (Input/Output) | IO           | W20      |
| MCASP2_AXR3     | MCASP Serial Data (Input/Output) | IO           | V14      |
| MCASP2_AXR4     | MCASP Serial Data (Input/Output) | IO           | W14      |
| MCASP2_AXR5     | MCASP Serial Data (Input/Output) | IO           | W19      |

**5.3.23 DMTIMER****5.3.23.1 MAIN Domain****Table 5-93. DMTIMER Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]  | PIN TYPE [3] | BALL [4] |
|-----------------|--|--------------|----------|
| TIMER_IO0       | Timer Inputs and Outputs (not tied to single timer instance) | IO           | N19, V1  |
| TIMER_IO1       | Timer Inputs and Outputs (not tied to single timer instance) | IO           | N20, W1  |
| TIMER_IO2       | Timer Inputs and Outputs (not tied to single timer instance) | IO           | N21      |
| TIMER_IO3       | Timer Inputs and Outputs (not tied to single timer instance) | IO           | M19      |
| TIMER_IO4       | Timer Inputs and Outputs (not tied to single timer instance) | IO           | P21      |
| TIMER_IO5       | Timer Inputs and Outputs (not tied to single timer instance) | IO           | M20      |
| TIMER_IO6       | Timer Inputs and Outputs (not tied to single timer instance) | IO           | T18      |

**Table 5-93. DMTIMER Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]  | PIN TYPE [3] | BALL [4] |
|-----------------|--|--------------|----------|
| TIMER_IO7       | Timer Inputs and Outputs (not tied to single timer instance) | IO           | T20      |

### 5.3.23.2 MCU Domain

**Table 5-94. DMTIMER Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]  | PIN TYPE [3] | BALL [4] |
|-----------------|--|--------------|----------|
| MCU_TIMER_IO0   | Timer Inputs and Outputs (not tied to single timer instance) | IO           | B17      |
| MCU_TIMER_IO1   | Timer Inputs and Outputs (not tied to single timer instance) | IO           | A19, C16 |
| MCU_TIMER_IO2   | Timer Inputs and Outputs (not tied to single timer instance) | IO           | C12      |
| MCU_TIMER_IO3   | Timer Inputs and Outputs (not tied to single timer instance) | IO           | B12      |
| MCU_TIMER_IO4   | Timer Inputs and Outputs (not tied to single timer instance) | IO           | C10      |
| MCU_TIMER_IO5   | Timer Inputs and Outputs (not tied to single timer instance) | IO           | A10      |
| MCU_TIMER_IO6   | Timer Inputs and Outputs (not tied to single timer instance) | IO           | C21, D21 |
| MCU_TIMER_IO7   | Timer Inputs and Outputs (not tied to single timer instance) | IO           | C19, E19 |
| MCU_TIMER_IO8   | Timer Inputs and Outputs (not tied to single timer instance) | IO           | E20      |
| MCU_TIMER_IO9   | Timer Inputs and Outputs (not tied to single timer instance) | IO           | E21      |

### 5.3.24 Emulation and Debug

#### 5.3.24.1 MAIN Domain

**Table 5-95. JTAG Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]             | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------------------|--------------|----------|
| EMU0            | Emulation Control 0         | IO           | A13      |
| EMU1            | Emulation Control 1         | IO           | D12      |
| TCK             | JTAG Test Clock Input       | I            | B15      |
| TDI             | JTAG Test Data Input        | I            | F19      |
| TDO             | JTAG Test Data Output       | OZ           | F21      |
| TMS             | JTAG Test Mode Select Input | I            | U4       |
| TRSTn           | JTAG Reset                  | I            | B20      |

**Table 5-96. Trace Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------|--------------|----------|
| TRC_CLK         | Trace Clock     | O            | W15      |
| TRC_CTL         | Trace Control   | O            | Y16      |
| TRC_DATA0       | Trace Data 0    | O            | W16      |
| TRC_DATA1       | Trace Data 1    | O            | Y21      |
| TRC_DATA2       | Trace Data 2    | O            | Y19      |

**Table 5-96. Trace Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2] | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------|--------------|----------|
| TRC_DATA3       | Trace Data 3    | O            | Y18      |
| TRC_DATA4       | Trace Data 4    | O            | Y20      |
| TRC_DATA5       | Trace Data 5    | O            | AA19     |
| TRC_DATA6       | Trace Data 6    | O            | Y17      |
| TRC_DATA7       | Trace Data 7    | O            | AA20     |
| TRC_DATA8       | Trace Data 8    | O            | Y15      |
| TRC_DATA9       | Trace Data 9    | O            | AA17     |
| TRC_DATA10      | Trace Data 10   | O            | U17      |
| TRC_DATA11      | Trace Data 11   | O            | U15      |
| TRC_DATA12      | Trace Data 12   | O            | U18      |
| TRC_DATA13      | Trace Data 13   | O            | T14      |
| TRC_DATA14      | Trace Data 14   | O            | U19      |
| TRC_DATA15      | Trace Data 15   | O            | T15      |
| TRC_DATA16      | Trace Data 16   | O            | U20      |
| TRC_DATA17      | Trace Data 17   | O            | V21      |
| TRC_DATA18      | Trace Data 18   | O            | U16      |
| TRC_DATA19      | Trace Data 19   | O            | U14      |
| TRC_DATA20      | Trace Data 20   | O            | T13      |
| TRC_DATA21      | Trace Data 21   | O            | V19      |
| TRC_DATA22      | Trace Data 22   | O            | W14      |
| TRC_DATA23      | Trace Data 23   | O            | W19      |

**5.3.25 System and Miscellaneous**

**5.3.25.1 Boot Mode Configuration**

**5.3.25.1.1 MAIN Domain**

**Table 5-97. Sysboot Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------|--------------|----------|
| BOOTMODE00      | Bootmode pin 0  | I            | D8       |
| BOOTMODE01      | Bootmode pin 1  | I            | C7       |
| BOOTMODE02      | Bootmode pin 2  | I            | A6       |
| BOOTMODE03      | Bootmode pin 3  | I            | B8       |
| BOOTMODE04      | Bootmode pin 4  | I            | D21      |
| BOOTMODE05      | Bootmode pin 5  | I            | E19      |
| BOOTMODE06      | Bootmode pin 6  | I            | D18      |
| BOOTMODE07      | Bootmode pin 7  | I            | C17      |

**5.3.25.1.2 MCU Domain**

**Table 5-98. Sysboot Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2] | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------|--------------|----------|
| MCU_BOOTMODE00  | Bootmode pin 00 | I            | C13      |
| MCU_BOOTMODE01  | Bootmode pin 01 | I            | A20      |
| MCU_BOOTMODE02  | Bootmode pin 02 | I            | B17      |
| MCU_BOOTMODE03  | Bootmode pin 03 | I            | B18      |

**Table 5-98. Sysboot Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2] | PIN TYPE [3] | BALL [4] |
|-----------------|-----------------|--------------|----------|
| MCU_BOOTMODE04  | Bootmode pin 04 | I            | B19      |
| MCU_BOOTMODE05  | Bootmode pin 05 | I            | D14      |
| MCU_BOOTMODE06  | Bootmode pin 06 | I            | E20      |
| MCU_BOOTMODE07  | Bootmode pin 07 | I            | E21      |
| MCU_BOOTMODE08  | Bootmode pin 08 | I            | D19      |
| MCU_BOOTMODE09  | Bootmode pin 09 | I            | D20      |

### 5.3.25.2 Clock

#### 5.3.25.2.1 MAIN Domain

**Table 5-99. Clock1 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                  | PIN TYPE [3] | BALL [4] |
|-----------------|----------------------------------|--------------|----------|
| OSC1_XI         | High frequency oscillator input  | I            | K19      |
| OSC1_XO         | High frequency oscillator output | O            | J19      |

#### 5.3.25.2.2 WKUP Domain

**Table 5-100. Clock0 Signal Descriptions**

| SIGNAL NAME [1] | DESCRIPTION [2]                             | PIN TYPE [3] | BALL [4] |
|-----------------|---|--------------|----------|
| WKUP_LF_CLKIN   | Low frequency (32.768 KHz) oscillator input | I            | C17      |
| WKUP_OSC0_XI    | High frequency oscillator input             | I            | K21      |
| WKUP_OSC0_XO    | High frequency oscillator output            | O            | L21      |

### 5.3.25.3 System

#### 5.3.25.3.1 MAIN Domain

**Table 5-101. System0 Signal Descriptions**

| SIGNAL NAME [1]   | DESCRIPTION [2]  | PIN TYPE [3] | BALL [4] |
|-------------------|--|--------------|----------|
| AUDIO_EXT_REFCLK0 | External clock routed to ATL or McASP as one of the selectable input clock sources, or as a output clock output for ATL or McASP   | IO           | V18      |
| AUDIO_EXT_REFCLK1 | External clock routed to ATL or McASP as one of the selectable input clock sources, or as a output clock output for ATL or McASP   | IO           | U21      |
| EXTINTn           | External Interrupt   | I            | U6       |
| EXT_REFCLK1       | External clock input to Main Domain, routed to Timer clock muxes as one of the selectable input clock sources for Timer/WDT modules, or as reference clock to MAIN_PLL2 (PER1 PLL) | I            | T3       |
| GPMC0_FCLK_MUX    | GPMC functional clock output selected through a mux logic  | O            | V14      |
| OBSCCLK0          | Observation clock output for test and debug purposes   | O            | W1       |
| OBSCCLK1          | Observation clock output for test and debug purposes   | O            | V16      |
| OBSCCLK2          | Observation clock output for test and debug purposes   | O            | V14      |
| RESETSTATz        | Main Domain warm reset status output   | O            | U2       |
| SOC_SAFETY_ERRORn | Error signal output from Main Domain ESM   | IO           | V2       |
| SYNC0_OUT         | CPTS Time Stamp Generator Bit 0  | O            | U3       |
| SYNC1_OUT         | CPTS Time Stamp Generator Bit 1  | O            | T3       |

**Table 5-101. System0 Signal Descriptions (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]   | PIN TYPE [3] | BALL [4] |
|-----------------|---|--------------|----------|
| SYNC2_OUT       | CPTS Time Stamp Generator Bit 2   | O            | W16      |
| SYNC3_OUT       | CPTS Time Stamp Generator Bit 3   | O            | V21      |
| SYSCLKOUT0      | SYSCLK0 output from Main PLL controller (divided by 6) for test and debug purposes only | O            | V1       |

**5.3.25.3.2 WKUP Domain****Table 5-102. System0 Signal Descriptions**

| SIGNAL NAME [1]   | DESCRIPTION [2]   | PIN TYPE [3] | BALL [4] |
|-------------------|---|--------------|----------|
| MCU_CLKOUT0       | Reference clock output for Ethernet PHYs (50MHz or 25MHz)       | OZ           | C16      |
| MCU_EXT_REFCLK0   | External system clock input                                     | I            | C20, E18 |
| MCU_OBSCLK0       | Observation clock output for test and debug purposes            | O            | C16      |
| MCU_PORz          | MCU Domain cold reset   | I            | G19      |
| MCU_RESETSTATz    | MCU Domain warm reset status output                             | O            | B13      |
| MCU_RESETz        | MCU Domain warm reset   | I            | A18      |
| MCU_SAFETY_ERRORn | Error signal output from MCU Domain ESM                         | IO           | G18      |
| MCU_SYSCLKOUT0    | MCU Domain system clock output for test and debug purposes only | O            | C20      |
| PMIC_POWER_EN1    | Power enable output for MAIN Domain supplies                    | O            | C15      |
| PMIC_WAKE0        | PMIC WakeUp (active low)  | O            | T19      |
| PMIC_WAKE1        | PMIC WakeUp (active low)  | O            | E18      |
| PORz              | Main Domain cold reset  | I            | H20      |
| RESET_REQz        | Main Domain external warm reset request input                   | I            | A15      |

**5.3.25.3.3 VMON****Table 5-103. VMON Signal Description**

| SIGNAL NAME [1]  | DESCRIPTION [2]   | PIN TYPE [3] | BALL [4] |
|------------------|---|--------------|----------|
| VMON1_ER_VSYS    | Voltage Monitor, fixed 0.45V (+/-3%) threshold. Use with external precision voltage divider to monitor a higher voltage rail such as the PMIC input supply. | PWR          | G15      |
| VMON2_IR_VCPU    | Recommended to be externally connected directly to VDD_CPU  | PWR          | D16      |
| VMON3_IR_VEXT1P8 | General purpose voltage monitor for external supplies, 1.8V threshold. With internal resistor Divider.  | PWR          | E17      |
| VMON4_IR_VEXT1P8 | General purpose voltage monitor for external supplies, 1.8V threshold. With internal resistor Divider.  | PWR          | F17      |
| VMON5_IR_VEXT3P3 | General purpose voltage monitor for external supplies, 3.3V threshold. With internal resistor Divider.  | PWR          | L14      |

**5.3.25.4 EFUSE****Table 5-104. EFUSE Signal Description**

| SIGNAL NAME [1]         | DESCRIPTION [2]                            | PIN TYPE [3] | BALL [4] |
|-------------------------|--|--------------|----------|
| VPP_CORE <sup>(1)</sup> | Programming voltage for MAIN Domain efuses | PWR          | N17      |

**Table 5-104. EFUSE Signal Description (continued)**

| SIGNAL NAME [1]        | DESCRIPTION [2]                           | PIN TYPE [3] | BALL [4] |
|------------------------|---|--------------|----------|
| VPP_MCU <sup>(1)</sup> | Programming voltage for MCU Domain efuses | PWR          | E11      |

(1) This signal is valid only for High-Security devices. For more details, see [Section 6.7, VPP Specification for One-Time Programmable \(OTP\) eFUSES](#). For General-Purpose devices do not connect any signal, test point, or board trace to this signal.

### 5.3.26 Power Supply

#### Note

All power balls must be supplied with the voltages specified in [Section 6.3, Recommended Operating Conditions](#), unless otherwise specified in [Section 5.3, Signal Descriptions](#).

**Table 5-105. Power Supply Signal Description**

| SIGNAL NAME [1]              | DESCRIPTION [2]   | PIN TYPE [3] | BALL [4]           |
|------------------------------|---|--------------|--------------------|
| CAP_VDDS0 <sup>(1)</sup>     | External capacitor connection for MAIN domain GENERAL IO group 0          | PWR          | M7                 |
| CAP_VDDS0_MCU <sup>(1)</sup> | External capacitor connection for MCUSS IO group 0                        | PWR          | G14                |
| CAP_VDDS1_MCU <sup>(1)</sup> | External capacitor connection for MCUSS IO group 1                        | PWR          | F9                 |
| CAP_VDDS2 <sup>(1)</sup>     | External capacitor connection for MAIN domain CANUART IO group 2          | PWR          | T12                |
| CAP_VDDS2_MCU <sup>(1)</sup> | External capacitor connection for MCUSS IO group 2                        | PWR          | F10                |
| CAP_VDDS5 <sup>(1)</sup>     | External capacitor connection for MAIN domain MMC1 IO group 5             | PWR          | L15                |
| VDDAR_CORE                   | MAIN domain RAM supply  | PWR          | K14, P14           |
| VDDAR_CPU                    | CPU RAM supply  | PWR          | J11, M10           |
| VDDAR_MCU                    | MCUSS RAM supply  | PWR          | H12, J14           |
| VDDA_0P8_PLL_DDR             | DDR PLL analog supply   | PWR          | K7                 |
| VDDA_0P8_USB                 | USB0 0.8 V analog supply  | PWR          | P7                 |
| VDDA_0P8_DLL_MMC0            | MMC0 DLL analog supply  | PWR          | M18                |
| VDDA_0P8_SERDES0             | SERDES0 analog supply low   | PWR          | R8, T7, U8         |
| VDDA_0P8_SERDES0_C           | SERDES0 clock supply  | PWR          | R9                 |
| VDDA_1P8_USB                 | USB0 1.8 V analog supply  | PWR          | R6                 |
| VDDA_1P8_SERDES0             | SERDES0 analog supply high  | PWR          | P8                 |
| VDDA_3P3_USB                 | USB0 3.3 V analog supply  | PWR          | R7                 |
| VDDA_ADC_MCU                 | ADC analog supply and high voltage reference (VREFP)                      | PWR          | J16                |
| VDDA_MCU_PLLGRP0             | Analog supply for MCU PLL group 0   | PWR          | F15                |
| VDDA_MCU_TEMP                | Analog supply for temperature sensor 0 in MCU domain                      | PWR          | F16                |
| VDDA_PLLGRP0                 | Analog supply for MAIN PLL group 0  | PWR          | N14                |
| VDDA_PLLGRP4                 | Analog supply for MAIN PLL group 4  | PWR          | N9                 |
| VDDA_PLLGRP6                 | Analog supply for MAIN PLL Group 6  | PWR          | J9                 |
| VDDA_PLLGRP8                 | Analog supply for MAIN PLL group 8  | PWR          | L7                 |
| VDDA_POR_WKUP                | WKUP domain analog supply   | PWR          | J15                |
| VDDA_TEMP0                   | Analog supply for MAIN domain TEMP sensor 0                               | PWR          | J8                 |
| VDDA_TEMP1                   | Analog supply for MAIN domain TEMP sensor 1                               | PWR          | P15                |
| VDDA_WKUP                    | Oscillator supply for WKUP domain   | PWR          | H16                |
| VDDSHV0                      | IO supply for MAIN domain GENERAL IO group                                | PWR          | N6, P6             |
| VDDSHV0_MCU                  | IO supply MCUSS general IO group, and MCU and MAIN domain warm reset pins | PWR          | E13, E14, F13, F14 |

**Table 5-105. Power Supply Signal Description (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]  | PIN TYPE [3] | BALL [4]  |
|-----------------|--|--------------|---|
| VDDSHV1_MCU     | IO supply for MCUSS IO group 1   | PWR          | E7, E8, F8  |
| VDDSHV2         | IO supply for MAIN domain CANUART IO group 2                               | PWR          | T10, U11, U9  |
| VDDSHV2_MCU     | IO supply for MCUSS IO group 2   | PWR          | F11, F12, G11   |
| VDDSHV5         | IO supply for MAIN domain MMC1 IO group 5                                  | PWR          | K16, L16  |
| VDDS_DDR        | DDR interface power supply   | PWR          | A1, G7, H6, J7, K6, M5, U1  |
| VDDS_DDR_BIAS   | Bias supply for LPDDR4   | PWR          | F7, L6  |
| VDDS_DDR_C      | IO power for DDR Memory Clock Bit (MCB) macro                              | PWR          | J6  |
| VDDS_MMC0       | MMC0 IO supply   | PWR          | M16, N16  |
| VDDA_OSC1       | HFOSC1 supply  | PWR          | G17   |
| VDD_CORE        | MAIN domain core supply  | PWR          | H8, K12, L13, M12, M14, N13, N15, N7, P10, P12, R11, R13, R15   |
| VDD_CPU         | CPU core supply  | PWR          | J10, L11, M9, N11, N8   |
| VDD_MCU         | MCUSS core supply  | PWR          | G9, H10, H14, J13, K15  |
| VDD_MCU_WAKE1   | Core supply for MCU WAKE function  | PWR          | G13   |
| VDD_WAKE0       | Core supply for MAIN domain WAKE function which includes all "CANUART" IO. | PWR          | P11   |
| VSS             | Ground   | GND          | B5, AA1, AA10, AA13, AA4, AA7, C11, D15, D17, D3, E10, E12, E15, E16, E6, E9, F1, G10, G12, G16, G6, G8, H11, H13, H15, H19, H4, H7, H9, J1, J12, J21, K11, K13, K3, L12, L19, L5, M11, M13, M15, M21, M6, M8, N10, N12, N3, P13, P5, P9, R10, R12, R14, T11, T2, T6, T8, T9, U10, U7, V11, V12, V9, W10, W13, W18, W4, W7, Y12, Y3, Y6, Y9 |

(1) This pin must always be connected via a 1- $\mu$ F  $\pm$  10% capacitor to VSS.

## 5.4 Pin Multiplexing

### Note

Many device pins support multiple signal functions. Some signal functions are selected via a single layer of multiplexers associated with pins. Other signal functions are selected via two or more layers of multiplexers, where one layer is associated with the pins and other layers are associated with peripheral logic functions.

[Table 5-106, Pin Multiplexing](#) only describes signal multiplexing at the pins. For more information, related to signal multiplexing at the pins, see *Pad Configuration Registers* section in *Device Configuration* chapter in the device TRM. Refer to the respective peripheral chapter in the device TRM for information associated with peripheral signal multiplexing.

### Note

When a pad is set into a pin multiplexing mode which is not defined, that pad's behavior is undefined. This should be avoided.

### Note

[Table 5-106, Pin Multiplexing](#) does not include SerDes signal functions. For more information, refer to the Serializer/Deserializer (SerDes) chapter in the device TRM.

### Note

The PRU contains a second layer of multiplexing to enable additional functionality on the PRU GPO and GPI signals. This internal wrapper multiplexing is described in the PRU chapter in the device TRM.

For more information on the I/O cell configurations, see *Pad Configuration Registers* section in *Device Configuration* chapter in the device TRM.

**Table 5-106. Pin Multiplexing**

| ADDRESS OFFSET | REGISTER NAME    | BALL NUMBER | MUXMODE[15:0] SETTINGS |                    |   |   |             |            |           |         |               |   |                |           |             |             |    |            |            |
|----------------|------------------|-------------|------------------------|--------------------|---|---|-------------|------------|-----------|---------|---------------|---|----------------|-----------|-------------|-------------|----|------------|------------|
|                |                  |             | 0                      | 1                  | 2 | 3 | 4           | 5          | 6         | 7       | 8             | 9 | 10             | 11        | 12          | 13          | 14 | Bootstrap  |            |
| 0x1C000        | WKUP_PADCONFIG_0 | B6          | MCU_OSPI0_CLK          | MCU_HYPERBUS0_CLK  |   |   |             |            |           |         | WKUP_GPIO0_16 |   |                |           |             |             |    |            |            |
| 0x1C000        | PADCONFIG_0      | U6          | EXTINTn                |                    |   |   |             |            |           |         | GPIO0_0       |   |                |           |             |             |    |            |            |
| 0x1C004        | WKUP_PADCONFIG_1 | C8          | MCU_OSPI0_LBCLKO       | MCU_HYPERBUS0_CLKn |   |   |             |            |           |         | WKUP_GPIO0_17 |   |                |           |             |             |    |            |            |
| 0x1C004        | PADCONFIG_1      | AA17        | RMII1_RXD0             |                    |   |   | RGMI11_RXD0 | RMII1_RXD0 | MCAN14_TX | GPIO0_2 |               |   | TRC_DATA9      | UART5_TXD | MCASP1_AXR3 |             |    | GPMC0_A D0 |            |
| 0x1C008        | PADCONFIG_2      | Y15         | RMII1_RXD1             |                    |   |   | RGMI11_RXD1 | RMII1_RXD1 | MCAN14_RX | GPIO0_3 |               |   | EHRPWM_TZn_IN2 | TRC_DATA8 | UART5_RXD   | MCASP1_AXR2 |    |            | GPMC0_A D1 |

**Table 5-106. Pin Multiplexing (continued)**

| ADDR<br>ESS<br>OFFSE<br>T | REGISTER<br>NAME  | BALL<br>NUMB<br>ER | MUXMODE[15:0] SETTINGS |                     |   |   |   |              |               |          |                |          |                |           |             |              | Bootstrap |                    |            |
|---------------------------|-------------------|--------------------|------------------------|---------------------|---|---|---|--------------|---------------|----------|----------------|----------|----------------|-----------|-------------|--------------|-----------|--------------------|------------|
|                           |                   |                    | 0                      | 1                   | 2 | 3 | 4 | 5            | 6             | 7        | 8              | 9        | 10             | 11        | 12          | 13           |           | 14                 |            |
| 0x1C008                   | WKUP_PADCONFIG_2  | B7                 | MCU_OSPI0_DQS          | MCU_HYP ERBUS0_RWDS |   |   |   |              |               |          | WKUP_GP IO0_18 |          |                |           |             |              |           |                    |            |
| 0x1C00C                   | PADCONFIG_3       | AA20               | RMII1_CR S_DV          |                     |   |   |   | RGMI1_RD2    | RMII1_CR S_DV |          | GPIO0_4        |          | EHRPWM2_B      | TRC_DATA7 | UART4_TX D  | MCASP1_AXR1  |           | GPMC0_AD2          |            |
| 0x1C00C                   | WKUP_PADCONFIG_3  | D8                 | MCU_OSPI0_D0           | MCU_HYP ERBUS0_DQ0  |   |   |   |              |               |          | WKUP_GP IO0_19 |          |                |           |             |              |           |                    | BOOTMODE0  |
| 0x1C010                   | PADCONFIG_4       | Y17                | RMII1_RX_ER            |                     |   |   |   | RGMI1_RD3    | RMII1_RX_ER   |          | GPIO0_5        |          | EHRPWM2_A      | TRC_DATA6 | UART6_TX D  | MCASP1_AXR0  |           | GPMC0_AD3          |            |
| 0x1C010                   | WKUP_PADCONFIG_4  | C7                 | MCU_OSPI0_D1           | MCU_HYP ERBUS0_DQ1  |   |   |   |              |               |          | WKUP_GP IO0_20 |          |                |           |             |              |           |                    | BOOTMODE01 |
| 0x1C014                   | WKUP_PADCONFIG_5  | C5                 | MCU_OSPI0_D2           | MCU_HYP ERBUS0_DQ2  |   |   |   |              |               |          | WKUP_GP IO0_21 |          |                |           |             |              |           |                    |            |
| 0x1C014                   | PADCONFIG_5       | Y16                | RMII1_TXD0             |                     |   |   |   | RGMI1_RX_CTL | RMII1_TXD0    |          | GPIO0_6        |          | EHRPWM0_SYNCO  | TRC_CTL   | UART6_RX D  | MCASP0_AFSX  |           | GPMC0_AD4          |            |
| 0x1C018                   | WKUP_PADCONFIG_6  | A5                 | MCU_OSPI0_D3           | MCU_HYP ERBUS0_DQ3  |   |   |   |              |               |          | WKUP_GP IO0_22 |          |                |           |             |              |           |                    |            |
| 0x1C018                   | PADCONFIG_6       | V17                | RMII1_TX_EN            |                     |   |   |   | RGMI1_RXC    | RMII1_TX_EN   |          | GPIO0_7        |          | EQEP2_A        |           | UART9_TX D  | MCASP0_AXR8  | I2C1_SCL  | GPMC0_AD5          |            |
| 0x1C01C                   | PADCONFIG_7       | AA19               | RMII1_TXD1             |                     |   |   |   | RGMI1_RXC    | RMII1_TXD1    |          | GPIO0_8        |          | EHRPWM_TZn_IN1 | TRC_DATA5 | UART9_RX D  | MCASP0_AXR3  | I2C1_SDA  | GPMC0_AD6          |            |
| 0x1C01C                   | WKUP_PADCONFIG_7  | A6                 | MCU_OSPI0_D4           | MCU_HYP ERBUS0_DQ4  |   |   |   |              |               |          | WKUP_GP IO0_23 |          |                |           |             |              |           |                    | BOOTMODE02 |
| 0x1C020                   | WKUP_PADCONFIG_8  | B8                 | MCU_OSPI0_D5           | MCU_HYP ERBUS0_DQ5  |   |   |   |              |               |          | WKUP_GP IO0_24 |          |                |           |             |              |           |                    | BOOTMODE03 |
| 0x1C020                   | PADCONFIG_8       | V18                | MCAN0_TX               |                     |   |   |   | RGMI14_RD0   |               | MCAN0_TX | GPIO0_9        |          | EQEP2_B        |           | GPMC0_A1    | MCASP0_AXR9  |           | AUDIO_EX T_REFCLK0 |            |
| 0x1C024                   | PADCONFIG_9       | V20                | MCAN0_RX               |                     |   |   |   | RGMI14_RD1   |               | MCAN0_RX | GPIO0_10       |          | EQEP2_S        |           | GPMC0_A2    | MCASP0_AXR10 |           |                    |            |
| 0x1C024                   | WKUP_PADCONFIG_9  | A8                 | MCU_OSPI0_D6           | MCU_HYP ERBUS0_DQ6  |   |   |   |              |               |          | WKUP_GP IO0_25 |          |                |           |             |              |           |                    |            |
| 0x1C028                   | PADCONFIG_10      | W21                | MCAN1_TX               |                     |   |   |   | RGMI12_TXC   | RMII2_TX_EN   | MCAN1_TX | GPIO0_11       | SPI6_CS0 | EHRPWM_SOC     |           | GPMC0_A3    | MCASP0_AXR11 |           |                    |            |
| 0x1C028                   | WKUP_PADCONFIG_10 | A7                 | MCU_OSPI0_D7           | MCU_HYP ERBUS0_DQ7  |   |   |   |              |               |          | WKUP_GP IO0_26 |          |                |           |             |              |           |                    |            |
| 0x1C02C                   | PADCONFIG_11      | V16                | MCAN1_RX               |                     |   |   |   | RGMI14_RD2   | RMII2_TXD1    | MCAN1_RX | GPIO0_12       | SPI6_CS1 | EQEP2_I        | GPMC0_AD7 | UART6_CT Sn | MCASP0_AXR12 |           | OBSCLK1            |            |
| 0x1C02C                   | WKUP_PADCONFIG_11 | D6                 | MCU_OSPI0_CSn0         | MCU_HYP ERBUS0_CSn0 |   |   |   |              |               |          | WKUP_GP IO0_27 |          |                |           |             |              |           |                    |            |

**Table 5-106. Pin Multiplexing (continued)**

| ADDRESS OFFSET | REGISTER NAME     | BALL NUMBER | MUXMODE[15:0] SETTINGS |                       |                       |                    |                     |                  |                    |                  |               |                |            |            |              |            | Bootstrap    |            |  |
|----------------|-------------------|-------------|------------------------|-----------------------|-----------------------|--------------------|---------------------|------------------|--------------------|------------------|---------------|----------------|------------|------------|--------------|------------|--------------|------------|--|
|                |                   |             | 0                      | 1                     | 2                     | 3                  | 4                   | 5                | 6                  | 7                | 8             | 9              | 10         | 11         | 12           | 13         |              | 14         |  |
| 0x1C030        | WKUP_PADCONFIG_12 | D7          | MCU_OSPI0_CSn1         | MCU_HYP ERBUS0_RESETh |                       |                    |                     |                  |                    |                  | WKUP_GPIO0_28 |                |            |            |              |            |              |            |  |
| 0x1C030        | PADCONFIG_12      | Y18         | MCAN2_TX               |                       |                       |                    | RGMI1_TD0           | RMII4_RXD0       | MCAN2_TX           | GPIO0_13         | SPI5_CS3      | EHRPWM1_A      | TRC_DATA3  | UART3_RXD  | MCASP1_AFSX  | UART9_CTSn | GPMC0_AD8    |            |  |
| 0x1C034        | PADCONFIG_13      | Y19         | MCAN2_RX               |                       |                       |                    | RGMI1_TD1           | RMII4_RXD1       | MCAN2_RX           | GPIO0_14         | SPI5_CS2      | EHRPWM0_B      | TRC_DATA2  | UART3_TXD  | MCASP1_ACLKX | UART9_RTSn | GPMC0_AD9    |            |  |
| 0x1C038        | PADCONFIG_14      | Y21         | MCAN3_TX               |                       |                       |                    | RGMI1_TD2           | RMII4_CRS_DV     | MCAN3_TX           | GPIO0_15         | SPI5_D0       | EHRPWM0_A      | TRC_DATA1  |            | MCASP0_AXR1  |            | GPMC0_AD10   |            |  |
| 0x1C038        | WKUP_PADCONFIG_14 | C6          | MCU_OSPI0_CSn2         | MCU_OSPI0_CSn2        | MCU_HYP ERBUS0_RESETh | MCU_HYP ERBUS0_WPn | MCU_HYP ERBUS0_CSn1 |                  | MCU_OSPI0_RESETh   | MCU_OSPI0_RESETh | WKUP_GPIO0_30 |                |            |            |              |            |              |            |  |
| 0x1C03C        | WKUP_PADCONFIG_15 | D5          | MCU_OSPI0_CSn3         | MCU_OSPI0_CSn3        | MCU_HYP ERBUS0_INTn   | MCU_HYP ERBUS0_WPn |                     | MCU_OSPI0_RESETh | MCU_OSPI0_ECC_FAIL | WKUP_GPIO0_31    |               |                |            |            |              |            |              |            |  |
| 0x1C03C        | PADCONFIG_15      | W16         | MCAN3_RX               |                       |                       |                    | RGMI1_TD3           | RMII4_RXER       | MCAN3_RX           | GPIO0_16         | SPI5_CS0      | EHRPWM_TZn_IN0 | TRC_DATA0  | GPMC0_A4   | MCASP0_AXR0  |            |              | SYNC2_OUT  |  |
| 0x1C040        | PADCONFIG_16      | W15         | MCAN4_TX               |                       |                       |                    | RGMI1_TX_CTL        | RMII4_TXD0       | MCAN4_TX           | GPIO0_17         | SPI5_CLK      | EHRPWM0_SYNCI  | TRC_CLK    | I2C2_SCL   | MCASP0_ACLKX |            |              | GPMC0_AD11 |  |
| 0x1C044        | PADCONFIG_17      | Y20         | MCAN4_RX               |                       |                       |                    | RGMI1_TXC           | RMII4_TXEN       | MCAN4_RX           | GPIO0_18         | SPI5_D1       | EHRPWM1_B      | TRC_DATA4  | I2C2_SDA   | MCASP0_AXR2  |            |              | GPMC0_AD12 |  |
| 0x1C048        | PADCONFIG_18      | V21         | MCAN5_TX               |                       |                       |                    | RGMI3_RXC           | RMII4_TXD1       | MCAN5_TX           | GPIO0_19         | SPI5_CS1      | EHRPWM4_B      | TRC_DATA17 | UART6_RTSn | MCASP0_AXR7  | GPMC0_DIR  | SYNC3_OUT    |            |  |
| 0x1C04C        | PADCONFIG_19      | V19         | MCAN5_RX               |                       |                       |                    | RGMI3_RXD0          | RMII3_RXD0       | MCAN5_RX           | GPIO0_20         | I2C3_SCL      | EHRPWM_TZn_IN5 | TRC_DATA21 | GPMC0_A5   | MCASP1_AXR7  |            |              |            |  |
| 0x1C050        | PADCONFIG_20      | T13         | MCAN6_TX               |                       |                       |                    | RGMI3_RXD1          | RMII3_RXD1       | MCAN6_TX           | GPIO0_21         | I2C3_SDA      | EHRPWM5_B      | TRC_DATA20 | GPMC0_A6   | MCASP1_AXR6  |            |              |            |  |
| 0x1C054        | PADCONFIG_21      | U14         | MCAN6_RX               |                       |                       |                    | RGMI3_RXD2          | RMII3_CRS_DV     | MCAN6_RX           | GPIO0_22         |               | EHRPWM5_A      | TRC_DATA19 |            | MCASP1_AXR5  |            |              | GPMC0_AD13 |  |
| 0x1C058        | PADCONFIG_22      | U16         | MCAN7_TX               |                       |                       |                    | RGMI3_RXD3          | RMII3_RXER       | MCAN7_TX           | GPIO0_23         | SPI3_CS0      | EHRPWM_TZn_IN4 | TRC_DATA18 |            | MCASP1_AXR4  |            |              | GPMC0_AD14 |  |
| 0x1C05C        | PADCONFIG_23      | U15         | MCAN7_RX               |                       |                       |                    | RGMI3_RX_CTL        | RMII3_TXD0       | MCAN7_RX           | GPIO0_24         | SPI3_CS1      | EHRPWM3_A      | TRC_DATA11 |            | MCASP0_AFSR  |            |              | GPMC0_AD15 |  |
| 0x1C060        | PADCONFIG_24      | T15         | MCAN8_TX               |                       |                       | GPMC0_A7           | RGMI3_RXD0          | RMII3_TXEN       | MCAN8_TX           | GPIO0_25         | SPI3_CS2      | EHRPWM_TZn_IN3 | TRC_DATA15 | UART3_CTSn | MCASP0_AXR5  |            |              | UART0_CDn  |  |
| 0x1C064        | PADCONFIG_25      | U19         | MCAN8_RX               |                       |                       |                    | RGMI3_RXD1          | RMII3_TXD1       | MCAN8_RX           | GPIO0_26         | SPI3_CS3      | EHRPWM3_SYNCO  | TRC_DATA14 | UART3_RTSn | MCASP0_AXR4  | GPMC0_A8   | UART0_DS Rn  |            |  |
| 0x1C068        | WKUP_PADCONFIG_26 | D11         | MCU_RGMII1_TX_CTL      | MCU_RMII1_CRS_DV      |                       |                    |                     |                  |                    | WKUP_GPIO0_29    |               |                |            |            |              |            |              |            |  |
| 0x1C068        | PADCONFIG_26      | T14         | MCAN9_TX               |                       |                       |                    | RGMI3_RXD2          |                  | MCAN9_TX           | GPIO0_27         | SPI3_CLK      | EHRPWM3_SYNCI  | TRC_DATA13 |            | MCASP1_AFSR  | GPMC0_A9   | MCASP1_AXR10 |            |  |
| 0x1C06C        | WKUP_PADCONFIG_27 | A11         | MCU_RGMII1_RX_CTL      | MCU_RMII1_RX_ER       |                       |                    |                     |                  |                    | WKUP_GPIO0_43    |               |                |            |            |              |            |              |            |  |
| 0x1C06C        | PADCONFIG_27      | U18         | MCAN9_RX               |                       |                       |                    | RGMI3_RXD3          |                  | MCAN9_RX           | GPIO0_28         | SPI3_D0       | EHRPWM3_B      | TRC_DATA12 |            | MCASP1_ACLKR | GPMC0_A10  | MCASP1_AXR11 |            |  |

**Table 5-106. Pin Multiplexing (continued)**

| ADDR<br>ESS<br>OFFSE<br>T | REGISTER<br>NAME  | BALL<br>NUMB<br>ER | MUXMODE[15:0] SETTINGS |                   |   |                      |               |              |           |          |               |              |                |            |              |                 |           | Bootstrap  |
|---------------------------|-------------------|--------------------|------------------------|-------------------|---|----------------------|---------------|--------------|-----------|----------|---------------|--------------|----------------|------------|--------------|-----------------|-----------|------------|
|                           |                   |                    | 0                      | 1                 | 2 | 3                    | 4             | 5            | 6         | 7        | 8             | 9            | 10             | 11         | 12           | 13              | 14        |            |
| 0x1C070                   | WKUP_PADCONFIG_28 | C12                | MCU_RGMII1_TD3         | MCU_TIMER_IO2     |   | MCU_ADC_EXT_TRIGGER0 |               |              |           |          | WKUP_GPIO0_44 |              |                |            |              |                 |           |            |
| 0x1C070                   | PADCONFIG_28      | U17                | MCAN10_TX              |                   |   |                      | RGMII3_TX_CTL |              | MCAN10_TX | GPIO0_29 | SPI3_D1       | EHRPWM_SOCB  | TRC_DATA10     | UART2_CTSn | MCASP0_ACLKR | GPMC0_WAIT1     | GPMC0_A22 |            |
| 0x1C074                   | PADCONFIG_29      | U20                | MCAN10_RX              |                   |   |                      | RGMII3_TXC    |              | MCAN10_RX | GPIO0_30 | SPI2_CLK      | EHRPWM4_A    | TRC_DATA16     | UART2_RTSn | MCASP0_AXR6  | GPMC0_BE0n_CLE  | GPMC0_A16 |            |
| 0x1C074                   | WKUP_PADCONFIG_29 | B12                | MCU_RGMII1_TD2         | MCU_TIMER_IO3     |   | MCU_ADC_EXT_TRIGGER1 |               |              |           |          |               |              |                |            |              |                 |           |            |
| 0x1C078                   | WKUP_PADCONFIG_30 | B11                | MCU_RGMII1_TD1         | MCU_RMII1_TXD1    |   |                      |               |              |           |          |               |              |                |            |              |                 |           |            |
| 0x1C078                   | PADCONFIG_30      | Y14                | MCAN11_TX              |                   |   |                      | RGMII2_RXC    |              | MCAN11_TX | GPIO0_31 | SPI2_CS0      | EQEP0_A      |                | SPI0_CS2   | UART3_RXD    | MCASP0_AXR13    | GPMC0_A11 | UART0_DTRn |
| 0x1C07C                   | PADCONFIG_31      | Y13                | MCAN11_RX              |                   |   |                      | RGMII2_RXD0   |              | MCAN11_RX | GPIO0_32 | SPI2_CS1      | EQEP0_B      |                |            | UART3_TXD    | MCASP0_AXR14    | GPMC0_A12 | UART0_RIn  |
| 0x1C07C                   | WKUP_PADCONFIG_31 | D10                | MCU_RGMII1_TD0         | MCU_RMII1_TXD0    |   |                      |               |              |           |          |               |              |                |            |              |                 |           |            |
| 0x1C080                   | PADCONFIG_32      | AA15               | MCAN12_TX              |                   |   |                      | RGMII2_RXD1   |              | MCAN12_TX | GPIO0_33 | SPI2_CS2      | EQEP1_A      | I2C6_SCL       | UART2_RXD  | MCASP0_AXR15 | GPMC0_BE1n      | GPMC0_A17 |            |
| 0x1C080                   | WKUP_PADCONFIG_32 | A12                | MCU_RGMII1_TXC         | MCU_RMII1_TX_EN   |   |                      |               |              |           |          |               |              |                |            |              |                 |           |            |
| 0x1C084                   | WKUP_PADCONFIG_33 | B10                | MCU_RGMII1_RXC         | MCU_RMII1_REF_CLK |   |                      |               |              |           |          |               |              |                |            |              |                 |           |            |
| 0x1C084                   | PADCONFIG_33      | AA14               | MCAN12_RX              |                   |   |                      | RGMII2_RXD2   |              | MCAN12_RX | GPIO0_34 | SPI2_CS3      | EQEP1_B      | I2C6_SDA       | UART2_TXD  | MCASP1_AXR8  | I3C0_SDA_PULLEN | GPMC0_A18 |            |
| 0x1C088                   | PADCONFIG_34      | AA18               | MCAN13_TX              |                   |   |                      | RGMII2_RXD3   | GPMC0_WPn    | MCAN13_TX | GPIO0_35 | SPI2_D0       | EQEP0_S      | I2C5_SCL       | UART8_CTSn | MCASP1_AXR9  | I3C0_SCL        | GPMC0_A19 |            |
| 0x1C088                   | WKUP_PADCONFIG_34 | C10                | MCU_RGMII1_RD3         | MCU_TIMER_IO4     |   |                      |               |              |           |          |               |              |                |            |              |                 |           |            |
| 0x1C08C                   | PADCONFIG_35      | AA16               | MCAN13_RX              |                   |   |                      | RGMII2_RX_CTL | GPMC0_CSn3   | MCAN13_RX | GPIO0_36 | SPI2_D1       | EQEP0_I      | I2C5_SDA       | UART8_RTSn | MCASP2_AXR0  | I3C0_SDA        | GPMC0_A20 |            |
| 0x1C08C                   | WKUP_PADCONFIG_35 | A10                | MCU_RGMII1_RD2         | MCU_TIMER_IO5     |   |                      |               |              |           |          |               |              |                |            |              |                 |           |            |
| 0x1C090                   | WKUP_PADCONFIG_36 | B9                 | MCU_RGMII1_RD1         | MCU_RMII1_RXD1    |   |                      |               |              |           |          |               |              |                |            |              |                 |           |            |
| 0x1C090                   | PADCONFIG_36      | W17                | MCAN15_TX              |                   |   |                      | RGMII2_TXD0   | RMII2_RXD0   |           | GPIO0_37 | SPI6_CS2      | EQEP1_S      | MCAN15_TX      | GPMC0_CSn2 | MCASP2_AXR1  | GPMC0_A0        | GPMC0_A21 |            |
| 0x1C094                   | PADCONFIG_37      | W20                | MCAN15_RX              |                   |   |                      | RGMII2_TXD1   | RMII2_RXD1   |           | GPIO0_38 | SPI6_CS3      | EQEP1_I      | MCAN15_RX      |            | MCASP2_AXR2  | GPMC0_A15       | GPMC0_A15 | GPMC0_A15  |
| 0x1C094                   | WKUP_PADCONFIG_37 | A9                 | MCU_RGMII1_RD0         | MCU_RMII1_RXD0    |   |                      |               |              |           |          |               |              |                |            |              |                 |           |            |
| 0x1C098                   | PADCONFIG_38      | V14                | UART2_RXD              |                   |   |                      | RGMII2_TXD2   | RMII2_CRS_DV |           | GPIO0_39 | SPI6_CLK      | GPMC0_CLKOUT | GPMC0_FCLK_MUX | UART2_RXD  | MCASP2_AXR3  |                 |           | OBSCLK2    |
| 0x1C098                   | WKUP_PADCONFIG_38 | C9                 | MCU_MDI0_MDIO          |                   |   |                      |               |              |           |          |               |              |                |            |              |                 |           |            |

**Table 5-106. Pin Multiplexing (continued)**

| ADDRESS OFFSET | REGISTER NAME     | BALL NUMBER | MUXMODE[15:0] SETTINGS |               |             |   |           |               |             |   |               |         |    |            |           |              | Bootstrap   |    |                |
|----------------|-------------------|-------------|------------------------|---------------|-------------|---|-----------|---------------|-------------|---|---------------|---------|----|------------|-----------|--------------|-------------|----|----------------|
|                |                   |             | 0                      | 1             | 2           | 3 | 4         | 5             | 6           | 7 | 8             | 9       | 10 | 11         | 12        | 13           |             | 14 |                |
| 0x1C09C        | PADCONFIG_39      | V13         | UART2_TXD              |               |             |   |           | RGMII2_T D3   | RMII2_RX_ER |   | GPIO0_40      | SPI6_D0 |    |            | UART2_TXD | MCASP2_AFSX  |             |    |                |
| 0x1C09C        | WKUP_PADCONFIG_39 | D9          | MCU_MDI00_MDC          |               |             |   |           |               |             |   | WKUP_GPIO0_55 |         |    |            |           |              |             |    |                |
| 0x1C0A0        | WKUP_PADCONFIG_40 | C13         | MCU_SPI0_CLK           |               |             |   |           |               |             |   | WKUP_GPIO0_56 |         |    |            |           |              |             |    | MCU_BOOTMODE00 |
| 0x1C0A0        | PADCONFIG_40      | U12         |                        |               |             |   |           | RGMII2_TX_CTL | RMII2_TXD0  |   | GPIO0_41      | SPI6_D1 |    |            | UART4_RXD | MCASP2_ACLKX | GPCM0_A13   |    |                |
| 0x1C0A4        | WKUP_PADCONFIG_41 | A20         | MCU_SPI0_D0            |               |             |   |           |               |             |   | WKUP_GPIO0_57 |         |    |            |           |              |             |    | MCU_BOOTMODE01 |
| 0x1C0A4        | PADCONFIG_41      | W14         | UART8_RXD              |               | I2C4_SCL    |   |           |               | MDIO0_M DIO |   | GPIO0_42      |         |    | TRC_DATA22 | UART8_RXD | MCASP2_AFSR  | MCASP2_AXR4 |    |                |
| 0x1C0A8        | WKUP_PADCONFIG_42 | B17         | MCU_SPI0_D1            |               |             |   |           | MCU_TIMER_IO0 |             |   | WKUP_GPIO0_58 |         |    |            |           |              |             |    | MCU_BOOTMODE02 |
| 0x1C0A8        | PADCONFIG_42      | W19         | UART8_TXD              | SPI1_CS3      | I2C4_SDA    |   |           |               | MDIO0_M DC  |   | GPIO0_43      |         |    | TRC_DATA23 | UART8_TXD | MCASP2_ACLKR | MCASP2_AXR5 |    |                |
| 0x1C0AC        | WKUP_PADCONFIG_43 | A19         | MCU_SPI0_CS0           |               |             |   |           | MCU_TIMER_IO1 |             |   | WKUP_GPIO0_59 |         |    |            |           |              |             |    |                |
| 0x1C0AC        | PADCONFIG_43      | U13         | GPCM0_C LK             | USB0_DR VVBUS |             |   |           | RGMII4_R D3   |             |   | GPIO0_44      |         |    | SPI0_CS3   | UART9_RXD |              |             |    |                |
| 0x1C0B0        | WKUP_PADCONFIG_44 | B14         | WKUP_UART0_RXD         |               |             |   |           |               |             |   | WKUP_GPIO0_60 |         |    |            |           |              |             |    |                |
| 0x1C0B0        | PADCONFIG_44      | T16         | UART0_RXD              |               |             |   |           | RGMII4_T XC   |             |   | GPIO0_47      |         |    |            |           |              |             |    | GPCM0_W AIT0   |
| 0x1C0B4        | PADCONFIG_45      | T17         | UART0_TXD              |               |             |   |           | RGMII4_T D2   |             |   | GPIO0_48      |         |    |            |           |              |             |    | GPCM0_W En     |
| 0x1C0B4        | WKUP_PADCONFIG_45 | A14         | WKUP_UART0_TXD         |               |             |   |           |               |             |   | WKUP_GPIO0_61 |         |    |            |           |              |             |    |                |
| 0x1C0B8        | PADCONFIG_46      | T18         | UART1_RXD              | MCAN17_T X    |             |   | TIMER_IO6 | RGMII4_T D3   |             |   | GPIO0_49      |         |    |            |           |              |             |    | GPCM0_O En_REn |
| 0x1C0B8        | WKUP_PADCONFIG_46 | A16         | MCU_MCAN0_TX           |               |             |   |           |               |             |   | WKUP_GPIO0_62 |         |    |            |           |              |             |    |                |
| 0x1C0BC        | PADCONFIG_47      | T20         | UART1_TXD              | MCAN17_RX     |             |   | TIMER_IO7 | RGMII4_TX_CTL |             |   | GPIO0_50      |         |    |            |           |              |             |    | GPCM0_C Sn0    |
| 0x1C0BC        | WKUP_PADCONFIG_47 | A17         | MCU_MCAN0_RX           |               |             |   |           |               |             |   | WKUP_GPIO0_63 |         |    |            |           |              |             |    |                |
| 0x1C0C0        | PADCONFIG_48      | W3          | SPI0_CS0               |               | UART0_CT Sn |   |           |               |             |   | GPIO0_51      |         |    |            |           |              |             |    |                |
| 0x1C0C0        | WKUP_PADCONFIG_48 | B18         | MCU_SPI1_CLK           | MCU_SPI1_CLK  |             |   |           |               |             |   | WKUP_GPIO0_0  |         |    |            |           |              |             |    | MCU_BOOTMODE03 |
| 0x1C0C4        | PADCONFIG_49      | U5          | SPI0_CS1               | CPTS0_TS_COMP | UART0_RT Sn |   |           |               |             |   | GPIO0_52      |         |    |            |           |              |             |    |                |
| 0x1C0C4        | WKUP_PADCONFIG_49 | B19         | MCU_SPI1_D0            | MCU_SPI1_D0   |             |   |           |               |             |   | WKUP_GPIO0_1  |         |    |            |           |              |             |    | MCU_BOOTMODE04 |
| 0x1C0C8        | PADCONFIG_50      | Y1          | SPI0_CLK               | UART1_CT Sn   | I2C2_SCL    |   |           |               |             |   | GPIO0_53      |         |    |            |           |              |             |    |                |

**Table 5-106. Pin Multiplexing (continued)**

| ADDR<br>ESS<br>OFFSE<br>T | REGISTER<br>NAME      | BALL<br>NUMB<br>ER | MUXMODE[15:0] SETTINGS    |                           |                             |                              |                           |                            |                 |                   |               |                   |    |    |    |    |    | Bootstrap |                    |
|---------------------------|-----------------------|--------------------|---------------------------|---------------------------|-----------------------------|------------------------------|---------------------------|----------------------------|-----------------|-------------------|---------------|-------------------|----|----|----|----|----|-----------|--------------------|
|                           |                       |                    | 0                         | 1                         | 2                           | 3                            | 4                         | 5                          | 6               | 7                 | 8             | 9                 | 10 | 11 | 12 | 13 | 14 |           |                    |
| 0x1C0<br>C8               | WKUP_PADCON<br>FIG_50 | D14                | MCU_SPI1<br>_D1           | MCU_SPI1<br>_D1           |                             |                              |                           |                            |                 |                   |               |                   |    |    |    |    |    |           | MCU_BOO<br>TMODE05 |
| 0x1C0<br>CC               | WKUP_PADCON<br>FIG_51 | B21                | MCU_SPI1<br>_CS0          | MCU_SPI1<br>_CS0          |                             |                              |                           |                            |                 |                   |               |                   |    |    |    |    |    |           |                    |
| 0x1C0<br>CC               | PADCONFIG_51          | V4                 | SPI0_D0                   | UART1_RT<br>Sn            | I2C2_SDA                    |                              |                           |                            |                 |                   |               |                   |    |    |    |    |    |           |                    |
| 0x1C0<br>D0               | WKUP_PADCON<br>FIG_52 | D13                | MCU_MCA<br>N1_TX          | MCU_MCA<br>N1_TX          | MCU_SPI0<br>_CS3            | MCU_ADC<br>_EXT_TRI<br>GGER0 |                           |                            |                 |                   |               |                   |    |    |    |    |    |           |                    |
| 0x1C0<br>D0               | PADCONFIG_52          | T5                 | SPI0_D1                   |                           |                             |                              |                           |                            |                 |                   |               |                   |    |    |    |    |    |           |                    |
| 0x1C0<br>D4               | PADCONFIG_53          | V3                 | I2C0_SCL                  |                           |                             |                              |                           |                            |                 |                   |               |                   |    |    |    |    |    |           |                    |
| 0x1C0<br>D4               | WKUP_PADCON<br>FIG_53 | B16                | MCU_MCA<br>N1_RX          | MCU_MCA<br>N1_RX          | MCU_SPI1<br>_CS3            | MCU_ADC<br>_EXT_TRI<br>GGER1 |                           |                            |                 |                   |               |                   |    |    |    |    |    |           |                    |
| 0x1C0<br>D8               | PADCONFIG_54          | W2                 | I2C0_SDA                  |                           |                             |                              |                           |                            |                 |                   |               |                   |    |    |    |    |    |           |                    |
| 0x1C0<br>D8               | WKUP_PADCON<br>FIG_54 | C14                | WKUP_UA<br>RT0_CTSn       | WKUP_UA<br>RT0_CTSn       | MCU_CPT<br>S0_HW1T<br>SPUSH | MCU_I2C1<br>_SCL             |                           |                            |                 |                   |               |                   |    |    |    |    |    |           |                    |
| 0x1C0<br>DC               | PADCONFIG_55          | U3                 | ECAP0_IN<br>_APWM_O<br>UT | SYNC0_O<br>UT             | CPTS0_RF<br>T_CLK           | I2C1_SCL                     | CPTS0_H<br>W1TSPUS<br>H   | UART3_RX<br>D              | SPI7_CS0        | GPIO0_58          |               |                   |    |    |    |    |    |           |                    |
| 0x1C0<br>DC               | WKUP_PADCON<br>FIG_55 | C18                | WKUP_UA<br>RT0_RTSn       | WKUP_UA<br>RT0_RTSn       | MCU_CPT<br>S0_HW2T<br>SPUSH | MCU_I2C1<br>_SDA             |                           |                            |                 |                   |               |                   |    |    |    |    |    |           |                    |
| 0x1C0<br>E0               | PADCONFIG_56          | T3                 | EXT_REFC<br>LK1           | SYNC1_O<br>UT             |                             | I2C1_SDA                     | CPTS0_H<br>W2TSPUS<br>H   | UART3_TX<br>D              | SPI7_CLK        | GPIO0_59          |               |                   |    |    |    |    |    |           |                    |
| 0x1C0<br>E0               | WKUP_PADCON<br>FIG_56 | C21                | MCU_I2C1<br>_SCL          | MCU_I2C1<br>_SCL          | MCU_CPT<br>S0_TS_SY<br>NC   | MCU_I3C0<br>_SCL             | MCU_TIME<br>R_IO6         |                            |                 |                   |               |                   |    |    |    |    |    |           |                    |
| 0x1C0<br>E4               | PADCONFIG_57          | V1                 | TIMER_IO<br>0             | ECAP1_IN<br>_APWM_O<br>UT | SYSCLKO<br>UT0              |                              |                           | UART3_CT<br>Sn             | SPI7_D0         | GPIO0_60          | MMC1_SD<br>CD |                   |    |    |    |    |    |           |                    |
| 0x1C0<br>E4               | WKUP_PADCON<br>FIG_57 | C19                | MCU_I2C1<br>_SDA          | MCU_I2C1<br>_SDA          | MCU_CPT<br>S0_TS_CO<br>MP   | MCU_I3C0<br>_SDA             | MCU_TIME<br>R_IO7         |                            |                 |                   |               |                   |    |    |    |    |    |           |                    |
| 0x1C0<br>E8               | PADCONFIG_58          | W1                 | TIMER_IO<br>1             | ECAP2_IN<br>_APWM_O<br>UT | OBSCLK0                     |                              |                           | UART3_RT<br>Sn             | SPI7_D1         | GPIO0_61          | MMC1_SD<br>WP | PCIE1_CL<br>KREQn |    |    |    |    |    |           |                    |
| 0x1C0<br>E8               | WKUP_PADCON<br>FIG_58 | C20                | MCU_EXT<br>_REFCLK0       | MCU_EXT<br>_REFCLK0       | MCU_UAR<br>T0_TXD           | MCU_ADC<br>_EXT_TRI<br>GGER0 | MCU_CPT<br>S0_RFT_C<br>LK | MCU_SYS<br>CLKOUT0         |                 |                   |               |                   |    |    |    |    |    |           |                    |
| 0x1C0<br>EC               | WKUP_PADCON<br>FIG_59 | C16                | MCU_OBS<br>CLK0           | MCU_OBS<br>CLK0           | MCU_UAR<br>T0_RXD           | MCU_ADC<br>_EXT_TRI<br>GGER1 | MCU_TIME<br>R_IO1         | MCU_I3C0<br>_SDAPULL<br>EN | MCU_CLK<br>OUT0 | WKUP_GP<br>IO0_11 |               |                   |    |    |    |    |    |           |                    |

**Table 5-106. Pin Multiplexing (continued)**

| ADDRESS OFFSET | REGISTER NAME     | BALL NUMBER | MUXMODE[15:0] SETTINGS |              |                   |           |               |                     |   |   |               |          |               |          |           |    |    |           |                |
|----------------|-------------------|-------------|------------------------|--------------|-------------------|-----------|---------------|---------------------|---|---|---------------|----------|---------------|----------|-----------|----|----|-----------|----------------|
|                |                   |             | 0                      | 1            | 2                 | 3         | 4             | 5                   | 6 | 7 | 8             | 9        | 10            | 11       | 12        | 13 | 14 | Bootstrap |                |
| 0x1C0EC        | PADCONFIG_59      | N19         | MMC1_DATA3             | UART7_RXD    | PCIE1_CLKREQn     | TIMER_IO0 |               |                     |   |   | GPIO0_62      | SPI1_CS0 | UART0_CTSn    | I2C3_SCL | UART5_RXD |    |    |           |                |
| 0x1C0F0        | WKUP_PADCONFIG_60 | D19         | MCU_UART0_TXD          | MCU_SPIO_CS1 |                   |           |               |                     |   |   | WKUP_GPIO0_12 |          |               |          |           |    |    |           | MCU_BOOTMODE08 |
| 0x1C0F0        | PADCONFIG_60      | N20         | MMC1_DATA2             | UART7_TXD    |                   | TIMER_IO1 |               |                     |   |   | GPIO0_63      | SPI1_CS1 | CPTS0_TS_SYNC | I2C3_SDA | UART5_TXD |    |    |           |                |
| 0x1C0F4        | PADCONFIG_61      | N21         | MMC1_DATA1             | UART7_CTSn   | ECAP1_IN_APWM_OUT | TIMER_IO2 |               | UART4_RXD           |   |   | GPIO0_64      | SPI1_CS2 | UART5_CTSn    | I2C4_SDA | UART2_RXD |    |    |           |                |
| 0x1C0F4        | WKUP_PADCONFIG_61 | D20         | MCU_UART0_RXD          | MCU_SPIO_CS1 |                   |           |               |                     |   |   | WKUP_GPIO0_13 |          |               |          |           |    |    |           | MCU_BOOTMODE09 |
| 0x1C0F8        | PADCONFIG_62      | M19         | MMC1_DATA0             | UART7_RTSn   | ECAP1_IN_APWM_OUT | TIMER_IO3 |               | UART4_TXD           |   |   | GPIO0_65      | SPI1_D0  | UART5_RTSn    | I2C4_SCL | UART2_TXD |    |    |           |                |
| 0x1C0F8        | WKUP_PADCONFIG_62 | E20         | MCU_UART0_CTSn         | MCU_SPIO_CS2 |                   |           | MCU_TIMER_IO8 |                     |   |   | WKUP_GPIO0_14 |          |               |          |           |    |    |           | MCU_BOOTMODE06 |
| 0x1C0FC        | WKUP_PADCONFIG_63 | E21         | MCU_UART0_RTSn         | MCU_SPIO_CS2 |                   |           | MCU_TIMER_IO9 |                     |   |   | WKUP_GPIO0_15 |          |               |          |           |    |    |           | MCU_BOOTMODE07 |
| 0x1C100        | PADCONFIG_64      | P21         | MMC1_CLK               | UART8_RXD    |                   | TIMER_IO4 |               | UART4_CTSn          |   |   | GPIO0_66      | SPI1_CLK | UART0_RTSn    | I2C6_SDA |           |    |    |           |                |
| 0x1C100        | WKUP_PADCONFIG_64 | F20         | WKUP_I2C0_SCL          |              |                   |           |               |                     |   |   | WKUP_GPIO0_64 |          |               |          |           |    |    |           |                |
| 0x1C104        | PADCONFIG_65      | M20         | MMC1_CMD               | UART8_TXD    |                   | TIMER_IO5 |               | UART4_RTSn          |   |   | GPIO0_67      | SPI1_D1  |               | I2C6_SCL |           |    |    |           |                |
| 0x1C104        | WKUP_PADCONFIG_65 | H21         | WKUP_I2C0_SDA          |              |                   |           |               |                     |   |   | WKUP_GPIO0_65 |          |               |          |           |    |    |           |                |
| 0x1C108        | WKUP_PADCONFIG_66 | G21         | MCU_I2C0_SCL           |              |                   |           |               |                     |   |   | WKUP_GPIO0_66 |          |               |          |           |    |    |           |                |
| 0x1C108        | PADCONFIG_66      | U2          | RESETSTATz             |              |                   |           |               |                     |   |   |               |          |               |          |           |    |    |           |                |
| 0x1C10C        | WKUP_PADCONFIG_67 | G20         | MCU_I2C0_SDA           |              |                   |           |               |                     |   |   | WKUP_GPIO0_67 |          |               |          |           |    |    |           |                |
| 0x1C110        | WKUP_PADCONFIG_68 | C15         | PMIC_POWER_EN1         |              |                   |           |               | MCU_I3C0_SDAPULL_EN |   |   | WKUP_GPIO0_68 |          |               |          |           |    |    |           |                |
| 0x1C110        | PADCONFIG_68      | V2          | SOC_SAFETY_ERRORn      |              |                   |           |               |                     |   |   |               |          |               |          |           |    |    |           |                |
| 0x1C114        | WKUP_PADCONFIG_69 | G18         | MCU_SAFETY_ERRORn      |              |                   |           |               |                     |   |   |               |          |               |          |           |    |    |           |                |
| 0x1C118        | WKUP_PADCONFIG_70 | A18         | MCU_RES ETz            |              |                   |           |               |                     |   |   |               |          |               |          |           |    |    |           |                |
| 0x1C11C        | PADCONFIG_71      | U4          | TMS                    |              |                   |           |               |                     |   |   |               |          |               |          |           |    |    |           |                |
| 0x1C11C        | WKUP_PADCONFIG_71 | B13         | MCU_RES ETSTATz        |              |                   |           |               |                     |   |   | WKUP_GPIO0_79 |          |               |          |           |    |    |           |                |

**Table 5-106. Pin Multiplexing (continued)**

| ADDRESS<br>OFFSET | REGISTER<br>NAME      | BALL<br>NUMBER | MUXMODE[15:0] SETTINGS |                   |   |   |                   |                   |   |   |                   |   |    |    |               |                | Bootstrap                 |                |
|-------------------|-----------------------|----------------|------------------------|-------------------|---|---|-------------------|-------------------|---|---|-------------------|---|----|----|---------------|----------------|---------------------------|----------------|
|                   |                       |                | 0                      | 1                 | 2 | 3 | 4                 | 5                 | 6 | 7 | 8                 | 9 | 10 | 11 | 12            | 13             |                           | 14             |
| 0x1C120           | WKUP_PADCON<br>FIG_72 | D21            |                        |                   |   |   | MCU_TIME<br>R_IO6 |                   |   |   | WKUP_GP<br>IO0_77 |   |    |    |               |                |                           | BOOTMOD<br>E04 |
| 0x1C120           | PADCONFIG_72          | T4             | USB0_DR<br>VVBUS       |                   |   |   |                   |                   |   |   | GPIO0_68          |   |    |    |               |                |                           |                |
| 0x1C124           | WKUP_PADCON<br>FIG_73 | B15            | TCK                    |                   |   |   |                   |                   |   |   |                   |   |    |    |               |                |                           |                |
| 0x1C124           | PADCONFIG_73          | T19            | PMIC_WA<br>KE0n        |                   |   |   |                   | RGMI4_T<br>D1     |   |   | GPIO0_1           |   |    |    |               |                |                           |                |
| 0x1C128           | WKUP_PADCON<br>FIG_74 | B20            | TRSTn                  |                   |   |   |                   |                   |   |   |                   |   |    |    |               |                |                           |                |
| 0x1C12C           | WKUP_PADCON<br>FIG_75 | A13            | EMU0                   |                   |   |   |                   |                   |   |   |                   |   |    |    |               |                |                           |                |
| 0x1C130           | WKUP_PADCON<br>FIG_76 | D12            | EMU1                   |                   |   |   |                   |                   |   |   |                   |   |    |    |               |                |                           |                |
| 0x1C134           | WKUP_PADCON<br>FIG_77 | H17            | MCU_ADC<br>0_AIN0      |                   |   |   |                   |                   |   |   |                   |   |    |    |               |                |                           |                |
| 0x1C138           | WKUP_PADCON<br>FIG_78 | K18            | MCU_ADC<br>0_AIN1      |                   |   |   |                   |                   |   |   |                   |   |    |    |               |                |                           |                |
| 0x1C13C           | WKUP_PADCON<br>FIG_79 | M17            | MCU_ADC<br>0_AIN2      |                   |   |   |                   |                   |   |   |                   |   |    |    |               |                |                           |                |
| 0x1C140           | WKUP_PADCON<br>FIG_80 | L18            | MCU_ADC<br>0_AIN3      |                   |   |   |                   |                   |   |   |                   |   |    |    |               |                |                           |                |
| 0x1C144           | WKUP_PADCON<br>FIG_81 | J18            | MCU_ADC<br>0_AIN4      |                   |   |   |                   |                   |   |   |                   |   |    |    |               |                |                           |                |
| 0x1C148           | WKUP_PADCON<br>FIG_82 | J17            | MCU_ADC<br>0_AIN5      |                   |   |   |                   |                   |   |   |                   |   |    |    |               |                |                           |                |
| 0x1C14C           | WKUP_PADCON<br>FIG_83 | K17            | MCU_ADC<br>0_AIN6      |                   |   |   |                   |                   |   |   |                   |   |    |    |               |                |                           |                |
| 0x1C150           | WKUP_PADCON<br>FIG_84 | L17            | MCU_ADC<br>0_AIN7      |                   |   |   |                   |                   |   |   |                   |   |    |    |               |                |                           |                |
| 0x1C164           | PADCONFIG_89          | V15            | MCAN16_T<br>X          | RMI1_REF_<br>CLK  |   |   |                   | RGMI4_R<br>X_CTL  |   |   | GPIO0_45          |   |    |    | UART7_TX<br>D | GPMC0_A<br>14  |                           |                |
| 0x1C168           | PADCONFIG_90          | U21            | MCAN16_<br>RX          | CLKOUT            |   |   |                   | RGMI4_T<br>D0     |   |   | GPIO0_46          |   |    |    | UART7_RX<br>D | GPMC0_C<br>Sn1 | AUDIO_EX<br>T_REFCLK<br>1 |                |
| 0x1C174           | WKUP_PADCON<br>FIG_93 | A15            | RESET_R<br>EQz         |                   |   |   |                   |                   |   |   |                   |   |    |    |               |                |                           |                |
| 0x1C178           | WKUP_PADCON<br>FIG_94 | H20            | PORz                   |                   |   |   |                   |                   |   |   |                   |   |    |    |               |                |                           |                |
| 0x1C17C           | WKUP_PADCON<br>FIG_95 | E19            |                        |                   |   |   |                   | MCU_TIME<br>R_IO7 |   |   | WKUP_GP<br>IO0_78 |   |    |    |               |                |                           | BOOTMOD<br>E05 |
| 0x1C180           | WKUP_PADCON<br>FIG_96 | D18            |                        |                   |   |   |                   |                   |   |   | WKUP_GP<br>IO0_80 |   |    |    |               |                |                           | BOOTMOD<br>E06 |
| 0x1C184           | WKUP_PADCON<br>FIG_97 | C17            |                        | WKUP_LF<br>_CLKIN |   |   |                   |                   |   |   | WKUP_GP<br>IO0_81 |   |    |    |               |                |                           | BOOTMOD<br>E07 |

**Table 5-106. Pin Multiplexing (continued)**

| ADDRESS OFFSET | REGISTER NAME       | BALL NUMBER | MUXMODE[15:0] SETTINGS |                 |                    |   |   |   |   |   |              |   |    |    |    |    | Bootstrap |    |
|----------------|---------------------|-------------|------------------------|-----------------|--------------------|---|---|---|---|---|--------------|---|----|----|----|----|-----------|----|
|                |                     |             | 0                      | 1               | 2                  | 3 | 4 | 5 | 6 | 7 | 8            | 9 | 10 | 11 | 12 | 13 |           | 14 |
| 0x1C188        | WKUP_PADCON FIG_98  | F19         | TDI                    |                 |                    |   |   |   |   |   |              |   |    |    |    |    |           |    |
| 0x1C18C        | WKUP_PADCON FIG_99  | F21         | TDO                    |                 |                    |   |   |   |   |   |              |   |    |    |    |    |           |    |
| 0x1C190        | WKUP_PADCON FIG_100 | E18         | PMIC_WAKE1n            | MCU_EXT_REFCLK0 | MCU_CPT_S0_RFT_CLK |   |   |   |   |   | WKUP_GPIO_84 |   |    |    |    |    |           |    |

## 5.5 Connections for Unused Pins

This section describes the Unused/Reserved balls connection requirements.

### Note

All power balls must be supplied with the voltages specified in [Section 6.3, Recommended Operating Conditions](#), unless otherwise specified in [Section 5.3, Signal Descriptions](#).

**Table 5-107. Unused Balls Specific Connection Requirements**

| BALL NUMBER | BALL NAME        | CONNECTION REQUIREMENTS   |
|-------------|------------------|---|
| V7          | SERDES0_REXT     | Each of these balls must be connected to VSS through a separate external pull resistor to ensure these balls are held to a valid logic low level if unused. |
| V5          | USB0_RCALIB      |   |
| K19         | OSC1_XI          |   |
| B20         | TRSTN            |   |
| H17         | MCU_ADC0_AIN0    |   |
| K18         | MCU_ADC0_AIN1    |   |
| M17         | MCU_ADC0_AIN2    |   |
| L18         | MCU_ADC0_AIN3    |   |
| J18         | MCU_ADC0_AIN4    |   |
| J17         | MCU_ADC0_AIN5    |   |
| K17         | MCU_ADC0_AIN6    |   |
| L17         | MCU_ADC0_AIN7    |   |
| B2          | DDR0_DQS0P       |   |
| E2          | DDR0_DQS1P       |   |
| M2          | DDR0_DQS2P       |   |
| R2          | DDR0_DQS3P       |   |
| V1          | MMC1_SDCD        |   |
| G15         | VMON1_ER_VSYS    |   |
| D16         | VMON2_IR_VCPU    |   |
| E17         | VMON3_IR_VEXT1P8 |   |
| F17         | VMON4_IR_VEXT1P8 |   |
| L14         | VMON5_IR_VEXT3P3 |   |

**Table 5-107. Unused Balls Specific Connection Requirements (continued)**

| BALL NUMBER | BALL NAME        | CONNECTION REQUIREMENTS  |
|-------------|------------------|--|
| A18         | MCU_RESETZ       | Each of these balls must be connected to the corresponding power supply through a separate external pull resistor to ensure these balls are held to a valid logic high level if unused. <sup>(1)</sup> |
| G19         | MCU_PORZ         |  |
| H20         | PORZ             |  |
| B15         | TCK              |  |
| U4          | TMS              |  |
| F20         | WKUP_I2C0_SCL    |  |
| H21         | WKUP_I2C0_SDA    |  |
| G20         | MCU_I2C0_SDA     |  |
| G21         | MCU_I2C0_SCL     |  |
| W2          | I2C0_SDA         |  |
| V3          | I2C0_SCL         |  |
| U6          | EXTINTN          |  |
| F19         | TDI              |  |
| F21         | TDO              |  |
| D12         | EMU1             |  |
| A13         | EMU0             |  |
| B1          | DDR0_DQS0N       |  |
| E1          | DDR0_DQS1N       |  |
| M1          | DDR0_DQS2N       |  |
| R1          | DDR0_DQS3N       |  |
| N17         | VPP_CORE         | Each of these balls must be left unconnected if unused.  |
| E11         | VPP_MCU          |  |
| P20         | MMC0_CALPAD      |  |
| AA8         | SERDES0_REFCLK_N |  |
| AA9         | SERDES0_REFCLK_P |  |
| AA11        | SERDES0_RX0_N    |  |
| AA12        | SERDES0_RX0_P    |  |
| W11         | SERDES0_TX0_N    |  |
| W12         | SERDES0_TX0_P    |  |
| W8          | SERDES0_RX1_N    |  |
| W9          | SERDES0_RX1_P    |  |
| Y10         | SERDES0_TX1_N    |  |
| Y11         | SERDES0_TX1_P    |  |
| Y7          | SERDES0_RX2_N    |  |
| Y8          | SERDES0_RX2_P    |  |
| AA5         | SERDES0_TX2_N    |  |
| AA6         | SERDES0_TX2_P    |  |
| W5          | SERDES0_RX3_N    |  |
| W6          | SERDES0_RX3_P    |  |
| Y4          | SERDES0_TX3_N    |  |
| Y5          | SERDES0_TX3_P    |  |

(1) To determine which power supply is associated with any IO refer to [Table 5-1, Pin Attributes](#).

**Table 5-108. Reserved Balls Specific Connection Requirements**

| BALLS                                      | CONNECTION REQUIREMENTS                  |
|--|--|
| A21 / AA21 / K8 / K9 / K10 / L8 / L9 / L10 | These balls do not exist on the package. |

**Table 5-108. Reserved Balls Specific Connection Requirements (continued)**

| BALLS  | CONNECTION REQUIREMENTS               |
|--|---------------------------------------|
| H18 / F18 / N18 / L20 / K20 / J20 / V8 / V10 / E5 / F6 | These balls must be left unconnected. |

**Note**

All other unused signal balls **without** Pad Configuration Register can be left unconnected.

**Note**

All other unused signal balls **with** a Pad Configuration Register can be left unconnected with their multiplexing mode set to GPIO input and internal pulldown resistor enabled.

Unused balls are defined as those which only connect to a PCB solder pad. This is the only use case where internal pull resistors are allowed as the only source/sink to hold a valid logic level.

Any balls connected to a via, test point, or PCB trace are considered used and must not depend on the internal pull resistor to hold a valid logic level.

Internal pull resistors are weak and may not source enough current to maintain a valid logic level for some operating conditions. This may be the case when connected to components with leakage to the opposite logic level, or when external noise sources couple to signal traces attached to balls which are only pulled to a valid logic level by the internal resistor. Therefore, external pull resistors may be required to hold a valid logic level on balls with external connections.

If balls are allowed to float between valid logic levels, the input buffer may enter a high-current state which could damage the IO cell.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

| PARAMETER                     |  | MIN  | MAX  | UNIT |
|-------------------------------|--|------|------|------|
| VDD_CORE                      | MAIN domain core supply  | -0.3 | 1.05 | V    |
| VDD_MCU                       | MCUSS core supply  | -0.3 | 1.05 | V    |
| VDD_CPU                       | CPU core supply  | -0.3 | 1.05 | V    |
| VDD_MCU_WAKE1                 | Core supply for MCU WAKE function  | -0.3 | 1.05 | V    |
| VDD_WAKE0                     | Core supply for MAIN domain WAKE function which includes all "CANUART" IO. | -0.3 | 1.05 | V    |
| VDDA_0P8_DLL_MMC0             | MMC0 DLL analog supply   | -0.3 | 1.05 | V    |
| VDDAR_CORE                    | MAIN domain RAM supply   | -0.3 | 1.05 | V    |
| VDDAR_MCU                     | MCUSS RAM supply   | -0.3 | 1.05 | V    |
| VDDAR_CPU                     | CPU RAM supply   | -0.3 | 1.05 | V    |
| VDDA_0P8_SERDES0              | SERDES0 analog supply low  | -0.3 | 1.05 | V    |
| VDDA_0P8_SERDES0_C            | SERDES0 clock supply   | -0.3 | 1.05 | V    |
| VDDA_0P8_USB                  | USB0 0.8 V analog supply   | -0.3 | 1.05 | V    |
| VDDA_0P8_PLL_DDR              | DDR PLL analog supply  | -0.3 | 1.05 | V    |
| VDDA_1P8_USB                  | USB0 1.8 V analog supply   | -0.3 | 2.2  | V    |
| VDDA_1P8_SERDES0              | SERDES0 analog supply high   | -0.3 | 2.2  | V    |
| VDDA_3P3_USB                  | USB0 3.3 V analog supply   | -0.3 | 3.8  | V    |
| VDDA_MCU_PLLGRP0              | Analog supply for MCU PLL Group 0  | -0.3 | 2.2  | V    |
| VDDA_PLLGRP0                  | Analog supply for MAIN PLL Group 0   | -0.3 | 2.2  | V    |
| VDDA_PLLGRP4                  | Analog supply for MAIN PLL Group 4   | -0.3 | 2.2  | V    |
| VDDA_PLLGRP6                  | Analog supply for MAIN PLL Group 6   | -0.3 | 2.2  | V    |
| VDDA_PLLGRP8                  | Analog supply for MAIN PLL Group 8   | -0.3 | 2.2  | V    |
| VDDA_WKUP                     | Oscillator supply for WKUP domain  | -0.3 | 2.2  | V    |
| VDDA_ADC_MCU                  | ADC analog supply  | -0.3 | 2.2  | V    |
| VDDA_MCU_TEMP                 | Analog supply for temperature sensor 0 in MCU domain                       | -0.3 | 2.2  | V    |
| VDDA_POR_WKUP                 | WKUP domain analog supply  | -0.3 | 2.2  | V    |
| VDDA_TEMP0                    | Analog supply for temperature sensor 0                                     | -0.3 | 2.2  | V    |
| VDDA_TEMP1                    | Analog supply for temperature sensor 1                                     | -0.3 | 2.2  | V    |
| VDDS_DDR <sup>(10)</sup>      | DDR interface power supply   | -0.3 | 1.2  | V    |
| VDDS_DDR_BIAS <sup>(10)</sup> | Bias supply for LPDDR4   | -0.3 | 1.2  | V    |
| VDDS_DDR_C <sup>(10)</sup>    | IO power for DDR Memory Clock Bit (MCB) macro                              | -0.3 | 1.2  | V    |
| VDDS_MMC0                     | MMC0 IO supply   | -0.3 | 2.2  | V    |
| VDDA_OSC1                     | HFOSC1 supply  | -0.3 | 2.2  | V    |
| VDDSHV0_MCU                   | IO supply MCUSS general IO group, and MCU and MAIN domain warm reset pins  | -0.3 | 3.8  | V    |
| VDDSHV0                       | IO supply for MAIN domain general  | -0.3 | 3.8  | V    |
| VDDSHV1_MCU                   | IO supply for MCUSS IO group 1   | -0.3 | 3.8  | V    |
| VDDSHV2_MCU                   | IO supply for MCUSS IO group 2   | -0.3 | 3.8  | V    |
| VDDSHV2                       | IO supply for MAIN domain IO group 2                                       | -0.3 | 3.8  | V    |
| VDDSHV5                       | IO supply for MAIN domain IO group 5                                       | -0.3 | 3.8  | V    |
| VPP_CORE                      | Supply voltage range for CORE EFUSE domain                                 | -0.3 | 1.89 | V    |
| VPP_MCU                       | Supply voltage range for MCU EFUSE domain                                  | -0.3 | 1.89 | V    |
| USB0_VBUS <sup>(9)</sup>      | Voltage range for USB VBUS comparator input                                | -0.3 | 3.6  | V    |

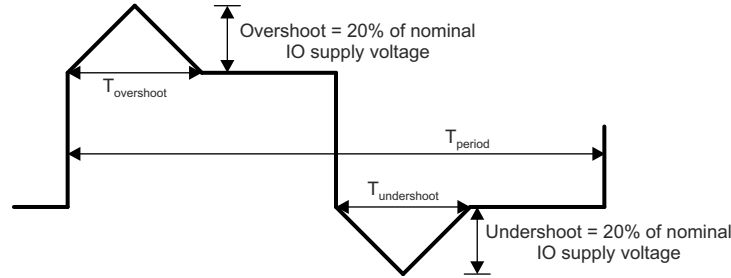
## 6.1 Absolute Maximum Ratings (continued)

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

| PARAMETER   |  | MIN  | MAX                      | UNIT |
|---|--|------|--------------------------|------|
| Steady State Max. Voltage at all fail-safe IO pins            | I2C0_SCL, I2C0_SDA, WKUP_I2C0_SCL, WKUP_I2C0_SDA, MCU_I2C0_SCL, MCU_I2C0_SDA, EXTINTn                                  | -0.3 | 3.8                      | V    |
|   | MCU_PORz, PORz   | -0.3 | 3.8                      | V    |
|   | VMON2_IR_VCPU  | -0.3 | 1.05                     | V    |
|   | VMON3_IR_VEXT1P8, VMON4_IR_VEXT1P8, VMON1_ER_VSYS <sup>(8)</sup>   | -0.3 | 2.2                      | V    |
|   | VMON5_IR_VEXT3P3   | -0.3 | 3.8                      | V    |
| Steady State Max. Voltage at all other IO pins <sup>(3)</sup> | All other IO pins  | -0.3 | IO supply voltage + 0.3  | V    |
| Transient Overshoot and Undershoot specification at IO pin    | 20% of IO supply voltage for up to 20% of signal period (see <a href="#">Figure 6-1, IO Transient Voltage Ranges</a> ) |      | 0.2 × VDD <sup>(6)</sup> | V    |
| Latch-up Performance, Class II (125°C) <sup>(4)</sup>         | I-Test   | -100 | 100                      | mA   |
|   | Over-Voltage (OV) Test   | NA   | 1.5 × VDD <sup>(7)</sup> | V    |
| T <sub>STG</sub> <sup>(5)</sup>                               | Storage temperature  | -55  | +150                     | °C   |

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the [Section 6.3, Recommended Operating Conditions](#) but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values are with respect to their associated VSS or VSSA\_x, unless otherwise noted.
- (3) This parameter applies to all IO pins which are not fail-safe and the requirement applies to all values of IO supply voltage. For example, if the voltage applied to a specific IO supply is 0 volts the valid input voltage range for any IO powered by that supply will be -0.3 to +0.3 volts. Special attention should be applied anytime peripheral devices are not powered from the same power sources used to power the respective IO supply. It is important the attached peripheral never sources a voltage outside the valid input voltage range, including power supply ramp-up and ramp-down sequences.
- (4) For current pulse injection:  
Pins stressed per JEDEC JESD78E (Class II) and passed with specified I/O pin injection current and clamp voltage of 1.5 times maximum recommended I/O voltage and negative 0.5 times maximum recommended I/O voltage.  
For overvoltage performance:  
Supplies stressed per JEDEC JESD78E (Class II) and passed specified voltage injection.
- (5) For tape and reel the storage temperature range is [-10°C; +50°C] with a maximum relative humidity of 70%. TI recommends returning to ambient room temperature before usage.
- (6) VDD is the voltage on the corresponding power-supply pin(s) for the IO.
- (7) An external resistor divider is required to create the VMON input value that triggers with V<sub>TH</sub> = 0.45 when the V<sub>SYS</sub> level reaches the minimum allowed threshold. A series resistor R2 (VMON\_ER\_VSYS = V<sub>SYS</sub> × R1 / (R1 + R2)) of at least 10kΩ is recommended to limit current.
- (8) The VMON1\_ER\_VSYS pin provides a way to monitor the system power supply. For more information, see [Section 8.3.4 System Power Supply Monitor Design Guidelines](#).
- (9) An external resistor divider is required to limit the voltage applied to this device pin. For more information, see [Section 8.3.3, USB VBUS Design Guidelines](#).
- (10) A single 1.1V source must drive all three VDDS\_DDR, VDDS\_DDR\_BIAS, VDDS\_DDR\_C supplies.

Fail-safe IO terminals are designed such they do not have dependencies on the respective IO power supply voltage. This allows external voltage sources to be connected to these IO terminals when the respective IO power supplies are turned off. The I2C0\_SCL, I2C0\_SDA, WKUP\_I2C0\_SCL, WKUP\_I2C0\_SDA, MCU\_I2C0\_SCL, MCU\_I2C0\_SDA, EXTINTn, MCU\_PORz, PORz, VMON1\_ER\_VSYS, VMON2\_IR\_VCPU, VMON3\_IR\_VEXT1P8, VMON4\_IR\_VEXT1P8, VMON5\_ER\_VEXT3P3 are the only fail-safe IO terminals. All other IO terminals are not fail-safe and the voltage applied to them should be limited to the value defined by the Steady State Max. Voltage at all IO pins parameter in [Section 6.1](#).



A.  $T_{overshoot} + T_{undershoot} < 20\% \text{ of } T_{period}$

**Figure 6-1. IO Transient Voltage Ranges**

## 6.2 ESD Ratings

|                    |                         |   | VALUE                  | UNIT |      |
|--------------------|-------------------------|---|------------------------|------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup> | ±1000                  | V    |      |
|                    |                         | Charged-device model (CDM), per AEC Q100-011            | All pins               |      | ±250 |
|                    |                         |   | Corner pins (A1, AJ29) |      | ±750 |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| SUPPLY NAME                       | DESCRIPTION  | MIN <sup>(1)</sup>                    | NOM                | MAX <sup>(1)</sup>                    | UNIT |
|-----------------------------------|--|---------------------------------------|--------------------|---------------------------------------|------|
| VDD_CORE <sup>(3)</sup>           | Boot/Active voltage for MAIN domain core supply                            | 0.76 <sup>(1)</sup>                   | 0.8                | 0.84 <sup>(1)</sup>                   | V    |
| VDD_MCU                           | Boot/Active voltage for MCUSS core supply                                  | 0.76 <sup>(1)</sup>                   | 0.8                | 0.89 <sup>(1)</sup>                   | V    |
| VDD_CPU                           | Boot voltage for CPU core supply, applied at cold power up event           | 0.76 <sup>(1)</sup>                   | 0.8                | 0.84 <sup>(1)</sup>                   | V    |
|                                   | Active voltage for CPU core supply, after AVS mode enabled in software     | AVS <sup>(5)</sup> -5% <sup>(1)</sup> | AVS <sup>(5)</sup> | AVS <sup>(5)</sup> +5% <sup>(1)</sup> | V    |
| VDD_CPU AVS Range                 | Efuse valid voltage range for VDD_CPU voltage                              | 0.6                                   |                    | 0.9                                   | V    |
| VDD_MCU_WAKE1                     | Core supply for MCU WAKE function  | 0.76                                  | 0.8                | 0.89                                  | V    |
| VDD_WAKE0                         | Core supply for MAIN domain WAKE function which includes all "CANUART" IO. | 0.76                                  | 0.8                | 0.89                                  | V    |
| VDDA_0P8_DLL_MMC0                 | MMC PLL analog supply  | 0.76                                  | 0.8                | 0.84                                  | V    |
| VDDAR_CORE                        | Main domain RAM supply   | 0.81                                  | 0.85               | 0.89                                  | V    |
| VDDAR_MCU                         | MCUSS RAM supply   | 0.81                                  | 0.85               | 0.89                                  | V    |
| VDDAR_CPU                         | CPU RAM supply   | 0.81                                  | 0.85               | 0.89                                  | V    |
| VDDA_0P8_SERDES0 <sup>(3)</sup>   | SERDES0 analog supply low  | 0.76                                  | 0.8                | 0.84                                  | V    |
| VDDA_0P8_SERDES0_C <sup>(3)</sup> | SERDES0-1 clock supply   | 0.76                                  | 0.8                | 0.84                                  | V    |
| VDDA_0P8_USB <sup>(3)</sup>       | USB 0.8v analog supply   | 0.76                                  | 0.8                | 0.84                                  | V    |
| VDDA_1P8_USB                      | USB 1.8v analog supply   | 1.71                                  | 1.8                | 1.89                                  | V    |

### 6.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

| SUPPLY NAME                  | DESCRIPTION   | MIN <sup>(1)</sup> | NOM                | MAX <sup>(1)</sup> | UNIT |   |
|------------------------------|---|--------------------|--------------------|--------------------|------|---|
| VDDA_1P8_SERDES0             | SERDES0 analog supply high  | 1.71               | 1.8                | 1.89               | V    |   |
| VDDA_3P3_USB                 | USB 3.3v analog supply  | 3.14               | 3.3                | 3.46               | V    |   |
| VDDA_MCU_PLLGRP0             | Analog supply for MCU PLL Group 0   | 1.71               | 1.8                | 1.89               | V    |   |
| VDDA_PLLGRP0                 | Analog supply for MAIN PLL Group 0  | 1.71               | 1.8                | 1.89               | V    |   |
| VDDA_PLLGRP4                 | Analog supply for MAIN PLL Group 4  | 1.71               | 1.8                | 1.89               | V    |   |
| VDDA_PLLGRP6                 | Analog supply for MAIN PLL Group 6  | 1.71               | 1.8                | 1.89               | V    |   |
| VDDA_PLLGRP8                 | Analog supply for MAIN PLL Group 8  | 1.71               | 1.8                | 1.89               | V    |   |
| VDDA_WKUP                    | Oscillator supply for WKUP domain   | 1.71               | 1.8                | 1.89               | V    |   |
| VDDA_ADC_MCU                 | ADC analog supply   | 1.71               | 1.8                | 1.89               | V    |   |
| VDDA_0P8_PLL_DDR             | DDR PLL analog supply   | 0.76               | 0.8                | 0.84               | V    |   |
| VDDA_MCU_TEMP                | Analog supply for temperature sensor 0 in MCU domain                      | 1.71               | 1.8                | 1.89               | V    |   |
| VDDA_POR_WKUP                | WKUP domain analog supply   | 1.71               | 1.8                | 1.89               | V    |   |
| VDDA_TEMP0                   | Analog supply for temperature sensor 0                                    | 1.71               | 1.8                | 1.89               | V    |   |
| VDDA_TEMP1                   | Analog supply for temperature sensor 1                                    | 1.71               | 1.8                | 1.89               | V    |   |
| VDDS_DDR <sup>(2)</sup>      | DDR interface power supply  | 1.05               | 1.1                | 1.15               | V    |   |
| VDDS_DDR_BIAS <sup>(2)</sup> | Bias supply for LPDDR4  | 1.05               | 1.1                | 1.15               | V    |   |
| VDDS_DDR_C <sup>(2)</sup>    | IO power for DDR Memory Clock Bit (MCB) macro                             | 1.05               | 1.1                | 1.15               | V    |   |
| VDDS_MMC0                    | MMC0 IO supply  | 1.71               | 1.8                | 1.89               | V    |   |
| VDDA_OSC1                    | HFOSC1 supply   | 1.71               | 1.8                | 1.89               | V    |   |
| VDDA_*                       | Peak to Peak Noise for all VDDA inputs                                    |                    |                    | 25                 | mV   |   |
| VDDSHV0                      | IO supply for main domain general   | 1.8-V operation    | 1.71               | 1.8                | 1.89 | V |
|                              |   | 3.3-V operation    | 3.14               | 3.3                | 3.46 | V |
| VDDSHV0_MCU                  | IO supply MCUSS general IO group, and MCU and Main domain warm reset pins | 1.8-V operation    | 1.71               | 1.8                | 1.89 | V |
|                              |   | 3.3-V operation    | 3.14               | 3.3                | 3.46 | V |
| VDDSHV1_MCU                  | IO supply for MCUSS IO group 1  | 1.8-V operation    | 1.71               | 1.8                | 1.89 | V |
|                              |   | 3.3-V operation    | 3.14               | 3.3                | 3.46 | V |
| VDDSHV2                      | IO supply for main domain IO group 2                                      | 1.8-V operation    | 1.71               | 1.8                | 1.89 | V |
|                              |   | 3.3-V operation    | 3.14               | 3.3                | 3.46 | V |
| VDDSHV2_MCU                  | IO supply for MCUSS IO group 2  | 1.8-V operation    | 1.71               | 1.8                | 1.89 | V |
|                              |   | 3.3-V operation    | 3.14               | 3.3                | 3.46 | V |
| VDDSHV5                      | IO supply for main domain IO group 5                                      | 1.8-V operation    | 1.71               | 1.8                | 1.89 | V |
|                              |   | 3.3-V operation    | 3.14               | 3.3                | 3.46 | V |
| USB0_VBUS                    | Voltage range for USB VBUS comparator input                               | 0                  | See <sup>(6)</sup> | 3.46               | V    |   |
| USB0_ID                      | Voltage range for the USB ID input  |                    | See <sup>(4)</sup> |                    | V    |   |
| VSS                          | Ground  |                    | 0                  |                    | V    |   |
| T <sub>J</sub>               | Operating junction temperature range                                      | Automotive         | –40                | 125                | °C   |   |
|                              |   | Extended           | –40                | 105                | °C   |   |
|                              |   | Commercial         | 0                  | 90                 | °C   |   |

- (1) For all VDD\* supply inputs, the voltage at the device ball must never be below the MIN voltage or above the MAX voltage for any amount of time. This requirement includes dynamic voltage events such as AC ripple, voltage transients, voltage dips, and so forth. This is required for all supply inputs, but special care should be given to the VDD\_CORE, VDD\_MCU, and VDD\_CPU domains which have higher transient current demand compared to other rails.
- (2) A single 1.1-V source must drive all three VDDS\_DDR, VDDS\_DDR\_BIAS, VDDS\_DDR\_C supplies. These supplies are required to still be powered with LPDDR4 voltage ranges, even if DDR interface is unused.

- (3) A single 0.8-V source must drive the VDD\_CORE and VDDA\_0P8\_PHY input supplies. Also, include Analog filter components on the individual VDDA\_0P8\_PHY input supplies for interfaces that are used in the system.
- (4) This terminal is connected to analog circuits in the respective USB PHY. The circuit sources a known current while measuring the voltage to determine if the terminal is connected to VSS with a resistance less than 10  $\Omega$  or greater than 100 k $\Omega$ . The terminal should be connected to ground for USB host operation or open-circuit for USB peripheral operation, and should never be connected to any external voltage source.
- (5) The AVS Voltages are device-dependent, voltage domain-dependent, and OPP-dependent. They must be read from the VTM\_DEVINFO\_VDn. For information about VTM\_DEVINFO\_VDn Registers address, please refer to Voltage and Thermal Manager section in the device TRM. The power supply should be adjustable over the ranges shown in the VDD\_CPU AVS Range entry.
- (6) An external resistor divider is required to limit the voltage applied to this device pin. For more information, see [Section 8.3.3, USB VBUS Design Guidelines](#)

## 6.4 Power-On-Hours (POH)

| IP <sup>1 2 3</sup> | VOLTAGE DOMAIN | VOLTAGE (V) (MAX) | FREQUENCY (MHz) (MAX) | Tj(°C)                    | POH    |
|---------------------|----------------|-------------------|-----------------------|---------------------------|--------|
| All                 | 100%           | All               | All Supported OPPs    | Automotive -40°C to 125°C | 20000  |
| All                 | 100%           | All               | All Supported OPPs    | Extended -40°C to 105°C   | 100000 |
| All                 | 100%           | All               | All Supported OPPs    | Commercial 0°C to 90°C    | 100000 |

1. This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.
2. Unless specified in the table above, all voltage domains and operating conditions are supported in the device at the noted temperatures.
3. POH is a function of voltage, temperature and time. Usage at higher voltages and temperatures will result in a reduction in POH.
4. Automotive profile is defined as 20000 power on hours with a junction temperature as follows: 5%@-40°C, 65%@70°C, 20%@110°C, and 10%@125°C.

## 6.5 Operating Performance Points

This section describes the maximum operating conditions of the device in [Table 6-1](#). This section also contains the description of each Operating Performance Point (OPP) for processor clocks and device core clocks in [Table 6-2](#).

**Table 6-1. Speed Grade Maximum Frequency**

| DEVICE   | MAXIMUM FREQUENCY (MHz) |        |            |        |      |                       |
|----------|-------------------------|--------|------------|--------|------|-----------------------|
|          | A72SS0                  | R5FSS0 | MCU_R5FSS0 | CBASS0 | DMSC | LPDDR4 <sup>(1)</sup> |
| DRA821xT | 2000                    | 1000   | 1000       | 500    | 333  | 1600 (DDR-3200)       |
| DRA821xL | 1500                    | 1000   | 1000       | 500    | 333  | 1600 (DDR-3200)       |
| DRA821xE | 1000                    | 1000   | 1000       | 500    | 333  | 1600 (DDR-3200)       |
| DRA821xC | 750                     | 500    | 1000       | 500    | 333  | 1600 (DDR-3200)       |

- (1) Maximum DDR Frequency will be limited based on the specific memory type (vendor) used in a system and by PCB implementation. TI strongly recommends all designs to follow the TI LPDDR4 EVM PCB layout exactly in every detail (routing, spacing, vias/backdrill, PCB material, etc.) in order to achieve the full specified clock frequency. Refer to the [Jacinto 7 DDR Board Design and Layout Guidelines](#) for details.

**Table 6-2. Supported OPP vs Max Frequency**

see (1) (2)

| CLOCK              | MAXIMUM FREQUENCY(MHz)                                    |                        |
|--------------------|---|------------------------|
|                    | OPP_LOW <sup>(4)</sup>                                    | OPP_NOM <sup>(3)</sup> |
| MPU_CLK (A72SS0)   | 1000  | 2000                   |
| MSMC_CLK           | 500   | 1000                   |
| DDRn_CLKP/DDRn_CKN | 1066 (2133 MT/s)<br>or<br>1333 (2666 MT/s) <sup>(5)</sup> | 1600 (3200 MT/s)       |

- (1) OPP and VDD\_CPU voltage should be selected/set at boot time. DVFS is *not* supported.
- (2) Frequency must be limited based on the lower frequency constraint from this table and [Speed Grade Maximum Frequency](#). For example, the T speed grade can operate A72SS/MSMC at 2 GHz/1GHz or 1 GHz/500 MHz. A72SS/MSMC at 2 GHz/1GHz operation must use OPP\_NOM. A72SS/MSMC at 1 GHz/500 MHz operation can use OPP\_NOM or OPP\_LOW voltage. Similarly, the E speed grade can operate A72SS/MSMC at a maximum of 1 GHz/500 MHz. In this case, OPP\_NOM or OPP\_LOW voltage is allowed (though OPP\_LOW voltage is recommended to reduce power consumption).
- (3) OPP\_NOM AVS voltage for VDD\_CPU should be set based on the OPP\_1 register setting.
- (4) If OPP\_0 is not equal to 0, OPP\_LOW AVS voltage for VDD\_CPU should be set based on the OPP\_0 register setting. If OPP\_0 is equal to 0, OPP\_1 register setting should be used.
- (5) DDR can be configured for up to 2666 MT/s in OPP\_LOW. 2132 MT/s is recommended in OPP\_LOW as it more closely matches the MPU\_CLK scaling and also saves power compared to 2666 MT/s.

## 6.6 Electrical Characteristics

### Note

The interfaces or signals described in [Section 6.6.10](#) through [Section 6.6.10](#) correspond to the interfaces or signals available in multiplexing mode 0 (Primary Function).

All interfaces or signals multiplexed on the balls described in these tables have the same DC electrical characteristics, unless multiplexing involves a PHY and GPIO combination, in which case different DC electrical characteristics are specified for the different multiplexing modes (Functions).

### 6.6.1 I2C, Open-Drain, Fail-Safe (I2C OD FS) Electrical Characteristics

over recommended operating conditions (unless otherwise noted) <sup>(1)</sup>

| PARAMETER  | TEST CONDITIONS                 | MIN                           | TYP | MAX                          | UNIT |
|--|---------------------------------|-------------------------------|-----|------------------------------|------|
| <b>BALL NAMES in Mode 0:</b> WKUP_I2C0_SDA, WKUP_I2C0_SCL, MCU_I2C0_SDA, MCU_I2C0_SCL, I2C0_SDA, I2C0_SCL, EXTINTN |                                 |                               |     |                              |      |
| <b>BALL NUMBERS:</b> H21 / F20 / G20 / G21 / W2 / V3 / U6  |                                 |                               |     |                              |      |
| <b>1.8 V MODE</b>  |                                 |                               |     |                              |      |
| V <sub>IL</sub>  | Input Low Voltage               |                               |     | 0.3 × VDDSHV <sup>(1)</sup>  | V    |
| V <sub>ILSS</sub>  | Input Low Voltage Steady State  |                               |     | 0.3 × VDDSHV <sup>(1)</sup>  | V    |
| V <sub>IH</sub>  | Input High Voltage              | 0.7 × VDDSHV <sup>(1)</sup>   |     |                              | V    |
| V <sub>IHSS</sub>  | Input High Voltage Steady State | 0.7 × VDDSHV <sup>(1)</sup>   |     |                              | V    |
| V <sub>HYS</sub>   | Input Hysteresis Voltage        | 0.1 × VDDSHV <sup>(1)</sup>   |     |                              | mV   |
| I <sub>IN</sub>  | Input Leakage Current.          | V <sub>I</sub> = 1.8 V or 0 V |     | ±10                          | µA   |
| V <sub>OL</sub>  | Output Low Voltage              |                               |     | 0.2 × VDDSHV <sup>(1)</sup>  | V    |
| I <sub>OL</sub>  | Low Level Output Current        | V <sub>OL(MAX)</sub>          |     | 10                           | mA   |
| <b>3.3 V MODE <sup>(2)</sup></b>   |                                 |                               |     |                              |      |
| V <sub>IL</sub>  | Input Low Voltage               |                               |     | 0.3 × VDDSHV <sup>(1)</sup>  | V    |
| V <sub>ILSS</sub>  | Input Low Voltage Steady State  |                               |     | 0.25 × VDDSHV <sup>(1)</sup> | V    |
| V <sub>IH</sub>  | Input High Voltage              | 0.7 × VDDSHV <sup>(1)</sup>   |     |                              | V    |
| V <sub>IHSS</sub>  | Input High Voltage Steady State | 0.7 × VDDSHV <sup>(1)</sup>   |     |                              | V    |
| V <sub>HYS</sub>   | Input Hysteresis Voltage        | 0.05 × VDDSHV <sup>(1)</sup>  |     |                              | mV   |
| I <sub>IN</sub>  | Input Leakage Current.          | V <sub>I</sub> = 3.3 V or 0 V |     | ±10                          | µA   |
| V <sub>OL</sub>  | Output Low Voltage              |                               |     | 0.4                          | V    |
| I <sub>OL</sub>  | Low Level Output Current        | V <sub>OL(MAX)</sub>          |     | 10                           | mA   |

(1) VDDSHV stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see [Table 5-1](#), POWER column.

(2) I2C HS-mode is not supported when operating the IO in 3.3 V mode.

### 6.6.2 Fail-Safe Reset (FS Reset) Electrical Characteristics

Over recommended operating conditions (unless otherwise noted)

| PARAMETER                                   | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-----------------|-----|-----|-----|------|
| <b>BALL NAMES in Mode 0:</b> MCU_PORz, PORz |                 |     |     |     |      |

Over recommended operating conditions (unless otherwise noted)

| PARAMETER                      |   | TEST CONDITIONS               | MIN                         | TYP | MAX                         | UNIT |
|--------------------------------|---|-------------------------------|-----------------------------|-----|-----------------------------|------|
| <b>BALL NUMBERS: G19 / H20</b> |   |                               |                             |     |                             |      |
| V <sub>IL</sub>                | Input low-level threshold               |                               |                             |     | 0.3 × VDDSHV <sup>(1)</sup> | V    |
| V <sub>ILSS</sub>              | Input low-level threshold steady state  |                               |                             |     | 0.3 × VDDSHV <sup>(1)</sup> | V    |
| V <sub>IH</sub>                | Input high-level threshold              |                               | 0.7 × VDDSHV <sup>(1)</sup> |     |                             | V    |
| V <sub>IHSS</sub>              | Input high-level threshold steady state |                               | 0.7 × VDDSHV <sup>(1)</sup> |     |                             | V    |
| V <sub>HYS</sub>               | Input Hysteresis Voltage                |                               | 200                         |     |                             | mV   |
| I <sub>IN</sub>                | Input Leakage Current                   | V <sub>I</sub> = 1.8 V or 0 V |                             |     | ±10                         | μA   |

(1) VDDSHV stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see [Pin Attributes](#), POWER column.

### 6.6.3 HFOSC Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER                                |                          | TEST CONDITIONS | MIN                          | TYP | MAX                          | UNIT |
|--|--------------------------|-----------------|------------------------------|-----|------------------------------|------|
| <b>HIGH FREQUENCY OSCILLATOR</b>         |                          |                 |                              |     |                              |      |
| <b>BALL NAMES: OSC1_X1, WKUP_OSC0_X1</b> |                          |                 |                              |     |                              |      |
| <b>BALL NUMBERS: K19 / K21</b>           |                          |                 |                              |     |                              |      |
| V <sub>IH</sub>                          | High-level input voltage |                 | 0.65 × VDDSHV <sup>(1)</sup> |     |                              | V    |
| V <sub>IL</sub>                          | Low-level input voltage  |                 |                              |     | 0.35 × VDDSHV <sup>(1)</sup> | V    |
| V <sub>HYS</sub>                         | Input Hysteresis Voltage |                 |                              | 49  |                              | mV   |

(1) VDDSHV stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see [Table 5-1](#), POWER column.

### 6.6.4 eMMC PHY Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER  |                                   | TEST CONDITIONS               | MIN                          | TYP | MAX                          | UNIT |
|--|-----------------------------------|-------------------------------|------------------------------|-----|------------------------------|------|
| <b>BALL NAMES in Mode 0: MMC0_DAT[7:0], MMC0_CALPAD, MMC0_CMD, MMC0_DS, MMC0_CLK</b>       |                                   |                               |                              |     |                              |      |
| <b>BALL NUMBERS: R16 / P17 / R18 / R20 / R19 / P16 / R21 / T21 / P20 / R17 / P19 / P18</b> |                                   |                               |                              |     |                              |      |
| V <sub>IL</sub>  | Input Low Voltage                 |                               |                              |     | 0.35 × VDDSHV <sup>(1)</sup> | V    |
| V <sub>ILSS</sub>  | Input Low Voltage Steady State    |                               |                              |     | 0.20                         | V    |
| V <sub>IH</sub>  | Input High Voltage                |                               | 0.65 × VDDSHV <sup>(1)</sup> |     |                              | V    |
| V <sub>IHSS</sub>  | Input High Voltage Steady State   |                               | 1.4                          |     |                              | V    |
| I <sub>IN</sub>  | Input Leakage Current.            | V <sub>I</sub> = 1.8 V or 0 V |                              |     | ±10                          | μA   |
| I <sub>OZ</sub>  | Tri-state Output Leakage Current. | V <sub>O</sub> = 1.8 V or 0 V |                              |     | ±10                          | μA   |
| R <sub>PU</sub>  | Pull-up Resistor                  |                               | 15                           | 20  | 25                           | kΩ   |
| R <sub>PD</sub>  | Pull-down Resistor                |                               | 15                           | 20  | 25                           | kΩ   |
| V <sub>OL</sub>  | Output Low Voltage                |                               |                              |     | 0.30                         | V    |
| V <sub>OH</sub>  | Output High Voltage               |                               | VDDSHV <sup>(1)</sup> -0.30  |     |                              | V    |
| I <sub>OL</sub>  | Low Level Output Current          | V <sub>OL(MAX)</sub>          | 2                            |     |                              | mA   |
| I <sub>OH</sub>  | High Level Output Current         | V <sub>OH(MIN)</sub>          | 2                            |     |                              | mA   |

over operating free-air temperature range (unless otherwise noted)

| PARAMETER       | TEST CONDITIONS | MIN  | TYP | MAX | UNIT |
|-----------------|-----------------|------|-----|-----|------|
| SR <sub>I</sub> | Input Slew Rate | 5E+8 |     |     | V/s  |

- (1) VDDSHV stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see [Table 5-1](#), POWER column.

### 6.6.5 SDIO Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER  | TEST CONDITIONS                 | MIN                           | TYP | MAX                           | UNIT |
|--|---------------------------------|-------------------------------|-----|-------------------------------|------|
| <b>BALL NAMES in Mode 0:</b> MMC1_CLK, MMC1_CMD, MMC1_DAT[3:0] |                                 |                               |     |                               |      |
| <b>BALL NUMBERS:</b> P21 / M20 / M19 / N21 / N20 / N19         |                                 |                               |     |                               |      |
| <b>1.8 V MODE</b>  |                                 |                               |     |                               |      |
| V <sub>IL</sub>  | Input Low Voltage               |                               |     | 0.58                          | V    |
| V <sub>ILSS</sub>  | Input Low Voltage Steady State  |                               |     | 0.58                          | V    |
| V <sub>IH</sub>  | Input High Voltage              | 1.27                          |     |                               | V    |
| V <sub>IHSS</sub>  | Input High Voltage Steady State | 1.7                           |     |                               | V    |
| V <sub>HYS</sub>   | Input Hysteresis Voltage        | 150                           |     |                               | mV   |
| I <sub>IN</sub>  | Input Leakage Current.          | V <sub>I</sub> = 1.8 V or 0 V |     | ±10                           | µA   |
| R <sub>PU</sub>  | Pull-up Resistor                | 40                            | 50  | 60                            | kΩ   |
| R <sub>PD</sub>  | Pull-down Resistor              | 40                            | 50  | 60                            | kΩ   |
| V <sub>OL</sub>  | Output Low Voltage              |                               |     | 0.45                          | V    |
| V <sub>OH</sub>  | Output High Voltage             | VDDSHV <sup>(1)</sup> - 0.45  |     |                               | V    |
| I <sub>OL</sub>  | Low Level Output Current        | V <sub>OL(MAX)</sub>          |     | 4                             | mA   |
| I <sub>OH</sub>  | High Level Output Current       | V <sub>OH(MIN)</sub>          |     | 4                             | mA   |
| <b>3.3 V MODE</b>  |                                 |                               |     |                               |      |
| V <sub>IL</sub>  | Input Low Voltage               |                               |     | 0.25 × VDDSHV <sup>(1)</sup>  | V    |
| V <sub>ILSS</sub>  | Input Low Voltage Steady State  |                               |     | 0.15 × VDDSHV <sup>(1)</sup>  | V    |
| V <sub>IH</sub>  | Input High Voltage              | 0.625 × VDDSHV <sup>(1)</sup> |     |                               | V    |
| V <sub>IHSS</sub>  | Input High Voltage Steady State | 0.625 × VDDSHV <sup>(1)</sup> |     |                               | V    |
| V <sub>HYS</sub>   | Input Hysteresis Voltage        | 150                           |     |                               | mV   |
| I <sub>IN</sub>  | Input Leakage Current.          | V <sub>I</sub> = 1.8 V or 0 V |     | ±10                           | µA   |
| R <sub>PU</sub>  | Pull-up Resistor                | 40                            | 50  | 60                            | kΩ   |
| R <sub>PD</sub>  | Pull-down Resistor              | 40                            | 50  | 60                            | kΩ   |
| V <sub>OL</sub>  | Output Low Voltage              |                               |     | 0.125 × VDDSHV <sup>(1)</sup> | V    |
| V <sub>OH</sub>  | Output High Voltage             | 0.75 × VDDSHV <sup>(1)</sup>  |     |                               | V    |
| I <sub>OL</sub>  | Low Level Output Current        | V <sub>OL(MAX)</sub>          |     | 6                             | mA   |
| I <sub>OH</sub>  | High Level Output Current       | V <sub>OH(MIN)</sub>          |     | 10                            | mA   |

- (1) VDDSHV stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see [Table 5-1](#), POWER column.

### 6.6.6 ADC12BT Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER  | TEST CONDITIONS                         | MIN  | TYP  | MAX                        | UNIT                     |
|--|---|--|--|----------------------------|--------------------------|
| <b>BALL NAMES in Mode 0:</b> MCU_ADC0_AIN[7:0]                     |   |  |  |                            |                          |
| <b>BALL NUMBERS:</b> J18 / H17 / K18 / J17 / M17 / K17 / L18 / L17 |   |  |  |                            |                          |
| V <sub>MCU_ADC0_AIN[7:0]</sub>                                     | Full-scale Input Range                  |  |  | VSS                        | VDDA <sup>(2)</sup><br>V |
| DNL  | Differential Non-Linearity              | -1   | 0.5  | 4                          | LSB                      |
| INL  | Integral Non-Linearity                  |  | ±1   | ±4                         | LSB                      |
| LSB <sub>GAIN-ERROR</sub>  | Gain Error                              |  | ±2   |                            | LSB                      |
| LSB <sub>OFFSET-ERROR</sub>  | Offset Error                            |  | ±2   |                            | LSB                      |
| C <sub>IN</sub>  | Input Sampling Capacitance              |  | 5.5  |                            | pF                       |
| SNR  | Signal-to-Noise Ratio                   | Input Signal: 200 kHz sine wave<br>at -0.5 dB Full Scale | 70   |                            | dB                       |
| THD  | Total Harmonic Distortion               | Input Signal: 200 kHz sine wave<br>at -0.5 dB Full Scale | 75   |                            | dB                       |
| SFDR   | Spurious Free Dynamic Range             | Input Signal: 200 kHz sine wave<br>at -0.5 dB Full Scale | 80   |                            | dB                       |
| SNR <sub>(PLUS)</sub>  | Signal-to-Noise Plus Distortion         | Input Signal: 200 kHz sine wave<br>at -0.5 dB Full Scale | 69   |                            | dB                       |
| R <sub>MCU_ADC0_AIN[0:7]</sub>                                     | Input Impedance of<br>MCU_ADC0_AIN[7:0] | f = input frequency                                      | [1/((65.97 × 10 <sup>-12</sup> ) ×<br>f <sub>SMPL_CLK</sub> )] |                            | Ω                        |
| I <sub>IN</sub>  | Input Leakage                           | MCU_ADC0_AIN[7:0] = VSS                                  |  | 5                          | μA                       |
|  |   | MCU_ADC0_AIN[7:0] =<br>VDDA_ADC_MCU                      |  | 10                         | μA                       |
| <b>Sampling Dynamics</b>   |   |  |  |                            |                          |
| F <sub>SMPL_CLK</sub>  | SMPL_CLK Frequency                      |  | 60   |                            | MHz                      |
| t <sub>C</sub>   | Conversion Time                         |  | 13   |                            | ADC0 SMPL_CLK<br>Cycles  |
| t <sub>ACQ</sub>   | Acquisition time                        |  | 2  | 257                        | ADC0 SMPL_CLK<br>Cycles  |
| T <sub>R</sub>   | Sampling Rate                           | ADC0 SMPL_CLK = 60 MHz                                   |  | 4                          | MSPS                     |
| CCISO  | Channel to Channel Isolation            |  | 100  |                            | dB                       |
| <b>General Purpose Input Mode<sup>(1)</sup></b>                    |   |  |  |                            |                          |
| V <sub>IL</sub>  | Input Low Voltage                       |  |  | 0.35 × VDDA <sup>(2)</sup> | V                        |
| V <sub>ILSS</sub>  | Input Low Voltage Steady State          |  |  | 0.35 × VDDA <sup>(2)</sup> | V                        |
| V <sub>IH</sub>  | Input High Voltage                      |  | 0.65 × VDDA <sup>(2)</sup>                                     |                            | V                        |

over recommended operating conditions (unless otherwise noted)

| PARAMETER         |                                 | TEST CONDITIONS               | MIN                                    | TYP | MAX | UNIT |
|-------------------|---------------------------------|-------------------------------|--|-----|-----|------|
| V <sub>IHSS</sub> | Input High Voltage Steady State |                               | 0.65 × V <sub>DDA</sub> <sup>(2)</sup> |     |     | V    |
| V <sub>HYS</sub>  | Input Hysteresis Voltage        |                               | 200                                    |     |     | mV   |
| I <sub>I</sub>    | Input Leakage Current           | V <sub>I</sub> = 1.8 V or 0 V |  |     | 2   | μA   |

- (1) MCU\_ADC0 can be configured to operate in General Purpose Input mode, where all MCU\_ADC0\_AIN[7:0] inputs are globally enabled to operate as digital inputs via the ADC0\_CTRL register (gpi\_mode\_en = 1).
- (2) V<sub>DDA</sub> stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see [Table 5-1](#), POWER column.

### 6.6.7 LVCMOS Electrical Characteristics

Over recommended operating conditions (unless otherwise noted)

| PARAMETER                          |                                 | TEST CONDITIONS               | MIN                       | TYP                       | MAX  | UNIT |
|------------------------------------|---------------------------------|-------------------------------|---------------------------|---------------------------|------|------|
| <b>BALL NAMES:</b> ALL other IOs   |                                 |                               |                           |                           |      |      |
| <b>BALL NUMBERS:</b> ALL other IOs |                                 |                               |                           |                           |      |      |
| <b>1.8-V MODE</b>                  |                                 |                               |                           |                           |      |      |
| V <sub>IL</sub>                    | Input Low Voltage               |                               |                           | 0.35 × VDD <sup>(1)</sup> |      | V    |
| V <sub>ILSS</sub>                  | Input Low Voltage Steady State  |                               |                           | 0.3 × VDD <sup>(1)</sup>  |      | V    |
| V <sub>IH</sub>                    | Input High Voltage              |                               | 0.65 × VDD <sup>(1)</sup> |                           |      | V    |
| V <sub>IHSS</sub>                  | Input High Voltage Steady State |                               | 0.85 × VDD <sup>(1)</sup> |                           |      | V    |
| V <sub>HYS</sub>                   | Input Hysteresis Voltage        |                               | 150                       |                           |      | mV   |
| I <sub>IN</sub>                    | Input Leakage Current.          | V <sub>I</sub> = 1.8 V or 0 V |                           |                           | ±10  | μA   |
| R <sub>PU</sub>                    | Pull-up Resistor                |                               | 15                        | 22                        | 30   | kΩ   |
| R <sub>PD</sub>                    | Pull-down Resistor              |                               | 15                        | 22                        | 30   | kΩ   |
| V <sub>OL</sub>                    | Output Low Voltage              |                               |                           |                           | 0.45 | V    |
| V <sub>OH</sub>                    | Output High Voltage             |                               | VDD <sup>(1)</sup> - 0.45 |                           |      | V    |
| I <sub>OL</sub>                    | Low Level Output Current        | V <sub>OL(MAX)</sub>          | 3                         |                           |      | mA   |
| I <sub>OH</sub>                    | High Level Output Current       | V <sub>OH(MIN)</sub>          | 3                         |                           |      | mA   |
| <b>3.3-V MODE</b>                  |                                 |                               |                           |                           |      |      |
| V <sub>IL</sub>                    | Input Low Voltage               |                               |                           |                           | 0.8  | V    |
| V <sub>ILSS</sub>                  | Input Low Voltage Steady State  |                               |                           |                           | 0.6  | V    |
| V <sub>IH</sub>                    | Input High Voltage              |                               | 2.0                       |                           |      | V    |
| V <sub>IHSS</sub>                  | Input High Voltage Steady State |                               | 2.0                       |                           |      | V    |
| V <sub>HYS</sub>                   | Input Hysteresis Voltage        |                               | 150                       |                           |      | mV   |
| I <sub>IN</sub>                    | Input Leakage Current.          | V <sub>I</sub> = 3.3 V or 0 V |                           |                           | ±10  | μA   |
| R <sub>PD</sub>                    | Pull-down Resistor              |                               | 15                        | 22                        | 30   | kΩ   |
| V <sub>OL</sub>                    | Output Low Voltage              |                               |                           |                           | 0.4  | V    |
| V <sub>OH</sub>                    | Output High Voltage             |                               | 2.4                       |                           |      | V    |
| I <sub>OL</sub>                    | Low Level Output Current        | V <sub>OL(MAX)</sub>          | 5                         |                           |      | mA   |
| I <sub>OH</sub>                    | High Level Output Current       | V <sub>OH(MIN)</sub>          | 6                         |                           |      | mA   |

(1) VDDSHV stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see [Table 5-1](#), POWER column.

### 6.6.8 USB2PHY Electrical Characteristics

#### Note

USB0 Electrical Characteristics are compliant with Universal Serial Bus Revision 2.0 Specification dated April 27, 2000 including ECNs and Errata as applicable.

### 6.6.9 SERDES Electrical Characteristics

#### Note

The PCIe interfaces are compliant with the electrical parameters specified in PCI Express® Base Specification Revision 4.0, September 27, 2017.

This Device imposes an additional limit on SERDES REFCLK when used in Input mode with internal termination enabled, as described by parameter  $V_{REFCLK\_TERM}$  in [Table 6-3, SERDES REFCLK Electrical Characteristics](#). Internal termination is enabled by default and must be disabled before applying a reference clock signal that exceeds the limits defined by  $V_{REFCLK\_TERM}$ . External termination should always be enabled on the source side.

**Table 6-3. SERDES REFCLK Electrical Characteristics**

Only applies when internal termination is enabled. Over recommended operating conditions (unless otherwise noted)

| PARAMETER   |  | MIN | TYP | MAX  | UNIT     |
|---|--|-----|-----|------|----------|
| <b>BALL NAMES in Mode 0:</b> SERDES0_REFCLK_P, SERDES0_REFCLK_N |  |     |     |      |          |
| <b>BALL NUMBERS:</b> AA9 / AA8                                  |  |     |     |      |          |
| $V_{REFCLK\_TERM}$  | Single ended voltage threshold at the reference clock pin when internal termination is enabled |     |     | 400  | mV       |
| $R_{TERM}$  | Internal termination   | 40  | 50  | 62.5 | $\Omega$ |

#### Note

The SerDes USB interface is compliant with the USB3.1 SuperSpeed Transmitter and Receiver Normative Electrical Parameters as defined in the Universal Serial Bus 3.1 Specification, Revision 1.0, July 26, 2013.

#### Note

The SGMII interfaces electrical characteristics are compliant with 1000BASE-KX per IEEE802.3 Clause 70.

#### Note

The SGMII 2.5G / XAUI interfaces electrical characteristics are compliant with IEEE802.3 Clause 47.

#### Note

The QSGMII interface electrical characteristics are compliant with QSGMII Specification revision 1.2.

#### Note

USXGMII supports IEEE 802.3 TX and RX electrical characteristics of Clause 72-7 and Annex 69B. It does not support 10GBase-KR auto-negotiation (Clause 73) and link training (Clause 72).

IEEE 802.3 Tables 72-7 and 72-8 are not required by USXGMII since these tables are associated with training (Clause 72-6), which is not a requirement of USXGMII.

The pre, main, and post cursors should be set by using BER sweeps.

**Note**

The XFI interface electrical characteristics are compliant with the INF-8077\_XFP\_XFI\_10Gbps\_1X specification revision 4.5, August 31, 2005.

**6.6.10 DDR Electrical Characteristics****Note**

The DDR interface is compatible with JEDEC JESD209-4B standards compliant LPDDR4 SDRAM devices.

**6.7 VPP Specifications for One-Time Programmable (OTP) eFuses**

This section specifies the operating conditions required for programming the OTP eFuses and is applicable only for High-Security Devices.

**6.7.1 Recommended Operating Conditions for OTP eFuse Programming**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER           | DESCRIPTION   | MIN                             | NOM | MAX    | UNIT |
|---------------------|---|---------------------------------|-----|--------|------|
| VDD_CORE            | Supply voltage range for the core domain during OTP operation                       | See <a href="#">Section 6.3</a> |     |        | V    |
| VDD_MCU             | Supply voltage range for the core domain during OTP operation                       | See <a href="#">Section 6.3</a> |     |        | V    |
| VPP_CORE            | Supply voltage range for the eFuse ROM domain during normal operation               | N/A                             |     |        |      |
|                     | Supply voltage range for the eFuse ROM domain during OTP programming <sup>(1)</sup> | 1.71                            | 1.8 | 1.89   | V    |
| VPP_MCU             | Supply voltage range for the eFuse ROM domain during normal operation               | N/A                             |     |        |      |
|                     | Supply voltage range for the eFuse ROM domain during OTP programming <sup>(1)</sup> | 1.71                            | 1.8 | 1.89   | V    |
| SR <sub>(VPP)</sub> | VPP Slew Rate   |                                 |     | 6E + 4 | V/s  |

(1) Supply voltage range includes DC errors and peak-to-peak noise. TI power management solutions [TLV70718](#) from the TLV707x family is a example device that meets the supply voltage range needed for VPP\_CORE and VPP\_MCU.

**6.7.2 Hardware Requirements**

The following hardware requirements must be met when programming keys in the OTP eFuses:

- The VPP\_CORE and VPP\_MCU power supplies must be disabled when not programming OTP registers.
- The VPP\_CORE and VPP\_MCU power supplies must be ramped up after the proper device power-up sequence (for more details, see [Section 6.10.2](#)).

**6.7.3 Programming Sequence**

Programming sequence for OTP eFuses:

- Power on the board per the power-up sequencing. No voltage should be applied on the VPP\_CORE and VPP\_MCU terminals during power up and normal operation.
- Load the OTP write software required to program the eFuse (contact your local TI representative for the OTP software package).
- Apply the voltage on the VPP\_CORE and VPP\_MCU terminals according to the specification in [Section 6.7.1](#).
- Run the software that programs the OTP registers.
- After validating the content of the OTP registers, remove the voltage from the VPP\_CORE and VPP\_MCU terminals.

### 6.7.4 Impact to Your Hardware Warranty

You recognize and accept at your own risk that your use of eFuse permanently alters the TI device. You acknowledge that eFuse can fail due to incorrect operating conditions or programming sequence. Such a failure may render the TI device inoperable and TI will be unable to confirm the TI device conformed to TI device specifications prior to the attempted eFuse. Consequently, TI will have no liability (*warranty or otherwise*) for any TI devices that have been incorrectly eFused by customers.

## 6.8 Thermal Resistance Characteristics

This section provides the thermal resistance characteristics used on this device.

For reliability and operability concerns, the maximum junction temperature of the device has to be at or below the  $T_J$  value identified in [Section 6.3, Recommended Operating Conditions](#).

### 6.8.1 Thermal Resistance Characteristics

It is recommended to perform thermal simulations at the system level with the worst case device power consumption.

| NO. | PARAMETER       | DESCRIPTION             | ALM PACKAGE             |                               |
|-----|-----------------|-------------------------|-------------------------|-------------------------------|
|     |                 |                         | °C/W <sup>(1) (3)</sup> | AIR FLOW (m/s) <sup>(2)</sup> |
| T1  | $R_{\theta JC}$ | Junction-to-case        | 0.54                    | N/A                           |
| T2  | $R_{\theta JB}$ | Junction-to-board       | 2.9                     | N/A                           |
| T3  | $R_{\theta JA}$ | Junction-to-free air    | 12.8                    | 0                             |
| T4  |                 | Junction-to-moving air  | 9.1                     | 1                             |
| T5  |                 |                         | 8.1                     | 2                             |
| T6  |                 |                         | 7.5                     | 3                             |
| T7  | $\Psi_{JT}$     | Junction-to-package top | 0.5                     | 0                             |
| T8  |                 |                         | 0.3                     | 1                             |
| T9  |                 |                         | 0.3                     | 2                             |
| T10 |                 |                         | 0.3                     | 3                             |
| T11 | $\Psi_{JB}$     | Junction-to-board       | 2.8                     | 0                             |
| T12 |                 |                         | 2.8                     | 1                             |
| T13 |                 |                         | 2.7                     | 2                             |
| T14 |                 |                         | 2.7                     | 3                             |

(1) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [ $R_{\theta JC}$ ] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Packages*

(2) m/s = meters per second.

(3) °C/W = degrees Celsius per watt.

## 6.9 Temperature Sensor Characteristics

This section summarizes the Voltage and Temperature Module (VTM) on die temperature sensor characteristics.

For reliability and operability concerns, the maximum junction temperature of the device has to be at or below the  $T_J$  value identified in the *Recommended Operating Conditions*.

**Table 6-4. VTM Die Temperature sensor Characteristics**

| PARAMETER        |                                 | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|---------------------------------|-----------------|-----|-----|-----|------|
| T <sub>acc</sub> | VTM temperature sensor accuracy | -40 to 110 °C   | -5  |     | 5   | °C   |
|                  |                                 | 110 to 125 °C   | -2  |     | 2   | °C   |

## 6.10 Timing and Switching Characteristics

### Note

The timings presented in this section are valid when the DRV\_STR (Drive Strength) control in the associated PADCONFIG registers are set to the default “0h – Nominal (recommended)” value.

### 6.10.1 Timing Parameters and Information

The timing parameter symbols used in [Section 6.10](#) are created in accordance with JEDEC Standard 100. To shorten the symbols, some pin names and other related terminologies have been abbreviated in [Table 6-5](#):

**Table 6-5. Timing Parameters Subscripts**

| SYMBOL | PARAMETER                              |
|--------|--|
| c      | Cycle time (period)                    |
| d      | Delay time                             |
| dis    | Disable time                           |
| en     | Enable time                            |
| h      | Hold time                              |
| su     | Setup time                             |
| START  | Start bit                              |
| t      | Transition time                        |
| v      | Valid time                             |
| w      | Pulse duration (width)                 |
| X      | Unknown, changing, or don't care level |
| F      | Fall time                              |
| H      | High                                   |
| L      | Low                                    |
| R      | Rise time                              |
| V      | Valid                                  |
| IV     | Invalid                                |
| AE     | Active Edge                            |
| FE     | First Edge                             |
| LE     | Last Edge                              |
| Z      | High impedance                         |

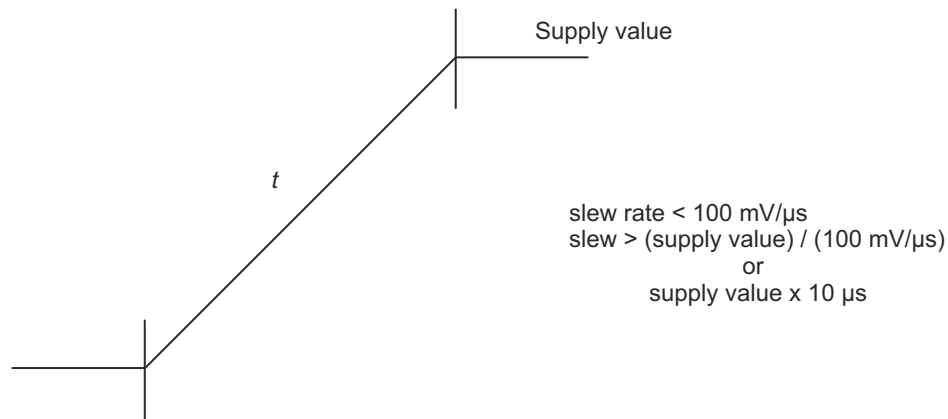
## 6.10.2 Power Supply Sequencing

This section describes power supply sequencing required to ensure proper device operation. The power supply names described in this section comprise a superset of a family of compatible devices. Some members of this family will not include a subset of these power supplies and their associated device modules.

### 6.10.2.1 Power Supply Slew Rate Requirement

To maintain the safe operating range of the internal ESD protection devices, TI recommends limiting the maximum slew rate of supplies to be less than 100 mV/ $\mu$ s. For instance, as shown in Figure 6-2, TI recommends having the supply ramp slew for a 1.8-V supply of more than 18  $\mu$ s.

Figure 6-2 describes the Power Supply Slew Rate Requirement in the device.

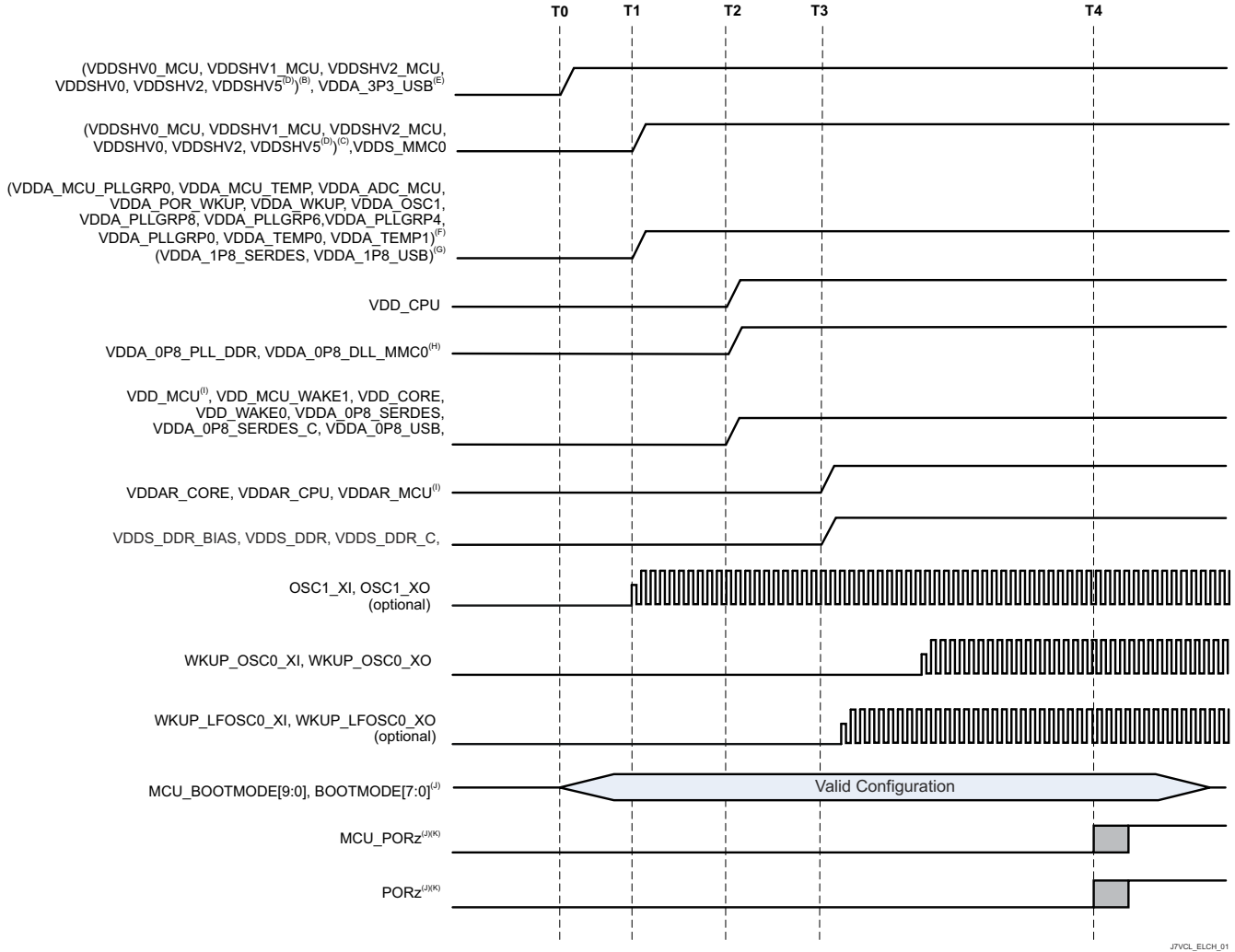


J7VC\_ELCH\_03

Figure 6-2. Power Supply Slew and Slew Rate

### 6.10.2.2 Combined MCU and Main Domains Power- Up Sequencing

Figure 6-3 describes the primary power-up sequencing when similar MCU and Main voltage domains are combined into common power rails. Combining MCU and Main voltage domains makes an SoC's MCU and Main processor sub-systems operational dependent on common power rails. The main reason an SoC's PDN design may want to group MCU and Main voltage domains is simplify the PDN by reducing total number of power rails and sources. This simplified PDN would be used in systems that do not desire independent MCU and Main processor sub-system operations.



#### A. Terminology:

- Primary = Essential power up sequence of all voltage domains to full active state.
- $V_{OPR\ MIN}$  = Minimum operational voltage level that ensures functionality as specified in , *Recommended Operating Conditions*.
- Ramp Up = Voltage supply transition time from off condition to  $V_{OPR\ MIN}$ .
- Domain\_“n” = multiple instances of similar voltage domains (that is, dual voltage IO domains, VDDSHVn = VDDSHV0, VDDSHV1, VDDSHV2 ... VDDSHV6)
- Domain\_“xxx” = different signal type/protocol domains using same voltage supply type and level (that is, VDDA\_1P8\_xx = VDDA\_1P8\_DSITX, VDDA\_1P8\_USB, VDDA\_0P8\_DSITX, VDDA\_0P8\_USB, etc.)

#### Time stamps:

Markers showing approximate elapsed times that are dependent upon PDN feature set, component selection and power mapping. Values shown are typical for PDNs combining MCU and Main voltage domains but could vary based upon PDN design.

Time Stamp definitions and (typical values for reference only):

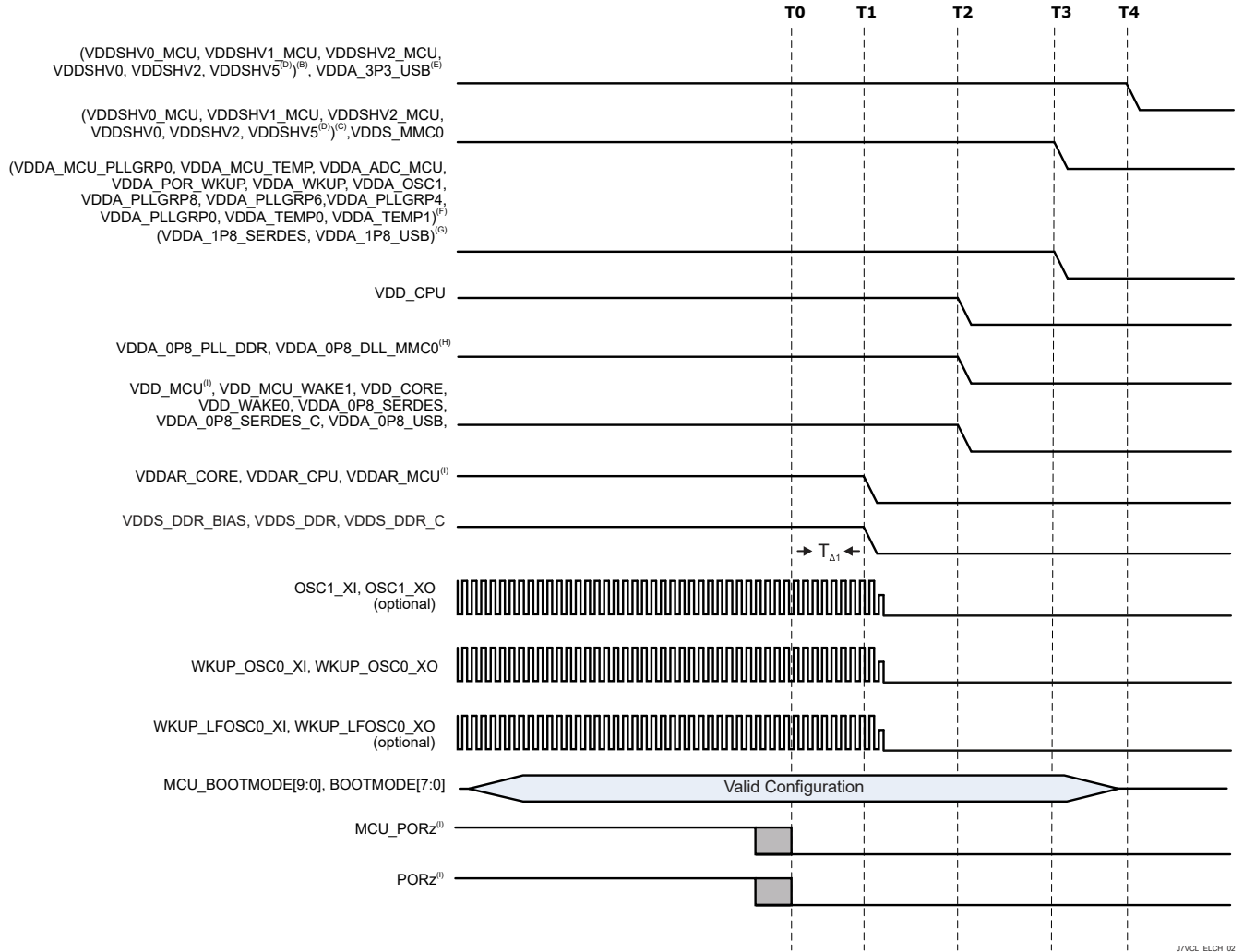
T0 – All 3.3-V voltages start supply ramp-up to  $V_{OPR\ MIN}$ . (0 ms)

- T1 – All 1.8-V voltages start supply ramp-up to  $V_{OPR\ MIN}$ . (0.5 ms)
- T2 – All core voltages start supply ramp-up to  $V_{OPR\ MIN}$ . (1.0 ms)
- T3 – All RAM array voltages start supply ramp-up to  $V_{OPR\ MIN}$ . (1.5 ms)
- T4 – OSC1 is stable and PORz/MCU\_PORz are de-asserted to release processor from reset. (11 ms)
- B. Any MCU or Main dual voltage IO domains (VDDSHVn\_MCU or VDDSHVn) being supplied by 3.3 V to support 3.3-V digital interfaces.
- C. Any MCU or Main dual voltage IO domains (VDDSHVn\_MCU or VDDSHVn) being supplied by 1.8 V to support 1.8-V digital interfaces.
- D. VDDSHV5 supports MMC1 signaling for SD memory cards. A dual voltage (3.3/1.8 V) power rail is required for compliant, high-speed SD card operations. If SD card is not needed or standard data rates with fixed 3.3-V operation is acceptable, then domain can be grouped with digital IO 3.3-V power rail. If a SD card is capable of operating with fixed 1.8 V, then domain can be grouped with digital IO 1.8-V power rail.
- E. VDDA\_3P3\_USB is 3.3-V analog domain used for USB 2.0 differential interface signaling. A low noise, analog supply is recommended to provide best signal integrity for USB data eye mask compliance. If USB interface is not needed or data bit errors can be tolerated, then domain can be grouped with 3.3-V digital IO power rail either directly or through a supply filter.
- F. VDDA\_1P8\_<clk/pll/ana> are 1.8-V analog domains supporting clock oscillator, PLL and analog circuitry needing a low noise supply for optimal performance. It is not recommended to combine digital VDDSHVn\_MCU and VDDSHVn IO domains since high frequency switching noise could negatively impact jitter performance of clock, PLL and DLL signals. Combining analog VDDA\_1p8\_<phy> domains should be avoided but if grouped, then in-line ferrite bead supply filtering is required.
- G. VDDA\_1P8\_<phy> are 1.8-V analog domains supporting multiple serial PHY interfaces. A low noise, analog supply is recommended to provide best signal integrity, interface performance and spec compliance. If any of these interfaces are not needed, data bit errors or non-compliant operation can be tolerated, then domains can be grouped with digital IO 1.8-V power rail either directly or through an in-line supply filter is allowed.
- H. VDDA\_0P8\_<dll/pll> are 0.8 V analog domains supporting PLL and DLL circuitry needing a low noise supply for optimal performance. It is not recommended to combine these domains with any other 0.8-V domains since high frequency switching noise could negatively impact jitter performance of PLL and DLL signals.
- I. VDD\_MCU is a digital voltage domain with a wide operational voltage range enabling it to be grouped either with VDDAR\_MCU domain or with VDD\_CORE; for the “Combined MCU and Main Domains Power-Up Sequencing,” VDD\_MCU can be grouped with VDD\_CORE, and VDDAR\_MCU can be grouped with VDDAR\_CPU and VDDAR\_CORE. If VDD\_MCU is grouped with VDD\_CORE, VDD\_MCU must be ramped-up from a common voltage resource with 0.8-V VDD\_CORE at T2. If VDD\_MCU is not grouped with VDD\_CORE, VDD\_MCU must be ramped-up before T2. In either case, the VDDAR supplies must be ramped at T3.
- J. Minimum set-up and hold times shown with respect to MCU\_PORz and PORz asserting high to latch MCU\_BOOTMODEn (referenced to MCU\_VDDSHV0) and BOOTMODEn (reference to VDDSHV2) settings into registers during power-up sequence.
- K. Minimum elapsed time from crystal oscillator circuitry being energized (VDDA\_OSC1 at T1) until stable clock frequency is reached depends upon on crystal oscillator, capacitor parameters and PCB parasitic values. A conservative 10- ms elapsed time defined by (T4 – T1) time stamps is shown. This could be reduced depending upon customer’s clock circuit (that is, crystal oscillator or clock generator) and PCB designs.

**Figure 6-3. Combined MCU and Main Domains, Primary Power-Up Sequence**

### 6.10.2.3 Combined MCU and Main Domains Power- Down Sequencing - Option 1

Figure 6-4 describes the device power-down sequencing for option 1.



#### A. Terminology:

- Primary = Essential power down sequence of all voltage domains to complete off state.
- $V_{OPR\ MIN}$  = Minimum operational voltage level that ensures functionality as specified in , *Recommended Operating Conditions*.
- Ramp-down = voltage supply transition time from  $V_{OPR\ MIN}$  to off condition.
- Domain\_“n” = multiple instances of similar voltage domains (that is, dual voltage IO domains, VDDSHVn = VDDSHV0, VDDSHV1, VDDSHV2 ... VDDSHV6)
- Domain\_“xxx” = different signal type/protocol domains using same voltage supply type and level (that is, VDDA\_1P8\_xx = VDDA\_1P8\_DSITX, VDDA\_1P8\_USB, VDDA\_0P8\_DSITX, VDDA\_0P8\_USB, etc.)

#### Time stamps:

Markers showing approximate elapsed times that are dependent upon PDN feature set, component selection and power mapping. Values shown are typical for PDNs combining MCU and Main voltage domains but could vary based upon PDN design.

Time Stamp definitions and (typical values for reference only):

- T0 – MCU\_PORz and PORz assert low to put all processor resources in safe state. (0ms)
- T1 – Main DDR, SRAM Core and SRAM CPU power domains start ramp-down. (0.5ms)
- T2 – All core voltages start supply ramp-down. (2.5ms)
- T3 – All 1.8V voltages start supply ramp-down. (3.0ms)
- T4 – All 3.3-V voltages start supply ramp-down. (3.5ms)

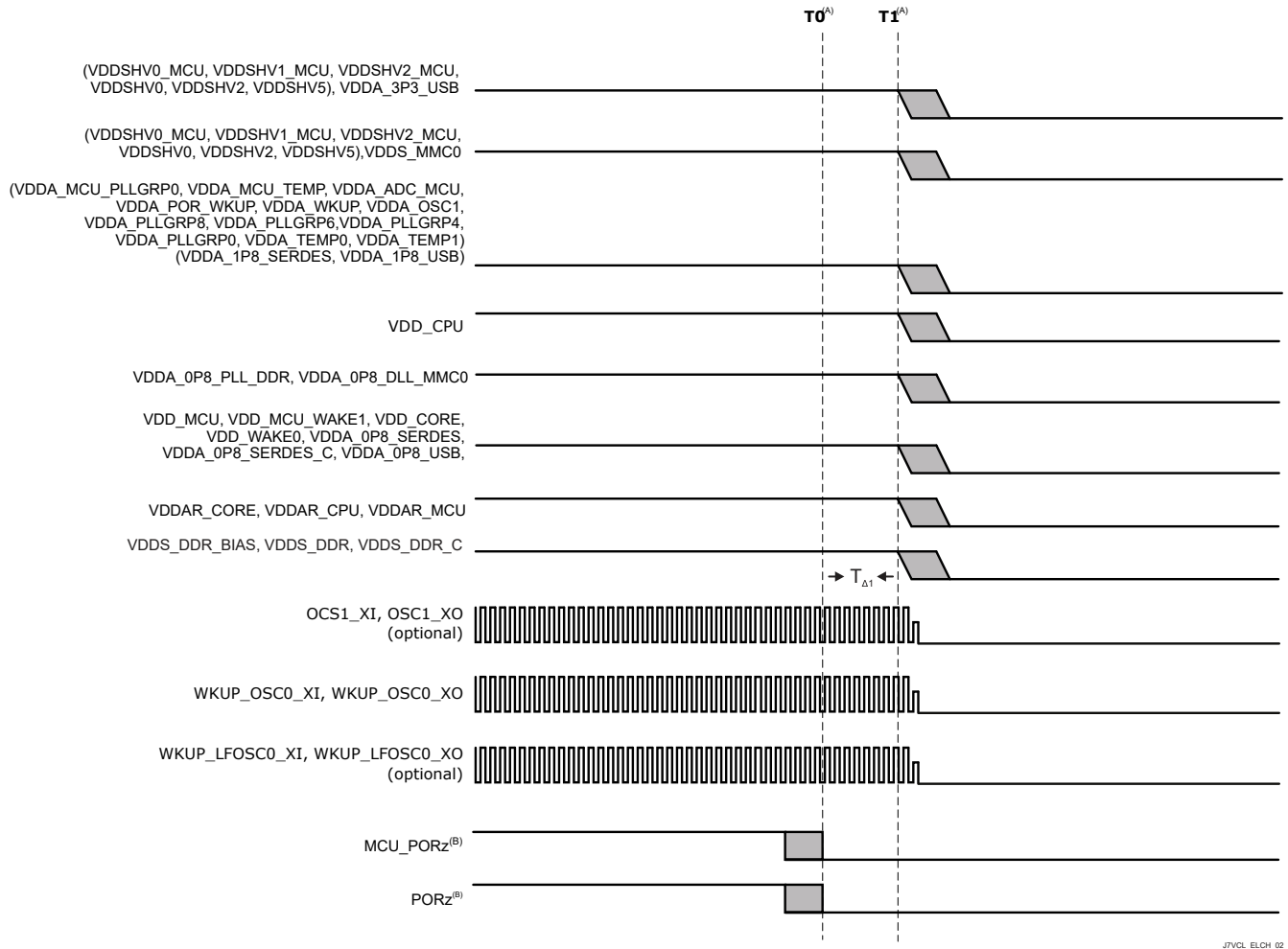
- B. Any MCU or Main dual voltage IO domains (VDDSHVn\_MCU or VDDSHVn) being supplied by 3.3V to support 3.3V digital interfaces.

- C. Any MCU or Main dual voltage IO domains (VDDSHVn\_MCU or VDDSHVn) being supplied by 1.8V to support 1.8V digital interfaces.
- D. VDDSHV5 supports MMC1 signaling for SD memory cards. A dual voltage (3.3/1.8V) power rail is required for compliant, high-speed SD card operations. If SD card is not needed or standard data rates with fixed 3.3V operation is acceptable, then domain can be grouped with digital IO 3.3V power rail. If a SD card is capable of operating with fixed 1.8V, then domain can be grouped with digital IO 1.8V power rail.
- E. VDDA\_3P3\_USB is 3.3V analog domain used for USB 2.0 differential interface signaling. A low noise, analog supply is recommended to provide best signal integrity for USB data eye mask compliance. If USB interface is not needed or data bit errors can be tolerated, then domain can be grouped with 3.3V digital IO power rail either directly or through a supply filter.
- F. VDDA\_1P8\_<clk/pll/ana> are 1.8-V analog domains supporting clock oscillator, PLL and analog circuitry needing a low noise supply for optimal performance. It is not recommended to combine digital VDDSHVn\_MCU and VDDSHVn IO domains since high frequency switching noise could negatively impact jitter performance of clock, PLL and DLL signals. Combining analog VDDA\_1p8\_<phy> domains should be avoided but if grouped, then in-line ferrite bead supply filtering is required.
- G. VDDA\_1P8\_<phy> are 1.8V analog domains supporting multiple serial PHY interfaces. A low noise, analog supply is recommended to provide best signal integrity, interface performance and spec compliance. If any of these interfaces are not needed, data bit errors or non-compliant operation can be tolerated, then domains can be grouped with digital IO 1.8-V power rail either directly or through an in-line supply filter is allowed.
- H. VDDA\_0P8\_<dll/pll> are 0.8V analog domains supporting PLL and DLL circuitry needing a low noise supply for optimal performance. It is not recommended to combine these domains with any other 0.8V domains since high frequency switching noise could negatively impact jitter performance of PLL and DLL signals.
- I. MCU\_PORz and PORz must be asserted low for  $T_{\Delta 1} = 200\mu\text{s}$  min to ensure SoC resources enter into safe state before any voltage begins to ramp down.

**Figure 6-4. Combined MCU and Main Domains, Primary Power-Down Sequence - Option 1**

### 6.10.2.4 Combined MCU and Main Domains Power- Down Sequencing - Option 2

Figure 6-5 describes the device power-down sequencing for option 2.



A. Time stamp markers:

T0 – MCU\_PORz and PORz assert low to put all processor resources in safe state. (0 ms)

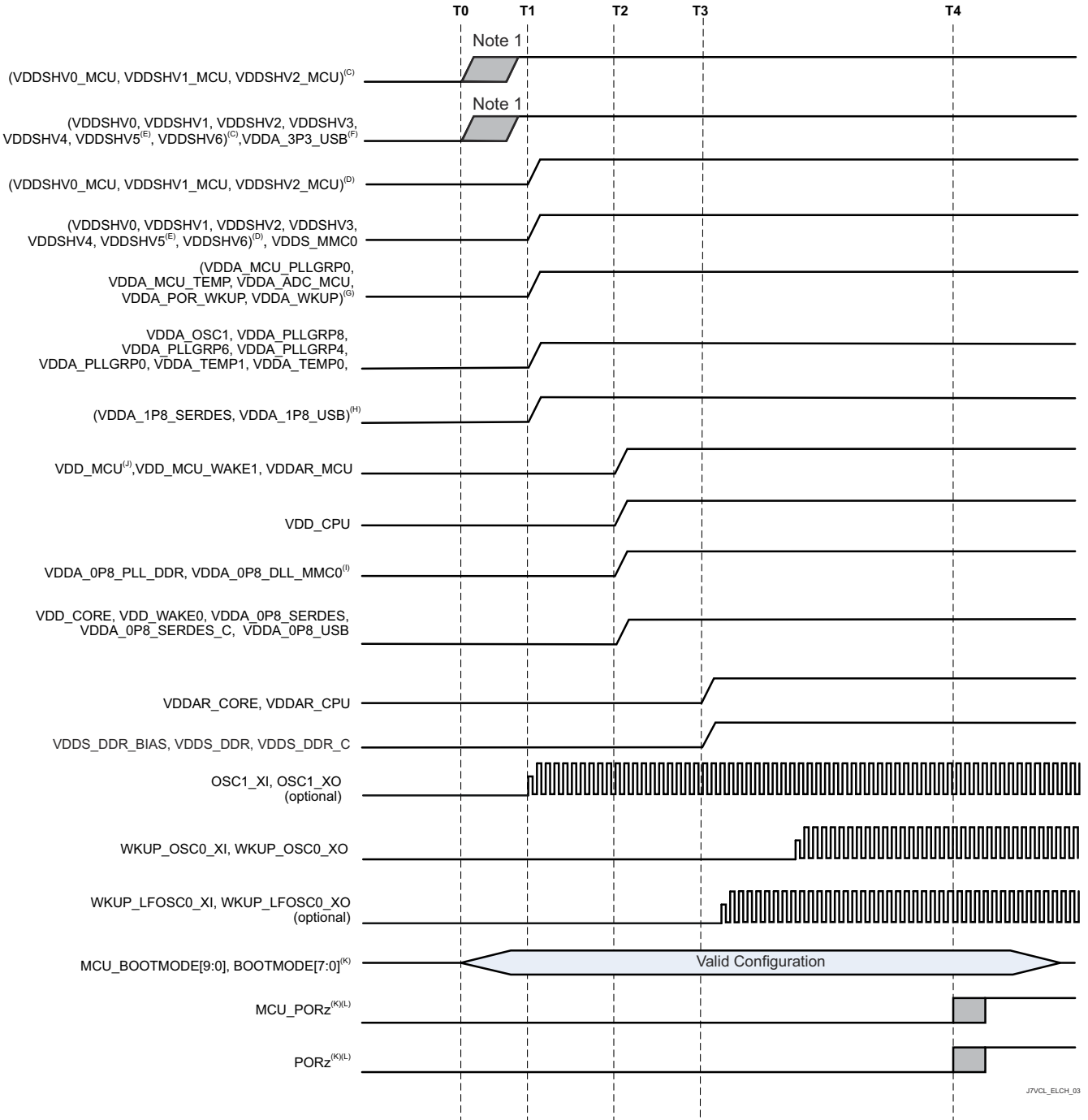
T1 – All power supplies start ramp-down. (1µs)

B. MCU\_PORz and PORz must be asserted low for  $T_{\Delta 1} = 200\mu s$  min to ensure SoC resources enter into safe state before any voltage begins to ramp down.

**Figure 6-5. Combined MCU and Main Domains, Primary Power-Down Sequence - Option 2**

#### 6.10.2.5 Independent MCU and Main Domains Power- Up Sequencing

Independent MCU and Main voltage domains enable an SoC's MCU and Main processor sub-systems to operate independently. There are 2 reasons an SoC's PDN design may need to support independent MCU and Main processor functionality. First is to provide flexibility to enable SoC low power modes that can significantly reduce SoC power dissipation when processor operations are not needed. Second is to enable robustness to gain freedom from interference (FFI) of a single fault impacting both MCU and Main processor sub-systems which is especially beneficial if using the SoC's MCU as the system safety monitoring processor. The number of additional PDN power rails needed is dependent upon number of different MCU IO signaling voltage levels. If only 1.8V IO signaling is used, the only 2 additional power rails could be required. If both 1.8 and 3.3V IO signaling is desired, then 4 additional power rails could be needed.



**A. Terminology:**

- Primary = Essential power up sequence of all voltage domains to full active state.
- $V_{OPR\ MIN}$  = Minimum operational voltage level that ensures functionality as specified in , *Recommended Operating Conditions*.
- Ramp Up = Voltage supply transition time from off condition to  $V_{OPR\ MIN}$ .
- Domain “n” = multiple instances of similar voltage domains (that is, dual voltage IO domains,  $VDDSHV_n = VDDSHV_0, VDDSHV_1, VDDSHV_2 \dots VDDSHV_6$ )
- Domain “xxx” = different signal type/protocol domains using same voltage supply type and level (that is,  $VDDA\_1P8\_xx = VDDA\_1P8\_DSITX, VDDA\_1P8\_USB, VDDA\_0P8\_DSITX, VDDA\_0P8\_USB, etc.$ )

Time stamp markers show approximate elapsed times that are dependent upon PDN feature set, component selection and power mapping. Values shown are typical for PDNs supporting independent MCU and Main voltage domains but could vary based upon PDN design.

Time Stamp definitions and (typical values for reference only):

T0 – All 3.3V voltages start supply ramp-up to  $V_{OPR\ MIN}$ . (0 ms)

T1 – All 1.8V voltages start supply ramp-up to  $V_{OPR\ MIN}$ . (2 ms)

T2 – All core voltages start supply ramp-up to  $V_{OPR\ MIN}$ . (3 ms)

T3 – All RAM array voltages start supply ramp-up to  $V_{OPR\ MIN}$ . (4 ms)

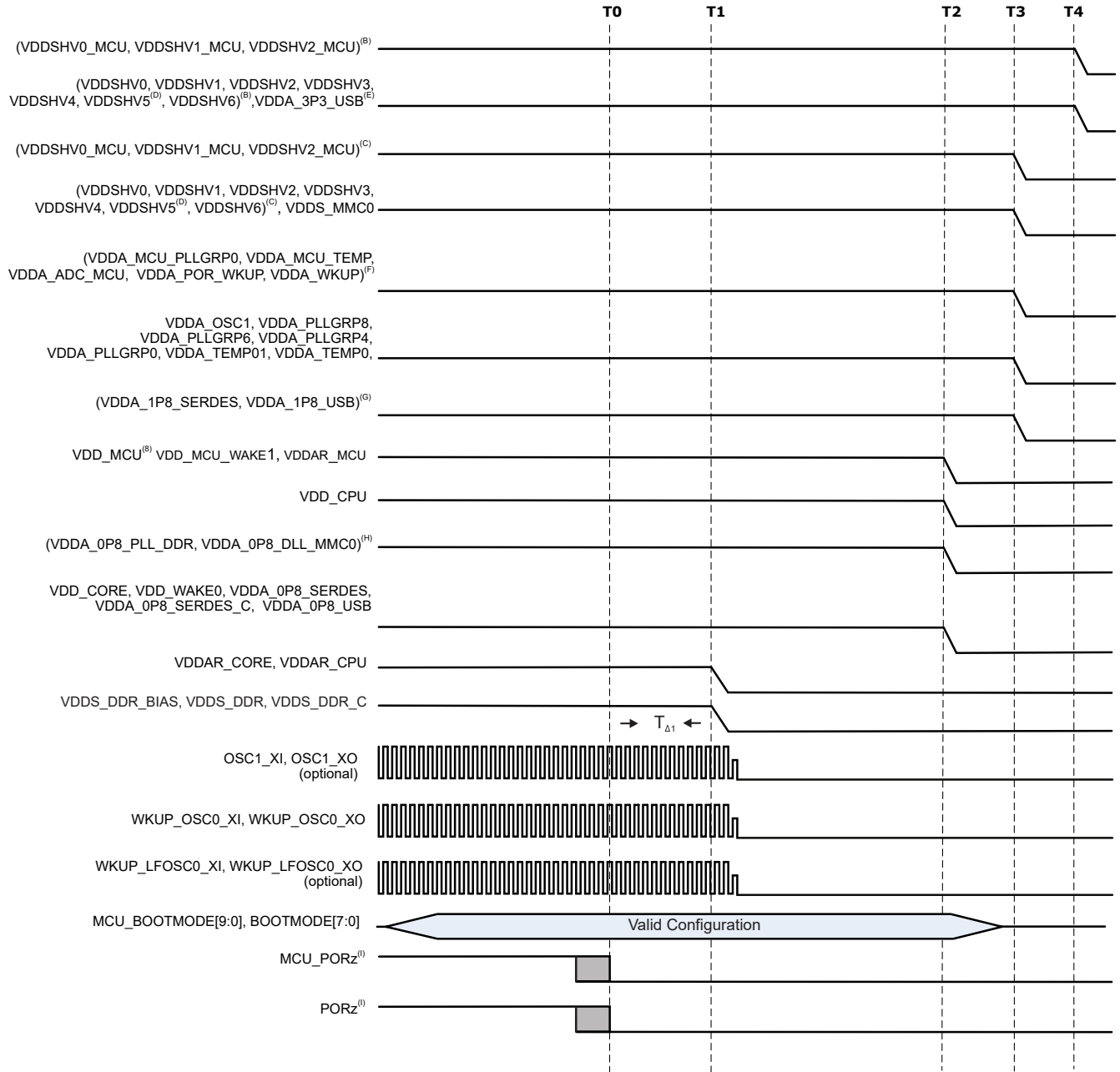
T4 – OSC1 is stable and PORz/MCU\_PORz are de-asserted to release processor from reset. (13 ms)

- B. VDDSHVx 3.3V IO domains may have additional ramp-up delay due to following:
1. Minimizing PMIC power dissipation during low power mode that includes disabling PMIC's VIO\_IN supply for GPIO output buffers.
  2. PDN component turn-on and ramp-up delays needed to isolate MCU and Main IO domains
- C. Any MCU or Main dual voltage IO domains (VDDSHVn\_MCU or VDDSHVn) being supplied by 3.3 V to support 3.3-V digital interfaces.
- D. Any MCU or Main dual voltage IO domains (VDDSHVn\_MCU or VDDSHVn) being supplied by 1.8 V to support 1.8-V digital interfaces.
- E. VDDSHV5 supports MMC1 signaling for SD memory cards. A dual voltage (3.3/1.8 V) power rail is required for compliant, high-speed SD card operations. If SD card is not needed or standard data rates with fixed 3.3 V operation is acceptable, then domain can be grouped with digital IO 3.3-V power rail. If a SD card is capable of operating with fixed 1.8 V, then domain can be grouped with digital IO 1.8-V power rail.
- F. VDDA\_3P3\_USB is 3.3-V analog domain used for USB 2.0 differential interface signaling. A low noise, analog supply is recommended to provide best signal integrity for USB data eye mask compliance. If USB interface is not needed or data bit errors can be tolerated, then domain can be grouped with 3.3-V digital IO power rail either directly or through a supply filter.
- G. VDDA\_1P8\_<clk/pll/ana> are 1.8-V analog domains supporting clock oscillator, PLL and analog circuitry needing a low noise supply for optimal performance. It is not recommended to combine digital VDDSHVn\_MCU and VDDSHVn IO domains since high frequency switching noise could negatively impact jitter performance of clock, PLL and DLL signals. Combining analog VDDA\_1p8\_<phy> domains should be avoided but if grouped, then in-line ferrite bead supply filtering is required.
- H. VDDA\_1P8\_<phy> are 1.8-V analog domains supporting multiple serial PHY interfaces. A low noise, analog supply is recommended to provide best signal integrity, interface performance and spec compliance. If any of these interfaces are not needed, data bit errors or non-compliant operation can be tolerated, then domains can be grouped with digital IO 1.8-V power rail either directly or through an in-line supply filter is allowed.
- I. VDDA\_0P8\_<dll/pll> are 0.8-V analog domains supporting PLL and DLL circuitry needing a low noise supply for optimal performance. It is not recommended to combine these domains with any other 0.8-V domains since high frequency switching noise could negatively impact jitter performance of PLL and DLL signals.
- J. VDD\_MCU is a digital voltage domain with a wide operational voltage range enabling it to be grouped either with VDDAR\_MCU domain or with VDD\_CORE; for the "Isolated MCU and Main Domains Power-Up Sequencing," VDD\_MCU can be grouped with VDDAR\_MCU; VDD\_MCU must be ramped-up before T2. If VDDAR\_MCU is not grouped with VDD\_MCU, it must be ramped at T3.
- K. Minimum set-up and hold times shown with respect to MCU\_PORz and PORz asserting high to latch MCU\_BOOTMODEn (referenced to MCU\_VDDSHV0) and BOOTMODEn (reference to VDDSHV2) settings into registers during power up sequence.
- L. Minimum elapsed time from crystal oscillator circuitry being energized (VDDA\_OSC1 at T1) until stable clock frequency is reached depends upon on crystal oscillator, capacitor parameters and PCB parasitic values. A conservative 10-ms elapsed time defined by (T4 – T1) time stamps is shown. This could be reduced depending upon customer's clock circuit (that is, crystal oscillator or clock generator) and PCB designs.

**Figure 6-6. Independent MCU and Main Domains, Primary Power-Up Sequence**

### 6.10.2.6 Independent MCU and Main Domains Power- Down Sequencing - Option 1

Figure 6-7 describes the device power-down sequencing for option 1.



J7VCL\_ELCH\_04

#### A. Terminology:

- Primary = Essential power down sequence of all voltage domains to complete off state.
- $V_{OPR\ MIN}$  = Minimum operational voltage level that ensures functionality as specified in , *Recommended Operating Conditions*.
- Ramp-down = voltage supply transition time from  $V_{OPR\ MIN}$  to off condition.
- Domain\_“n” = multiple instances of similar voltage domains (that is, dual voltage IO domains, VDDSHVn = VDDSHV0, VDDSHV1, VDDSHV2 ... VDDSHV6)
- Domain\_“xxx” = different signal type/protocol domains using same voltage supply type and level (that is, VDDA\_1P8\_xx = VDDA\_1P8\_DSITX, VDDA\_1P8\_USB, VDDA\_0P8\_DSITX, VDDA\_0P8\_USB, etc.)

Time stamps:

Markers showing approximate elapsed times that are dependent upon PDN feature set, component selection and power mapping. Values shown are typical for PDNs combining MCU and Main voltage domains but could vary based upon PDN design.

Time Stamp definitions and (typical values for reference only):

T0 – MCU\_PORz and PORz assert low to put all processor resources in safe state. (0ms)

T1 – Main DDR, SRAM Core and SRAM CPU power domains start ramp-down. (0.5ms)

T2 – All core voltages start supply ramp-down. (2.5ms)

T3 – All 1.8V voltages start supply ramp-down. (3.0ms)

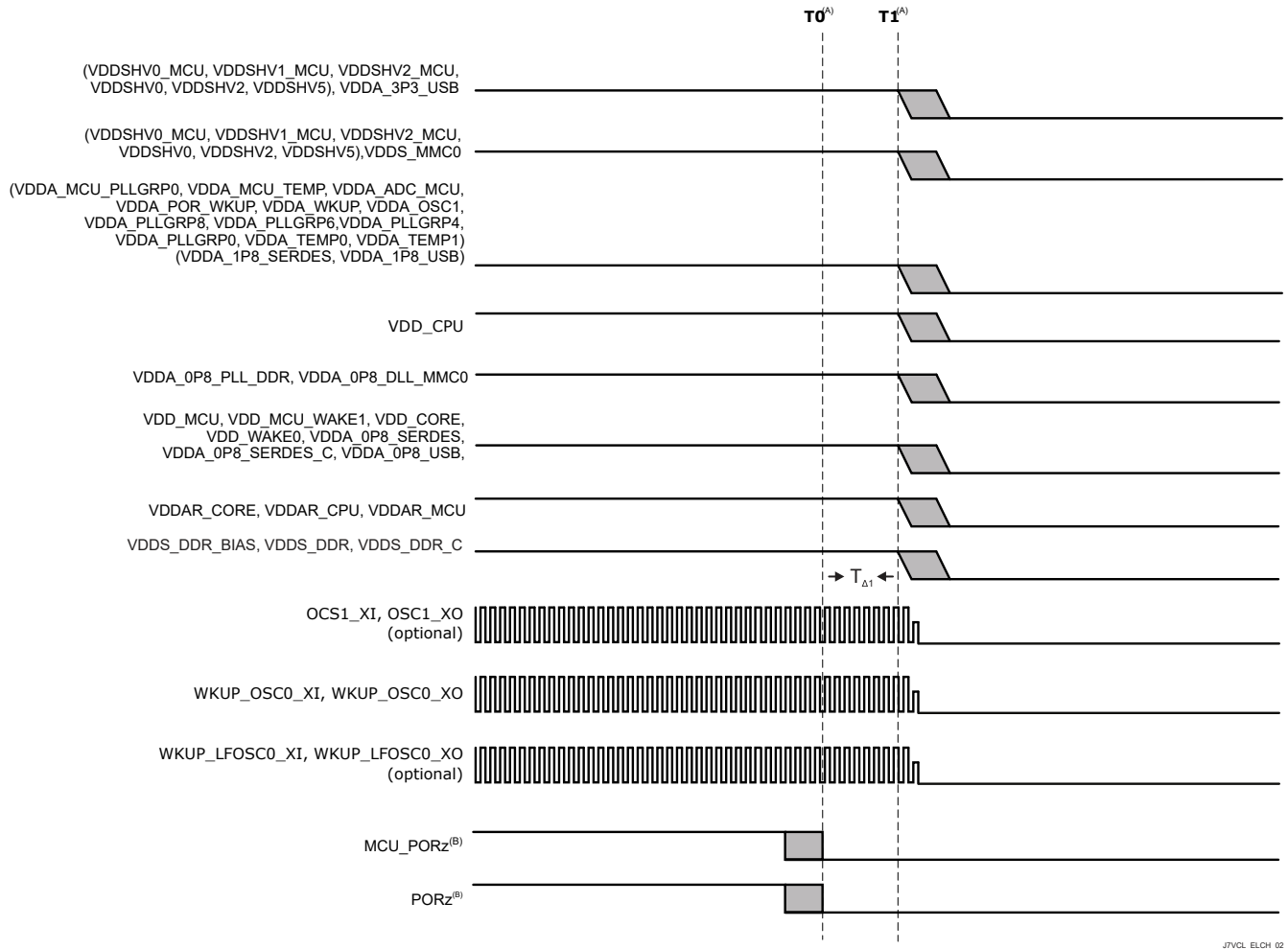
T4 – All 3.3-V voltages start supply ramp-down. (3.5ms)

- B. Any MCU or Main dual voltage IO domains (VDDSHVn\_MCU or VDDSHVn) being supplied by 3.3V to support 3.3V digital interfaces.
- C. Any MCU or Main dual voltage IO domains (VDDSHVn\_MCU or VDDSHVn) being supplied by 1.8V to support 1.8V digital interfaces.
- D. VDDSHV5 supports MMC1 signaling for SD memory cards. A dual voltage (3.3/1.8V) power rail is required for compliant, high-speed SD card operations. If SD card is not needed or standard data rates with fixed 3.3V operation is acceptable, then domain can be grouped with digital IO 3.3V power rail. If a SD card is capable of operating with fixed 1.8V, then domain can be grouped with digital IO 1.8V power rail.
- E. VDDA\_3P3\_USB is 3.3V analog domain used for USB 2.0 differential interface signaling. A low noise, analog supply is recommended to provide best signal integrity for USB data eye mask compliance. If USB interface is not needed or data bit errors can be tolerated, then domain can be grouped with 3.3V digital IO power rail either directly or through a supply filter.
- F. VDDA\_1P8\_<clk/pll/ana> are 1.8V analog domains supporting clock oscillator, PLL and analog circuitry needing a low noise supply for optimal performance. It is not recommended to combine digital VDDSHVn\_MCU and VDDSHVn IO domains since high frequency switching noise could negatively impact jitter performance of clock, PLL and DLL signals. Combining analog VDDA\_1p8\_<phy> domains should be avoided but if grouped, then in-line ferrite bead supply filtering is required.
- G. VDDA\_1P8\_<phy> are 1.8V analog domains supporting multiple serial PHY interfaces. A low noise, analog supply is recommended to provide best signal integrity, interface performance and spec compliance. If any of these interfaces are not needed, data bit errors or non-compliant operation can be tolerated, then domains can be grouped with digital IO 1.8V power rail either directly or through an in-line supply filter is allowed.
- H. VDDA\_0P8\_<dll/pll> are 0.8V analog domains supporting PLL and DLL circuitry needing a low noise supply for optimal performance. It is not recommended to combine these domains with any other 0.8V domains since high frequency switching noise could negatively impact jitter performance of PLL and DLL signals.
- I. MCU\_PORz and PORz must be asserted low for  $T_{\Delta 1} = 200\mu\text{s}$  min to ensure SoC resources enter into safe state before any voltage begins to ramp down.

**Figure 6-7. Independent MCU and Main Domains, Primary Power- Down Sequencing - Option 1**

### 6.10.2.7 Independent MCU and Main Domains Power- Down Sequencing - Option 2

Figure 6-8 describes the device power-down sequencing for option 2.

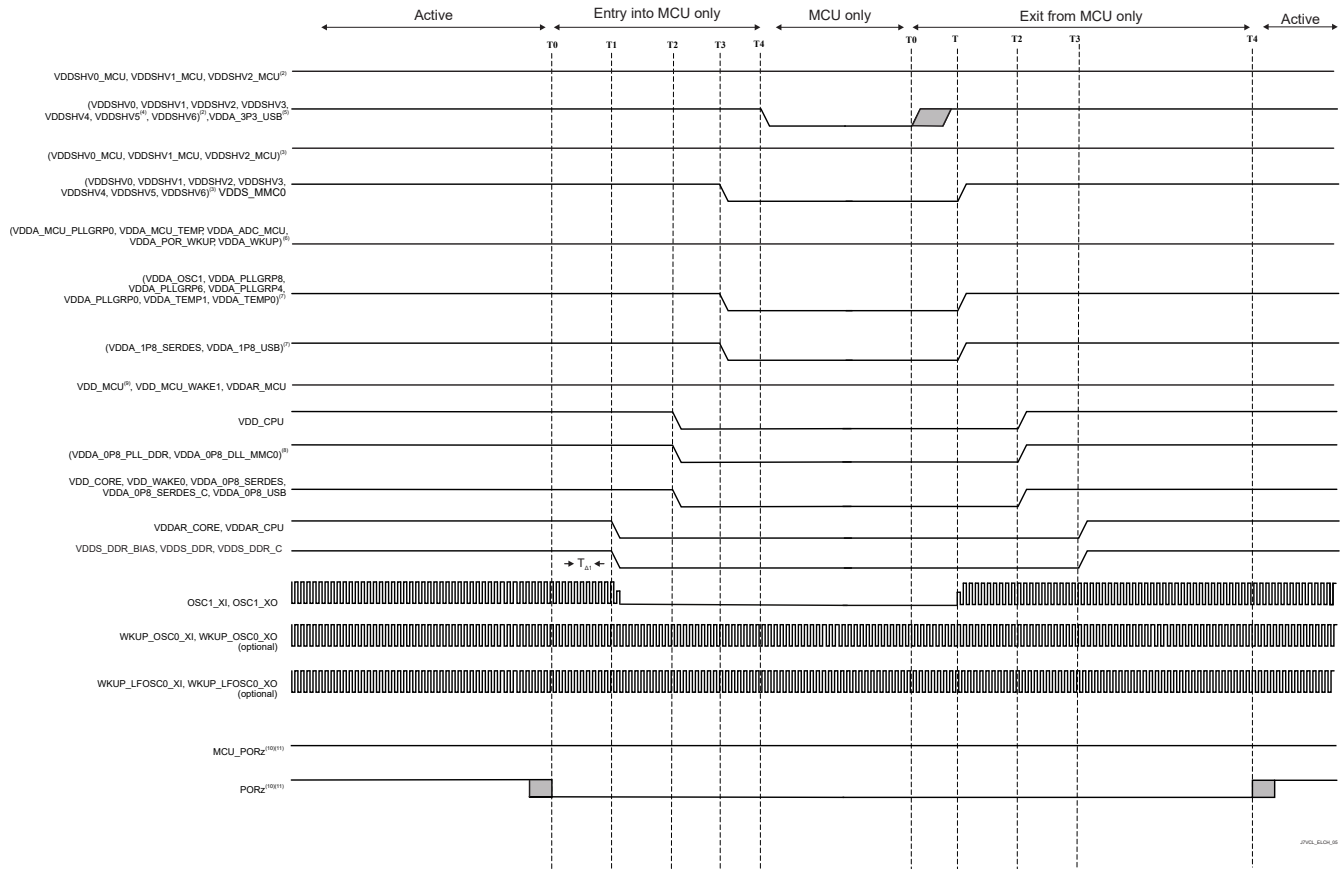


- A. Time stamp markers:  
 T0 – MCU\_PORz and PORz assert low to put all processor resources in safe state. (0ms)  
 T1 – All power supplies start ramp-down. (1μs)
- B. MCU\_PORz and PORz must be asserted low for  $T_{\Delta 1} = 200\mu s$  min to ensure SoC resources enter into safe state before any voltage begins to ramp down.

**Figure 6-8. Independent MCU and Main Domains, Primary Power- Down Sequencing - Option 2**

### 6.10.2.8 Independent MCU and Main Domains, Entry and Exit of MCU Only Sequencing

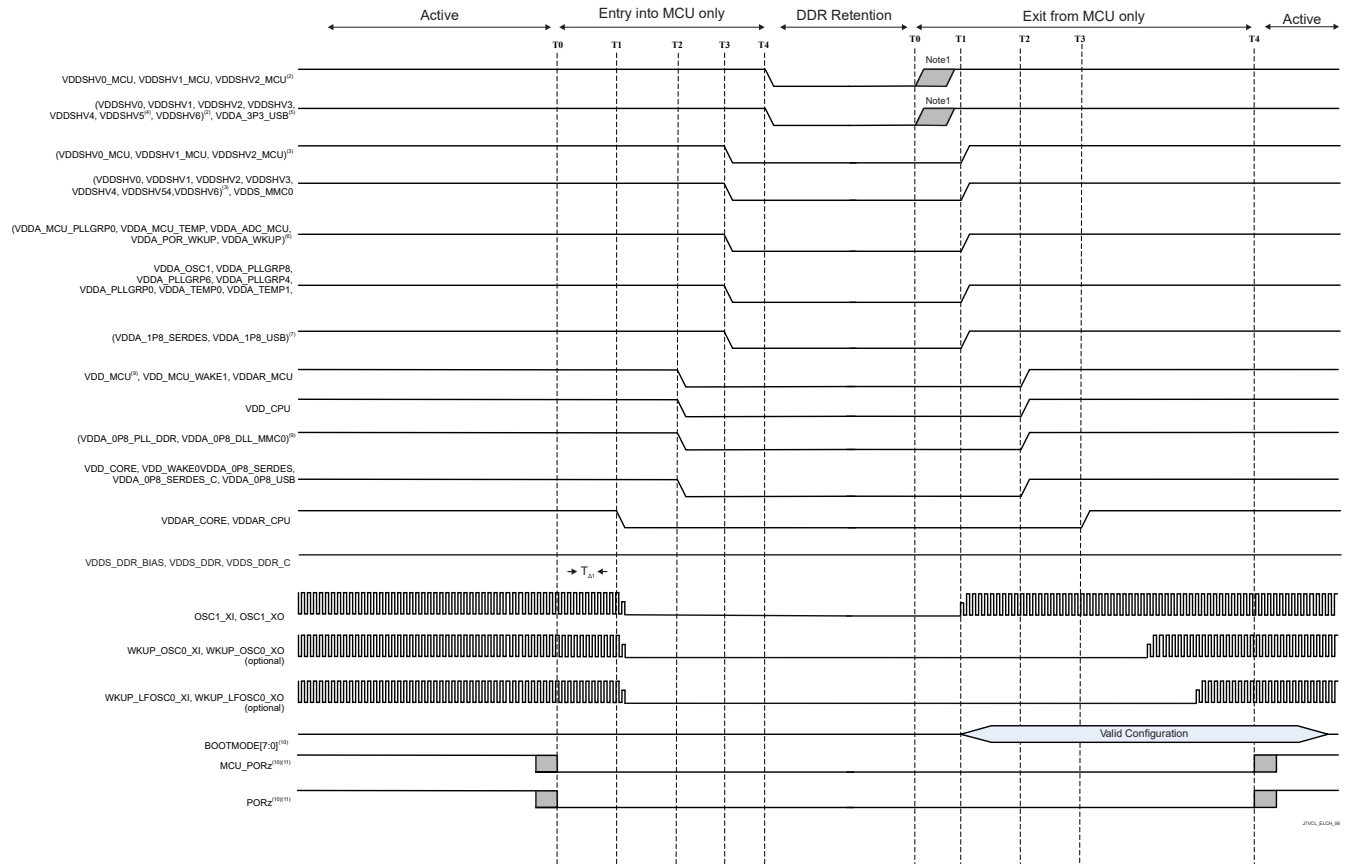
Entry into MCU Only state is accomplished by executing a power down sequence except for the 4 MCU domains that remain energized. Exit from MCU Only state is accomplished by executing a power up sequence with the 4 MCU domains remaining energized throughout the sequence. The example diagram shown is for an Isolated MCU & Main PDN type with eMMC support.



**Figure 6-9. Independent MCU and Main Domains, Entry and Exit of MCU Only Sequencing**

**6.10.2.9 Independent MCU and Main Domains, Entry and Exit of DDR Retention State**

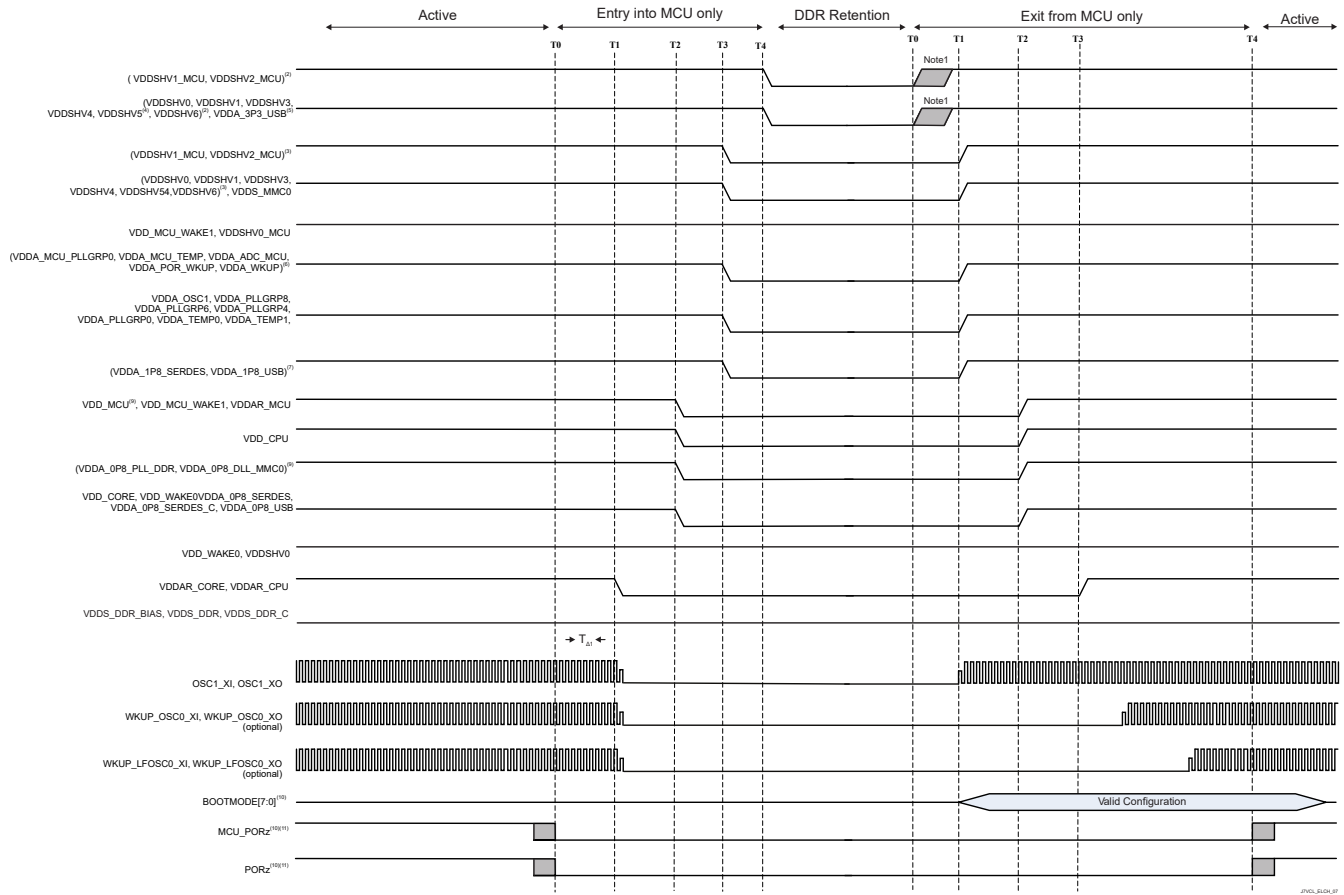
Entry into DDR Retention state is accomplished by executing a power down sequence except for the 4 DDR domains that remain energized. Exit from DDR Retention state is accomplished by executing a power up sequence with the 3 DDR domains remaining energized throughout the sequence.



**Figure 6-10. Independent MCU and Main Domains, Entry and Exit of DDR Retention State**

**6.10.2.10 Independent MCU and Main Domains, Entry and Exit of GPIO Retention Sequencing**

Entry into GPIO Retention state is accomplished by executing a power down sequence except for the 2 or 4 wake domains that remain energized. Exit from GPIO Retention state is accomplished by executing a power up sequence with the 2 or 4 wake DDR domains remaining energized throughout the sequence.



**Figure 6-11. Independent MCU and Main Domains, Entry and Exit of GPIO Retention Sequencing**

### 6.10.3 System Timing

For more details about features and additional description information on the subsystem multiplexing signals, see the corresponding sections within [Section 5.3, Signal Descriptions](#).

#### 6.10.3.1 Reset Timing

The tables and figures provided in this section define the timing conditions, timing requirements, and switching characteristics for reset related signals.

**Table 6-6. Reset Timing Conditions**

| PARAMETER                |                         | MIN                       | MAX    | UNIT |
|--------------------------|-------------------------|---------------------------|--------|------|
| <b>INPUT CONDITIONS</b>  |                         |                           |        |      |
| SR <sub>I</sub>          | Input slew rate         | VDD <sup>(1)</sup> = 1.8V | 0.0018 | V/ns |
|                          |                         | VDD <sup>(1)</sup> = 3.3V | 0.0033 | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |                           |        |      |
| C <sub>L</sub>           | Output load capacitance |                           | 30     | pF   |

(1) VDD stands for the corresponding power supply. For more information on the power supply name and the corresponding ball/balls, see the POWER column of the [Pin Attributes](#) table.

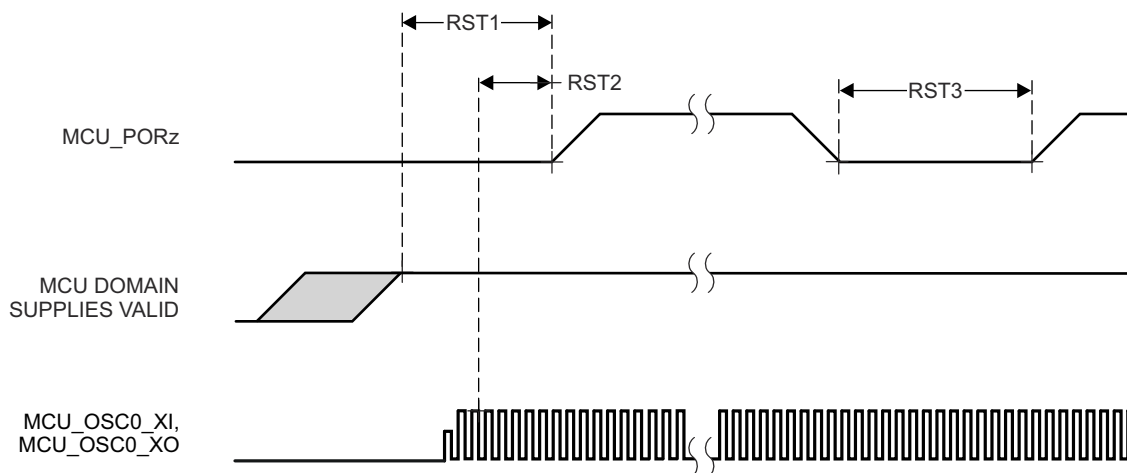
**Table 6-7. MCU\_PORz Timing Requirements**

see [Figure 6-12](#)

| NO.  |  | MIN                     | TYP     | MAX | UNIT |
|------|--|-------------------------|---------|-----|------|
| RST1 | Hold time, MCU_PORz active (low) at Power-up after all MCU_DOMAIN supplies valid (using external crystal)  | N + 1200 <sup>(2)</sup> | 9500000 |     | ns   |
| RST2 | t <sub>h</sub> (MCUD_SUPPLIES_VALID - MCU_PORz) Hold time, MCU_PORz active (low) at Power-up after all MCU_DOMAIN supplies <sup>(1)</sup> valid and external clock stable (using external LVCMOS oscillator) | 1200                    |         |     | ns   |
| RST3 | t <sub>w</sub> (MCU_PORzL) Pulse Width minimum, MCU_PORz low after Power-up (without removal of Power or system reference clock MCU_OSC0_XI/XO)  | 1200                    |         |     | ns   |

(1) For definition of the MCU DOMAIN supplies, see the [Combined MCU and Main Domains Power- Up Sequencing](#).

(2) N = oscillator start-up time



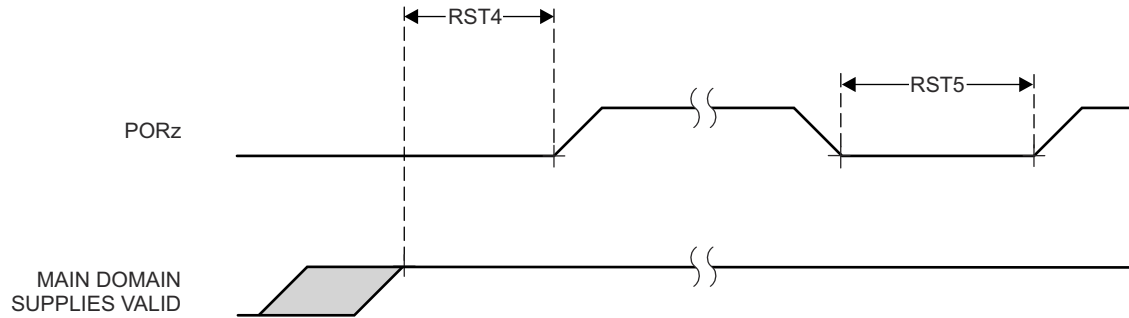
**Figure 6-12. MCU\_PORz Timing Requirements**

**Table 6-8. PORz Timing Requirements**

see [Figure 6-13](#)

| NO.  |   | MIN  | MAX | UNIT |
|------|---|------|-----|------|
| RST4 | $t_{h(MAIN\_SUPPLIES\_VALID - PORz)}$<br>Hold time, PORz active (low) at Power-up after all MAIN DOMAIN supplies <sup>(1)</sup> valid | 1200 |     | ns   |
| RST5 | $t_{w(PORzL)}$<br>Pulse Width minimum, PORz low after Power-up  | 1200 |     | ns   |

(1) For definition of the MAIN DOMAIN supplies, see the [Combined MCU and Main Domains Power-Up Sequencing](#).



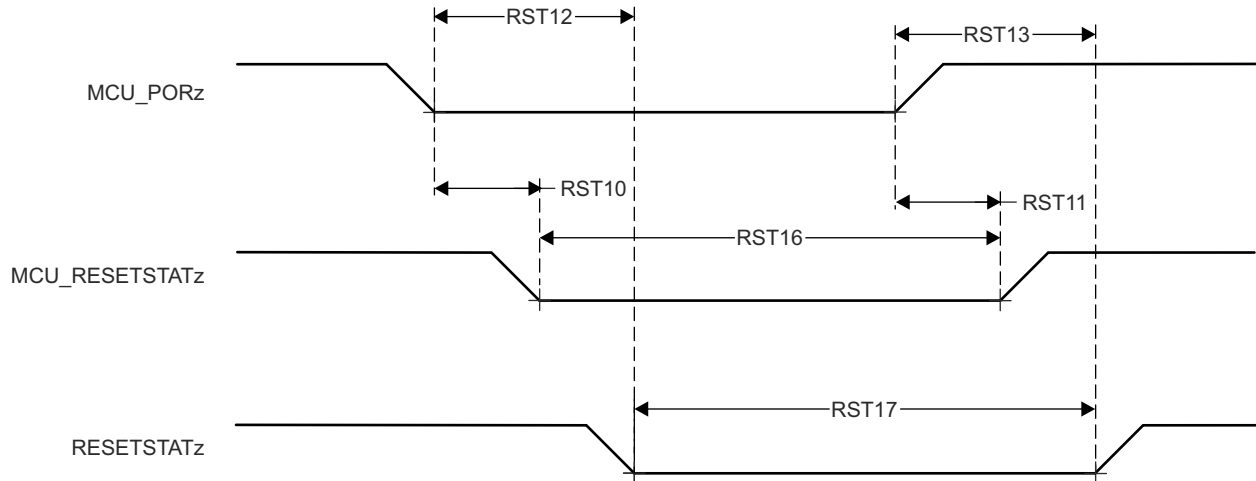
**Figure 6-13. PORz Timing Requirements**

**Table 6-9. MCU\_PORz initiates; MCU\_RESETSTATz, and RESETSTATz Switching Characteristics**

see [Figure 6-14](#)

| NO.   | PARAMETER  | MODE        | MIN                    | MAX | UNIT |
|-------|--|-------------|------------------------|-----|------|
| RST10 | $t_{d(MCU\_PORzL-MCU\_RESETSTATzL)}$<br>Delay time, MCU_PORz active (low) to MCU_RESETSTATz active (low)       |             | 0                      |     | ns   |
| RST11 | $t_{d(MCU\_PORzH-MCU\_RESETSTATzH)}$<br>Delay time, MCU_PORz inactive (high) to MCU_RESETSTATz inactive (high) | POST bypass | 12000*S <sup>(1)</sup> |     | ns   |
| RST12 | $t_{d(MCU\_PORzL-RESETSTATzL)}$<br>Delay time, MCU_PORz active (low) to RESETSTATz active (low)                |             | 0                      |     | ns   |
| RST13 | $t_{d(MCU\_PORzH-RESETSTATzH)}$<br>Delay time, MCU_PORz inactive (high) to RESETSTATz inactive (high)          |             | 14500*S <sup>(1)</sup> |     | ns   |
| RST16 | $t_{w(MCU\_RESETSTATzL)}$<br>Pulse Width Minimum MCU_RESETSTATz low  |             | 3900*S <sup>(1)</sup>  |     | ns   |
| RST17 | $t_{w(RESETSTATzL)}$<br>Pulse Width Minimum RESETSTATz low   |             | 2650*S <sup>(1)</sup>  |     | ns   |

(1) S = MCU\_OSC0\_XI/XO clock period.



**Figure 6-14. MCU\_PORz initiates; MCU\_RESETSTATz, and RESETSTATz Switching Characteristics**

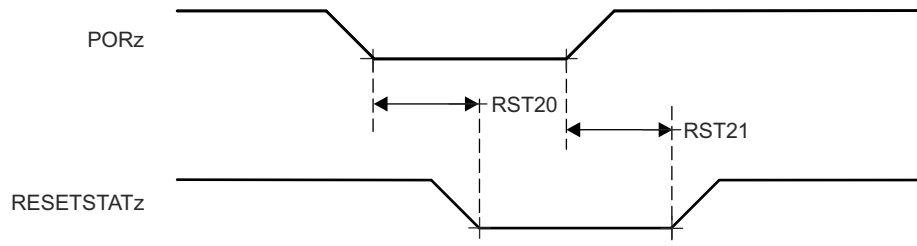
**Table 6-10. PORz Initiates; RESETSTATz Switching Characteristics**

see [Figure 6-15](#)

| NO.   | PARAMETER                  |  | MODE  | MIN                    | MAX | UNIT |
|-------|----------------------------|--|---|------------------------|-----|------|
| RST20 | $t_{d(PORzL-RESETSTATzL)}$ | Delay time, PORz active (low) to RESETSTATz active (low)   |   | $T^{(1)}$              |     |      |
|       |                            |  | CTRLMMR_WKUP_POR_RST_CTRL[0].POR_RST_ISO_DONE_Z = 0 | 0                      |     | ns   |
| RST21 | $t_{d(PORzH-RESETSTATzH)}$ | Delay time, PORz active (high) to RESETSTATz active (high) |   | 14500*S <sup>(2)</sup> |     | ns   |

(1) T = Reset Isolation Time (Software Dependent).

(2) S = MCU\_OSC0\_XI/XO clock period.



**Figure 6-15. PORz initiates; RESETSTATz Switching Characteristics**

**Table 6-11. MCU\_RESETz Timing Requirements**

see Figure 6-16

| NO.   |                                      | MIN  | MAX  | UNIT |
|-------|--------------------------------------|--|------|------|
| RST22 | $t_{w(MCU\_RESETzL)}$ <sup>(1)</sup> | Pulse Width minimum, MCU_RESETz active (low) | 1200 | ns   |

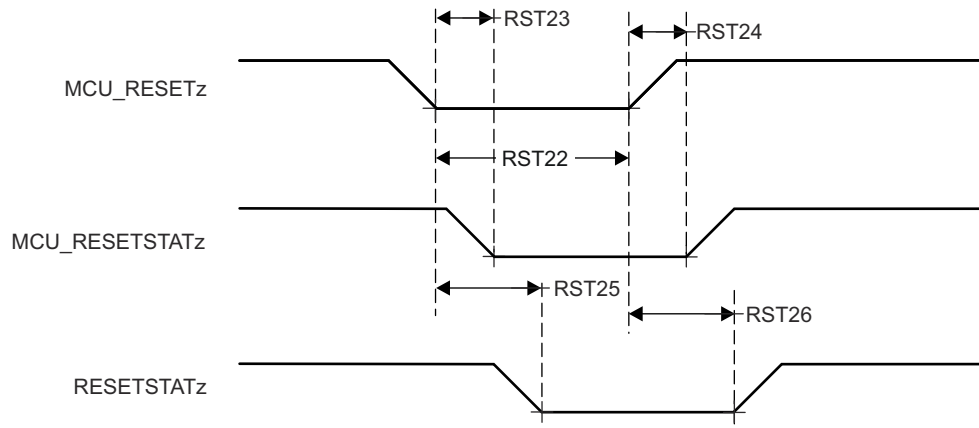
(1) Timing for MCU\_RESETz is valid only after all supplies are valid and MCU\_PORz has been asserted for the specified time.

**Table 6-12. MCU\_RESETz initiates; MCU\_RESETSTATz, and RESETSTATz Switching Characteristics**

see Figure 6-16

| NO.   | PARAMETER                              | MIN  | MAX                   | UNIT |
|-------|--|--|-----------------------|------|
| RST23 | $t_{d(MCU\_RESETzL-MCU\_RESETSTATzL)}$ | Delay time, MCU_RESETz active (low) to MCU_RESETSTATz active (low)       | 800                   | ns   |
| RST24 | $t_{d(MCU\_RESETzH-MCU\_RESETSTATzH)}$ | Delay time, MCU_RESETz inactive (high) to MCU_RESETSTATz inactive (high) | 3900*S <sup>(1)</sup> | ns   |
| RST25 | $t_{d(MCU\_RESETzL-RESETSTATzL)}$      | Delay time, MCU_RESETz active (low) to RESETSTATz active (low)           | 800                   | ns   |
| RST26 | $t_{d(MCU\_RESETzH-RESETSTATzH)}$      | Delay time, MCU_RESETz inactive (high) to RESETSTATz inactive (high)     | 3900*S <sup>(1)</sup> | ns   |

(1) S = MCU\_OSC0\_XI/XO clock period.



**Figure 6-16. MCU\_RESETz initiates; MCU\_RESETSTATz, and RESETSTATz Timing Requirements and Switching Characteristics**

**Table 6-13. RESET\_REQz Timing Requirements**

see [Figure 6-17](#)

| NO.   |                                       | MIN  | MAX | UNIT |    |
|-------|---------------------------------------|--|-----|------|----|
| RST27 | $t_{w(RESSET\_REQzL)}$ <sup>(1)</sup> | Pulse Width minimum, RESET_REQz active (low) |     | 1200 | ns |

(1) Timing for RESET\_REQz is valid only after all supplies are valid and MCU\_PORz has been asserted for the specified time.

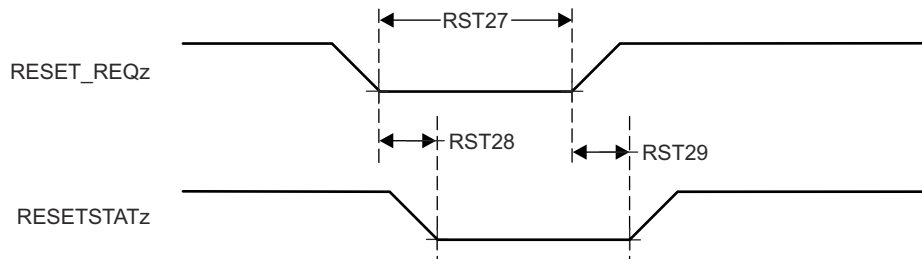
**Table 6-14. RESET\_REQz initiates; RESETSTATz Switching Characteristics**

see [Figure 6-17](#)

| NO.   | PARAMETER                           | MODE  | MIN                   | MAX | UNIT |
|-------|-------------------------------------|---|-----------------------|-----|------|
| RST28 | $t_{d(RESSET\_REQzL-RESSETSTATzL)}$ | software control of SOC_WARMRST_ISO_DONE_Z                    | T <sup>(1)</sup>      |     |      |
|       |                                     | CTRLMMR_WKUP_MAIN_WARM_RST_CTRL[0].SOC_WARMRST_ISO_DONE_Z = 0 | 740                   |     | ns   |
| RST29 | $t_{d(RESSET\_REQzH-RESSETSTATzH)}$ |   | 2650*S <sup>(2)</sup> |     | ns   |

(1) T = Reset Isolation Time (Software Dependent).

(2) S = MCU\_OSC0\_XI/XO clock period.



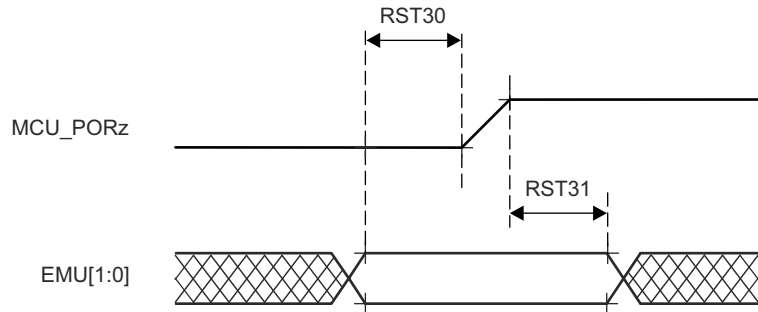
**Figure 6-17. RESET\_REQz initiates; RESETSTATz Timing Requirements and Switching Characteristics**

**Table 6-15. EMUx Timing Requirements**

see [Figure 6-18](#)

| NO.   |                          |  | MIN               | MAX | UNIT |
|-------|--------------------------|--|-------------------|-----|------|
| RST30 | $t_{su}(EMUx-MCU\_PORz)$ | Setup time, EMU[1:0] before MCU_PORz inactive (high) | $3 \cdot S^{(1)}$ |     | ns   |
| RST31 | $t_h(MCU\_PORz - EMUx)$  | Hold time, EMU[1:0] after MCU_PORz inactive (high)   | 10                |     | ns   |

(1) S = MCU\_OSC0\_XI/XO clock period.



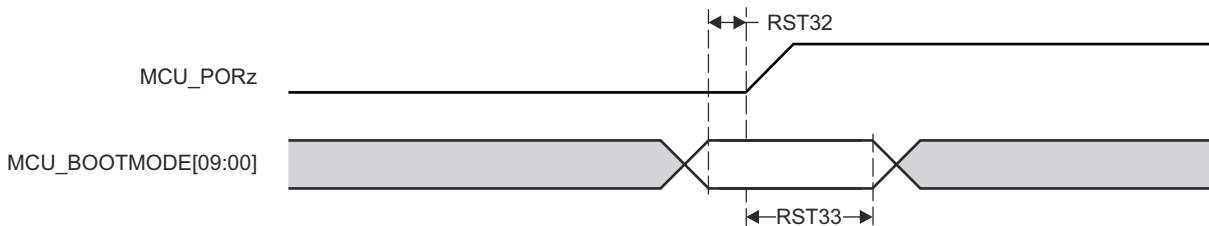
**Figure 6-18. EMUx Timing Requirements**

**Table 6-16. MCU\_BOOTMODE Timing Requirements**

see [Figure 6-19](#)

| NO.   |                                   |  | MIN               | MAX | UNIT |
|-------|-----------------------------------|--|-------------------|-----|------|
| RST32 | $t_{su}(MCU\_BOOTMODE-MCU\_PORz)$ | Setup time, MCU_BOOTMODE[09:00] before MCU_PORz high | $3 \cdot S^{(1)}$ |     | ns   |
| RST33 | $t_h(MCU\_PORz - MCU\_BOOTMODE)$  | Hold time, MCU_BOOTMODE[09:00] after MCU_PORz high   | 0                 |     | ns   |

(1) S = MCU\_OSC0\_XI/XO clock period.



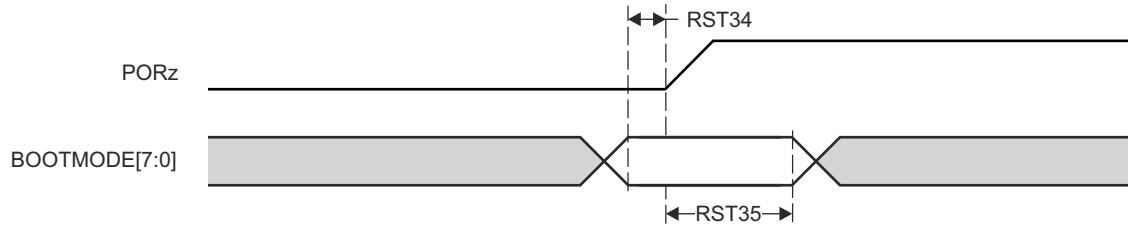
**Figure 6-19. MCU\_BOOTMODE Timing Requirements**

**Table 6-17. BOOTMODE Timing Requirements**

see [Figure 6-20](#)

| NO.   |                                |  | MIN               | MAX | UNIT |
|-------|--------------------------------|--|-------------------|-----|------|
| RST34 | $t_{su}(\text{BOOTMODE-PORz})$ | Setup time, BOOTMODE[7:0] before PORz high | $3 \cdot S^{(1)}$ |     | ns   |
| RST35 | $t_h(\text{PORz - BOOTMODE})$  | Hold time, BOOTMODE[7:0] after PORz high   | 0                 |     | ns   |

(1) S = MCU\_OSC0\_XI/XO clock period.



**Figure 6-20. BOOTMODE Timing Requirements**

### 6.10.3.2 Safety Signal Timing

Tables and figures provided in this section define timing conditions, switching characteristics for MCU\_SAFETY\_ERRORn and SOC\_SAFETY\_ERRORn.

**Table 6-18. Error Signal Timing Conditions**

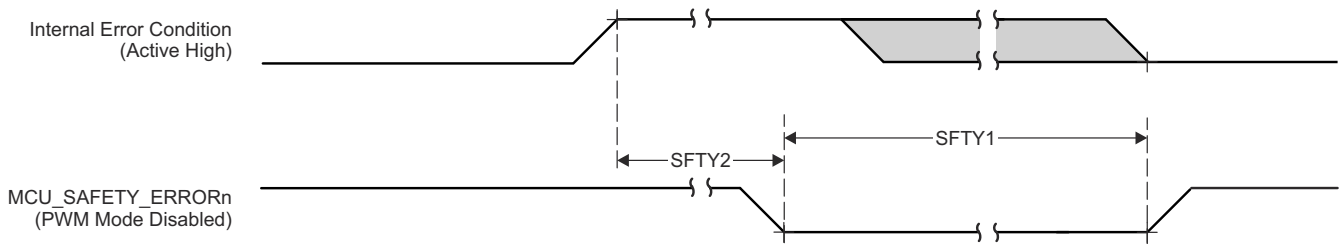
| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | 0.5 | 2   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 3   | 30  | pF   |

**Table 6-19. MCU\_SAFETY\_ERRORn Switching Characteristics**

see [Figure 6-21](#)

| NO.   | PARAMETER  | MIN                    | MAX | UNIT |
|-------|--|------------------------|-----|------|
| SFTY1 | t <sub>w</sub> (MCU_SAFETY_ERRORn)<br>Pulse width minimum, MCU_SAFETY_ERRORn active (PWM mode disabled)        | P*R <sup>(1) (2)</sup> |     | ns   |
| SFTY2 | t <sub>d</sub> (ERROR_CONDITION-MCU_SAFETY_ERRORnL)<br>Delay time, ERROR CONDITION to MCU_SAFETY_ERRORn active | 50*P <sup>(1)</sup>    |     | ns   |

- (1) P = ESM functional clock (MCU\_SYSCLK0 /6).
- (2) R = Error Pin Counter Pre-Load Register count value.

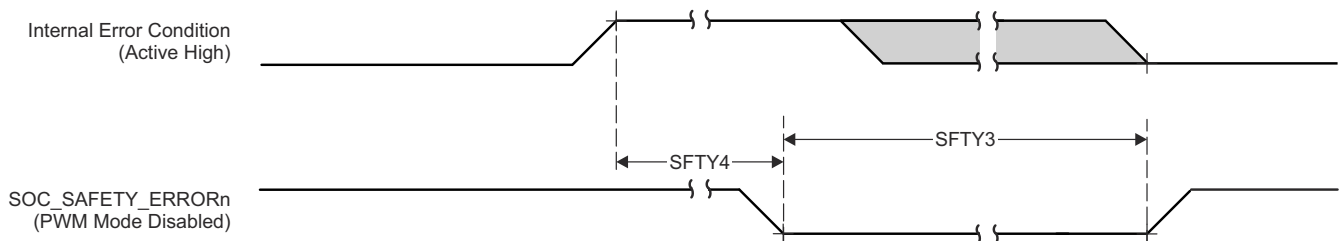


**Figure 6-21. MCU\_SAFETY\_ERRORn Switching Characteristics**

**Table 6-20. SOC\_SAFETY\_ERRORn Switching Characteristics**

see [Figure 6-22](#)

| NO.   | PARAMETER  | MIN                    | MAX | UNIT |
|-------|--|------------------------|-----|------|
| SFTY3 | t <sub>w</sub> (SOC_SAFETY_ERRORn)<br>Pulse width minimum, SOC_SAFETY_ERRORn active (PWM mode disabled)        | P*R <sup>(1) (2)</sup> |     | ns   |
| SFTY4 | t <sub>d</sub> (ERROR_CONDITION-SOC_SAFETY_ERRORnL)<br>Delay time, ERROR CONDITION to SOC_SAFETY_ERRORn active | 50*P <sup>(1)</sup>    |     | ns   |



**Figure 6-22. SOC\_SAFETY\_ERRORn Switching Characteristics**

### 6.10.3.3 Clock Timing

Tables and figures provided in this section define timing conditions, timing requirements, and switching characteristics for clock signals.

**Table 6-21. Clock Timing Conditions**

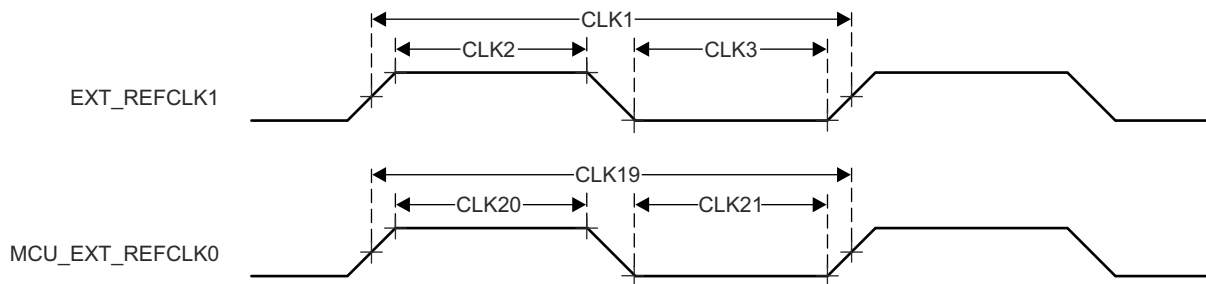
| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | 0.5 | 2   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 3   | 30  | pF   |

**Table 6-22. Clock Timing Requirements**

see [Figure 6-23](#)

| NO.  | PARAMETER                     | DESCRIPTION                              | MIN                   | MAX                   | UNIT |
|------|-------------------------------|--|-----------------------|-----------------------|------|
| CLK1 | t <sub>c</sub> (EXT_REFCLK1)  | Cycle time minimum, EXT_REFCLK1          | 10                    |                       | ns   |
| CLK2 | t <sub>w</sub> (EXT_REFCLK1H) | Pulse Duration minimum, EXT_REFCLK1 high | E*0.45 <sup>(1)</sup> | E*0.55 <sup>(1)</sup> | ns   |
| CLK3 | t <sub>w</sub> (EXT_REFCLK1L) | Pulse Duration minimum, EXT_REFCLK1 low  | E*0.45 <sup>(1)</sup> | E*0.55 <sup>(1)</sup> | ns   |

(1) E = EXT\_REFCLK1 cycle time.



**Figure 6-23. Clock Timing Requirements**

**Table 6-23. Clock Switching Characteristics**

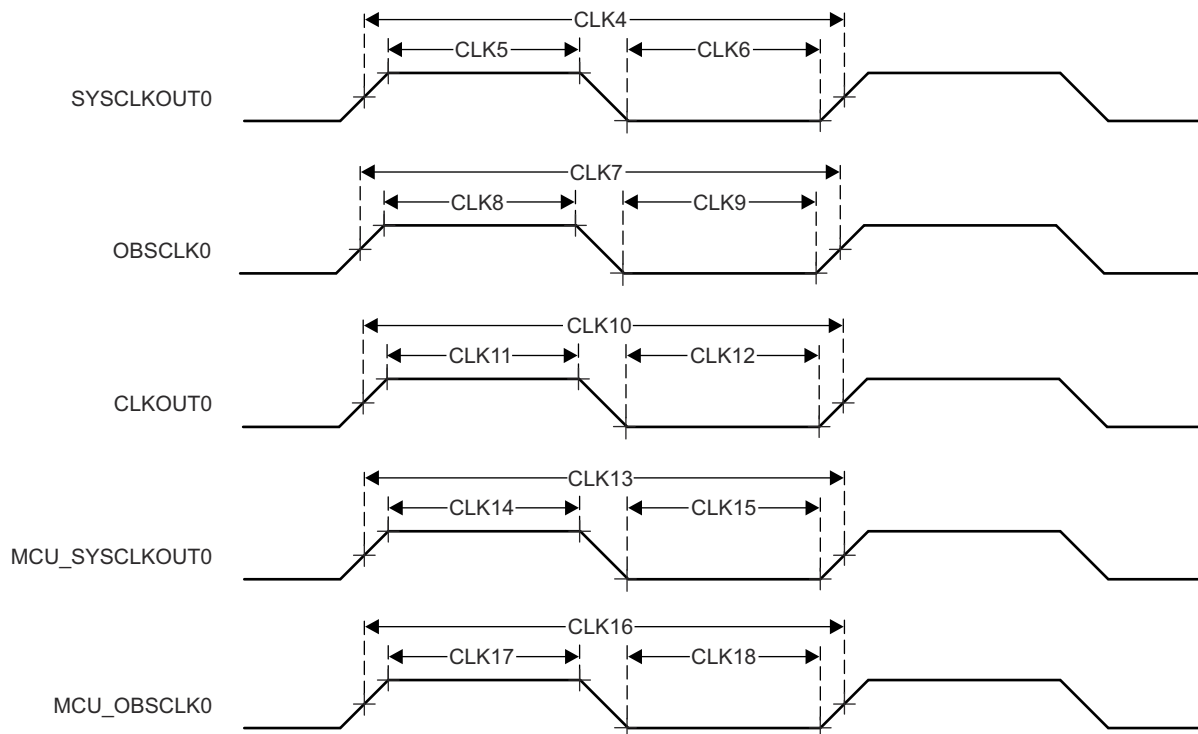
see [Figure 6-24](#)

| NO.   | PARAMETER                    | DESCRIPTION                             | MIN                  | MAX                  | UNIT |
|-------|------------------------------|---|----------------------|----------------------|------|
| CLK4  | t <sub>c</sub> (SYSCLKOUT0)  | Cycle time minimum, SYSCLKOUT0          | 8                    |                      | ns   |
| CLK5  | t <sub>w</sub> (SYSCLKOUT0H) | Pulse Duration minimum, SYSCLKOUT0 high | A*0.4 <sup>(1)</sup> | A*0.6 <sup>(1)</sup> | ns   |
| CLK6  | t <sub>w</sub> (SYSCLKOUT0L) | Pulse Duration minimum, SYSCLKOUT0 low  | A*0.4 <sup>(1)</sup> | A*0.6 <sup>(1)</sup> | ns   |
| CLK7  | t <sub>c</sub> (OBSCLK0)     | Cycle time minimum, OBSCLK0             | 5                    |                      | ns   |
| CLK8  | t <sub>w</sub> (OBSCLK0H)    | Pulse Duration minimum, OBSCLK0 high    | B*0.4 <sup>(2)</sup> | B*0.6 <sup>(2)</sup> | ns   |
| CLK9  | t <sub>w</sub> (OBSCLK0L)    | Pulse Duration minimum, OBSCLK0 low     | B*0.4 <sup>(2)</sup> | B*0.6 <sup>(2)</sup> | ns   |
| CLK10 | t <sub>c</sub> (CLKOUT0)     | Cycle time minimum, CLKOUT0             | 20                   |                      | ns   |
| CLK11 | t <sub>w</sub> (CLKOUT0H)    | Pulse Duration minimum, CLKOUT0 high    | C*0.4 <sup>(3)</sup> | C*0.6 <sup>(3)</sup> | ns   |
| CLK12 | t <sub>w</sub> (CLKOUT0L)    | Pulse Duration minimum, CLKOUT0 low     | C*0.4 <sup>(3)</sup> | C*0.6 <sup>(3)</sup> | ns   |

(1) A = SYSCLKOUT0 cycle time.

(2) B = OBSCLK0 cycle time.

(3) C = CLKOUT0 cycle time.



**Figure 6-24. Clock Switching Characteristics**

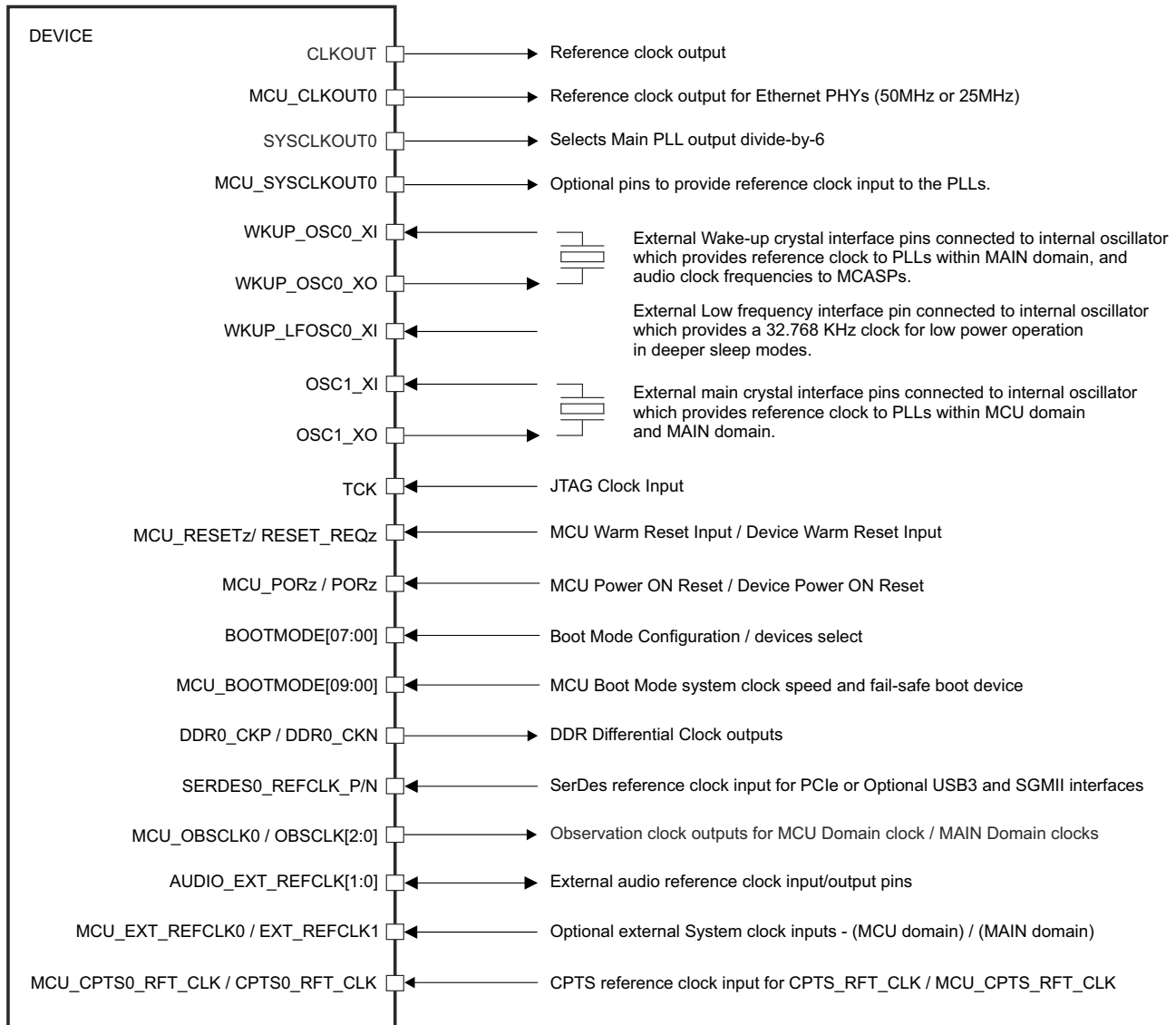
## 6.10.4 Clock Specifications

### 6.10.4.1 Input Clocks / Oscillators

Various external clock inputs/outputs are needed to drive the device. Summary of these input clock signals is as follows:

- OSC1\_XO/OSC1\_XI — External main crystal interface pins connected to internal oscillator which sources reference clock and provides reference clock to PLLs within MAIN domain. Also, for audio applications, high-frequency oscillator 0 is used to provide audio clock frequencies to MCASPs.
- High frequency oscillators inputs
  - OSC1\_XO/OSC1\_XI — external main crystal interface pins connected to internal oscillator which sources reference clock. Provides reference clock to PLLs within MAIN domain. This highfrequency oscillator is used to provide audio clock frequencies to MCASPs.
  - WKUP\_OSC0\_XO/WKUP\_OSC0\_XI — external main crystal interface pins of the internal oscillator which sources a reference clock. Provides reference clock to PLLs within WKUP/MCU and MAIN domain.
- Low frequency oscillator input
  - WKUP\_LF\_CLKIN — External 32.768 kHz clock input.
- General purpose clock inputs
  - MCU\_EXT\_REFCLK0 — optional external. Provides system clock input (MCU domain).
  - EXT\_REFCLK1 — optional external system clock input (MAIN domain). Optionally PLL2 (PER1) and MCASP can be sourced by EXT\_REFCLK1 (sourced externally).
  - SERDES0\_REFCLK\_P/N — SerDes reference clock input for PCIe or Optional USB3 and SGMII interfaces.
- External CPTS reference clock inputs
  - MCU\_CPTS0\_RFT\_CLK — CPTS reference clock inputs for MCU\_CPTS\_RFT\_CLK.
  - CPTS0\_RFT\_CLK — CPTS reference clock inputs for CPTS\_RFT\_CLK.
- External audio reference clock input/output pins
  - AUDIO\_EXT\_REFCLK0
  - AUDIO\_EXT\_REFCLK1

Figure 6-25 shows the external input clock sources and the output clocks to peripherals.



**Figure 6-25. Input Clocks Interface**

For more information about Input clock interfaces, see *Clocking* section in *Device Configuration* chapter in the device TRM.

**6.10.4.1.1 WKUP\_OSC0 Internal Oscillator Clock Source**

Figure 6-26 shows the recommended crystal circuit. All discrete components used to implement the oscillator circuit should be placed as close as possible to the WKUP\_OSC0\_XI and WKUP\_OSC0\_XO pins.

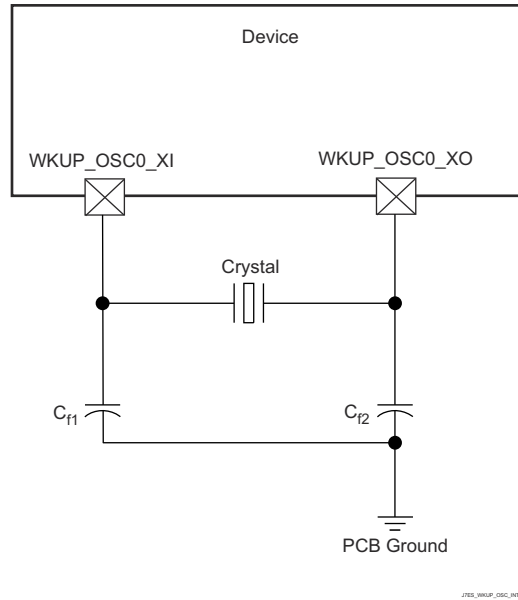


Figure 6-26. WKUP\_OSC0 Crystal Implementation

The crystal must be in the fundamental mode of operation and parallel resonant. Table 6-24 summarizes the required electrical constraints.

Table 6-24. WKUP\_OSC0 Crystal Electrical Characteristics

| PARAMETER                                 |   | MIN   | TYP                                       | MAX  | UNIT |    |
|---|---|---|---|------|------|----|
| F <sub>xtal</sub>                         | Crystal Parallel Resonance Frequency                | 19.2, 20, 24, 25, 26, 27                    |   |      | MHz  |    |
| F <sub>xtal</sub>                         | Crystal Frequency Stability and Tolerance           | Ethernet RGMII and RMII not used            |   | ±100 | ppm  |    |
|   |   | Ethernet RGMII and RMII using derived clock |   | ±50  |      |    |
| C <sub>L1+PCBXI</sub>                     | Capacitance of C <sub>L1</sub> + C <sub>PCBXI</sub> | 12  |   | 24   | pF   |    |
| C <sub>L2+PCBXO</sub>                     | Capacitance of C <sub>L2</sub> + C <sub>PCBXO</sub> | 12  |   | 24   | pF   |    |
| C <sub>L</sub>                            | Crystal Load Capacitance                            | 6   |   | 12   | pF   |    |
| C <sub>shunt</sub>                        | Crystal Circuit Shunt Capacitance                   | 19.2 MHz,<br>20MHz                          | ESR <sub>xtal</sub> ≤ 30 Ω                |      | 7    | pF |
|   |   |   | 30 Ω < ESR <sub>xtal</sub> ≤ 80 Ω         |      | 5    | pF |
|   |   |   | 80 Ω < ESR <sub>xtal</sub> ≤ 100 Ω        |      | 3    | pF |
|   |   | 24MHz                                       | ESR <sub>xtal</sub> ≤ 30 Ω                |      | 7    | pF |
|   |   |   | 30 Ω < ESR <sub>xtal</sub> ≤ 60 Ω         |      | 5    | pF |
|   |   |   | 60 Ω < ESR <sub>xtal</sub> ≤ 80 Ω         |      | 3    | pF |
|   |   |   | Not Supported: 80 Ω ≤ ESR <sub>xtal</sub> |      | –    |    |
|   |   | 25MHz                                       | ESR <sub>xtal</sub> ≤ 30 Ω                |      | 7    | pF |
|   |   |   | 30 Ω < ESR <sub>xtal</sub> ≤ 50 Ω         |      | 5    | pF |
|   |   |   | 50 Ω < ESR <sub>xtal</sub> ≤ 80 Ω         |      | 3    | pF |
|   |   |   | Not Supported: 80 Ω ≤ ESR <sub>xtal</sub> |      | –    |    |
|   |   | 26 MHz,<br>27 MHz                           | ESR <sub>xtal</sub> ≤ 30 Ω                |      | 7    | pF |
| 30 Ω < ESR <sub>xtal</sub> ≤ 50 Ω         |   |   | 5   | pF   |      |    |
| Not Supported: 50 Ω ≤ ESR <sub>xtal</sub> |   |   | –   |      |      |    |

**Table 6-24. WKUP\_OSC0 Crystal Electrical Characteristics (continued)**

| PARAMETER   | MIN | TYP | MAX | UNIT |
|---|-----|-----|-----|------|
| ESR <sub>xtal</sub> Crystal Effective Series Resistance |     |     | (1) | Ω    |

(1) The maximum ESR of the crystal is a function of the crystal frequency and shunt capacitance. See the C<sub>shunt</sub> parameter.

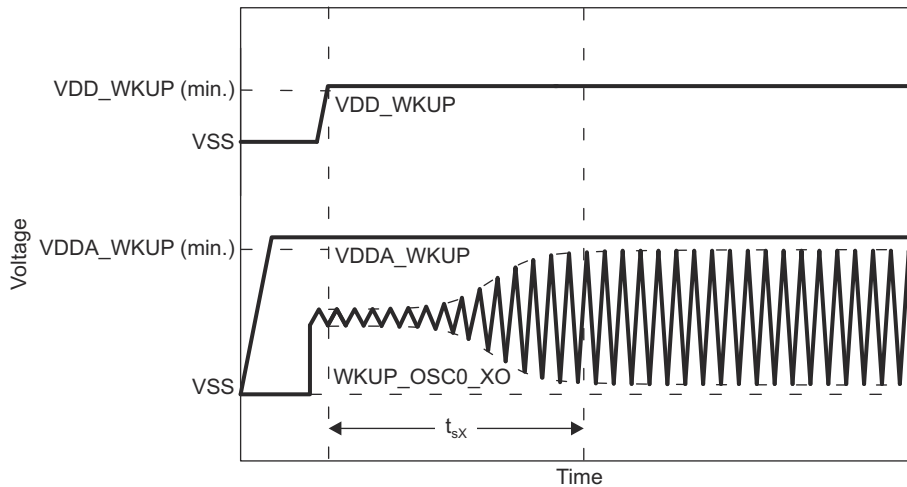
When selecting a crystal, the system design must consider temperature and aging characteristics of the crystal based on worst case environment and expected life expectancy of the system.

Table 6-25 details the switching characteristics of the oscillator.

**Table 6-25. WKUP\_OSC0 Switching Characteristics – Crystal Mode**

| NAME              | DESCRIPTION                 | MIN | TYP                | MAX   | UNIT |
|-------------------|-----------------------------|-----|--------------------|-------|------|
| C <sub>XI</sub>   | XI Capacitance              |     |                    | 1.316 | pF   |
| C <sub>XO</sub>   | XO Capacitance              |     |                    | 1.333 | pF   |
| C <sub>XIXO</sub> | XI to XO Mutual Capacitance |     |                    | 0.01  | pF   |
| t <sub>s</sub>    | Start-up Time               |     | 9.5 <sup>(1)</sup> |       | ms   |

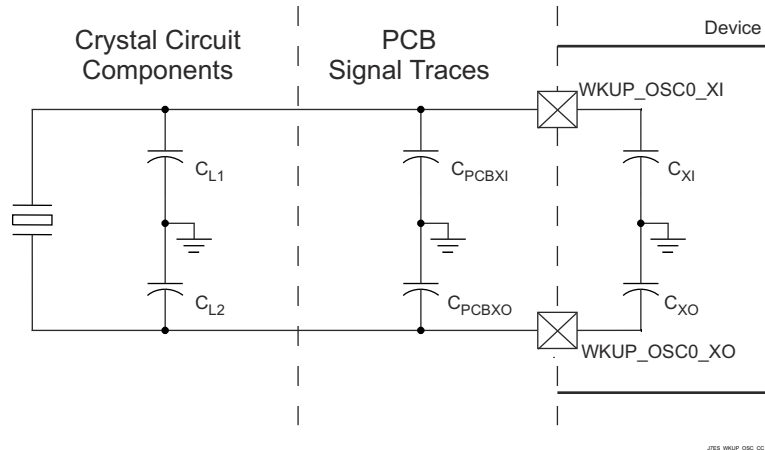
(1) TI strongly encourages each customer to submit samples of the device to the resonator/crystal vendors for validation. The vendors are equipped to determine what load capacitors will best tune their resonator/crystal to the microcontroller device for optimum startup and operation over temperature/voltage extremes.



**Figure 6-27. WKUP\_OSC0 Start-up Time**

**6.10.4.1.1 Load Capacitance**

The crystal circuit must be designed such that it applies the appropriate capacitive load to the crystal, as defined by the crystal manufacturer. The capacitive load, C<sub>L</sub>, of this circuit is a combination of discrete capacitors C<sub>L1</sub>, C<sub>L2</sub>, and several parasitic contributions. PCB signal traces which connect crystal circuit components to WKUP\_OSC0\_XI and WKUP\_OSC0\_XO have parasitic capacitance to ground, C<sub>PCBXI</sub> and C<sub>PCBXO</sub>, where the PCB designer should be able to extract parasitic capacitance for each signal trace. The WKUP\_OSC0 circuits and device package have combined parasitic capacitance to ground, C<sub>PCBXI</sub> and C<sub>PCBXO</sub>, where these parasitic capacitance values are defined in Table 6-25.



**Figure 6-28. Load Capacitance**

Load capacitors,  $C_{L1}$  and  $C_{L2}$  in [Figure 6-26](#), should be chosen such that the below equation is satisfied.  $C_L$  in the equation is the load specified by the crystal manufacturer.

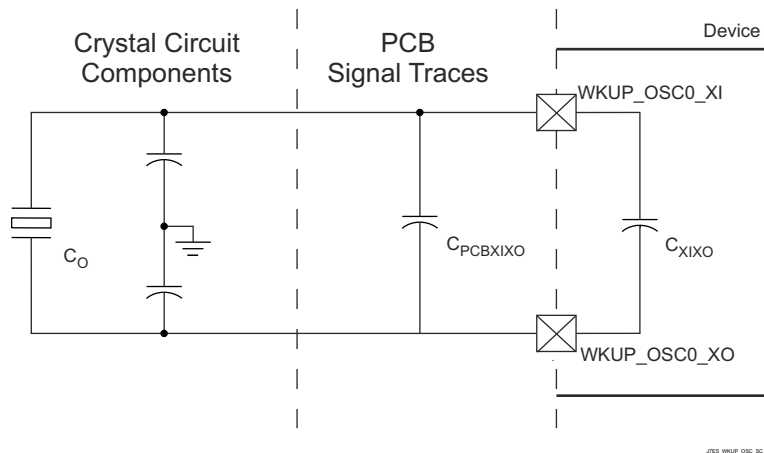
$$C_L = [(C_{L1} + C_{PCBXI} + C_{XI}) \times (C_{L2} + C_{PCBXO} + C_{XO})] / [(C_{L1} + C_{PCBXI} + C_{XI}) + (C_{L2} + C_{PCBXO} + C_{XO})]$$

To determine the value of  $C_{L1}$  and  $C_{L2}$ , multiply the capacitive load value  $C_L$  by 2. Using this result, subtract the combined values of  $C_{PCBXI} + C_{XI}$  to determine the value of  $C_{L1}$  and the combined values of  $C_{PCBXO} + C_{XO}$  to determine the value of  $C_{L2}$ . For example, if  $C_L = 10$  pF,  $C_{PCBXI} = 2.9$  pF,  $C_{XI} = 0.5$  pF,  $C_{PCBXO} = 3.7$  pF,  $C_{XO} = 0.5$  pF, the value of  $C_{L1} = [(2C_L) - (C_{PCBXI} + C_{XI})] = [(2 \times 10 \text{ pF}) - 2.9 \text{ pF} - 0.5 \text{ pF}] = 16.6$  pF and  $C_{L2} = [(2C_L) - (C_{PCBXO} + C_{XO})] = [(2 \times 10 \text{ pF}) - 3.7 \text{ pF} - 0.5 \text{ pF}] = 15.8$  pF

#### 6.10.4.1.1.2 Shunt Capacitance

The crystal circuit must also be designed such that it does not exceed the maximum shunt capacitance for WKUP\_OSC0 operating conditions defined in [Table 6-24](#). Shunt capacitance,  $C_{shunt}$ , of the crystal circuit is a combination of crystal shunt capacitance and parasitic contributions. PCB signal traces which connect crystal circuit components to WKUP\_OSC0 have mutual parasitic capacitance to each other,  $C_{PCBXIXO}$ , where the PCB designer should be able to extract mutual parasitic capacitance between these signal traces. The device package also has mutual parasitic capacitance,  $C_{XIXO}$ , where this mutual parasitic capacitance value is defined in [Table 6-25](#).

PCB routing should be designed to minimize mutual capacitance between XI and XO signal traces. This is typically done by keeping signal traces short and not routing them in close proximity. Mutual capacitance can also be minimized by placing a ground trace between these signals when the layout requires them to be routed in close proximity. It is important to minimize the mutual capacitance on the PCB to provide as much margin as possible when selecting a crystal.



**Figure 6-29. Shunt Capacitance**

A crystal should be chosen such that the below equation is satisfied.  $C_O$  in the equation is the maximum shunt capacitance specified by the crystal manufacturer.

$$C_{\text{shunt}} \geq C_O + C_{\text{PCBXIXO}} + C_{\text{XIXO}}$$

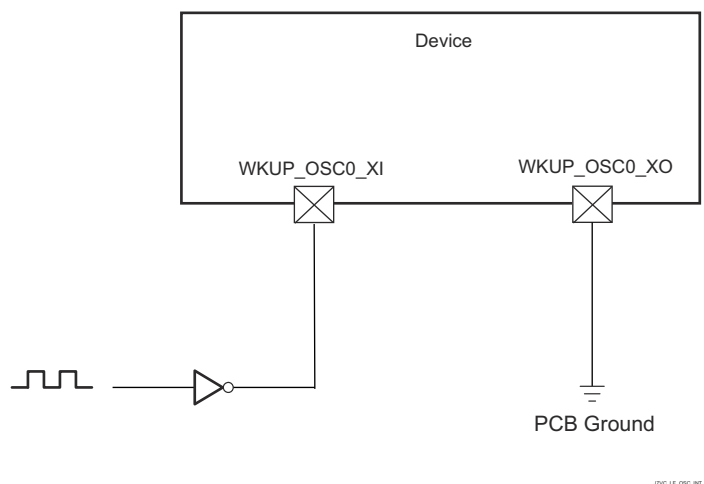
For example, the equation would be satisfied when the crystal being used is 25 MHz with an ESR = 30  $\Omega$ ,  $C_{\text{PCBXIXO}} = 0.04$  pF,  $C_{\text{XIXO}} = 0.01$  pF, and shunt capacitance of the crystal is less than or equal to 6.95 pF.

#### 6.10.4.1.2 WKUP\_OSC0 LVC MOS Digital Clock Source

Figure 6-30 shows the recommended oscillator connections when WKUP\_OSC0\_XI is connected to a 1.8-V LVC MOS square-wave digital clock source.

#### Note

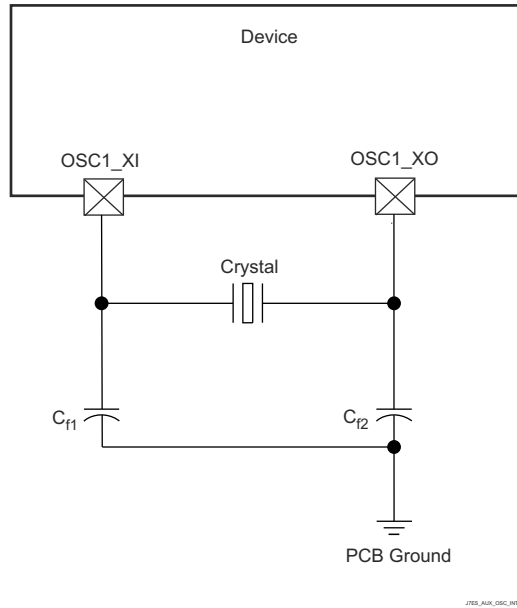
A DC steady-state condition is not allowed on WKUP\_OSC0\_XI when the oscillator is powered up. This is not allowed because WKUP\_OSC0\_XI is internally AC coupled to a comparator that may enter a unknown state when DC is applied to the input. Therefore, application software should power down WKUP\_OSC0 any time WKUP\_OSC0\_XI is not toggling between logic states.



**Figure 6-30. 1.8-V LVC MOS-Compatible Clock Input**

**6.10.4.1.3 Auxiliary OSC1 Internal Oscillator Clock Source**

Figure 6-31 shows the recommended crystal circuit. All discrete components used to implement the oscillator circuit should be placed as close as possible to the OSC1\_XI and OSC1\_XO pins.



**Figure 6-31. OSC1 Crystal Implementation**

The crystal must be in the fundamental mode of operation and parallel resonant. Table 6-26 summarizes the required electrical constraints.

**Table 6-26. OSC1 Crystal Electrical Characteristics**

| PARAMETER                                 |   | MIN   | TYP                                       | MAX  | UNIT |    |
|---|---|---|---|------|------|----|
| F <sub>xtal</sub>                         | Crystal Parallel Resonance Frequency                | 19.2  |   | 27   | MHz  |    |
| F <sub>xtal</sub>                         | Crystal Frequency Stability and Tolerance           | Ethernet RGMII and RMII not used            |   | ±100 | ppm  |    |
|   |   | Ethernet RGMII and RMII using derived clock |   | ±50  |      |    |
| C <sub>L1+PCBXI</sub>                     | Capacitance of C <sub>L1</sub> + C <sub>PCBXI</sub> | 12  |   | 24   | pF   |    |
| C <sub>L2+PCBXO</sub>                     | Capacitance of C <sub>L2</sub> + C <sub>PCBXO</sub> | 12  |   | 24   | pF   |    |
| C <sub>L</sub>                            | Crystal Load Capacitance                            | 6   |   | 12   | pF   |    |
| C <sub>shunt</sub>                        | Crystal Circuit Shunt Capacitance                   | 19.2MHz ≤ F <sub>xtal</sub> ≤ 20MHz         | ESR <sub>xtal</sub> ≤ 30 Ω                |      | 7    | pF |
|   |   |   | 30 Ω ≤ ESR <sub>xtal</sub> ≤ 80 Ω         |      | 5    | pF |
|   |   |   | 80 Ω ≤ ESR <sub>xtal</sub> ≤ 100 Ω        |      | 3    | pF |
|   |   | 20MHz ≤ F <sub>xtal</sub> ≤ 24.576MHz       | ESR <sub>xtal</sub> ≤ 30 Ω                |      | 7    | pF |
|   |   |   | 30 Ω ≤ ESR <sub>xtal</sub> ≤ 60 Ω         |      | 5    | pF |
|   |   |   | 60 Ω ≤ ESR <sub>xtal</sub> ≤ 80 Ω         |      | 3    | pF |
|   |   |   | Not Supported: 80 Ω ≤ ESR <sub>xtal</sub> |      | –    |    |
|   |   | 24.576MHz ≤ F <sub>xtal</sub> ≤ 25MHz       | ESR <sub>xtal</sub> ≤ 30 Ω                |      | 7    | pF |
|   |   |   | 30 Ω ≤ ESR <sub>xtal</sub> ≤ 50 Ω         |      | 5    | pF |
|   |   |   | 50 Ω ≤ ESR <sub>xtal</sub> ≤ 80 Ω         |      | 3    | pF |
|   |   |   | Not Supported: 80 Ω ≤ ESR <sub>xtal</sub> |      | –    |    |
|   |   | 25MHz ≤ F <sub>xtal</sub> ≤ 27MHz           | ESR <sub>xtal</sub> ≤ 30 Ω                |      | 7    | pF |
| 30 Ω ≤ ESR <sub>xtal</sub> ≤ 50 Ω         |   |   | 5   | pF   |      |    |
| Not Supported: 50 Ω ≤ ESR <sub>xtal</sub> |   |   | –   |      |      |    |

**Table 6-26. OSC1 Crystal Electrical Characteristics (continued)**

| PARAMETER           |                                     | MIN | TYP | MAX | UNIT |
|---------------------|-------------------------------------|-----|-----|-----|------|
| ESR <sub>xtal</sub> | Crystal Effective Series Resistance |     |     | 100 | Ω    |

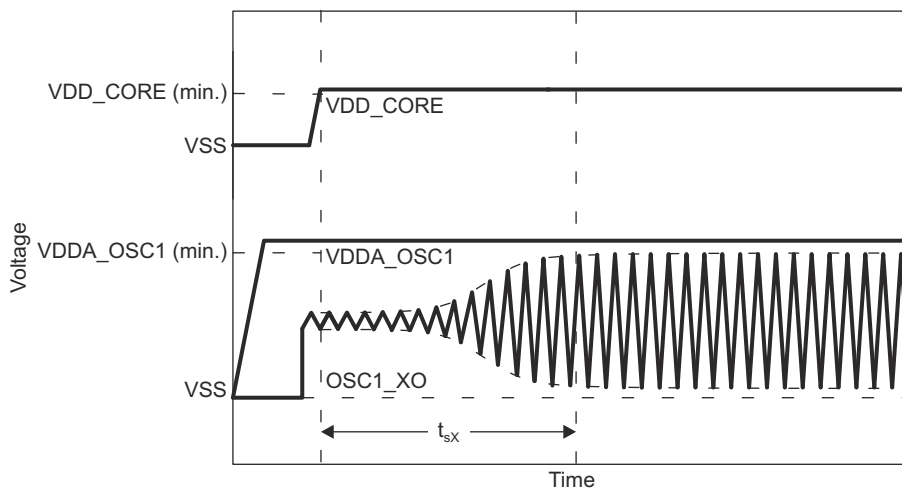
When selecting a crystal, the system design must consider the temperature and aging characteristics of a based on the worst case environment and expected life expectancy of the system.

Table 6-27 details the switching characteristics of the oscillator and the requirements of the input clock.

**Table 6-27. OSC1 Switching Characteristics – Crystal Mode**

| PARAMETER         |                             | MIN | TYP                | MAX   | UNIT |
|-------------------|-----------------------------|-----|--------------------|-------|------|
| C <sub>XI</sub>   | XI Capacitance              |     |                    | 1.139 | pF   |
| C <sub>XO</sub>   | XO Capacitance              |     |                    | 1.106 | pF   |
| C <sub>XIXO</sub> | XI to XO Mutual Capacitance |     |                    | 0.01  | pF   |
| t <sub>s</sub>    | Start-up Time               |     | 9.5 <sup>(1)</sup> |       | ms   |

- (1) TI strongly encourages each customer to submit samples of the device to the resonator/crystal vendors for validation. The vendors are equipped to determine what load capacitors will best tune their resonator/crystal to the microcontroller device for optimum startup and operation over temperature/voltage extremes.



**Figure 6-32. OSC1 Start-up Time**

#### 6.10.4.1.3.1 Load Capacitance

The crystal circuit must be designed such that it applies the appropriate capacitive load to the crystal, as defined by the crystal manufacturer. The capacitive load, C<sub>L</sub>, of this circuit is a combination of discrete capacitors C<sub>L1</sub>, C<sub>L2</sub>, and several parasitic contributions. PCB signal traces which connect crystal circuit components to OSC1\_XI and OSC1\_XO have parasitic capacitance to ground, C<sub>PCBXI</sub> and C<sub>PCBXO</sub>, where the PCB designer should be able to extract parasitic capacitance for each signal trace. The OSC1 circuits and device package have combined parasitic capacitance to ground, C<sub>PCBXI</sub> and C<sub>PCBXO</sub>, where these parasitic capacitance values are defined in Table 6-25.

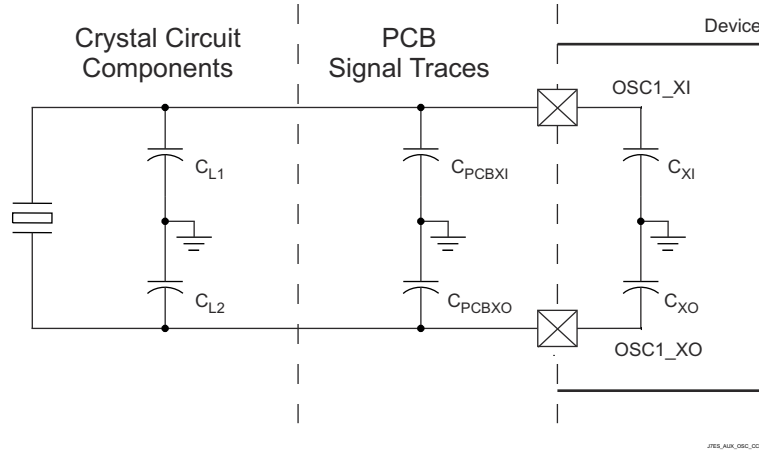


Figure 6-33. Load Capacitance

Load capacitors,  $C_{L1}$  and  $C_{L2}$  in Figure 6-26, should be chosen such that the below equation is satisfied.  $C_L$  in the equation is the load specified by the crystal manufacturer.

$$C_L = [(C_{L1} + C_{PCBXI} + C_{XI}) \times (C_{L2} + C_{PCBXO} + C_{XO})] / [(C_{L1} + C_{PCBXI} + C_{XI}) + (C_{L2} + C_{PCBXO} + C_{XO})]$$

To determine the value of  $C_{L1}$  and  $C_{L2}$ , multiply the capacitive load value  $C_L$  by 2. Using this result, subtract the combined values of  $C_{PCBXI} + C_{XI}$  to determine the value of  $C_{L1}$  and the combined values of  $C_{PCBXO} + C_{XO}$  to determine the value of  $C_{L2}$ . For example, if  $C_L = 10$  pF,  $C_{PCBXI} = 2$  pF,  $C_{XI} = 1$  pF,  $C_{PCBXO} = 2$  pF,  $C_{XO} = 1$  pF, the value of  $C_{L1} = C_{L2} = [(2C_L) - (C_{PCBXI} + C_{XI})] = [(2C_L) - (C_{PCBXO} + C_{XO})] = [(2 \times 10 \text{ pF}) - 2 \text{ pF} - 1 \text{ pF}] = 17$  pF.

#### 6.10.4.1.3.2 Shunt Capacitance

The crystal circuit must also be designed such that it does not exceed the maximum shunt capacitance for OSC1 operating conditions defined in Table 6-24. Shunt capacitance,  $C_{shunt}$ , of the crystal circuit is a combination of crystal shunt capacitance and parasitic contributions. PCB signal traces which connect crystal circuit components to OSC1 have mutual parasitic capacitance to each other,  $C_{PCBXIXO}$ , where the PCB designer should be able to extract mutual parasitic capacitance between these signal traces. The device package also has mutual parasitic capacitance,  $C_{XIXO}$ , where this mutual parasitic capacitance value is defined in Table 6-25.

PCB routing should be designed to minimize mutual capacitance between XI and XO signal traces. This is typically done by keeping signal traces short and not routing them in close proximity. Mutual capacitance can also be minimized by placing a ground trace between these signals when the layout requires them to be routed in close proximity. It is important to minimize the mutual capacitance on the PCB to provide as much margin as possible when selecting a crystal.

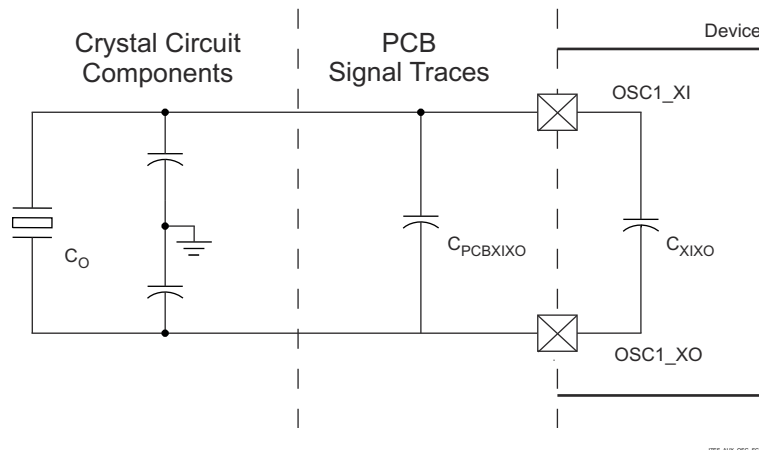


Figure 6-34. Shunt Capacitance

A crystal should be chosen such that the below equation is satisfied.  $C_O$  in the equation is the maximum shunt capacitance specified by the crystal manufacturer.

$$C_{\text{shunt}} \geq C_O + C_{\text{PCBXIXO}} + C_{\text{XIXO}}$$

For example, the equation would be satisfied when the crystal being used is 25 MHz with an ESR = 30  $\Omega$ ,  $C_{\text{PCBXIXO}} = 0.7$  pF,  $C_{\text{XIXO}} = 0.01$  pF, and shunt capacitance of the crystal is less than or equal to 6.29 pF.

#### 6.10.4.1.4 Auxiliary OSC1 LVCMOS Digital Clock Source

Figure 6-35 shows the recommended oscillator connections when OSC1\_XI is connected to a 1.8-V LVCMOS square-wave digital clock source.

#### Note

A DC steady-state condition is not allowed on OSC1\_XI when the oscillator is powered up. This is not allowed because OSC1\_XI is internally AC coupled to a comparator that may enter a unknown state when DC is applied to the input. Therefore, application software should power down OSC1 any time OSC1\_XI is not toggling between logic states.

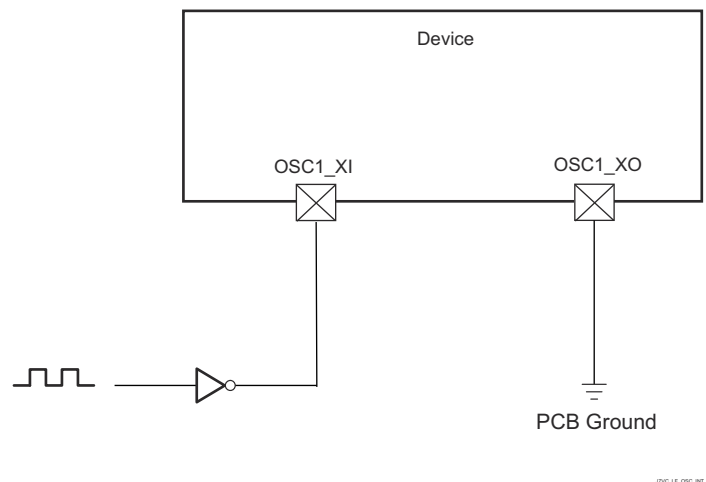


Figure 6-35. 1.8-V LVCMOS-Compatible Clock Input

#### 6.10.4.1.5 Auxiliary OSC1 Not Used

Figure 6-36 shows the recommended oscillator connections when OSC1 is not used. OSC1\_XI must be connected to VSS through an external pull resistor ( $R_{pd}$ ) to ensure this input is held to a valid low level when unused since the internal pull-down resistor is disabled by default.

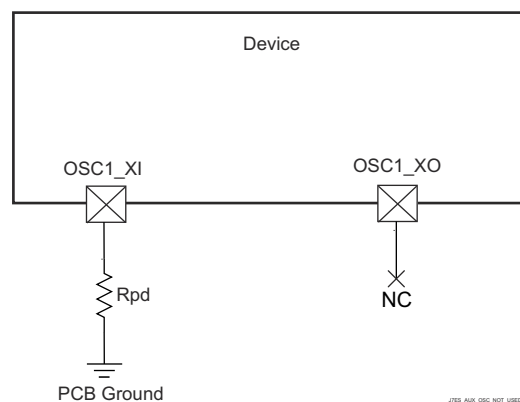


Figure 6-36. OSC1 Not Used

#### 6.10.4.1.6 WKUP\_LF\_CLKIN Internal Oscillator Clock Source

Figure 6-37 shows the recommended oscillator connections when WKUP\_LF\_CLKIN is connected to an LVCMOS square-wave digital clock source.

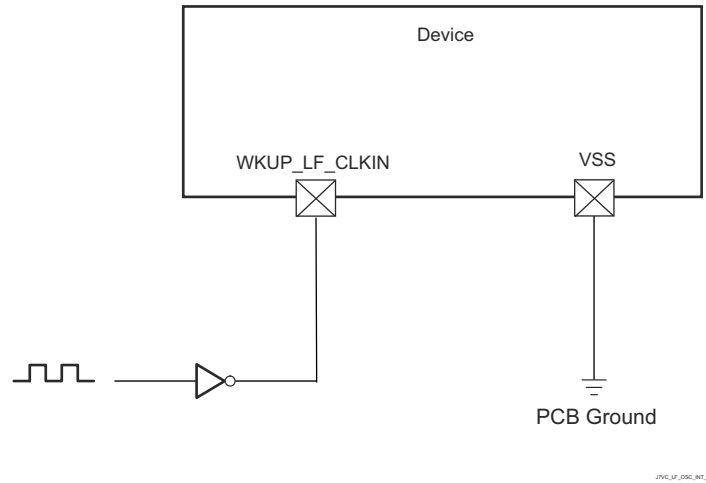


Figure 6-37. WKUP\_LF\_CLKIN Crystal Implementation

Table 6-28 details the WKUP\_LF\_CLKIN input clock timing requirements..

Table 6-28. WKUP\_LF\_CLKIN Input Clock Timing Requirements <sup>(2)</sup>

| NAME | DESCRIPTION  | MIN                  | TYP   | MAX                  | UNIT |
|------|--|----------------------|-------|----------------------|------|
| CK0  | $1 / t_c(\text{WKUP\_LF\_CLKIN})$<br>Frequency, WKUP_LF_CLKIN              |                      | 32768 |                      | Hz   |
| CK1  | $t_w(\text{WKUP\_LF\_CLKIN})$<br>Pulse duration, WKUP_LF_CLKIN low or high | $0.45 \cdot P^{(1)}$ |       | $0.55 \cdot P^{(1)}$ | ns   |

(1) P is WKUP\_LF\_CLKIN cycle time in ns.

(2) Refer to Section 6.6.7 LVCMOS Electrical Characteristics for voltage and slew rate information.

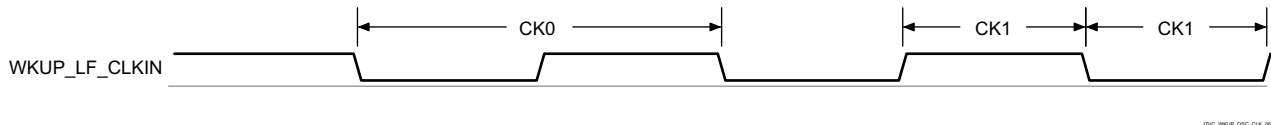
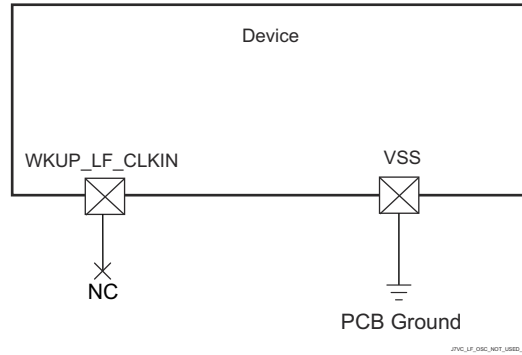


Figure 6-38. WKUP\_LF\_CLKIN Start-up Time

#### 6.10.4.1.7 WKUP\_LF\_CLKIN Not Used

Figure 6-39 shows the recommended oscillator connections when WKUP\_LF\_CLKIN is not used. WKUP\_LF\_CLKIN may be a no-connect while the oscillator remains disabled since the internal pull-down resistor is enabled by default.



**Figure 6-39. WKUP\_LF\_CLKIN Not Used**

#### 6.10.4.2 Output Clocks

The device provides several system clock outputs. Summary of these output clocks are as follows:

- **MCU\_CLKOUT0**
  - Reference clock output for Ethernet PHYs (50MHz or 25MHz)
- **MCU\_SYSCLKOUT0**
  - SYSCLK0 of WKUP\_PLLCTRL0 is divided by 6 and then sent out of the device as a LVCMOS clock signal (MCU\_SYSCLKOUT0). This signal can be used to test if the main chip clock is functioning or not.
- **MCU\_OBSCLK0**
  - On the clock output MCU\_OBSCLK0, oscillators and PLLs clocks can be observed for tests and debug.
- **SYSCLKOUT0**
  - SYSCLK0 from the MAIN\_PLL controller is divided by 6 and then sent out of the device as a LVCMOS clock signal (SYSCLKOUT0). This signal can be used to test if the main chip clock is functioning or not.
- **CLKOUT**
  - Reference clock output
- **OBSCLK[2:0]**
  - On the clock output OBSCLK0, oscillators and PLLs clocks can be observed for tests and debug.

### 6.10.4.3 PLLs

Power is supplied to the Phase-Locked Loop circuitries (PLLs) by internal regulators that derive their power from off-chip power sources.

There are total of three PLLs in the device in WKUP and MCU domains:

- MCU\_PLL0 (MCU R5FSS PLL) with WKUP\_PLLCTRL0
- MCU\_PLL1 (MCU PERIPHERAL PLL)
- MCU\_PLL2 (MCU CPSW PLL)

There are total of ten PLLs in MAIN domain:

- PLL0 (MAIN PLL) with PLLCTRL0
- PLL1 (PER0 PLL)
- PLL2 (PER1 PLL)
- PLL3 (CPSW5X PLL)
- PLL4 (AUDIO0 PLL)
- PLL7 (MSMC PLL)
- PLL8 (ARM0 PLL)
- PLL12 (DDR PLL)
- PLL13 (C66 PLL)
- PLL14 (R5FSS PLL)

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#### Note

For more information, see:

- *Device Configuration / Clocking / PLLs* section in the device TRM.
  - *Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem - Gigabit (PRU)* section in the device TRM.
- 

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#### Note

The input reference clock (OSC1\_XI/OSC1\_XO) is specified and the lock time is ensured by the PLL controller, as documented in the *Device Configuration* chapter in the device TRM.

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### 6.10.4.4 Recommended Clock and Control Signal Transition Behavior

All clocks and strobe signals must transition between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ) in a monotonic manner. Monotonic transitions are more easily ensured with faster switching signals. Slower input transitions are more susceptible to glitches due to noise, and special care must be taken for slow input clocks.

### 6.10.4.5 Interface Clock Specifications

#### 6.10.4.5.1 Interface Clock Terminology

The interface clock is used at the system level to sequence the data and to control transfers accordingly with the interface protocol.

#### 6.10.4.5.2 Interface Clock Frequency

The two interface clock characteristics are:

- The maximum clock frequency
- The maximum operating frequency

The interface clock frequency documented here is the maximum clock frequency, which corresponds to the maximum frequency programmable on this output clock. This frequency defines the maximum limit supported by the Device IC and does not take into account any system consideration (PCB, peripherals).

The system designer must take into account these system considerations and the Device IC timing characteristics to properly define the maximum operating frequency that corresponds to the maximum frequency supported to transfer the data on this interface.

## 6.10.5 Peripherals

### 6.10.5.1 ATL

The device contains ATL module that can be used for asynchronous sample rate conversion of audio. The ATL calculates the error between two time bases, such as audio syncs, and optionally generates an averaged clock using cycle stealing via software.

#### Note

For more information about ATL, see *Audio Tracking Logic (ATL)* section in *Peripherals* chapter in the device TRM.

Table 6-29 represents ATL timing conditions.

**Table 6-29. ATL Timing Conditions**

| PARAMETER                |                         | MODE                   | MIN | MAX | UNIT |
|--------------------------|-------------------------|------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |                        |     |     |      |
| SR <sub>I</sub>          | Input slew rate         | External reference CLK | 0.5 | 5   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |                        |     |     |      |
| C <sub>L</sub>           | Output load capacitance | Internal reference CLK | 1   | 10  | pF   |

Section 6.10.5.1.1, Section 6.10.5.1.2, Section 6.10.5.1.3, and Section 6.10.5.1.4 present timing requirements and switching characteristics for ATL.

#### 6.10.5.1.1 ATL\_PCLK Timing Requirements

| NO. | PARAMETER             |                               | MODE                   | MIN                           | MAX | UNIT |
|-----|-----------------------|-------------------------------|------------------------|-------------------------------|-----|------|
| D1  | t <sub>c(pclk)</sub>  | Cycle time, ATL_PCLK          | External reference CLK | 5                             |     | ns   |
| D2  | t <sub>w(pclkL)</sub> | Pulse Duration, ATL_PCLK low  | External reference CLK | 0.45 × M <sup>(1)</sup> + 2.5 |     | ns   |
| D3  | t <sub>w(pclkH)</sub> | Pulse Duration, ATL_PCLK high | External reference CLK | 0.45 × M <sup>(1)</sup> + 2.5 |     | ns   |

(1) M = ATL\_CLK[x] period

#### 6.10.5.1.2 ATL\_AWS[x] Timing Requirements

| NO. | PARAMETER            |  | MODE                   | MIN                           | MAX | UNIT |
|-----|----------------------|--|------------------------|-------------------------------|-----|------|
| D4  | t <sub>c(aws)</sub>  | Cycle Time, ATL_AWS[x] <sup>(3)</sup>          | External reference CLK | 2 × M <sup>(1)</sup>          |     | ns   |
| D5  | t <sub>w(awsL)</sub> | Pulse Duration, ATL_AWS[x] <sup>(3)</sup> low  | External reference CLK | 0.45 × A <sup>(2)</sup> + 2.5 |     | ns   |
| D6  | t <sub>w(awsH)</sub> | Pulse Duration, ATL_AWS[x] <sup>(3)</sup> high | External reference CLK | 0.45 × A <sup>(2)</sup> + 2.5 |     | ns   |

(1) M = ATL\_CLK[x] period

(2) A = ATL\_AWS[x] period

(3) x = 0 to 3

#### 6.10.5.1.3 ATL\_BWS[x] Timing Requirements

| NO. | PARAMETER            |   | MODE                     | MIN                           | MAX | UNIT |
|-----|----------------------|---|--------------------------|-------------------------------|-----|------|
| D7  | t <sub>c(bws)</sub>  | Cycle Time, ATL_BWS[x] <sup>(3)</sup>         | External reference clock | 2 × M <sup>(1)</sup>          |     | ns   |
| D8  | t <sub>w(bwsL)</sub> | Pulse Duration, ATL_BWS[x] low <sup>(3)</sup> | External reference clock | 0.45 × B <sup>(2)</sup> + 2.5 |     | ns   |

| NO. |               |   | MODE                     | MIN                         | MAX | UNIT |
|-----|---------------|---|--------------------------|-----------------------------|-----|------|
| D9  | $t_{w(bwsh)}$ | Pulse Duration, ATCL_BWS[x] high <sup>(3)</sup> | External reference clock | $0.45 \times B^{(2)} + 2.5$ |     | ns   |

- (1) M = ATCL\_CLK[x] period  
(2) B = ATCL\_BWS[x] period  
(3) x = 0 to 3

#### 6.10.5.1.4 ATCLK[x] Switching Characteristics

| NO. | PARAMETER       |  | MODE                   | MIN                                   | MAX | UNIT |
|-----|-----------------|--|------------------------|---------------------------------------|-----|------|
| D10 | $t_{c(atclk)}$  | Cycle time, ATCLK[x] <sup>(3)</sup>          | Internal reference CLK | 20                                    |     | ns   |
| D11 | $t_{w(atclkL)}$ | Pulse Duration, ATCLK[x] low <sup>(3)</sup>  | Internal reference CLK | $0.45 \times P^{(2)} - M^{(1)} - 0.3$ |     | ns   |
| D12 | $t_{w(atclkH)}$ | Pulse Duration, ATCLK[x] high <sup>(3)</sup> | Internal reference CLK | $0.45 \times P^{(2)} - M^{(1)} - 0.3$ |     | ns   |

- (1) M = ATCL\_CLK[x] period  
(2) P = ATCLK[x] period  
(3) x = 0 to 3

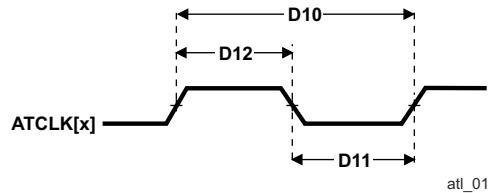


Figure 6-40. ATCLK[x] Timing

#### 6.10.5.2 CPSW2G

For more details about features and additional description information on the device Gigabit Ethernet MAC, see the corresponding sections within [Section 5.3, Signal Descriptions](#) and [Section 7, Detailed Description](#).

Table 6-30 represents CPSW2G timing conditions.

Table 6-30. CPSW2G Timing Conditions

| PARAMETER                            | DESCRIPTION                                  |   | MIN | MAX | UNIT |
|--------------------------------------|--|---|-----|-----|------|
| <b>INPUT CONDITIONS</b>              |  |   |     |     |      |
| $t_R$                                | Input signal rise time                       |   | 1   | 5   | V/ns |
| $t_F$                                | Input signal fall time                       |   | 1   | 5   | V/ns |
| <b>OUTPUT CONDITIONS</b>             |  |   |     |     |      |
| $C_{LOAD}$                           | Output load capacitance                      |   | 2   | 20  | pF   |
| <b>PCB CONNECTIVITY REQUIREMENTS</b> |  |   |     |     |      |
| $t_d$ (Trace Mismatch Delay)         | Propagation delay mismatch across all traces | RGMII[x]_RXC,<br>RGMII[x]_RD[3:0],<br>RGMII[x]_RX_CTL |     | 50  | ps   |
|                                      |  | RGMII[x]_TXC,<br>RGMII[x]_TD[3:0],<br>RGMII[x]_TX_CTL |     | 50  | ps   |

##### 6.10.5.2.1 CPSW2G RMII Timings

[Section 6.10.5.2.1.1](#), [Section 6.10.5.2.1.2](#), and [Figure 6-41](#) present timing requirements for CPSW2G RMII receive.

6.10.5.2.1.1 Timing Requirements for RMII[x]\_REFCLK – RMII Mode

| NO.   | PARAMETER          | DESCRIPTION                  | MIN    | TYP | MAX    | UNIT |
|-------|--------------------|------------------------------|--------|-----|--------|------|
| RMII1 | $t_{c(REF\_CLK)}$  | Cycle time, REF_CLK          | 19.999 |     | 20.001 | ns   |
| RMII2 | $t_{w(REF\_CLKH)}$ | Pulse Duration, REF_CLK High | 7      |     | 13     | ns   |
| RMII3 | $t_{w(REF\_CLKL)}$ | Pulse Duration, REF_CLK Low  | 7      |     | 13     | ns   |

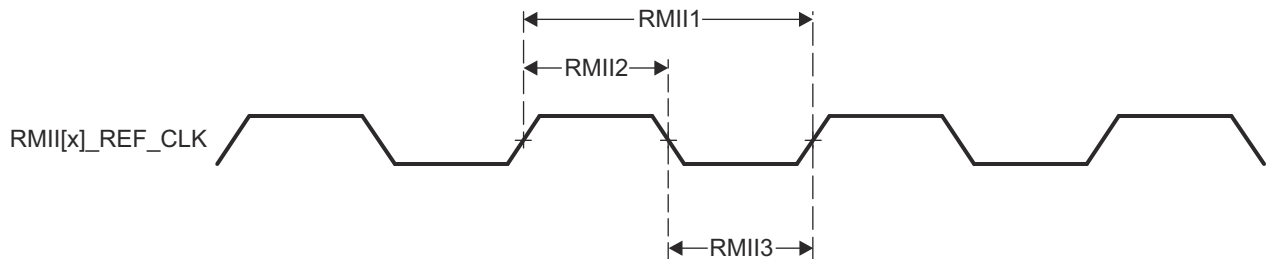


Figure 6-41. RMII[x]\_REFCLK Timing – RMII Mode

6.10.5.2.1.2 Timing Requirements for RMII[x]\_RXD[1:0], RMII[x]\_CRS\_DV, and RMII[x]\_RXER – RMII Mode

| NO.   | PARAMETER                  | DESCRIPTION                               | MIN | TYP | MAX | UNIT |
|-------|----------------------------|---|-----|-----|-----|------|
| RMII4 | $t_{su(RXD-REF\_CLK)}$     | Setup time, RXD[1:0] valid before REF_CLK | 4   |     |     | ns   |
|       | $t_{su(CRS\_DV-REF\_CLK)}$ | Setup time, CRS_DV valid before REF_CLK   | 4   |     |     | ns   |
|       | $t_{su(RX\_ER-REF\_CLK)}$  | Setup time, RX_ER valid before REF_CLK    | 4   |     |     | ns   |
| RMII5 | $t_{h(REF\_CLK-RXD)}$      | Hold time RXD[1:0] valid after REF_CLK    | 2   |     |     | ns   |
|       | $t_{h(REF\_CLK-CRS\_DV)}$  | Hold time, CRS_DV valid after REF_CLK     | 2   |     |     | ns   |
|       | $t_{h(REF\_CLK-RX\_ER)}$   | Hold time, RX_ER valid after REF_CLK      | 2   |     |     | ns   |

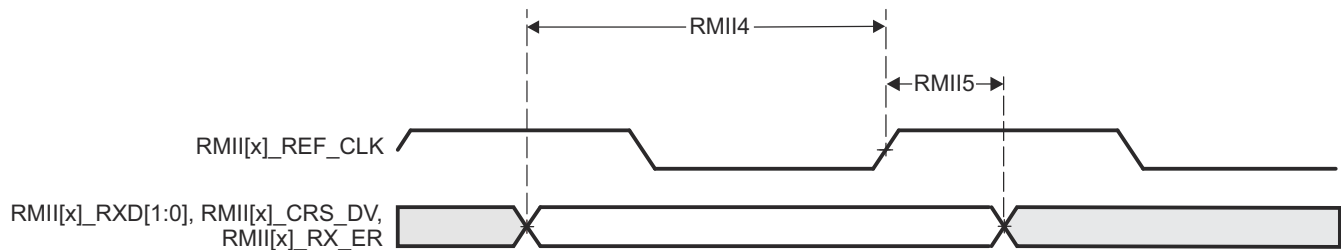


Figure 6-42. RMII[x]\_RXD[1:0], RMII[x]\_CRS\_DV, RMII[x]\_RXER Timing – RMII Mode

Section 6.10.5.2.1.3, and Section 6.10.5.2.1.3, present switching characteristics for CPSW2G RMII Transmit.

6.10.5.2.1.3 Switching Characteristics for RMII[x]\_TXD[1:0], and RMII[x]\_TXEN – RMII Mode

| NO.   | PARAMETER            | DESCRIPTION                                | MIN | TYP | MAX | UNIT |
|-------|----------------------|--|-----|-----|-----|------|
| RMII6 | $t_d(REF\_CLK-TXD)$  | Delay time, REF_CLK High to TXD[1:0] valid | 2   |     | 10  | ns   |
|       | $t_d(REF\_CLK-TXEN)$ | Delay time, REF_CLK to TXEN valid          | 2   |     | 10  | ns   |
| RMII7 | $t_r(TXD)$           | Rise Time, TXD Outputs                     | 1   |     | 5   | ns   |
|       | $t_r(TX\_EN)$        | Rise Time, TX_EN Output                    | 1   |     | 5   | ns   |
| RMII8 | $t_f(TXD)$           | Fall Time, TXD Outputs                     | 1   |     | 5   | ns   |
|       | $t_f(TX\_EN)$        | Fall Time, TX_EN Output                    | 1   |     | 5   | ns   |

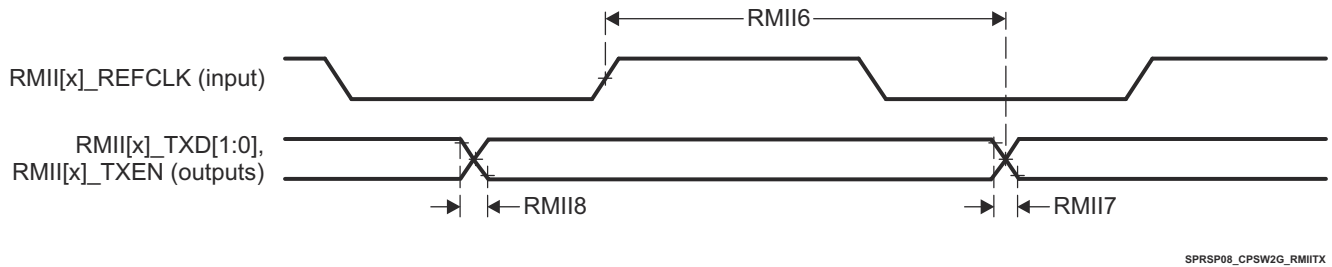


Figure 6-43. SPI Master Mode Receive Timing

### 6.10.5.2.2 CPSW2G RGMII Timings

Section 6.10.5.2.2.1, Section 6.10.5.2.2.2, and Figure 6-44 present timing requirements for receive RGMII operation.

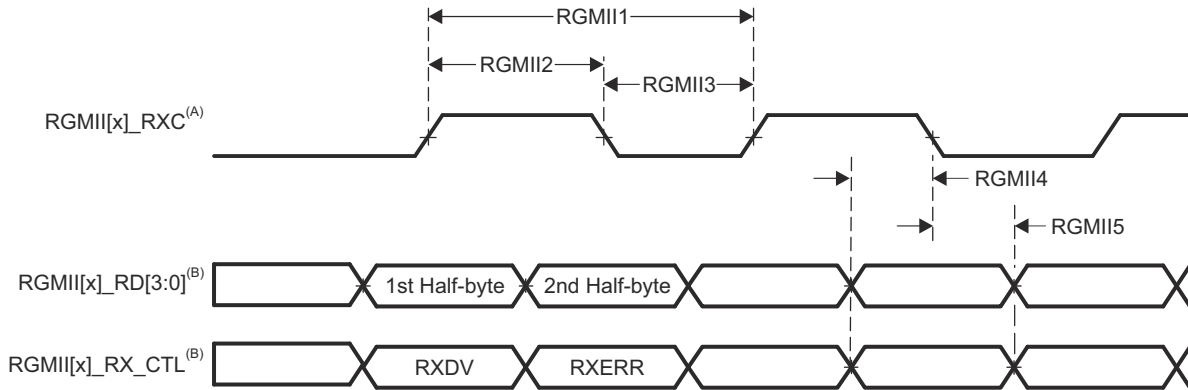
#### 6.10.5.2.2.1 Timing Requirements for RGMII[x]\_RCLK – RGMII Mode

| NO.    | PARAMETER     | DESCRIPTION              | MODE     | MIN | TYP | MAX  | UNIT |
|--------|---------------|--------------------------|----------|-----|-----|------|------|
| RGMII1 | $t_{c(RXC)}$  | Cycle time, RXC          | 10Mbps   | 360 |     | 440  | ns   |
|        |               |                          | 100Mbps  | 36  |     | 44   | ns   |
|        |               |                          | 1000Mbps | 7.2 |     | 8.8  | ns   |
| RGMII2 | $t_{w(RXCH)}$ | Pulse duration, RXC high | 10Mbps   | 160 |     | 240  | ns   |
|        |               |                          | 100Mbps  | 16  |     | 24   | ns   |
|        |               |                          | 1000Mbps | 3.6 |     | 4.4  | ns   |
| RGMII3 | $t_{w(RXCL)}$ | Pulse duration, RXC low  | 10Mbps   | 160 |     | 240  | ns   |
|        |               |                          | 100Mbps  | 16  |     | 24   | ns   |
|        |               |                          | 1000Mbps | 3.6 |     | 4.4  | ns   |
| RGMII4 | $t_{t(RXC)}$  | Transition time, RXC     | 10Mbps   |     |     | 0.75 | ns   |
|        |               |                          | 100Mbps  |     |     | 0.75 | ns   |
|        |               |                          | 1000Mbps |     |     | 0.75 | ns   |

#### 6.10.5.2.2.2 Timing Requirements for RGMII[x]\_RD[3:0], and RGMII[x]\_RCTL – RGMII Mode

| NO.    | PARAMETER             | DESCRIPTION                                   | MODE     | MIN | TYP | MAX | UNIT |
|--------|-----------------------|---|----------|-----|-----|-----|------|
| RGMII5 | $t_{su(RD-RXC)}$      | Setup time, RD[3:0] valid before RXC high/low | 10Mbps   | 1   |     |     | ns   |
|        |                       |   | 100Mbps  | 1   |     |     | ns   |
|        |                       |   | 1000Mbps | 1   |     |     | ns   |
|        | $t_{su(RX\_CTL-RXC)}$ | Setup time, RX_CTL valid before RXC high/low  | 10Mbps   | 1   |     |     | ns   |
|        |                       |   | 100Mbps  | 1   |     |     | ns   |
|        |                       |   | 1000Mbps | 1   |     |     | ns   |
| RGMII6 | $t_{h(RXC-RD)}$       | Hold time, RD[3:0] valid after RXC high/low   | 10Mbps   | 1   |     |     | ns   |
|        |                       |   | 100Mbps  | 1   |     |     | ns   |
|        |                       |   | 1000Mbps | 1   |     |     | ns   |
|        | $t_{h(RXC-RX\_CTL)}$  | Hold time, RX_CTL valid after RXC high/low    | 10Mbps   | 1   |     |     | ns   |
|        |                       |   | 100Mbps  | 1   |     |     | ns   |
|        |                       |   | 1000Mbps | 1   |     |     | ns   |

| NO.    | PARAMETER       | DESCRIPTION             | MODE     | MIN | TYP | MAX  | UNIT |
|--------|-----------------|-------------------------|----------|-----|-----|------|------|
| RGMII7 | $t_{(RD)}$      | Transition time, RD     | 10Mbps   |     |     | 0.75 | ns   |
|        |                 |                         | 100Mbps  |     |     | 0.75 | ns   |
|        |                 |                         | 1000Mbps |     |     | 0.75 | ns   |
|        | $t_{(RX\_CTL)}$ | Transition time, RX_CTL | 10Mbps   |     |     | 0.75 | ns   |
|        |                 |                         | 100Mbps  |     |     | 0.75 | ns   |
|        |                 |                         | 1000Mbps |     |     | 0.75 | ns   |



- A. RGMII\_RXC must be externally delayed relative to the data and control pins.
- B. Data and control information is received using both edges of the clocks. RGMII\_RXD[3:0] carries data bits 3-0 on the rising edge of RGMII\_RXC and data bits 7-4 on the falling edge of RGMII\_RXC. Similarly, RGMII\_RXCTL carries RXDV on rising edge of RGMII\_RXC and RXERR on falling edge of RGMII\_RXC.

**Figure 6-44. CPSW2G Receive Interface Timing, RGMII Operation**

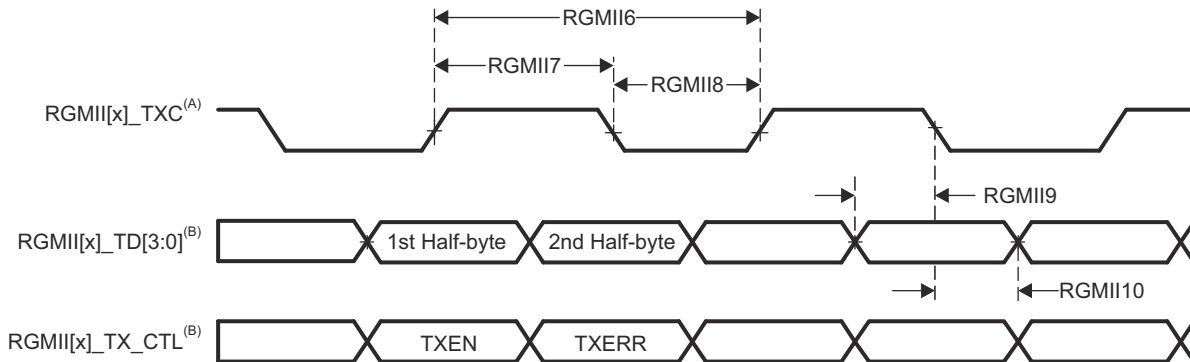
Section 6.10.5.2.2.3, Section 6.10.5.2.2.4, and Figure 6-45 present switching characteristics for transmit - RGMII for 10 Mbps, 100 Mbps, and 1000 Mbps.

**6.10.5.2.2.3 Switching Characteristics for RGMII[x]\_TCLK – RGMII Mode**

| NO.    | PARAMETER     | DESCRIPTION              | MODE     | MIN | TYP | MAX  | UNIT |
|--------|---------------|--------------------------|----------|-----|-----|------|------|
| RGMII1 | $t_{c(TXC)}$  | Cycle time, TXC          | 10Mbps   | 360 |     | 440  | ns   |
|        |               |                          | 100Mbps  | 36  |     | 44   | ns   |
|        |               |                          | 1000Mbps | 7.2 |     | 8.8  | ns   |
| RGMII2 | $t_{w(TXCH)}$ | Pulse duration, TXC high | 10Mbps   | 160 |     | 240  | ns   |
|        |               |                          | 100Mbps  | 16  |     | 24   | ns   |
|        |               |                          | 1000Mbps | 3.6 |     | 4.4  | ns   |
| RGMII3 | $t_{w(TXCL)}$ | Pulse duration, TXC low  | 10Mbps   | 160 |     | 240  | ns   |
|        |               |                          | 100Mbps  | 16  |     | 24   | ns   |
|        |               |                          | 1000Mbps | 3.6 |     | 4.4  | ns   |
| RGMII4 | $t_{t(TXC)}$  | Transition time, TXC     | 10Mbps   |     |     | 0.75 | ns   |
|        |               |                          | 100Mbps  |     |     | 0.75 | ns   |
|        |               |                          | 1000Mbps |     |     | 0.75 | ns   |

6.10.5.2.4 Switching Characteristics for RGMII[x]\_TD[3:0], and RGMII[x]\_TCTL – RGMII Mode

| NO.    | PARAMETER                     | DESCRIPTION  | MODE     | MIN  | TYP | MAX | UNIT |
|--------|-------------------------------|--|----------|------|-----|-----|------|
| RGMII5 | t <sub>osu</sub> (TD-TXC)     | Output setup time, RGMII[x]_TD[3:0] valid to RGMII[x]_TXC high/low   | 10Mbps   | 1.2  |     |     | ns   |
|        |                               |  | 100Mbps  | 1.2  |     |     | ns   |
|        |                               |  | 1000Mbps | 1.05 |     |     | ns   |
|        | t <sub>osu</sub> (TX_CTL-TXC) | Output setup time, RGMII[x]_TX_CTL valid to RGMII[x]_TXC high/low    | 10Mbps   | 1.2  |     |     | ns   |
|        |                               |  | 100Mbps  | 1.2  |     |     | ns   |
|        |                               |  | 1000Mbps | 1.05 |     |     | ns   |
| RGMII6 | t <sub>oh</sub> (TD-TXC)      | Output hold time, RGMII[x]_TD[3:0] valid after RGMII[x]_TXC high/low | 10Mbps   | 1.2  |     |     | ns   |
|        |                               |  | 100Mbps  | 1.2  |     |     | ns   |
|        |                               |  | 1000Mbps | 1.0  |     |     | ns   |
|        | t <sub>oh</sub> (TX_CTL-TXC)  | Output hold time, RGMII[x]_TX_CTL valid after RGMII[x]_TXC high/low  | 10Mbps   | 1.2  |     |     | ns   |
|        |                               |  | 100Mbps  | 1.2  |     |     | ns   |
|        |                               |  | 1000Mbps | 1.05 |     |     | ns   |



- A. TXC is delayed internally before being driven to the RGMII[x]\_TXC pin. This internal delay is always enabled.
- B. Data and control information is received using both edges of the clocks. RGMII\_TD[3:0] carries data bits 3-0 on the rising edge of RGMII\_TXC and data bits 7-4 on the falling edge of RGMII\_TXC. Similarly, RGMII\_TX\_CTL carries TXDV on rising edge of RGMII\_TXC and RTXERR on falling edge of RGMII\_TXC.

Figure 6-45. CPSW2G Transmit Interface Timing RGMII Mode

For more information, see *Gigabit Ethernet MAC (MCU\_CPSW0)* section in *Peripherals* chapter in the device TRM.

6.10.5.3 CPSW5G

The Gigabit Ethernet MAC supports standards shown in Table 6-31.

Table 6-31. CPSW5G Supported Standards

| INDUSTRIAL STANDARDS | BAUD <sup>(1)</sup> | LINK/ DATA RATE <sup>(1)</sup> |
|----------------------|---------------------|--------------------------------|
| USXGMII/ XFI         | 5.15625 GBaud       | 5 Gbps                         |
|                      | 10.3125 GBaud       | 10 Gbps                        |
| QSGMII               | 5 GBaud             | 4x 1Gbps                       |
| XAUI (2.5G SGMII)    | 3.125 GBaud         | 2.5 Gbps                       |
| 1G SGMII             | 1.25 GBaud          | 1 Gbps                         |

(1) Lower data rates are achieved through replication

For more details about features and additional description on the device Gigabit Ethernet MAC, see the corresponding sections within Section 5.3, *Signal Descriptions* and Section 7, *Detailed Description*.

Table 6-32 represents CPSW5G timing conditions.

**Table 6-32. CPSW5G Timing Conditions**

| PARAMETER                            | DESCRIPTION                                  | MIN   | MAX | UNIT |
|--------------------------------------|--|---|-----|------|
| <b>INPUT CONDITIONS</b>              |  |   |     |      |
| $t_R$                                | Input signal rise time                       | 1   | 5   | V/ns |
| $t_F$                                | Input signal fall time                       | 1   | 5   | V/ns |
| <b>OUTPUT CONDITIONS</b>             |  |   |     |      |
| $C_{LOAD}$                           | Output load capacitance                      | 2   | 20  | pF   |
| <b>PCB CONNECTIVITY REQUIREMENTS</b> |  |   |     |      |
| $t_d$ (Trace Mismatch Delay)         | Propagation delay mismatch across all traces | RGMII[x]_RXC,<br>RGMII[x]_RD[3:0],<br>RGMII[x]_RX_CTL | 50  | ps   |
|                                      |  | RGMII[x]_TXC,<br>RGMII[x]_TD[3:0],<br>RGMII[x]_TX_CTL | 50  | ps   |

**6.10.5.3.1 CPSW5G MDIO Interface Timings**

Table 6-33, Table 6-34, Table 6-35, and Figure 6-46 present timing requirements for MDIO.

**Table 6-33. CPSW5G MDIO Timing Conditions**

| PARAMETER                | DESCRIPTION             | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| $SR_i$                   | Input signal slew rate  | 0.9 | 3.6 | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| $C_L$                    | Output load capacitance | 10  | 470 | pF   |

**Table 6-34. Timing Requirements for MDIO Input**

| NO.   | PARAMETER           | DESCRIPTION                                      | MIN | MAX | UNIT |
|-------|---------------------|--|-----|-----|------|
| MDIO1 | $t_{su(MDIO\_MDC)}$ | Setup time, MDIO_DATA valid before MDIO_CLK high | 90  |     | ns   |
| MDIO2 | $t_{h(MDIO\_MDC)}$  | Hold time, MDIO_DATA valid after MDIO_CLK high   | 0   |     | ns   |

**Table 6-35. Switching Characteristics Over Recommended Operating Conditions for MDIO Output**

| NO.   | PARAMETER        | DESCRIPTION                                  | MIN  | MAX | UNIT |
|-------|------------------|--|------|-----|------|
| MDIO3 | $t_c(MDC)$       | Cycle time, MDIO_CLK                         | 400  |     | ns   |
| MDIO4 | $t_w(MDCH)$      | Pulse Duration, MDIO_CLK high                | 160  |     | ns   |
| MDIO5 | $t_w(MDCL)$      | Pulse Duration, MDIO_CLK low                 | 160  |     | ns   |
| MDIO6 | $t_t(MDC)$       | Transition time, MDIO_CLK                    |      | 5   | ns   |
| MDIO7 | $t_d(MDC\_MDIO)$ | Delay time, MDIO_CLK High to MDIO_DATA valid | -150 | 150 | ns   |

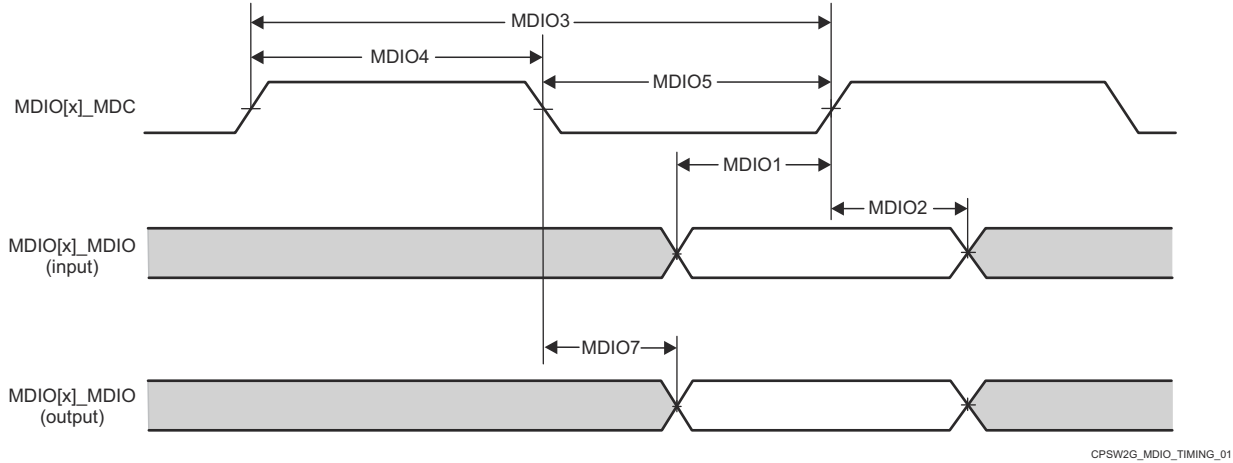


Figure 6-46. CPSW5G MDIO Diagrams Receive and Transmit

### 6.10.5.3.2 CPSW5G RMIITimings

Section 6.10.5.3.2.1, Section 6.10.5.3.2.2, and Figure 6-47 present timing requirements for CPSW5G RMI receive.

#### 6.10.5.3.2.1 Timing Requirements for RMI[x]\_REFCLK – RMI Mode

| NO.  | PARAMETER          | DESCRIPTION                  | MIN    | TYP    | MAX | UNIT |
|------|--------------------|------------------------------|--------|--------|-----|------|
| RMI1 | $t_{c(REF\_CLK)}$  | Cycle time, REF_CLK          | 19.999 | 20.001 |     | ns   |
| RMI2 | $t_{w(REF\_CLKH)}$ | Pulse Duration, REF_CLK High | 7      |        | 13  | ns   |
| RMI3 | $t_{w(REF\_CLKL)}$ | Pulse Duration, REF_CLK Low  | 7      |        | 13  | ns   |

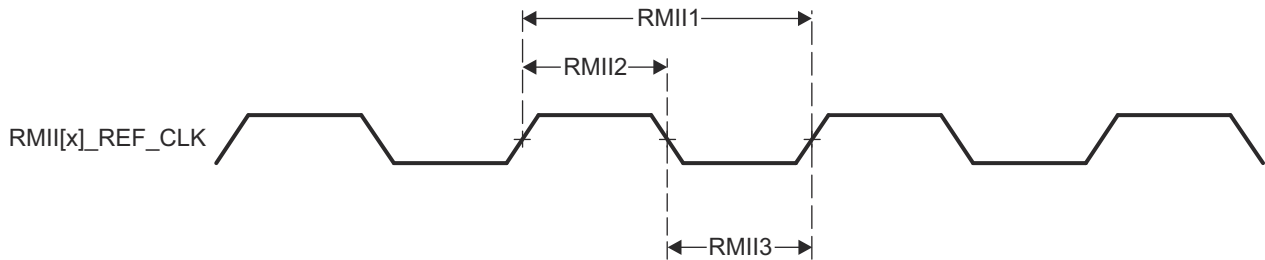
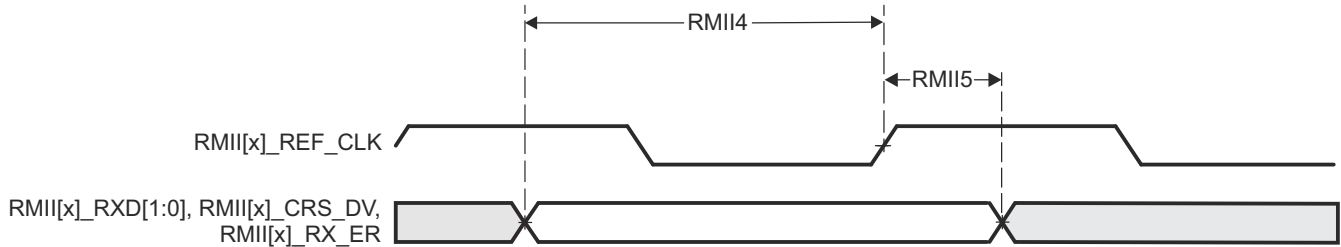


Figure 6-47. RMI[x]\_REFCLK Timing – RMI Mode

#### 6.10.5.3.2.2 Timing Requirements for RMI[x]\_RXD[1:0], RMI[x]\_CRS\_DV, and RMI[x]\_RXER – RMI Mode

| NO.  | PARAMETER                  | DESCRIPTION                               | MIN | TYP | MAX | UNIT |
|------|----------------------------|---|-----|-----|-----|------|
| RMI4 | $t_{su(RXD-REF\_CLK)}$     | Setup time, RXD[1:0] valid before REF_CLK | 4   |     |     | ns   |
|      | $t_{su(CRS\_DV-REF\_CLK)}$ | Setup time, CRS_DV valid before REF_CLK   | 4   |     |     | ns   |
|      | $t_{su(RX\_ER-REF\_CLK)}$  | Setup time, RX_ER valid before REF_CLK    | 4   |     |     | ns   |
| RMI5 | $t_{h(REF\_CLK-RXD)}$      | Hold time RXD[1:0] valid after REF_CLK    | 2   |     |     | ns   |
|      | $t_{h(REF\_CLK-CRS\_DV)}$  | Hold time, CRS_DV valid after REF_CLK     | 2   |     |     | ns   |
|      | $t_{h(REF\_CLK-RX\_ER)}$   | Hold time, RX_ER valid after REF_CLK      | 2   |     |     | ns   |



**Figure 6-48. RMII[x]\_RXD[1:0], RMII[x]\_CRS\_DV, RMII[x]\_RXER Timing – RMII Mode**

Section 6.10.5.3.2.3, Section 6.10.5.2.1.3, and present switching characteristics for CPSW5G RMII transmit.

**6.10.5.3.2.3 Switching Characteristics for RMII[x]\_TXD[1:0], and RMII[x]\_TXEN – RMII Mode**

| NO.   | PARAMETER              | DESCRIPTION                                | MIN | TYP | MAX | UNIT |
|-------|------------------------|--|-----|-----|-----|------|
| RMII6 | $t_{d(REF\_CLK-TXD)}$  | Delay time, REF_CLK High to TXD[1:0] valid | 2   |     | 10  | ns   |
|       | $t_{d(REF\_CLK-TXEN)}$ | Delay time, REF_CLK to TXEN valid          | 2   |     | 10  | ns   |
| RMII7 | $t_{r(TXD)}$           | Rise Time, TXD Outputs                     | 1   |     | 5   | ns   |
|       | $t_{r(TX\_EN)}$        | Rise Time, TX_EN Output                    | 1   |     | 5   | ns   |
| RMII8 | $t_{f(TXD)}$           | Fall Time, TXD Outputs                     | 1   |     | 5   | ns   |
|       | $t_{f(TX\_EN)}$        | Fall Time, TX_EN Output                    | 1   |     | 5   | ns   |

**6.10.5.3.3 CPSW5G RGMII Timings**

Section 6.10.5.3.3.1, Section 6.10.5.3.3.2, and Figure 6-49 present timing requirements for receive RGMII operation.

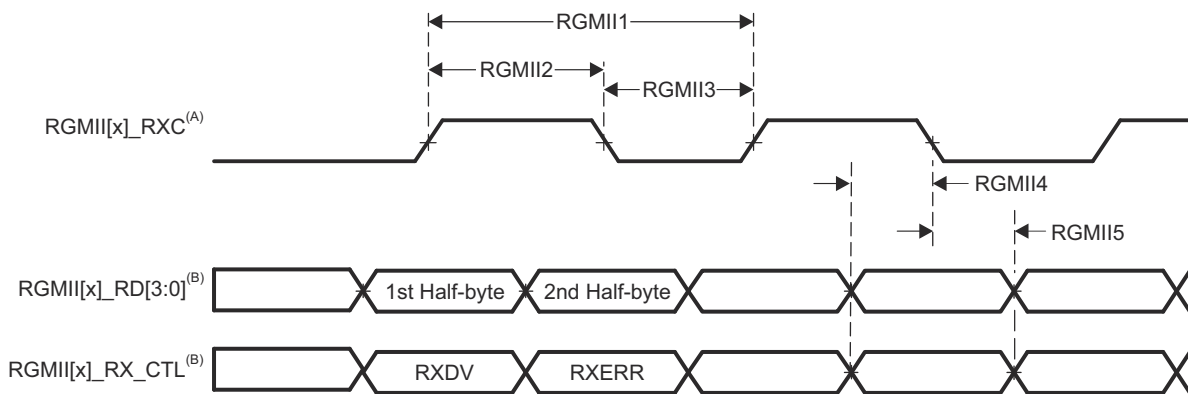
**6.10.5.3.3.1 Timing Requirements for RGMII[x]\_RCLK – RGMII Mode**

| NO.    | PARAMETER     | DESCRIPTION              | MODE     | MIN | TYP | MAX  | UNIT |
|--------|---------------|--------------------------|----------|-----|-----|------|------|
| RGMII1 | $t_{c(RXC)}$  | Cycle time, RXC          | 10Mbps   | 360 |     | 440  | ns   |
|        |               |                          | 100Mbps  | 36  |     | 44   | ns   |
|        |               |                          | 1000Mbps | 7.2 |     | 8.8  | ns   |
| RGMII2 | $t_{w(RXCH)}$ | Pulse duration, RXC high | 10Mbps   | 160 |     | 240  | ns   |
|        |               |                          | 100Mbps  | 16  |     | 24   | ns   |
|        |               |                          | 1000Mbps | 3.6 |     | 4.4  | ns   |
| RGMII3 | $t_{w(RXCL)}$ | Pulse duration, RXC low  | 10Mbps   | 160 |     | 240  | ns   |
|        |               |                          | 100Mbps  | 16  |     | 24   | ns   |
|        |               |                          | 1000Mbps | 3.6 |     | 4.4  | ns   |
| RGMII4 | $t_{t(RXC)}$  | Transition time, RXC     | 10Mbps   |     |     | 0.75 | ns   |
|        |               |                          | 100Mbps  |     |     | 0.75 | ns   |
|        |               |                          | 1000Mbps |     |     | 0.75 | ns   |

**6.10.5.3.3.2 Timing Requirements for RGMII[x]\_RD[3:0], and RGMII[x]\_RCTL – RGMII Mode**

| NO.    | PARAMETER             | DESCRIPTION                                   | MODE     | MIN | TYP | MAX | UNIT |
|--------|-----------------------|---|----------|-----|-----|-----|------|
| RGMII5 | $t_{su(RD-RXC)}$      | Setup time, RD[3:0] valid before RXC high/low | 10Mbps   | 1   |     |     | ns   |
|        |                       |   | 100Mbps  | 1   |     |     | ns   |
|        |                       |   | 1000Mbps | 1   |     |     | ns   |
|        | $t_{su(RX\_CTL-RXC)}$ | Setup time, RX_CTL valid before RXC high/low  | 10Mbps   | 1   |     |     | ns   |
|        |                       |   | 100Mbps  | 1   |     |     | ns   |
|        |                       |   | 1000Mbps | 1   |     |     | ns   |

| NO.    | PARAMETER            | DESCRIPTION                                 | MODE     | MIN | TYP | MAX  | UNIT |
|--------|----------------------|---|----------|-----|-----|------|------|
| RGMII6 | $t_{h(RXC-RD)}$      | Hold time, RD[3:0] valid after RXC high/low | 10Mbps   | 1   |     |      | ns   |
|        |                      |   | 100Mbps  | 1   |     |      | ns   |
|        |                      |   | 1000Mbps | 1   |     |      | ns   |
|        | $t_{h(RXC-RX\_CTL)}$ | Hold time, RX_CTL valid after RXC high/low  | 10Mbps   | 1   |     |      | ns   |
|        |                      |   | 100Mbps  | 1   |     |      | ns   |
|        |                      |   | 1000Mbps | 1   |     |      | ns   |
| RGMII7 | $t_{t(RD)}$          | Transition time, RD                         | 10Mbps   |     |     | 0.75 | ns   |
|        |                      |   | 100Mbps  |     |     | 0.75 | ns   |
|        |                      |   | 1000Mbps |     |     | 0.75 | ns   |
|        | $t_{t(RX\_CTL)}$     | Transition time, RX_CTL                     | 10Mbps   |     |     | 0.75 | ns   |
|        |                      |   | 100Mbps  |     |     | 0.75 | ns   |
|        |                      |   | 1000Mbps |     |     | 0.75 | ns   |



- A. RGMII\_RXC must be externally delayed relative to the data and control pins.  
 B. Data and control information is received using both edges of the clocks. RGMII\_RXD[3:0] carries data bits 3-0 on the rising edge of RGMII\_RXC and data bits 7-4 on the falling edge of RGMII\_RXC. Similarly, RGMII\_RXCTL carries RXDV on rising edge of RGMII\_RXC and RXERR on falling edge of RGMII\_RXC.

**Figure 6-49. CPSW5G Receive Interface Timing, RGMII Operation**

Section 6.10.5.3.3.3, Section 6.10.5.3.3.4, and Figure 6-50 present switching characteristics for transmit - RGMII for 10 Mbps, 100 Mbps, and 1000 Mbps.

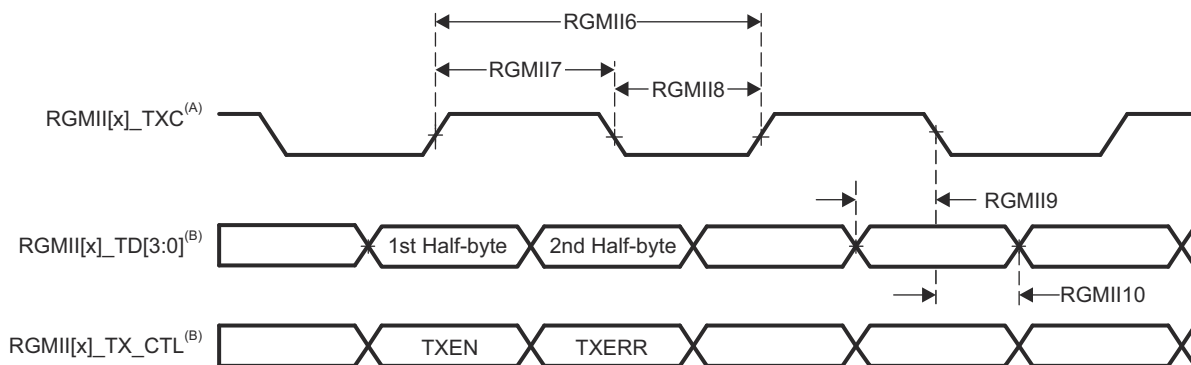
**6.10.5.3.3.3 Switching Characteristics for RGMII[x]\_TCLK – RGMII Mode**

| NO.    | PARAMETER     | DESCRIPTION              | MODE     | MIN | TYP | MAX | UNIT |
|--------|---------------|--------------------------|----------|-----|-----|-----|------|
| RGMII1 | $t_{c(TXC)}$  | Cycle time, TXC          | 10Mbps   | 360 |     | 440 | ns   |
|        |               |                          | 100Mbps  | 36  |     | 44  | ns   |
|        |               |                          | 1000Mbps | 7.2 |     | 8.8 | ns   |
| RGMII2 | $t_{w(TXCH)}$ | Pulse duration, TXC high | 10Mbps   | 160 |     | 240 | ns   |
|        |               |                          | 100Mbps  | 16  |     | 24  | ns   |
|        |               |                          | 1000Mbps | 3.6 |     | 4.4 | ns   |
| RGMII3 | $t_{w(TXCL)}$ | Pulse duration, TXC low  | 10Mbps   | 160 |     | 240 | ns   |
|        |               |                          | 100Mbps  | 16  |     | 24  | ns   |
|        |               |                          | 1000Mbps | 3.6 |     | 4.4 | ns   |

| NO.    | PARAMETER    | DESCRIPTION          | MODE     | MIN | TYP | MAX  | UNIT |
|--------|--------------|----------------------|----------|-----|-----|------|------|
| RGMII4 | $t_{t(TXC)}$ | Transition time, TXC | 10Mbps   |     |     | 0.75 | ns   |
|        |              |                      | 100Mbps  |     |     | 0.75 | ns   |
|        |              |                      | 1000Mbps |     |     | 0.75 | ns   |

**6.10.5.3.4 Switching Characteristics for RGMII[x]\_TD[3:0], and RGMII[x]\_TCTL – RGMII Mode**

| NO.    | PARAMETER              | DESCRIPTION  | MODE     | MIN  | TYP | MAX | UNIT |
|--------|------------------------|--|----------|------|-----|-----|------|
| RGMII5 | $t_{osu(TD-TXC)}$      | Output setup time, RGMII[x]_TD[3:0] valid to RGMII[x]_TXC high/low   | 10Mbps   | 1.2  |     |     | ns   |
|        |                        |  | 100Mbps  | 1.2  |     |     | ns   |
|        |                        |  | 1000Mbps | 1.05 |     |     | ns   |
| RGMII5 | $t_{osu(TX\_CTL-TXC)}$ | Output setup time, RGMII[x]_TX_CTL valid to RGMII[x]_TXC high/low    | 10Mbps   | 1.2  |     |     | ns   |
|        |                        |  | 100Mbps  | 1.2  |     |     | ns   |
|        |                        |  | 1000Mbps | 1.05 |     |     | ns   |
| RGMII6 | $t_{oh(TD-TXC)}$       | Output hold time, RGMII[x]_TD[3:0] valid after RGMII[x]_TXC high/low | 10Mbps   | 1.2  |     |     | ns   |
|        |                        |  | 100Mbps  | 1.2  |     |     | ns   |
|        |                        |  | 1000Mbps | 1.05 |     |     | ns   |
| RGMII6 | $t_{oh(TX\_CTL-TXC)}$  | Output hold time, RGMII[x]_TX_CTL valid after RGMII[x]_TXC high/low  | 10Mbps   | 1.2  |     |     | ns   |
|        |                        |  | 100Mbps  | 1.2  |     |     | ns   |
|        |                        |  | 1000Mbps | 1.05 |     |     | ns   |



- A. TXC is delayed internally before being driven to the RGMII[x]\_TXC pin. This internal delay is always enabled.
- B. Data and control information is received using both edges of the clocks. RGMII\_TD[3:0] carries data bits 3-0 on the rising edge of RGMII\_TXC and data bits 7-4 on the falling edge of RGMII\_TXC. Similarly, RGMII\_TX\_CTL carries TXDV on rising edge of RGMII\_TXC and RTXERR on falling edge of RGMII\_TXC.

**Figure 6-50. CPSW5G Transmit Interface Timing RGMII Mode**

For more information, see *Gigabit Ethernet Switch (CPSW0)* section in *Peripherals* chapter in the device TRM.

**6.10.5.4 DDRSS**

For more details about features and additional description information on the device LPDDR4 Memory Interfaces, see the corresponding sections within [Section 5.3, Signal Descriptions](#) and [Section 7, Detailed Description](#).

The device has dedicated interface to LPDDR4. It supports JEDEC JESD209-4B standard compliant LPDDR4 SDRAM devices with the following features:

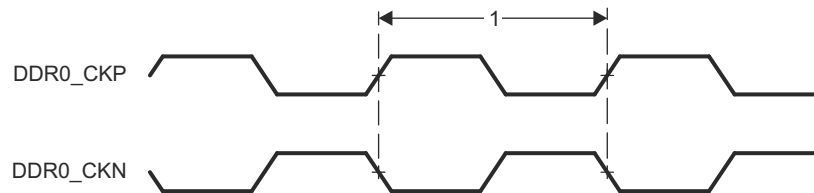
- 32-bit and 16-bit data path to external SDRAM memory
- Memory device capacity: Up to 8GB address space available over two chip selects (4GB per rank)
- No support for byte mode LPDDR4 memories, or memories with more than 17 row address bits

[Table 6-36](#) and [Figure 6-51](#) present switching characteristics for DDRSS.

**Table 6-36. Switching Characteristics for DDRSS**

| NO. | PARAMETER   | DDR TYPE | MIN                  | MAX   | UNIT |
|-----|---|----------|----------------------|-------|------|
| 1   | $t_{c(DDR\_CKP/DDR\_CKN)}$<br>Cycle time, DDR0_CKP and DDR0_CKN | LPDDR4   | 0.625 <sup>(1)</sup> | 3.003 | ns   |

- (1) Maximum DDR Frequency will be limited based on the specific memory type (vendor) used in a system and by PCB implementation. Maximum DDR Frequency will be limited based on the specific memory type (vendor) used in a system and by PCB implementation. TI strongly recommends all designs to follow the TI LPDDR4 EVM PCB layout exactly in every detail (routing, spacing, vias/backdrill, PCB material, etc.) in order to achieve the full specified clock frequency. Refer to the [Jacinto 7 DDR Board Design and Layout Guidelines](#) for details.



**Figure 6-51. DDRSS Memory Interface Clock Timing**

For more information, see *DDR Subsystem (DDRSS)* section in *Memory Controllers* chapter in the device TRM.

#### 6.10.5.5 ECAP

The supported features by the device ECAP are:

- 32-bit time base counter
- 4-event time-stamp registers (each 32 bits)
- Independent edge polarity selection for up to four sequenced time-stamp capture events
- Interrupt capabilities on any of the four capture events
- Input capture signal pre-scaling (from 1 to 16)
- Support of different capture modes (single shot capture, continuous mode capture, absolute timestamp capture or difference mode time-stamp capture)

Table 6-37 represents ECAP timing conditions.

**Table 6-37. ECAP Timing Conditions**

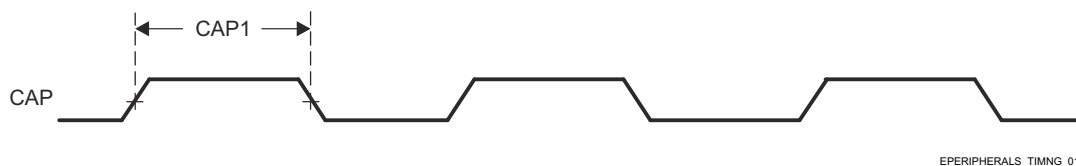
| PARAMETER                | DESCRIPTION             | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>Input Conditions</b>  |                         |     |     |      |
| $t_{SR}$                 | Input slew rate         | 1   | 4   | V/ns |
| <b>Output Conditions</b> |                         |     |     |      |
| $C_{LOAD}$               | Output load capacitance | 2   | 7   | pF   |

Section 6.10.5.5.1 and Section 6.10.5.5.2 present timing and switching characteristics for ECAP (see Figure 6-52 and Figure 6-53).

#### 6.10.5.5.1 Timing Requirements for ECAP

| NO.  | PARAMETER    | DESCRIPTION                        | MIN            | MAX | UNIT |
|------|--------------|------------------------------------|----------------|-----|------|
| CAP1 | $t_{w(CAP)}$ | Pulse duration, CAP (asynchronous) | $2 + 2P^{(1)}$ |     | ns   |

- (1) P = sysclk period in ns



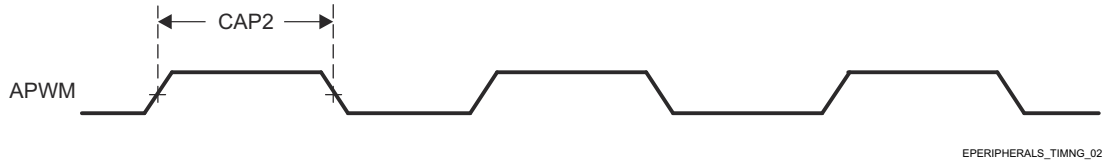
EPERIPHERALS\_TIMNG\_01

**Figure 6-52. ECAP Input Timings**

### 6.10.5.5.2 Switching Characteristics for ECAP

| NO.  | PARAMETER          | DESCRIPTION                    | MIN             | MAX | UNIT |
|------|--------------------|--------------------------------|-----------------|-----|------|
| CAP2 | $t_w(\text{APWM})$ | Pulse duration, APWMx high/low | $-2 + 2P^{(1)}$ |     | ns   |

(1) P = sysclk period in ns



**Figure 6-53. ECAP Output Timings**

For more information, see *Enhanced Capture (ECAP) Module* section in *Peripherals* chapter in the device TRM.

### 6.10.5.6 EPWM

The supported features by the device EPWM are:

- Dedicated 16-bit time-base counter with period and frequency control
- Two independent PWM outputs which can be used in different configurations (with single-edge operation, with dual-edge symmetric operation or one independent PWM output with dual-edge asymmetric operation)
- Asynchronous override control of PWM signals during fault conditions
- Programmable phase-control support for lag or lead operation relative to other EPWM modules
- Dead-band generation with independent rising and falling edge delay control
- Programmable trip zone allocation of both latched and un-latched fault conditions
- Events enabling to trigger both CPU interrupts and start of ADC conversions

Table 6-38 represents EPWM timing conditions.

**Table 6-38. EPWM Timing Conditions**

| PARAMETER                | DESCRIPTION             | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>Input Conditions</b>  |                         |     |     |      |
| $t_{SR}$                 | Input slew rate         | 1   | 4   | V/ns |
| <b>Output Conditions</b> |                         |     |     |      |
| $C_{LOAD}$               | Output load capacitance | 2   | 7   | pF   |

Section 6.10.5.6.1, and Section 6.10.5.6.2 present timing and switching characteristics for EPWM (see Figure 6-54, Figure 6-55, Figure 6-56, and Figure 6-57).

#### 6.10.5.6.1 Timing Requirements for EPWM

| NO.  | PARAMETER              | DESCRIPTION  | MIN           | MAX | UNIT |
|------|------------------------|--|---------------|-----|------|
| PWM1 | $t_w(\text{PWM})$      | Pulse duration, PWM output high/low                  | $P - 3^{(1)}$ |     | ns   |
| PWM2 | $t_w(\text{SYNCOOUT})$ | Pulse duration, Sync output                          | $P - 3^{(1)}$ |     | ns   |
| PWM3 | $t_d(\text{TZ-PWM})$   | Delay time, trip input active to PWM forced high/low |               | 11  | ns   |
| PWM4 | $t_d(\text{TZ-PWMZ})$  | Delay time, trip input active to PWM Hi-Z            |               | 11  | ns   |

| NO.  | PARAMETER    | DESCRIPTION                               | MIN           | MAX | UNIT |
|------|--------------|---|---------------|-----|------|
| PWM5 | $t_{w(SOC)}$ | Pulse duration, SOC output (asynchronous) | $P - 3^{(1)}$ |     | ns   |

(1) P = sysclk period in ns

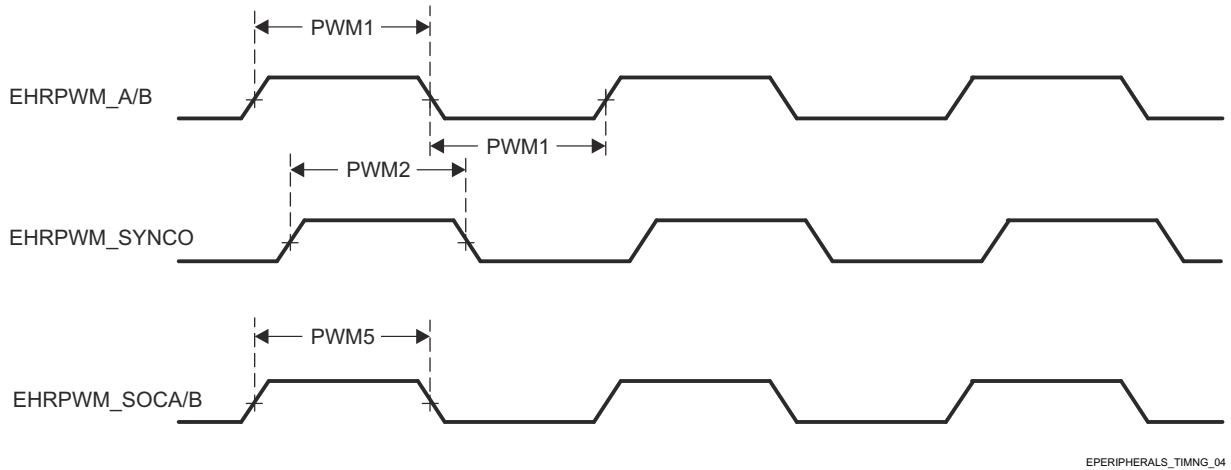


Figure 6-54. EPWM\_A/B\_out, ePWM\_SYNCO, and ePWM\_SOCA/B Input Timings

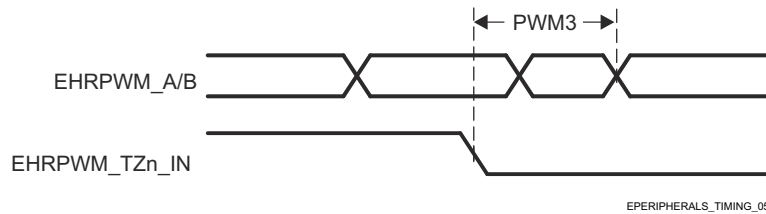


Figure 6-55. EPWM\_A/B and ePWM\_TZn\_IN Forced High/Low Input Timings

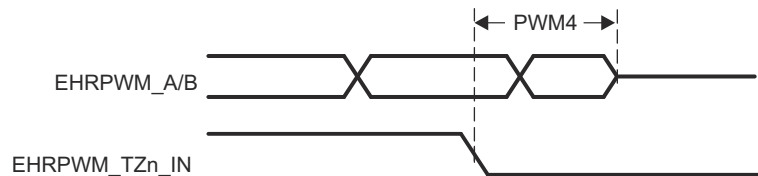


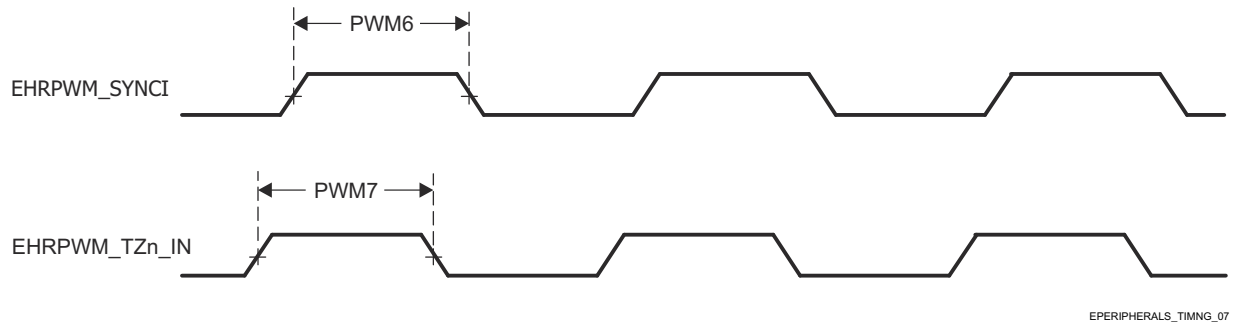
Figure 6-56. EPWM\_A/B and ePWM\_TZn\_IN Hi-Z Input Timings

#### 6.10.5.6.2 Switching Characteristics for EPWM

| NO.  | PARAMETER       | DESCRIPTION                               | MIN            | MAX | UNIT |
|------|-----------------|---|----------------|-----|------|
| PWM6 | $t_{w(SYNCIN)}$ | Pulse duration, Sync input (asynchronous) | $2 + 2P^{(1)}$ |     | ns   |

| NO.  | PARAMETER | DESCRIPTION                                  | MIN            | MAX | UNIT |
|------|-----------|--|----------------|-----|------|
| PWM7 | $t_w(TZ)$ | Pulse duration, TZx input low (asynchronous) | $2 + 3P^{(1)}$ |     | ns   |

(1) P = sysclk period in ns



**Figure 6-57. ePWM\_SYNCI and ePWM\_TZn\_IN Output Timings**

For more information, see *Enhanced Pulse Width Modulation (EPWM) Module* section in *Peripherals* chapter in the device TRM.

### 6.10.5.7 EQEP

The supported features by the device EQEP are:

- Input Synchronization
- Three Stage/Six Stage Digital Noise Filter
- Quadrature Decoder Unit
- Position Counter and Control unit for position measurement
- Quadrature Edge Capture unit for low speed measurement
- Unit Time base for speed/frequency measurement
- Watchdog Timer for detecting stalls

Table 6-39 represents EQEP timing conditions.

**Table 6-39. EQEP Timing Conditions**

| PARAMETER                | DESCRIPTION             | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>Input Conditions</b>  |                         |     |     |      |
| $SR_i$                   | Input slew rate         | 1   | 4   | V/ns |
| <b>Output Conditions</b> |                         |     |     |      |
| $C_L$                    | Output load capacitance | 2   | 7   | pF   |

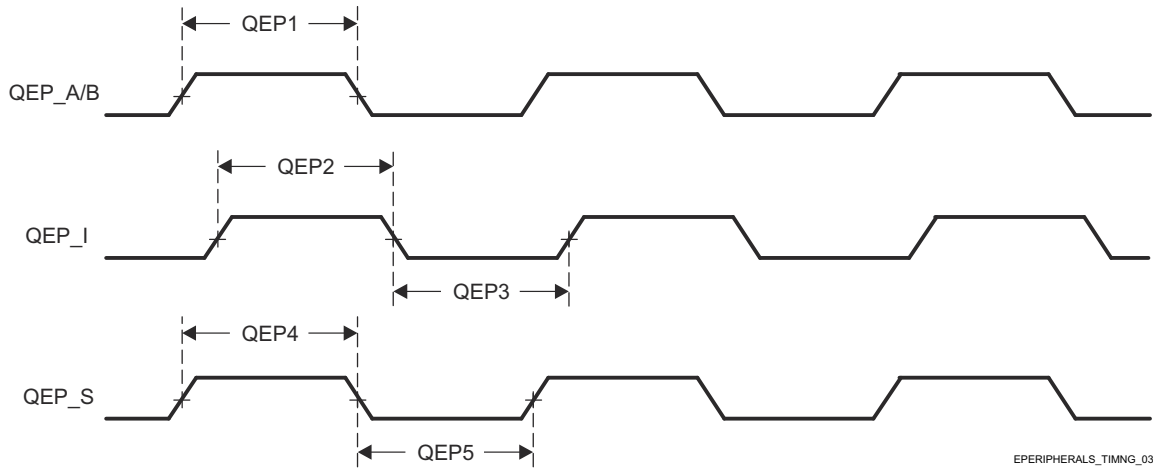
Section 6.10.5.7.1 and Section 6.10.5.7.2 present timing requirements and switching characteristics for EQEP (see Figure 6-58).

#### 6.10.5.7.1 Timing Requirements for EQEP

| NO.  | PARAMETER     | DESCRIPTION                | MIN            | MAX | UNIT |
|------|---------------|----------------------------|----------------|-----|------|
| QEP1 | $t_w(QEP)$    | Pulse duration, QEP_A/B    | $2 + 2P^{(1)}$ |     | ns   |
| QEP2 | $t_w(QEPIH)$  | Pulse duration, QEP_I high | $2 + 2P^{(1)}$ |     | ns   |
| QEP3 | $t_w(QEPI L)$ | Pulse duration, QEP_I low  | $2 + 2P^{(1)}$ |     | ns   |
| QEP4 | $t_w(QEP SH)$ | Pulse duration, QEP_S high | $2 + 2P^{(1)}$ |     | ns   |

| NO.  | PARAMETER         | DESCRIPTION               | MIN            | MAX | UNIT |
|------|-------------------|---------------------------|----------------|-----|------|
| QEP5 | $t_{w(QEP_{SL})}$ | Pulse duration, QEP_S low | $2 + 2P^{(1)}$ |     | ns   |

(1) P = sysclk period in ns



**Figure 6-58. EQEP Input Timings**

#### 6.10.5.7.2 Switching Characteristics for EQEP

| NO.  | PARAMETER         | DESCRIPTION                                     | MIN | MAX | UNIT |
|------|-------------------|---|-----|-----|------|
| QEP6 | $t_{d(QEP-CNTR)}$ | Delay time, external clock to counter increment |     | 24  | ns   |

For more information, see *Enhanced Quadrature Encoder Pulse (EQEP) Module* section in *Peripherals* chapter in the device TRM.

#### 6.10.5.8 GPIO

The device has ten instances of GPIO modules. The GPIO modules are integrated in three groups.

- Group one: WKUP\_GPIO0 and WKUP\_GPIO1
- Group two: GPIO0, GPIO2, GPIO4, and GPIO6
- Group three: GPIO1, GPIO3, GPIO5, and GPIO7

Within each group, exactly one module is selected to control the corresponding I/O pins and pin interrupts.

The GPIO pins are grouped into banks (16 pins per bank), which means that each GPIO module provides up to 144 dedicated general-purpose pins with input and output capabilities; thus, the general-purpose interface supports up to 432 (3 instances × (9 banks × 16 pins)) pins. Since WKUP\_GPIOu\_[84:143] (u = 0, 1), GPIO<sub>n</sub>\_[128:143] (n = 0, 2, 4, 6), and GPIO<sub>m</sub>\_[36:143] (m = 1, 3, 5, 7) are reserved in this device, general purpose interface supports up to 248 I/O pins.

For more details about features and additional description information on the device General-Purpose Interface, see the corresponding sections within [Section 5.3, Signal Descriptions](#) and [Section 7, Detailed Description](#).

#### Note

The general-purpose input/output *i* (*i* = 0 to 1) is also referred to as GPIO<sub>*i*</sub>.

[Table 6-40](#), [Table 6-41](#), and [Table 6-42](#) present timing conditions, requirements, and switching characteristics for GPIO.

**Table 6-40. GPIO Timing Conditions**

| PARAMETER               | BUFFER TYPE | MIN | MAX | UNIT |
|-------------------------|-------------|-----|-----|------|
| <b>INPUT CONDITIONS</b> |             |     |     |      |

**Table 6-40. GPIO Timing Conditions (continued)**

| PARAMETER                |                         | BUFFER TYPE | MIN | MAX | UNIT |
|--------------------------|-------------------------|-------------|-----|-----|------|
| SR <sub>I</sub>          | Input slew rate         | LVC MOS     | 0.2 | 6.6 | V/ns |
|                          |                         | I2C OD FS   | 0.2 | 0.8 | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |             |     |     |      |
| C <sub>L</sub>           | Output load capacitance | LVC MOS     | 3   | 10  | pF   |
|                          |                         | I2C OD FS   | 3   | 100 | pF   |

**Table 6-41. GPIO Timing Requirements**

| NO.   | PARAMETER                | DESCRIPTION                       | MODE  | MIN                     | MAX | UNIT |
|-------|--------------------------|-----------------------------------|-------|-------------------------|-----|------|
| GPIO1 | t <sub>w</sub> (GPIO_IN) | Pulse width, GPIO <sub>n</sub> _x | 1.8 V | 2P + 2.6 <sup>(1)</sup> |     | ns   |
|       |                          |                                   | 3.3 V | 2P + 3.4 <sup>(1)</sup> |     | ns   |

(1) P = functional clock period in ns.

**Table 6-42. GPIO Switching Characteristics**

| NO. | PARAMETER                 | DESCRIPTION                     | BUFFER TYPE    | MIN                          | MAX | UNIT |
|-----|---------------------------|---------------------------------|----------------|------------------------------|-----|------|
| GP3 | t <sub>w</sub> (GPIO_OUT) | Minimum Output Pulse Width      | LVC MOS        | -3.6 + 0.975P <sup>(1)</sup> |     | ns   |
| GP4 | t <sub>w</sub> (GPIO_OUT) | Minimum Output Pulse Width Low  | I2C Open Drain | 160                          |     | ns   |
| GP5 | t <sub>w</sub> (GPIO_OUT) | Minimum Output Pulse Width High | I2C Open Drain | 60                           |     | ns   |

(1) P = functional clock period in ns.

For more information, see *General-Purpose Interface (GPIO)* section in *Peripherals* chapter in the device TRM.

#### 6.10.5.9 GPMC

For more details about features and additional description information on the device General-Purpose Memory Controller, see the corresponding sections within [Section 5.3, Signal Descriptions](#) and [Section 7, Detailed Description](#).

**Table 6-43. GPMC Timing Conditions**

| PARAMETER                             | DESCRIPTION                            | MIN                      | MAX | UNIT |    |
|---------------------------------------|--|--------------------------|-----|------|----|
| <b>Input Conditions</b>               |  |                          |     |      |    |
| SR <sub>I</sub>                       | Input slew rate                        | 1.65                     | 4   | V/ns |    |
| <b>Output Conditions</b>              |  |                          |     |      |    |
| C <sub>L</sub>                        | Output load capacitance                | 5                        | 20  | pF   |    |
| <b>PCB Connectivity Requirements</b>  |  |                          |     |      |    |
| t <sub>d</sub> (Trace Delay)          | Propagation delay of each trace        | 133 MHz Synchronous Mode | 140 | 360  | ps |
|                                       |  | All other modes          | 140 | 720  |    |
| t <sub>d</sub> (Trace Mismatch Delay) | Propagation mismatch across all traces |                          | 200 | ps   |    |

##### 6.10.5.9.1 GPMC and NOR Flash — Synchronous Mode

[Section 6.10.5.9.1.1](#) and [Section 6.10.5.9.1.2](#) assume testing over the recommended operating conditions and electrical characteristic conditions below (see [Figure 6-59](#) through [Figure 6-63](#)).

**6.10.5.9.1 GPMC and NOR Flash Timing Requirements — Synchronous Mode**

| NO. | PARAMETER                   | DESCRIPTION  | MODE <sup>(2)</sup>  | MIN     | MAX | MIN     | MAX | UNIT |
|-----|-----------------------------|--|--|---------|-----|---------|-----|------|
|     |                             |  |  | 100 MHz |     | 133 MHz |     |      |
| F12 | t <sub>su(dv-clkH)</sub>    | Setup time, input data GPMC_AD[15:0] valid before output clock GPMC_CLK high               | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1     | 1.81    |     | 1.11    |     | ns   |
|     |                             |  | not_div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | 1.06    |     |         |     | ns   |
| F13 | t <sub>h(clkH-dV)</sub>     | Hold time, input data GPMC_AD[15:0] valid after output clock GPMC_CLK high                 | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1     | 1.78    |     | 2.28    |     | ns   |
|     |                             |  | not_div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | 1.78    |     |         |     | ns   |
| F21 | t <sub>su(waitV-clkH)</sub> | Setup time, input wait GPMC_WAIT[j] valid before output clock GPMC_CLK high <sup>(1)</sup> | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1     | 1.81    |     | 1.11    |     | ns   |
|     |                             |  | not_div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | 1.06    |     |         |     | ns   |
| F22 | t <sub>h(clkH-waitV)</sub>  | Hold time, input wait GPMC_WAIT[j] valid after output clock GPMC_CLK high <sup>(1)</sup>   | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1     | 1.78    |     | 2.28    |     | ns   |
|     |                             |  | not_div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | 1.78    |     |         |     | ns   |

(1) In GPMC\_WAIT[j], j is equal to 0 or 1.

(2) For div\_by\_1\_mode:

- GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 0h:
  - GPMC\_CLK frequency = GPMC\_FCLK frequency

For not\_div\_by\_1\_mode:

- GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 1h to 3h:
  - GPMC\_CLK frequency = GPMC\_FCLK frequency / (2 to 4)

For GPMC\_FCLK\_MUX:

- CTRLMMR\_GPMC\_CLKSEL[1-0] CLK\_SEL = 01 = PER1\_PLL\_CLKOUT / 3 = 300 / 3 = 100MHz

For TIMEPARAGRANULARITY\_X1:

- GPMC\_CONFIG1\_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

**6.10.5.9.1.2 GPMC and NOR Flash Switching Characteristics – Synchronous Mode**

| NO. <sup>(2)</sup> | PARAMETER            | DESCRIPTION  | MODE <sup>(19)</sup>                                       | MIN                                  | MAX | MIN                                  | MAX | UNIT |
|--------------------|----------------------|--|--|--------------------------------------|-----|--------------------------------------|-----|------|
|                    |                      |  |  | 100 MHz                              |     | 133 MHz                              |     |      |
| F0                 | 1 / tc(clk)          | Period, output clock GPMC_CLK <sup>(18)</sup>      | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | 10                                   |     | 7.52                                 |     | ns   |
| F1                 | t <sub>w(clkH)</sub> | Typical pulse duration, output clock GPMC_CLK high | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | -0.3+<br>0.475*<br>P <sup>(15)</sup> |     | -0.3+<br>0.475*<br>P <sup>(15)</sup> |     | ns   |
| F1                 | t <sub>w(clkL)</sub> | Typical pulse duration, output clock GPMC_CLK low  | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | -0.3+<br>0.475*<br>P <sup>(15)</sup> |     | -0.3+<br>0.475*<br>P <sup>(15)</sup> |     | ns   |

| NO.<br>(2) | PARAMETER                     | DESCRIPTION  | MODE <sup>(19)</sup>  | MIN                   | MAX                  | MIN                  | MAX                  | UNIT |
|------------|-------------------------------|--|---|-----------------------|----------------------|----------------------|----------------------|------|
|            |                               |  |   | 100 MHz               |                      | 133 MHz              |                      |      |
| F2         | $t_{d(\text{clkH-csnV})}$     | Delay time, output clock GPMC_CLK rising edge to output chip select GPMC_CS[n][i] transition <sup>(14)</sup>   | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1;<br>no extra_delay | -2.2+F<br>(6)         | 3.75+F<br>(6)        | -2.2+F<br>(6)        | 3.75+F<br>(6)        | ns   |
| F3         | $t_{d(\text{clkH-CSn[i]V})}$  | Delay time, output clock GPMC_CLK rising edge to output chip select GPMC_CS[n][i] invalid <sup>(14)</sup>  | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1;<br>no extra_delay | -2.2+E<br>(5)         | 3.75+E<br>(5)        | -2.2+E<br>(5)        | 3.75+E<br>(5)        | ns   |
| F4         | $t_{d(\text{aV-clk})}$        | Delay time, output address GPMC_A[27:1] valid to output clock GPMC_CLK first edge  | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                    | -2.3+B<br>(2)         | 4.5+B<br>(2)         | -2.3+B<br>(2)        | 4.5+B<br>(2)         | ns   |
| F5         | $t_{d(\text{clkH-aIV})}$      | Delay time, output clock GPMC_CLK rising edge to output address GPMC_A[27:1] invalid   | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                    | -2.3                  | 4.5                  | -2.3                 | 4.5                  | ns   |
| F6         | $t_{d(\text{be[x]nV-clk})}$   | Delay time, output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n valid to output clock GPMC_CLK first edge                    | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                    | -2.3+B<br>(2)         | 1.9+B<br>(2)         | -2.3+B<br>(2)        | 1.9+B<br>(2)         | ns   |
| F7         | $t_{d(\text{clkH-be[x]nIV})}$ | Delay time, output clock GPMC_CLK rising edge to output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n invalid <sup>(11)</sup> | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                    | -2.3+D<br>(4)         | 1.9+D<br>(4)         | -2.3+D<br>(4)        | 1.9+D<br>(4)         | ns   |
| F7         | $t_{d(\text{clkL-be[x]nIV})}$ | Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n invalid <sup>(12)</sup>  | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                    | -2.3+D<br>(4)         | 1.9+D<br>(4)         | -2.3+D<br>(4)        | 1.9+D<br>(4)         | ns   |
| F7         | $t_{d(\text{clkL-be[x]nIV})}$ | Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n invalid <sup>(13)</sup>  | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                    | -2.3+D<br>(4)         | 1.9+D<br>(4)         | -2.3+D<br>(4)        | 1.9+D<br>(4)         | ns   |
| F8         | $t_{d(\text{clkH-advn})}$     | Delay time, output clock GPMC_CLK rising edge to output address valid and address latch enable GPMC_ADVn_ALE transition  | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1;<br>no extra_delay | -2.3+G<br>(7)         | 4.5+G<br>(7)         | -2.3+G<br>(7)        | 4.5+G<br>(7)         | ns   |
| F9         | $t_{d(\text{clkH-advnIV})}$   | Delay time, output clock GPMC_CLK rising edge to output address valid and address latch enable GPMC_ADVn_ALE invalid   | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1;<br>no extra_delay | -2.3+D<br>(4)         | 4.5+D<br>(4)         | -2.3+D<br>(4)        | 4.5+D<br>(4)         | ns   |
| F10        | $t_{d(\text{clkH-oen})}$      | Delay time, output clock GPMC_CLK rising edge to output enable GPMC_OEn_REn transition   | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1;<br>no extra_delay | -2.3H <sup>(8)</sup>  | 3.5+H<br>(8)         | -2.3H <sup>(8)</sup> | 3.5+H<br>(8)         | ns   |
| F11        | $t_{d(\text{clkH-oenIV})}$    | Delay time, output clock GPMC_CLK rising edge to output enable GPMC_OEn_REn invalid  | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1;<br>no extra_delay | -2.3+E<br>(8)         | 3.5+E<br>(8)         | -2.3+E<br>(8)        | 3.5+E<br>(8)         | ns   |
| F14        | $t_{d(\text{clkH-wen})}$      | Delay time, output clock GPMC_CLK rising edge to output write enable GPMC_WEn transition   | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1;<br>no extra_delay | -2.3+I <sup>(9)</sup> | 4.5+I <sup>(9)</sup> | -2.3+I<br>(9)        | 4.5+I <sup>(9)</sup> | ns   |
| F15        | $t_{d(\text{clkH-do})}$       | Delay time, output clock GPMC_CLK rising edge to output data GPMC_AD[15:0] transition <sup>(11)</sup>  | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                    | -2.3+J<br>(10)        | 2.7+J<br>(10)        | -2.3+J<br>(10)       | 2.7+J<br>(10)        | ns   |
| F15        | $t_{d(\text{clkL-do})}$       | Delay time, GPMC_CLK falling edge to GPMC_AD[15:0] data bus transition <sup>(12)</sup>   | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1                    | -2.3+J<br>(10)        | 2.7+J<br>(10)        | -2.3+J<br>(10)       | 2.7+J<br>(10)        | ns   |

| NO.<br>(2) | PARAMETER                   | DESCRIPTION   | MODE <sup>(19)</sup>                                       | MIN               | MAX           | MIN               | MAX           | UNIT |
|------------|-----------------------------|---|--|-------------------|---------------|-------------------|---------------|------|
|            |                             |   |  | 100 MHz           |               | 133 MHz           |               |      |
| F15        | t <sub>d(clkL-do)</sub>     | Delay time, GPMC_CLK falling edge to GPMC_AD[15:0] data bus transition <sup>(13)</sup>  | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | -2.3+J<br>(10)    | 2.7+J<br>(10) | -2.3+J<br>(10)    | 2.7+J<br>(10) | ns   |
| F17        | t <sub>d(clkH-be[x]n)</sub> | Delay time, output clock GPMC_CLK rising edge to output lower byte enable and command latch enable GPMC_BE0n_CLE transition <sup>(11)</sup> | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | -2.3+J<br>(10)    | 1.9+J<br>(10) | -2.3+J<br>(10)    | 1.9+J<br>(10) | ns   |
| F17        | t <sub>d(clkL-be[x]n)</sub> | Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n transition <sup>(12)</sup>  | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | -2.3+J<br>(10)    | 1.9+J<br>(10) | -2.3+J<br>(10)    | 1.9+J<br>(10) | ns   |
| F17        | t <sub>d(clkL-be[x]n)</sub> | Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n transition <sup>(13)</sup>  | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | -2.3+J<br>(10)    | 1.9+J<br>(10) | -2.3+J<br>(10)    | 1.9+J<br>(10) | ns   |
| F18        | t <sub>w(csnV)</sub>        | Pulse duration, output chip select GPMC_CSn[i] low <sup>(14)</sup>  | Read   | A <sup>(1)</sup>  |               | A <sup>(1)</sup>  |               | ns   |
|            |                             |   | Write  | A <sup>(1)</sup>  |               | A <sup>(1)</sup>  |               | ns   |
| F19        | t <sub>w(be[x]nV)</sub>     | Pulse duration, output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n low                     | Read   | C <sup>(3)</sup>  |               | C <sup>(3)</sup>  |               | ns   |
|            |                             |   | Write  | C <sup>(3)</sup>  |               | C <sup>(3)</sup>  |               | ns   |
| F20        | t <sub>w(advnV)</sub>       | Pulse duration, output address valid and address latch enable GPMC_ADVn_ALE low   | Read   | K <sup>(16)</sup> |               | K <sup>(16)</sup> |               | ns   |
|            |                             |   | Write  | K <sup>(16)</sup> |               | K <sup>(16)</sup> |               | ns   |

- (1) For single read:  $A = (\text{CSRdOffTime} - \text{CSONTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$   
 For burst read:  $A = (\text{CSRdOffTime} - \text{CSONTime} + (n - 1) \times \text{PageBurstAccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$   
 For burst write:  $A = (\text{CSWrOffTime} - \text{CSONTime} + (n - 1) \times \text{PageBurstAccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$   
 With n being the page burst access number.
- (2)  $B = \text{ClkActivationTime} \times \text{GPMC\_FCLK}^{(17)}$
- (3) For single read:  $C = \text{RdCycleTime} \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$   
 For burst read:  $C = (\text{RdCycleTime} + (n - 1) \times \text{PageBurstAccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$   
 For burst write:  $C = (\text{WrCycleTime} + (n - 1) \times \text{PageBurstAccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$   
 With n being the page burst access number.
- (4) For single read:  $D = (\text{RdCycleTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$   
 For burst read:  $D = (\text{RdCycleTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$   
 For burst write:  $D = (\text{WrCycleTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$
- (5) For single read:  $E = (\text{CSRdOffTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$   
 For burst read:  $E = (\text{CSRdOffTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$   
 For burst write:  $E = (\text{CSWrOffTime} - \text{AccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$
- (6) For csn falling edge (CS activated):
- Case GPMCFCLKDIVIDER = 0:
    - $F = 0.5 \times \text{CSExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$
  - Case GPMCFCLKDIVIDER = 1:
    - $F = 0.5 \times \text{CSExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if (ClkActivationTime and CSONTime are odd) or (ClkActivationTime and CSONTime are even)
    - $F = (1 + 0.5 \times \text{CSExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  otherwise
  - Case GPMCFCLKDIVIDER = 2:
    - $F = 0.5 \times \text{CSExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if ((CSONTime - ClkActivationTime) is a multiple of 3)
    - $F = (1 + 0.5 \times \text{CSExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((CSONTime - ClkActivationTime - 1) is a multiple of 3)
    - $F = (2 + 0.5 \times \text{CSExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((CSONTime - ClkActivationTime - 2) is a multiple of 3)
- (7) For ADV falling edge (ADV activated):
- Case GPMCFCLKDIVIDER = 0:
    - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$
  - Case GPMCFCLKDIVIDER = 1:
    - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)
    - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  otherwise
  - Case GPMCFCLKDIVIDER = 2:

- $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if  $((\text{ADVOnTime} - \text{ClkActivationTime})$  is a multiple of 3)
- $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if  $((\text{ADVOnTime} - \text{ClkActivationTime} - 1)$  is a multiple of 3)
- $G = (2 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if  $((\text{ADVOnTime} - \text{ClkActivationTime} - 2)$  is a multiple of 3)

For ADV rising edge (ADV deactivated) in Reading mode:

- Case GPMCFCLKDIVIDER = 0:
  - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$
- Case GPMCFCLKDIVIDER = 1:
  - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if  $(\text{ClkActivationTime}$  and  $\text{ADVRdOffTime}$  are odd) or  $(\text{ClkActivationTime}$  and  $\text{ADVRdOffTime}$  are even)
  - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  otherwise
- Case GPMCFCLKDIVIDER = 2:
  - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if  $((\text{ADVRdOffTime} - \text{ClkActivationTime})$  is a multiple of 3)
  - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if  $((\text{ADVRdOffTime} - \text{ClkActivationTime} - 1)$  is a multiple of 3)
  - $G = (2 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if  $((\text{ADVRdOffTime} - \text{ClkActivationTime} - 2)$  is a multiple of 3)

For ADV rising edge (ADV deactivated) in Writing mode:

- Case GPMCFCLKDIVIDER = 0:
  - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$
- Case GPMCFCLKDIVIDER = 1:
  - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if  $(\text{ClkActivationTime}$  and  $\text{ADVWrOffTime}$  are odd) or  $(\text{ClkActivationTime}$  and  $\text{ADVWrOffTime}$  are even)
  - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  otherwise
- Case GPMCFCLKDIVIDER = 2:
  - $G = 0.5 \times \text{ADVExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if  $((\text{ADVWrOffTime} - \text{ClkActivationTime})$  is a multiple of 3)
  - $G = (1 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if  $((\text{ADVWrOffTime} - \text{ClkActivationTime} - 1)$  is a multiple of 3)
  - $G = (2 + 0.5 \times \text{ADVExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if  $((\text{ADVWrOffTime} - \text{ClkActivationTime} - 2)$  is a multiple of 3)

(8) For OE falling edge (OE activated) and IO DIR rising edge (Data Bus input direction):

- Case GPMCFCLKDIVIDER = 0:
  - $H = 0.5 \times \text{OEEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$
- Case GPMCFCLKDIVIDER = 1:
  - $H = 0.5 \times \text{OEEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if  $(\text{ClkActivationTime}$  and  $\text{OEOnTime}$  are odd) or  $(\text{ClkActivationTime}$  and  $\text{OEOnTime}$  are even)
  - $H = (1 + 0.5 \times \text{OEEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  otherwise
- Case GPMCFCLKDIVIDER = 2:
  - $H = 0.5 \times \text{OEEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if  $((\text{OEOnTime} - \text{ClkActivationTime})$  is a multiple of 3)
  - $H = (1 + 0.5 \times \text{OEEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if  $((\text{OEOnTime} - \text{ClkActivationTime} - 1)$  is a multiple of 3)
  - $H = (2 + 0.5 \times \text{OEEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if  $((\text{OEOnTime} - \text{ClkActivationTime} - 2)$  is a multiple of 3)

For OE rising edge (OE deactivated):

- Case GPMCFCLKDIVIDER = 0:
  - $H = 0.5 \times \text{OEEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$
- Case GPMCFCLKDIVIDER = 1:
  - $H = 0.5 \times \text{OEEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if  $(\text{ClkActivationTime}$  and  $\text{OEOffTime}$  are odd) or  $(\text{ClkActivationTime}$  and  $\text{OEOffTime}$  are even)
  - $H = (1 + 0.5 \times \text{OEEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  otherwise
- Case GPMCFCLKDIVIDER = 2:
  - $H = 0.5 \times \text{OEEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if  $((\text{OEOffTime} - \text{ClkActivationTime})$  is a multiple of 3)
  - $H = (1 + 0.5 \times \text{OEEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if  $((\text{OEOffTime} - \text{ClkActivationTime} - 1)$  is a multiple of 3)
  - $H = (2 + 0.5 \times \text{OEEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if  $((\text{OEOffTime} - \text{ClkActivationTime} - 2)$  is a multiple of 3)

(9) For WE falling edge (WE activated):

- Case GPMCFCLKDIVIDER = 0:
  - $I = 0.5 \times \text{WEEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$
- Case GPMCFCLKDIVIDER = 1:

- $I = 0.5 \times \text{WEEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if (ClkActivationTime and WEOnTime are odd) or (ClkActivationTime and WEOnTime are even)
- $I = (1 + 0.5 \times \text{WEEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  otherwise
- Case GPMCFCLKDIVIDER = 2:
  - $I = 0.5 \times \text{WEEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if ((WEOnTime - ClkActivationTime) is a multiple of 3)
  - $I = (1 + 0.5 \times \text{WEEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((WEOnTime - ClkActivationTime - 1) is a multiple of 3)
  - $I = (2 + 0.5 \times \text{WEEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((WEOnTime - ClkActivationTime - 2) is a multiple of 3)

For WE rising edge (WE deactivated):

- Case GPMCFCLKDIVIDER = 0:
  - $I = 0.5 \times \text{WEEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$
- Case GPMCFCLKDIVIDER = 1:
  - $I = 0.5 \times \text{WEEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if (ClkActivationTime and WEOffTime are odd) or (ClkActivationTime and WEOffTime are even)
  - $I = (1 + 0.5 \times \text{WEEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  otherwise
- Case GPMCFCLKDIVIDER = 2:
  - $I = 0.5 \times \text{WEEExtraDelay} \times \text{GPMC\_FCLK}^{(17)}$  if ((WEOffTime - ClkActivationTime) is a multiple of 3)
  - $I = (1 + 0.5 \times \text{WEEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((WEOffTime - ClkActivationTime - 1) is a multiple of 3)
  - $I = (2 + 0.5 \times \text{WEEExtraDelay}) \times \text{GPMC\_FCLK}^{(17)}$  if ((WEOffTime - ClkActivationTime - 2) is a multiple of 3)

(10)  $J = \text{GPMC\_FCLK}^{(17)}$

(11) First transfer only for CLK DIV 1 mode.

(12) Half cycle; for all data after initial transfer for CLK DIV 1 mode.

(13) Half cycle of GPMC\_CLKOUT; for all data for modes other than CLK DIV 1 mode. GPMC\_CLKOUT divide down from GPMC\_FCLK.

(14) In GPMC\_CS*n*[*i*], *i* is equal to 0, 1, 2 or 3. In GPMC\_WAIT[*j*], *j* is equal to 0 or 1.

(15)  $P = \text{GPMC\_CLK}$  period in ns

(16) For read:  $K = (\text{ADVrDOffTime} - \text{ADVOnTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$

For write:  $K = (\text{ADVWrOffTime} - \text{ADVOnTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(17)}$

(17) GPMC\_FCLK is general-purpose memory controller internal functional clock period in ns.

(18) Related to the GPMC\_CLK output clock maximum and minimum frequencies programmable in the GPMC module by setting the GPMC\_CONFIG1\_*i* configuration register bit field GPMCFCLKDIVIDER.

(19) For div\_by\_1\_mode:

- GPMC\_CONFIG1\_*i* register: GPMCFCLKDIVIDER = 0h:
  - GPMC\_CLK frequency = GPMC\_FCLK frequency

For GPMC\_FCLK\_MUX:

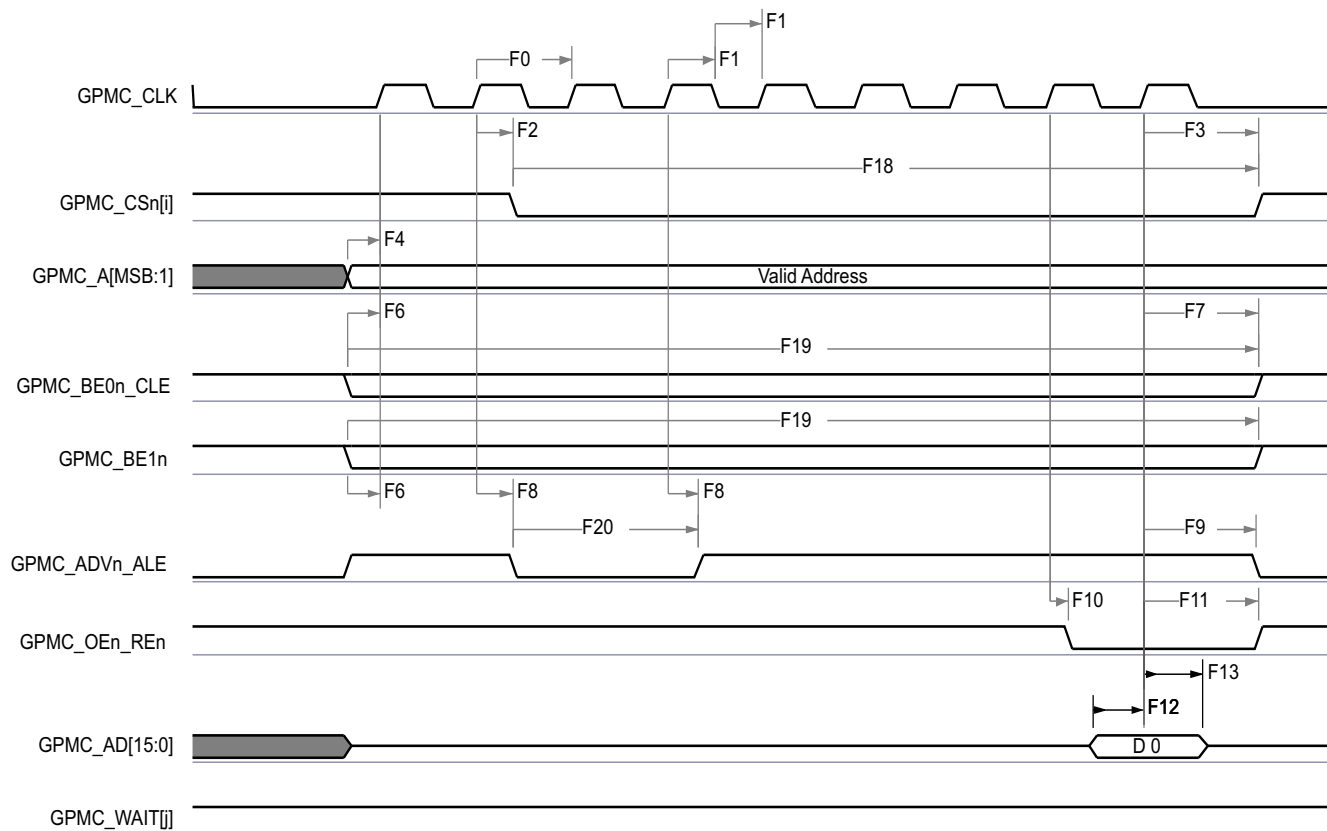
- CTRLMMR\_GPMC\_CLKSEL[1-0] CLK\_SEL = 01 = PER1\_PLL\_CLKOUT / 3 = 300 / 3 = 100MHz

For TIMEPARAGRANULARITY\_X1:

- GPMC\_CONFIG1\_*i* Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

For no extra\_delay:

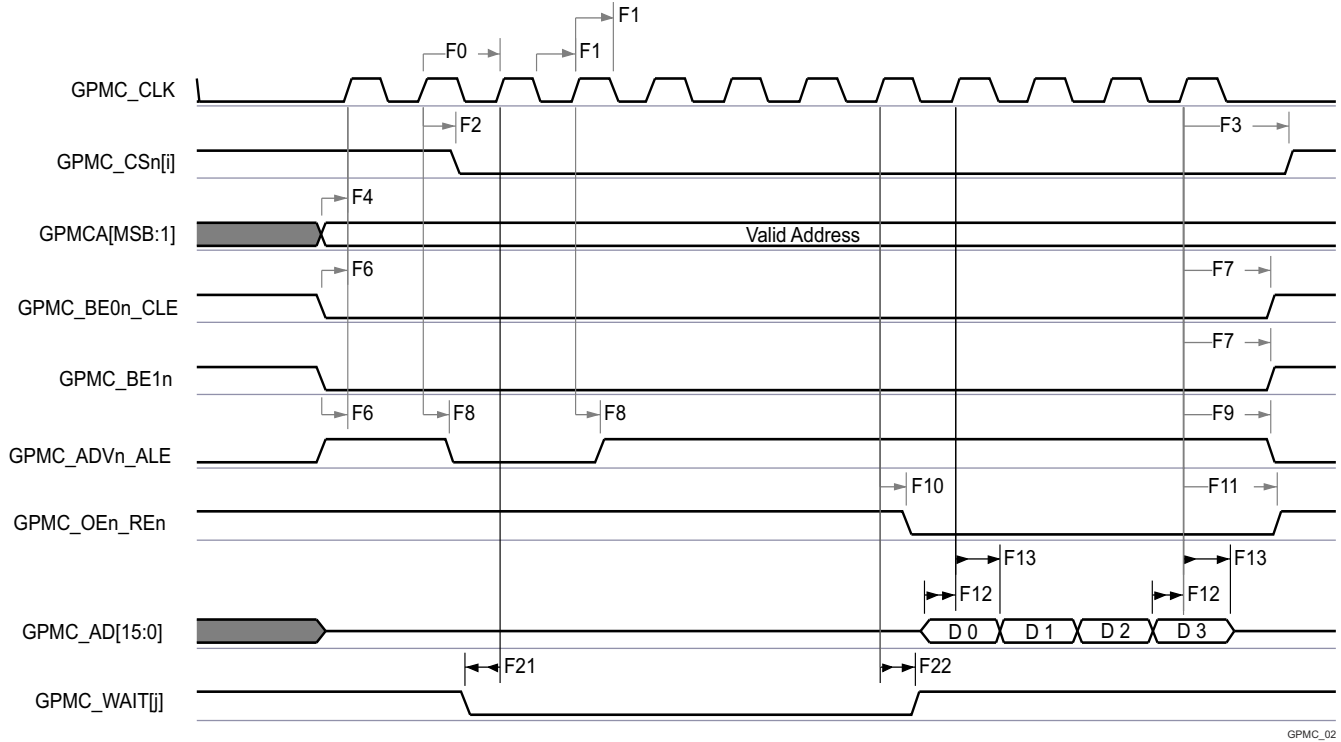
- GPMC\_CONFIG2\_*i* Register: CSEXTRADELAY = 0h = CS*n* Timing control signal is not delayed
- GPMC\_CONFIG4\_*i* Register: WEEXTRADELAY = 0h = nWE timing control signal is not delayed
- GPMC\_CONFIG4\_*i* Register: OEEXTRADELAY = 0h = nOE timing control signal is not delayed
- GPMC\_CONFIG3\_*i* Register: ADVEXTRADELAY = 0h = nADV timing control signal is not delayed



GPMC\_01

- A. In GPMC\_CSn[i], i is equal to 0, 1, 2 or 3.
- B. In GPMC\_WAIT[j], j is equal to 0 or 1.

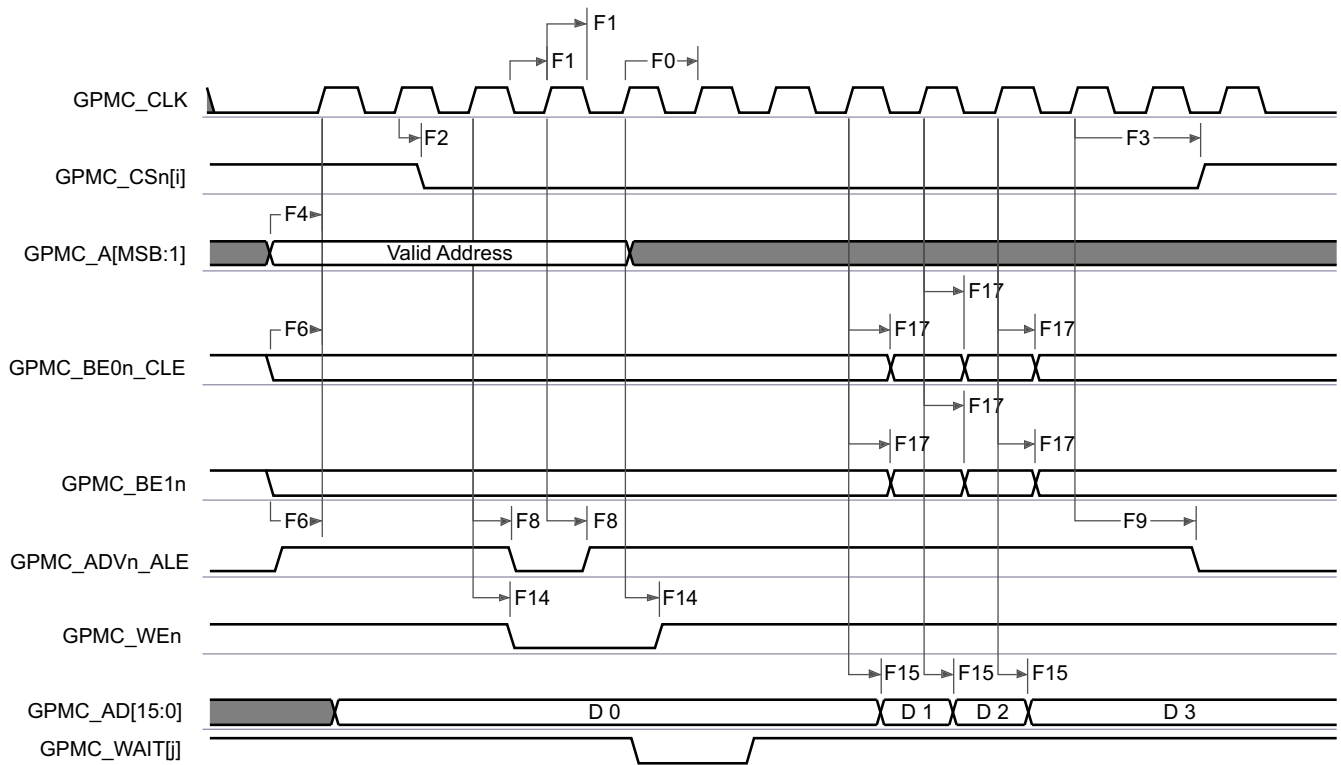
**Figure 6-59. GPMC and NOR Flash — Synchronous Single Read (GPMCFCLKDIVIDER = 0)**



GPMC\_02

- A. In GPMC\_CS*n*[i], i is equal to 0, 1, 2 or 3.
- B. In GPMC\_WAIT[i], j is equal to 0 or 1.

**Figure 6-60. GPMC and NOR Flash — Synchronous Burst Read — 4x16-bit (GPMCFCLKDIVIDER = 0)**

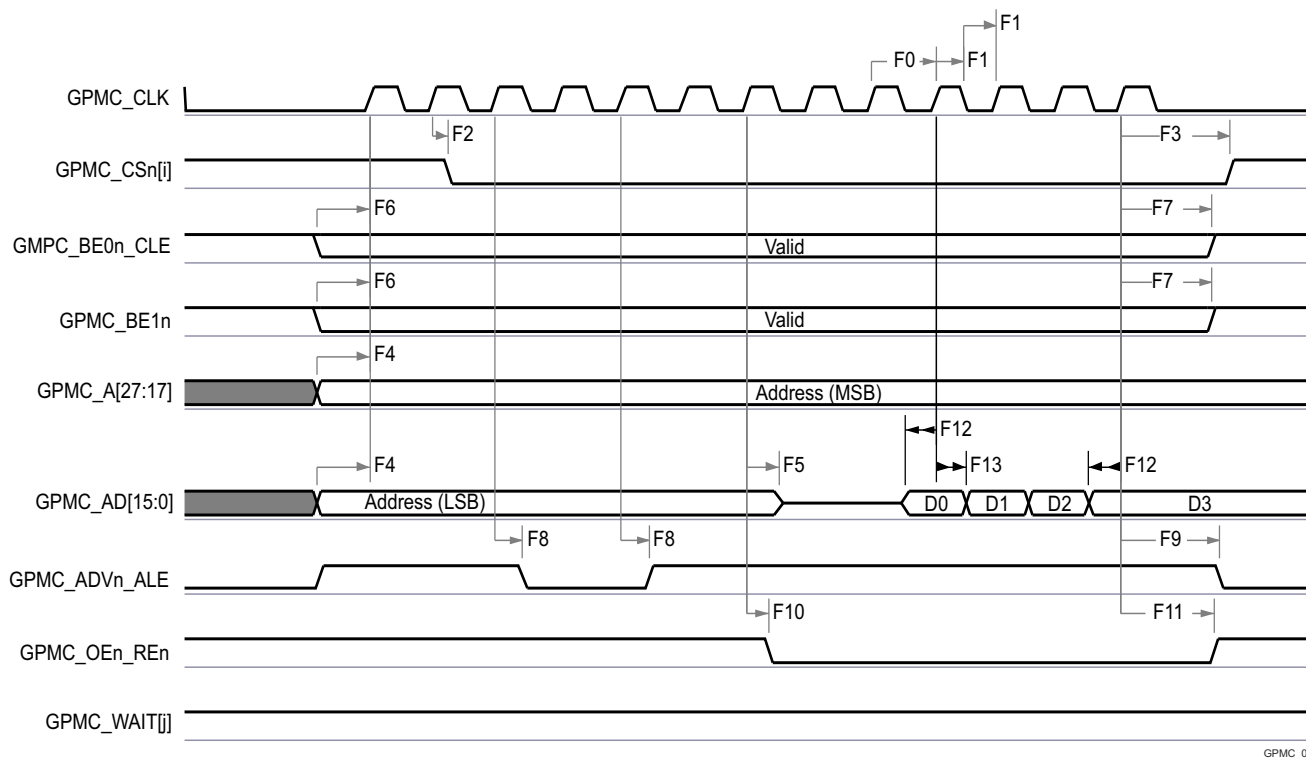


GPMC\_03

- A. In GPMC\_CS*n*[i], i is equal to 0, 1, 2 or 3.

B. In GPMC\_WAIT[j], j is equal to 0 or 1.

**Figure 6-61. GPMC and NOR Flash—Synchronous Burst Write (GPMCFCLKDIVIDER = 0)**

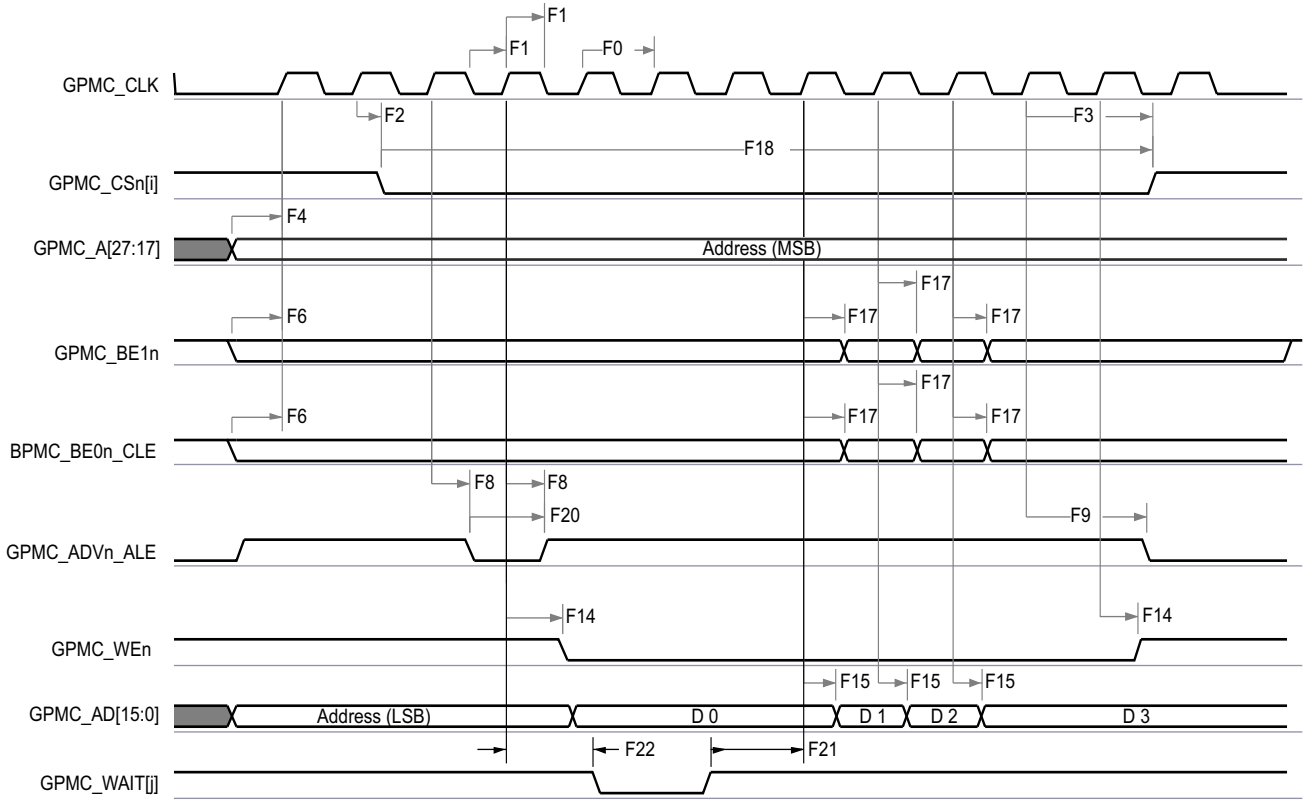


GPMC\_04

A. In GPMC\_CSn[i], i is equal to 0, 1, 2 or 3.

B. In GPMC\_WAIT[j], j is equal to 0 or 1.

**Figure 6-62. GPMC and Multiplexed NOR Flash — Synchronous Burst Read**



GPMC\_05

- A. In GPMC\_CS[n], i is equal to 0, 1, 2 or 3.
- B. In GPMC\_WAIT[j], j is equal to 0 or 1.

**Figure 6-63. GPMC and Multiplexed NOR Flash — Synchronous Burst Write**

**6.10.5.9.2 GPMC and NOR Flash — Asynchronous Mode**

Section 6.10.5.9.2.1 and Section 6.10.5.9.2.2 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-64 through Figure 6-69).

**6.10.5.9.2.1 GPMC and NOR Flash Timing Requirements – Asynchronous Mode**

| NO.                 | PARAMETER                   | DESCRIPTION                           | MODE   | MIN | MAX              | UNIT |
|---------------------|-----------------------------|---------------------------------------|--|-----|------------------|------|
| FA5 <sup>(1)</sup>  | t <sub>acc(d)</sub>         | Data access time                      | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 |     | H <sup>(4)</sup> | ns   |
| FA20 <sup>(2)</sup> | t <sub>acc1-pgmode(d)</sub> | Page mode successive data access time | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 |     | P <sup>(3)</sup> | ns   |
| FA21 <sup>(1)</sup> | t <sub>acc2-pgmode(d)</sub> | Page mode first data access time      | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 |     | H <sup>(4)</sup> | ns   |

- (1) The FA5 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data is internally sampled by active functional clock edge. FA5 value must be stored inside the AccessTime register bit field.
- (2) The FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data is internally sampled by active functional clock edge after FA20 functional clock cycles. The FA20 value must be stored in the PageBurstAccessTime register bit field.
- (3) P = PageBurstAccessTime × (TimeParaGranularity + 1) × GPMC\_FCLK<sup>(5)</sup>
- (4) H = AccessTime × (TimeParaGranularity + 1) × GPMC\_FCLK<sup>(5)</sup>
- (5) GPMC\_FCLK is general-purpose memory controller internal functional clock period in ns.

### 6.10.5.9.2 GPMC and NOR Flash Switching Characteristics – Asynchronous Mode

| NO.  | PARAMETER                           | DESCRIPTION   | MODE <sup>(15)</sup>                                       | MIN                  | MAX                 | UNIT |
|------|-------------------------------------|---|--|----------------------|---------------------|------|
|      |                                     |   |  | 133 MHz              |                     |      |
| FA0  | $t_{w(\text{be}[x]nV)}$             | Pulse duration, output lower-byte enable and command latch enable GPMC_BE0n_CLE, output upper-byte enable GPMC_BE1n valid time  | Read   |                      | N <sup>(12)</sup>   | ns   |
|      |                                     |   | Write  |                      | N <sup>(12)</sup>   |      |
| FA1  | $t_{w(\text{csn}V)}$                | Pulse duration, output chip select GPMC_CS[n][j] <sup>(13)</sup> low  | Read   |                      | A <sup>(1)</sup>    | ns   |
|      |                                     |   | Write  |                      | A <sup>(1)</sup>    |      |
| FA3  | $t_{d(\text{csn}V\text{-advn}V)}$   | Delay time, output chip select GPMC_CS[n][j] <sup>(13)</sup> valid to output address valid and address latch enable GPMC_ADVn_ALE invalid                                       | Read   | -2+B <sup>(2)</sup>  | 2+B <sup>(2)</sup>  | ns   |
|      |                                     |   | Write  | -2+B <sup>(2)</sup>  | 2+B <sup>(2)</sup>  |      |
| FA4  | $t_{d(\text{csn}V\text{-oen}V)}$    | Delay time, output chip select GPMC_CS[n][j] <sup>(13)</sup> valid to output enable GPMC_OEn_REn invalid (Single read)  | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | -2+C <sup>(3)</sup>  | 2+C <sup>(3)</sup>  | ns   |
| FA9  | $t_{d(\text{a}V\text{-csn}V)}$      | Delay time, output address GPMC_A[27:1] valid to output chip select GPMC_CS[n][j] <sup>(13)</sup> valid   | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | -2+J <sup>(9)</sup>  | 2+J <sup>(9)</sup>  | ns   |
| FA10 | $t_{d(\text{be}[x]nV\text{-csn}V)}$ | Delay time, output lower-byte enable and command latch enable GPMC_BE0n_CLE, output upper-byte enable GPMC_BE1n valid to output chip select GPMC_CS[n][j] <sup>(13)</sup> valid | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | -2+J <sup>(9)</sup>  | 2+J <sup>(9)</sup>  | ns   |
| FA12 | $t_{d(\text{csn}V\text{-advn}V)}$   | Delay time, output chip select GPMC_CS[n][j] <sup>(13)</sup> valid to output address valid and address latch enable GPMC_ADVn_ALE valid   | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | -2+K <sup>(10)</sup> | 2+K <sup>(10)</sup> | ns   |
| FA13 | $t_{d(\text{csn}V\text{-oen}V)}$    | Delay time, output chip select GPMC_CS[n][j] <sup>(13)</sup> valid to output enable GPMC_OEn_REn valid  | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | -2+L <sup>(11)</sup> | 2+L <sup>(11)</sup> | ns   |
| FA16 | $t_{w(\text{a}V)}$                  | Pulse duration output address GPMC_A[26:1] invalid between 2 successive read and write accesses   | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | G <sup>(7)</sup>     |                     | ns   |
| FA18 | $t_{d(\text{csn}V\text{-oen}V)}$    | Delay time, output chip select GPMC_CS[n][j] <sup>(13)</sup> valid to output enable GPMC_OEn_REn invalid (Burst read)   | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | -2+I <sup>(8)</sup>  | 2+I <sup>(8)</sup>  | ns   |
| FA20 | $t_{w(\text{a}V)}$                  | Pulse duration, output address GPMC_A[27:1] valid - 2nd, 3rd, and 4th accesses  | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | D <sup>(4)</sup>     |                     | ns   |
| FA25 | $t_{d(\text{csn}V\text{-wen}V)}$    | Delay time, output chip select GPMC_CS[n][j] <sup>(13)</sup> valid to output write enable GPMC_WEn valid  | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | -2+E <sup>(5)</sup>  | 2+E <sup>(5)</sup>  | ns   |
| FA27 | $t_{d(\text{csn}V\text{-wen}V)}$    | Delay time, output chip select GPMC_CS[n][j] <sup>(13)</sup> valid to output write enable GPMC_WEn invalid  | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | -2+F <sup>(6)</sup>  | 2+F <sup>(6)</sup>  | ns   |
| FA28 | $t_{d(\text{wen}V\text{-d}V)}$      | Delay time, output write enable GPMC_WEn valid to output data GPMC_AD[15:0] valid   | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 |                      | 2                   | ns   |
| FA29 | $t_{d(\text{d}V\text{-csn}V)}$      | Delay time, output data GPMC_AD[15:0] valid to output chip select GPMC_CS[n][j] <sup>(13)</sup> valid   | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | -2+J <sup>(9)</sup>  | 2+J <sup>(9)</sup>  | ns   |
| FA37 | $t_{d(\text{oen}V\text{-a}V)}$      | Delay time, output enable GPMC_OEn_REn valid to output address GPMC_AD[15:0] phase end  | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 |                      | 2                   | ns   |

- (1) For single read:  $A = (\text{CSRdOffTime} - \text{CSONTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(14)}$   
 For single write:  $A = (\text{CSWrOffTime} - \text{CSONTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(14)}$   
 For burst read:  $A = (\text{CSRdOffTime} - \text{CSONTime} + (n - 1) \times \text{PageBurstAccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(14)}$   
 For burst write:  $A = (\text{CSWrOffTime} - \text{CSONTime} + (n - 1) \times \text{PageBurstAccessTime}) \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(14)}$   
 with n being the page burst access number
- (2) For reading:  $B = ((\text{ADVrdOffTime} - \text{CSONTime}) \times (\text{TimeParaGranularity} + 1) + 0.5 \times (\text{ADVExtraDelay} - \text{CSEExtraDelay})) \times \text{GPMC\_FCLK}^{(14)}$

- For writing:  $B = ((ADVWrOffTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (ADVExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$
- (3)  $C = ((OEOffTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (OEExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$
- (4)  $D = PageBurstAccessTime \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$
- (5)  $E = ((WEOnTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (WEEExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$
- (6)  $F = ((WEOffTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (WEEExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$
- (7)  $G = Cycle2CycleDelay \times GPMC\_FCLK^{(14)}$
- (8)  $I = ((OEOffTime + (n - 1) \times PageBurstAccessTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (OEExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$
- (9)  $J = (CSOnTime \times (TimeParaGranularity + 1) + 0.5 \times CSEExtraDelay) \times GPMC\_FCLK^{(14)}$
- (10)  $K = ((ADVOnTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (ADVExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$
- (11)  $L = ((OEOnTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (OEExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$
- (12) For single read:  $N = RdCycleTime \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$   
For single write:  $N = WrCycleTime \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$   
For burst read:  $N = (RdCycleTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$   
For burst write:  $N = (WrCycleTime + (n - 1) \times PageBurstAccessTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$
- (13) In GPMC\_CS*n*[*i*], *i* is equal to 0, 1, 2 or 3.
- (14) GPMC\_FCLK is general-purpose memory controller internal functional clock period in ns.
- (15) For div\_by\_1\_mode:

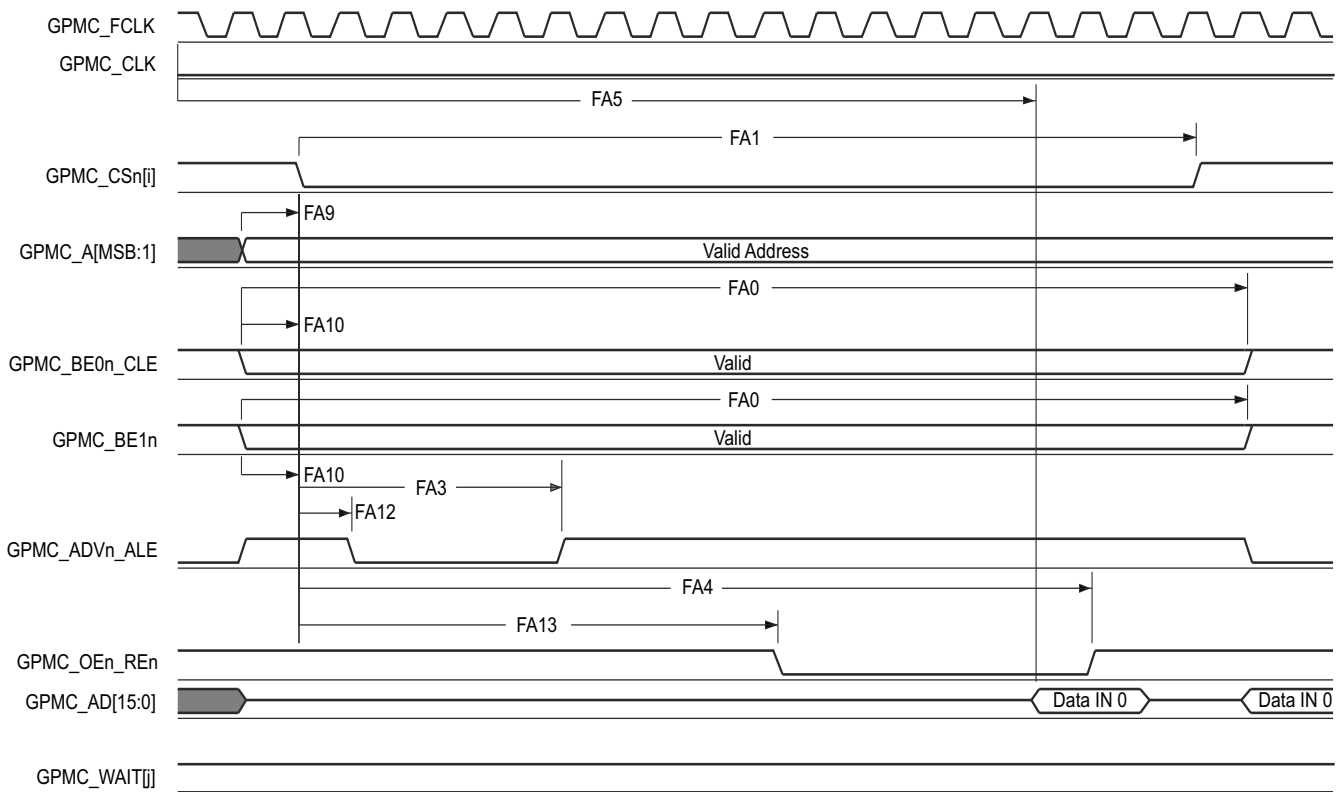
- GPMC\_CONFIG1\_0 Register: GPMCFCLKDIVIDER = 0h:
  - GPMC\_CLK frequency = GPMC\_FCLK frequency

For GPMC\_FCLK\_MUX:

- CTRLMMR\_GPMC\_CLKSEL[1-0] CLK\_SEL = 00 = CPSWHSIDIV\_CLKOUT3 = 2000/15 = 133.33 MHz

For TIMEPARAGRANULARITY\_X1:

- GPMC\_CONFIG1\_0 Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

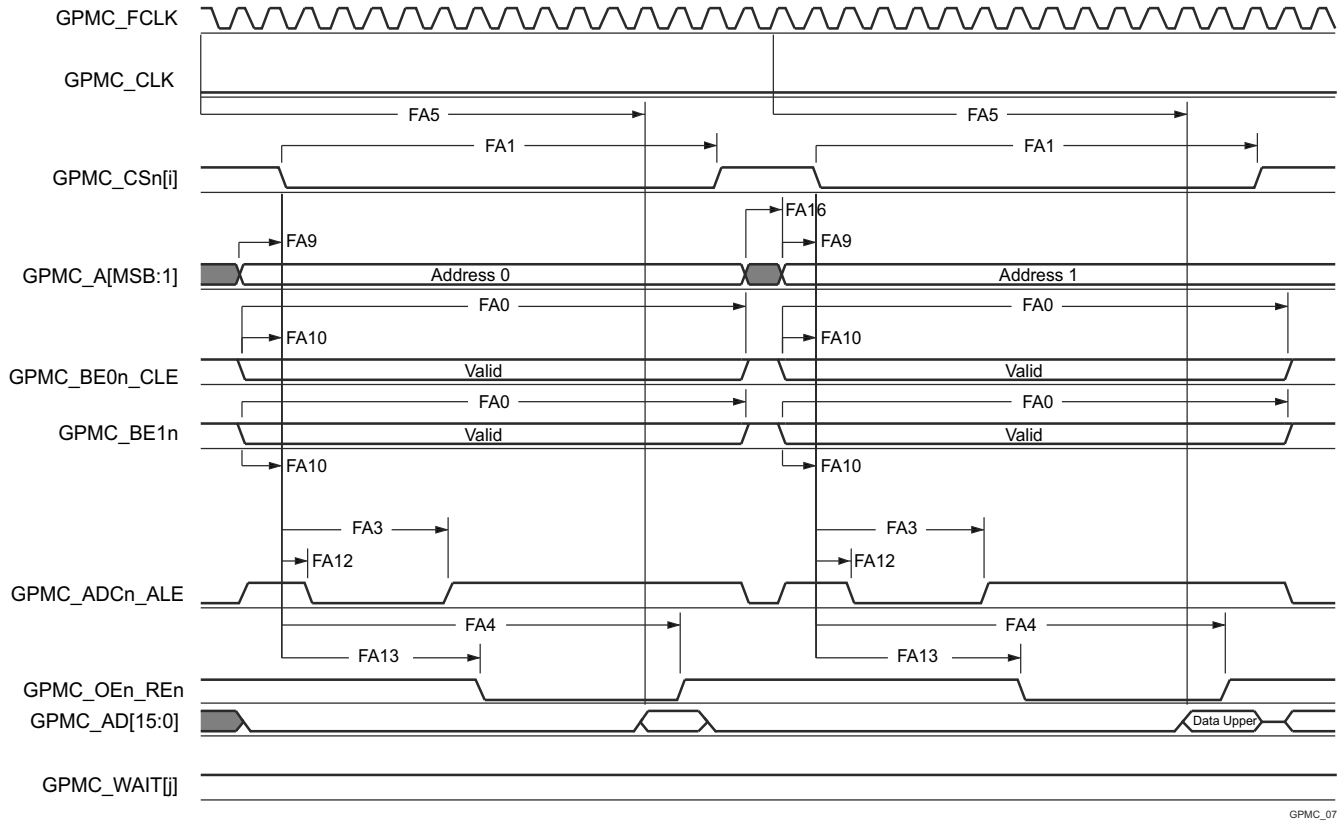


GPMC\_06

- A. In GPMC\_CS*n*[*i*], *i* is equal to 0, 1, 2 or 3. In GPMC\_WAIT[*j*], *j* is equal to 0 or 1.

- B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
- C. GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.

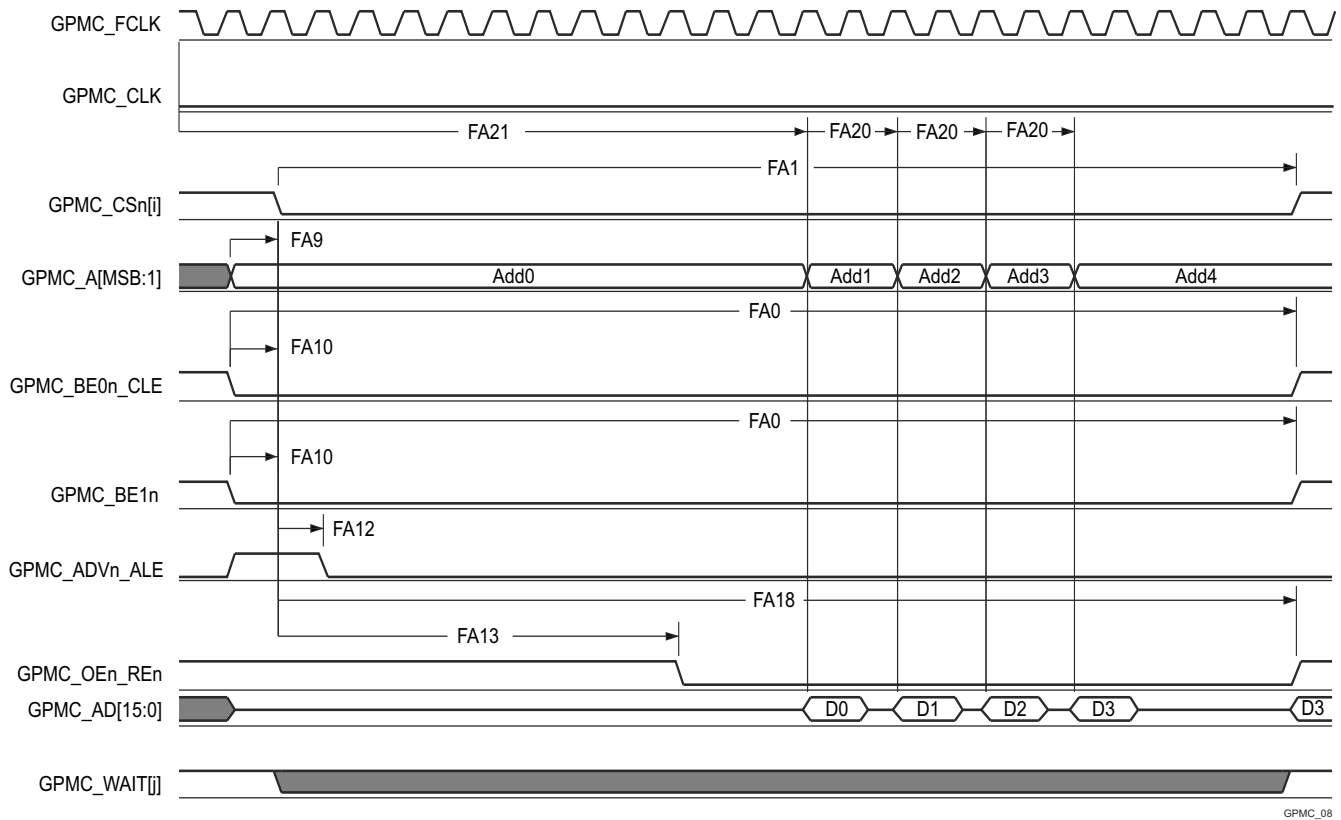
**Figure 6-64. GPMC and NOR Flash — Asynchronous Read — Single Word**



GPMC\_07

- A. In GPMC\_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0 or 1.
- B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
- C. GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.

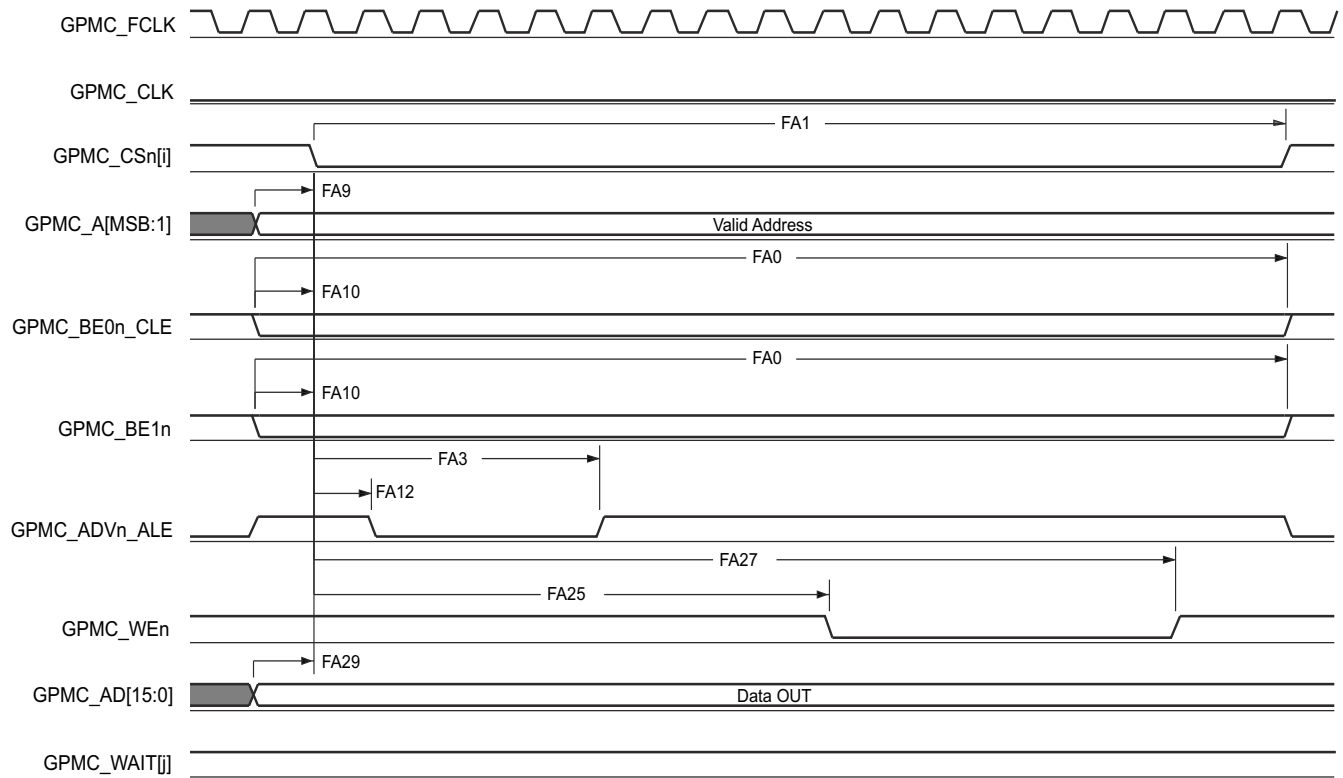
**Figure 6-65. GPMC and NOR Flash — Asynchronous Read — 32-Bit**



GPMC\_08

- In GPMC\_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0 or 1.
- FA21 parameter illustrates amount of time required to internally sample first input page data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, first input page data will be internally sampled by active functional clock edge. FA21 calculation must be stored inside AccessTime register bits field.
- FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data will be internally sampled by active functional clock edge after FA20 functional clock cycles. FA20 is also the duration of address phases for successive input page data (excluding first input page data). FA20 value must be stored in PageBurstAccessTime register bits field.
- GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.

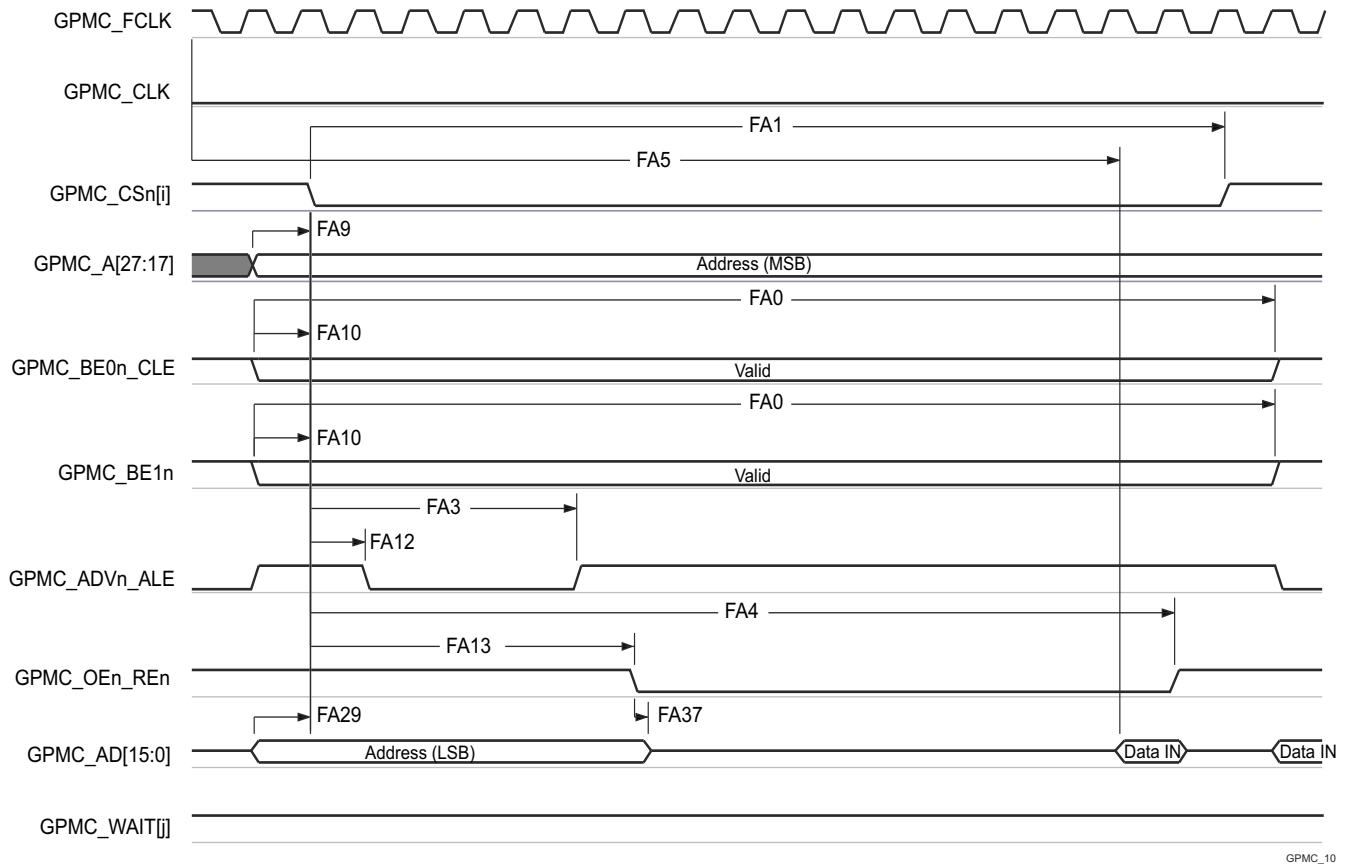
**Figure 6-66. GPMC and NOR Flash — Asynchronous Read — Page Mode 4x16-Bit**



GPMC\_09

A. In GPMC\_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0 or 1.

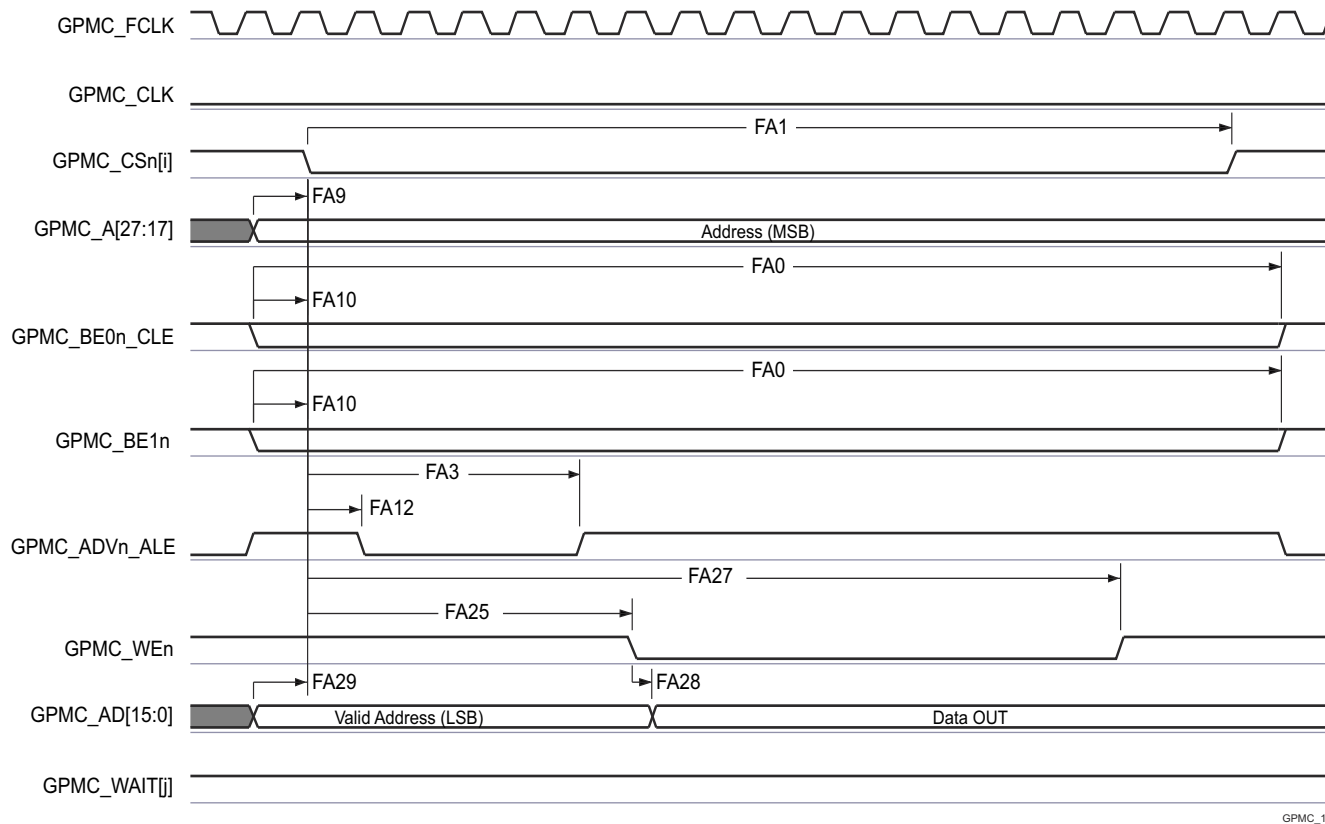
**Figure 6-67. GPMC and NOR Flash — Asynchronous Write — Single Word**



GPMC\_10

- A. In GPMC\_CS[n], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0 or 1.
- B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
- C. GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.

**Figure 6-68. GPMC and Multiplexed NOR Flash — Asynchronous Read — Single Word**



GPMC\_11

A. In GPMC\_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], j is equal to 0 or 1.

**Figure 6-69. GPMC and Multiplexed NOR Flash — Asynchronous Write — Single Word**

### 6.10.5.9.3 GPMC and NAND Flash — Asynchronous Mode

Section 6.10.5.9.3.1 and Section 6.10.5.9.3.2 assume testing over the recommended operating conditions and electrical characteristic conditions below (see Figure 6-70 through Figure 6-73).

For more information, see *General-Purpose Memory Controller (GPMC)* section in *Peripherals* chapter in the device TRM.

#### 6.10.5.9.3.1 GPMC and NAND Flash Timing Requirements – Asynchronous Mode

| NO.                  | PARAMETER           | DESCRIPTION  | MODE <sup>(4)</sup>  | MIN     | MAX              | UNIT |
|----------------------|---------------------|--|--|---------|------------------|------|
|                      |                     |  |  | 133 MHz |                  |      |
| GNF12 <sup>(1)</sup> | t <sub>acc(d)</sub> | Access time, input data GPMC_AD[15:0] <sup>(3)</sup> | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 |         | J <sup>(2)</sup> | ns   |

(1) The GNF12 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of the read cycle and after GNF12 functional clock cycles, input data is internally sampled by the active functional clock edge. The GNF12 value must be stored inside AccessTime register bit field.

(2)  $J = \text{AccessTime} \times (\text{TimeParaGranularity} + 1) \times \text{GPMC\_FCLK}^{(3)}$

(3) GPMC\_FCLK is general-purpose memory controller internal functional clock period in ns.

(4) For div\_by\_1\_mode:

- GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 0h:
  - GPMC\_CLK frequency = GPMC\_FCLK frequency

For GPMC\_FCLK\_MUX:

- CTRLMMR\_GPMC\_CLKSEL[1-0] CLK\_SEL = 00 = CPSWHS DIV\_CLKOUT3 = 2000/15 = 133.33 MHz

For TIMEPARAGRANULARITY\_X1:

- GPMC\_CONFIG1\_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRD/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEONTIME, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)

#### 6.10.5.9.3.2 GPMC and NAND Flash Switching Characteristics – Asynchronous Mode

| NO.  | PARAMETER                     | DESCRIPTION  | MODE <sup>(15)</sup>                                       | MIN                 | MAX                | UNIT |
|------|-------------------------------|--|--|---------------------|--------------------|------|
| GNF0 | t <sub>w(wenV)</sub>          | Pulse duration, output write enable GPMC_WEn valid   | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | A <sup>(1)</sup>    |                    | ns   |
| GNF1 | t <sub>d(csnV-wenV)</sub>     | Delay time, output chip select GPMC_CS <sub>n</sub> [i] <sup>(13)</sup> valid to output write enable GPMC_WEn valid                      | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | -2+B <sup>(2)</sup> | 2+B <sup>(2)</sup> | ns   |
| GNF2 | t <sub>w(cleH-wenV)</sub>     | Delay time, output lower-byte enable and command latch enable GPMC_BE0 <sub>n</sub> _CLE high to output write enable GPMC_WEn valid      | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | -2+C <sup>(3)</sup> | 2+C <sup>(3)</sup> | ns   |
| GNF3 | t <sub>w(wenV-dV)</sub>       | Delay time, output data GPMC_AD[15:0] valid to output write enable GPMC_WEn valid  | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | -2+D <sup>(4)</sup> | 2+D <sup>(4)</sup> | ns   |
| GNF4 | t <sub>w(wenIV-dIV)</sub>     | Delay time, output write enable GPMC_WEn invalid to output data GPMC_AD[15:0] invalid  | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | -2+E <sup>(5)</sup> | 2+E <sup>(6)</sup> | ns   |
| GNF5 | t <sub>w(wenIV-cleIV)</sub>   | Delay time, output write enable GPMC_WEn invalid to output lower-byte enable and command latch enable GPMC_BE0 <sub>n</sub> _CLE invalid | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | -2+F <sup>(6)</sup> | 2+F <sup>(6)</sup> | ns   |
| GNF6 | t <sub>w(wenIV-CSn[i]V)</sub> | Delay time, output write enable GPMC_WEn invalid to output chip select GPMC_CS <sub>n</sub> [i] <sup>(13)</sup> invalid                  | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | -2+G <sup>(7)</sup> | 2+G <sup>(7)</sup> | ns   |
| GNF7 | t <sub>w(aleH-wenV)</sub>     | Delay time, output address valid and address latch enable GPMC_ADV <sub>n</sub> _ALE high to output write enable GPMC_WEn valid          | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | -2+C <sup>(3)</sup> | 2+C <sup>(3)</sup> | ns   |

| NO.   | PARAMETER   | MODE <sup>(15)</sup>                                       | MIN                  | MAX                 | UNIT |
|-------|---|--|----------------------|---------------------|------|
| GNF8  | $t_{w(wenIV-aleIV)}$<br>Delay time, output write enable GPMC_WEn invalid to output address valid and address latch enable GPMC_ADVn_ALE invalid | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | -2+F <sup>(6)</sup>  | 2+F <sup>(6)</sup>  | ns   |
| GNF9  | $t_{c(wen)}$<br>Cycle time, write   | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 |                      | H <sup>(8)</sup>    | ns   |
| GNF10 | $t_{d(csnV-oenV)}$<br>Delay time, output chip select GPMC_CSn[i] <sup>(13)</sup> valid to output enable GPMC_OEn_REn valid                      | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | -2+I <sup>(9)</sup>  | 2+I <sup>(9)</sup>  | ns   |
| GNF13 | $t_{w(oenV)}$<br>Pulse duration, output enable GPMC_OEn_REn valid   | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 |                      | K <sup>(10)</sup>   | ns   |
| GNF14 | $t_{c(oen)}$<br>Cycle time, read  | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | L <sup>(11)</sup>    |                     | ns   |
| GNF15 | $t_{w(oenIV-CSn[i]V)}$<br>Delay time, output enable GPMC_OEn_REn invalid to output chip select GPMC_CSn[i] <sup>(13)</sup> invalid              | div_by_1_mode;<br>GPMC_FCLK_MUX;<br>TIMEPARAGRANULARITY_X1 | -2+M <sup>(12)</sup> | 2+M <sup>(12)</sup> | ns   |

- (1)  $A = (WEOffTime - WEOnTime) \times (TimeParaGranularity + 1) \times GPMC\_FCLK^{(14)}$   
(2)  $B = ((WEOnTime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (WEEExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$   
(3)  $C = ((WEOnTime - ADVOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (WEEExtraDelay - ADVExtraDelay)) \times GPMC\_FCLK^{(14)}$   
(4)  $D = (WEOnTime \times (TimeParaGranularity + 1) + 0.5 \times WEEExtraDelay) \times GPMC\_FCLK^{(14)}$   
(5)  $E = ((WrCycleTime - WEOffTime) \times (TimeParaGranularity + 1) - 0.5 \times WEEExtraDelay) \times GPMC\_FCLK^{(14)}$   
(6)  $F = ((ADVWrOffTime - WEOffTime) \times (TimeParaGranularity + 1) + 0.5 \times (ADVExtraDelay - WEEExtraDelay)) \times GPMC\_FCLK^{(14)}$   
(7)  $G = ((CSWrOffTime - WEOffTime) \times (TimeParaGranularity + 1) + 0.5 \times (CSEExtraDelay - WEEExtraDelay)) \times GPMC\_FCLK^{(14)}$   
(8)  $H = WrCycleTime \times (1 + TimeParaGranularity) \times GPMC\_FCLK^{(14)}$   
(9)  $I = ((OEOntime - CSOnTime) \times (TimeParaGranularity + 1) + 0.5 \times (OEEExtraDelay - CSEExtraDelay)) \times GPMC\_FCLK^{(14)}$   
(10)  $K = (OEOffTime - OEOntime) \times (1 + TimeParaGranularity) \times GPMC\_FCLK^{(14)}$   
(11)  $L = RdCycleTime \times (1 + TimeParaGranularity) \times GPMC\_FCLK^{(14)}$   
(12)  $M = ((CSRdOffTime - OEOffTime) \times (TimeParaGranularity + 1) + 0.5 \times (CSEExtraDelay - OEEExtraDelay)) \times GPMC\_FCLK^{(14)}$   
(13) In GPMC\_CSn[i], i is equal to 0, 1, 2 or 3.  
(14) GPMC\_FCLK is general-purpose memory controller internal functional clock period in ns.  
(15) For div\_by\_1\_mode:

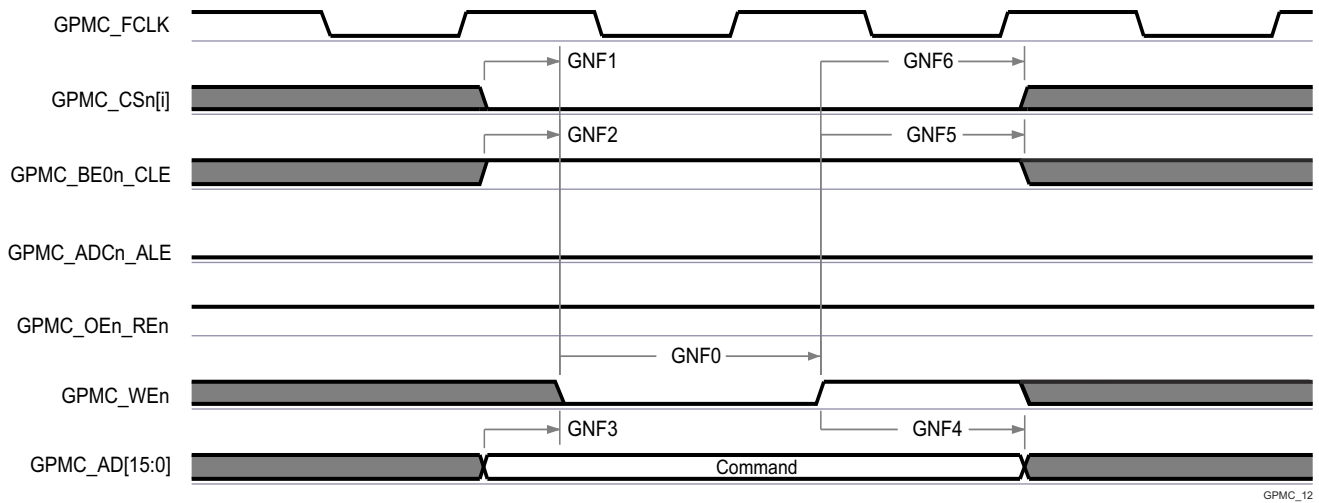
- GPMC\_CONFIG1\_i Register: GPMCFCLKDIVIDER = 0h:  
– GPMC\_CLK frequency = GPMC\_FCLK frequency

For GPMC\_FCLK\_MUX:

- CTRLMMR\_GPMC\_CLKSEL[1-0] CLK\_SEL = 00 = CPSWHS DIV\_CLKOUT3 = 2000/15 = 133.33 MHz

For TIMEPARAGRANULARITY\_X1:

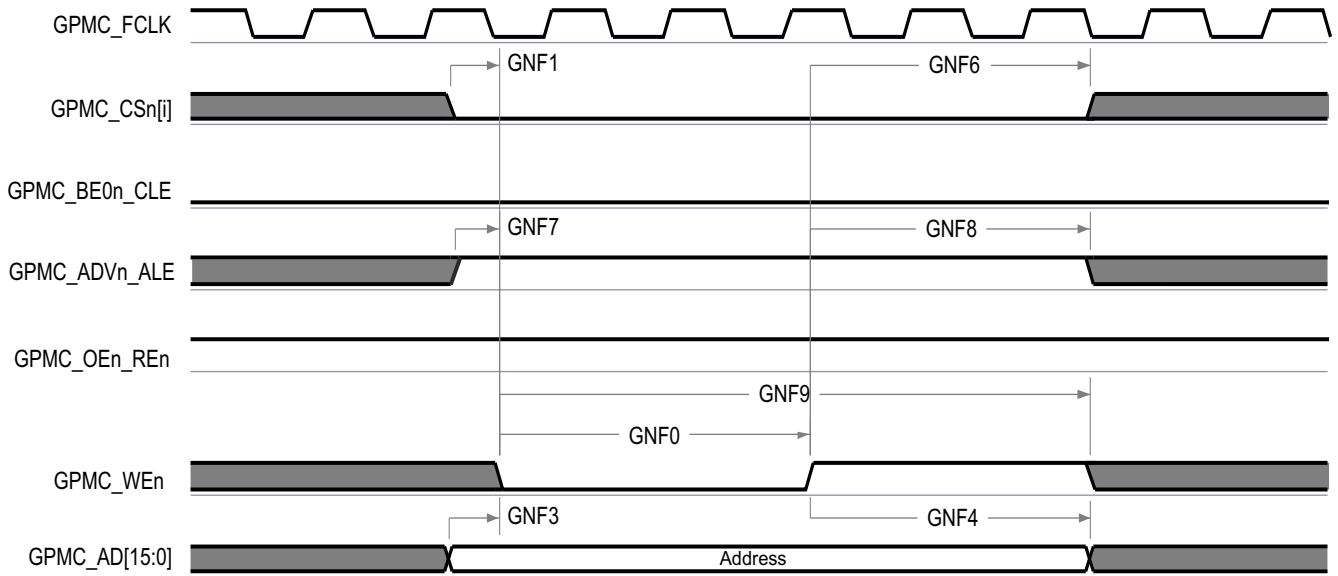
- GPMC\_CONFIG1\_i Register: TIMEPARAGRANULARITY = 0h = x1 latencies (affecting RD/WRCYCLETIME, RD/WRACCESSTIME, PAGEBURSTACCESSTIME, CSONTIME, CSRd/WROFFTIME, ADVONTIME, ADVRD/WROFFTIME, OEOntime, OEOFFTIME, WEONTIME, WEOFFTIME, CYCLE2CYCLEDELAY, BUSTURNAROUND, TIMEOUTSTARTVALUE, WRDATAONADMUXBUS)



GPMC\_12

A. In GPMC\_CS[n], i is equal to 0, 1, 2 or 3.

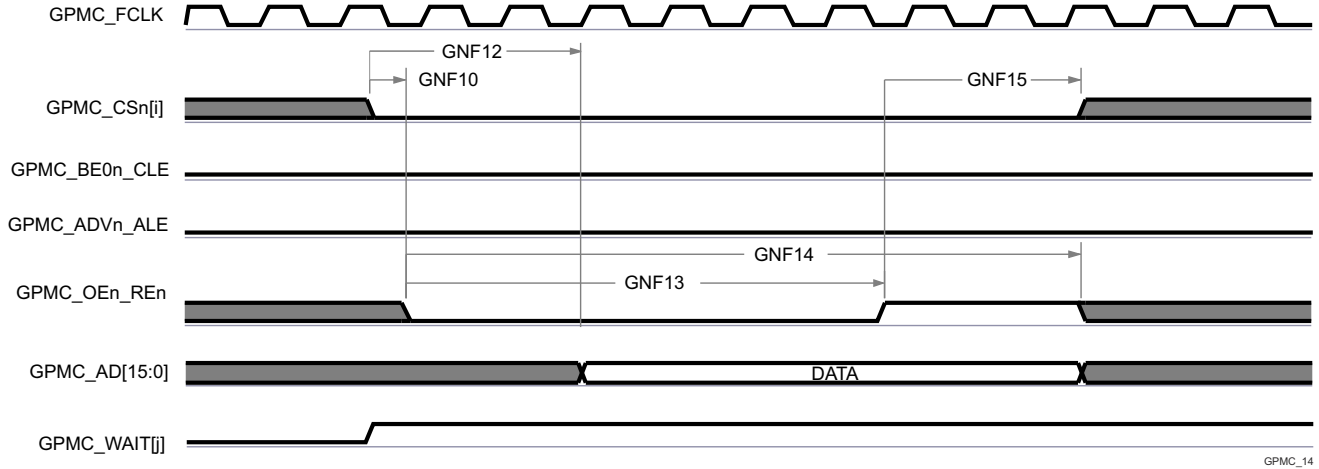
**Figure 6-70. GPMC and NAND Flash — Command Latch Cycle**



GPMC\_13

A. In GPMC\_CS[n], i is equal to 0, 1, 2 or 3.

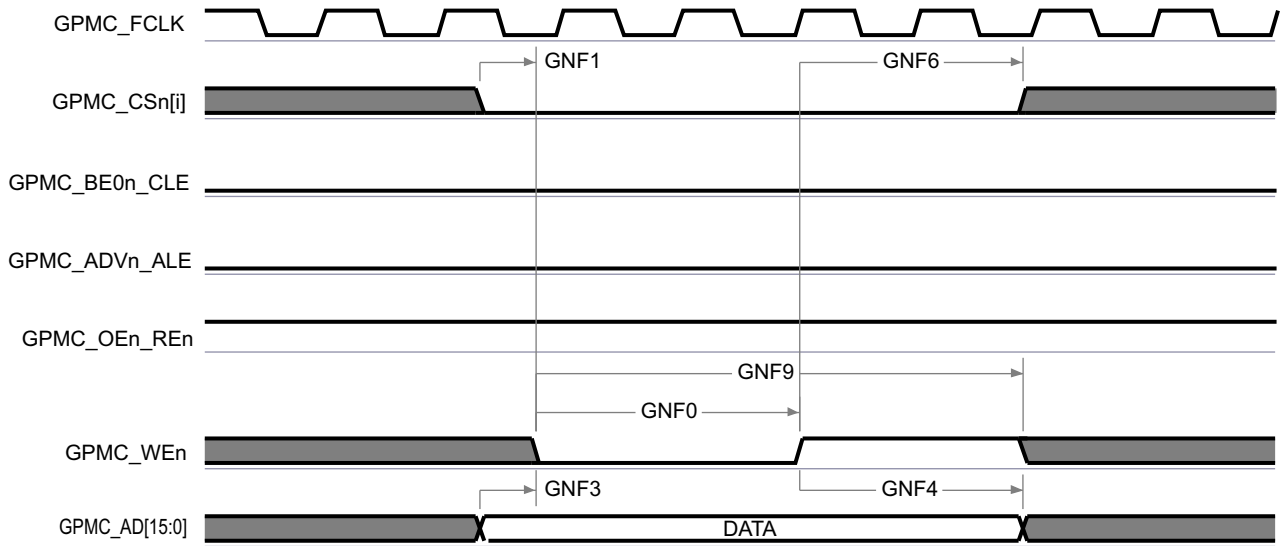
**Figure 6-71. GPMC and NAND Flash — Address Latch Cycle**



GPMC\_14

- A. GNF12 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after GNF12 functional clock cycles, input data will be internally sampled by active functional clock edge. GNF12 value must be stored inside AccessTime register bits field.
- B. GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.
- C. In GPMC\_CS*n*[*i*], *i* is equal to 0, 1, 2 or 3. In GPMC\_WAIT[j], *j* is equal to 0 or 1.

**Figure 6-72. GPMC and NAND Flash — Data Read Cycle**



GPMC\_15

- A. In GPMC\_CS*n*[*i*], *i* is equal to 0, 1, 2 or 3.

**Figure 6-73. GPMC and NAND Flash — Data Write Cycle**

**6.10.5.10 HyperBus**

For more details about features and additional description information on the device HyperBus, see the corresponding sections within [Section 5.3, Signal Descriptions](#) and [Section 7, Detailed Description](#).

[Section 6.10.5.10.1](#), [Section 6.10.5.10.2](#), and [Section 6.10.5.10.3](#) assume testing over the recommended operating conditions and electrical characteristic conditions (see [Figure 6-74](#), [Figure 6-75](#), and [Figure 6-76](#)).

[Table 6-44](#) represents HyperBus timing conditions.

**Table 6-44. HyperBus Timing Conditions**

| PARAMETER                | DESCRIPTION             | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>Input Conditions</b>  |                         |     |     |      |
| $t_{SR}$                 | Input slew rate         | 2   | 5   | V/ns |
| <b>Output Conditions</b> |                         |     |     |      |
| $C_{LOAD}$               | Output load capacitance | 1.5 | 10  | pF   |

**6.10.5.10.1 Timing Requirements for HyperBus Initialization**

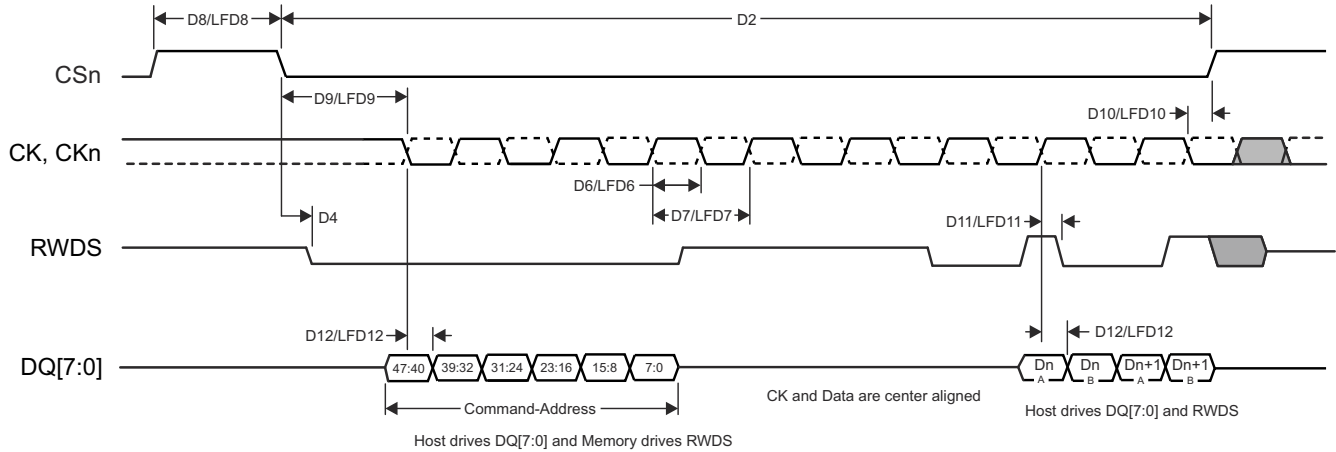
| NO. | PARAMETER            | DESCRIPTION                               | MIN    | MAX | UNIT |
|-----|----------------------|---|--------|-----|------|
| D1  | $t_{W(RESETn)}$      | RESETn Pulse Width                        | 200    |     | ns   |
| D2  | $t_{W(csL)}$         | Chip Select Pulse Width                   | 1000   |     | ns   |
| D3  | $t_{d(RESETnH-csL)}$ | Delay time, RESETn inactive to CSn active | 200.34 |     | ns   |
| D4  | $t_{d(csL-RWDSL)}$   | Delay time, CSn active to RWDS falling    | 115    |     | ns   |

**6.10.5.10.2 HyperBus 166 MHz Switching Characteristics**

| NO. | PARAMETER             | DESCRIPTION  | MIN   | MAX   | UNIT |
|-----|-----------------------|--|-------|-------|------|
| D5  | $t_{skn(rwdsX-dV)}$   | Input skew, RWDS transitioning to D0:D7 valid                  | -0.46 | 0.46  | ns   |
| D6  | $t_{c(clk/clkn)}$     | CLK period, CLK/CLKn   | 6     |       | ns   |
| D7  | $t_{W(clk/clkn)}$     | Pulse width, CLK/CLKn  | 2.7   |       | ns   |
| D8  | $t_{W(csIV)}$         | Pulse width, CS0 invalid between operations                    | 6     |       | ns   |
| D9  | $t_{d(clkH-csL)}$     | Delay time, CS0 active to CLK rising/ CLKn falling             |       | -3.34 | ns   |
| D10 | $t_{d(clkL[LE]-csH)}$ | Delay time, last falling CLK/ rising CLKn edge to CS0 inactive | 0.41  |       | ns   |
| D11 | $t_{d(clkX-rwdsV)}$   | Delay time, CLK transition to RWDS valid                       | 1.01  | 2.08  | ns   |
| D12 | $t_{d(clkX-d[0:7]V)}$ | Delay time, CLK transitioning to D0:D7 valid                   | 0.84  | 2.17  | ns   |

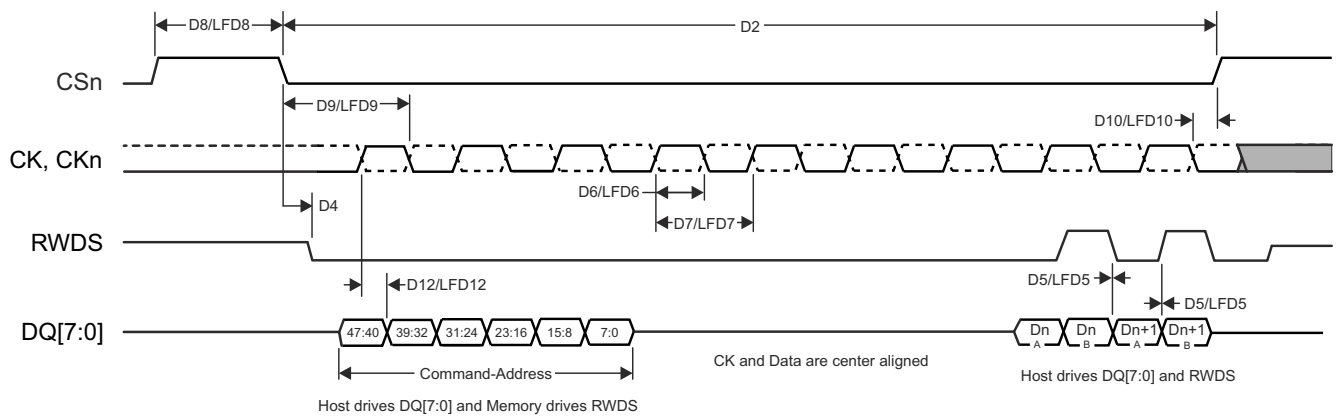
**6.10.5.10.3 HyperBus 100 MHz Switching Characteristics**

| NO.   | PARAMETER             | DESCRIPTION                                       | MIN   | MAX   | UNIT |
|-------|-----------------------|---|-------|-------|------|
| LFD5  | $t_{skn(rwdsX-dV)}$   | Input skew, RWDS transitioning to D0:D7 valid     | -0.81 | 0.81  | ns   |
| LFD6  | $t_{c(clk)}$          | CLK period, CLK                                   | 10    |       | ns   |
| LFD7  | $t_{W(clk)}$          | Pulse width, CLK                                  | 4.75  |       | ns   |
| LFD8  | $t_{W(csIV)}$         | Pulse width, CS0 invalid between operations       | 10    |       | ns   |
| LFD9  | $t_{d(clkH-csL)}$     | Delay time, CS0 active to CLK rising              |       | -3.51 | ns   |
| LFD10 | $t_{d(clkL[LE]-csH)}$ | Delay time, last falling CLK edge to CS0 inactive | 0.51  |       | ns   |
| LFD11 | $t_{d(clkX-rwdsV)}$   | Delay time, CLK transition to RWDS valid          | 1.51  | 3.49  | ns   |
| LFD12 | $t_{d(clkX-d[0:7]V)}$ | Delay time, CLK transitioning to D0:D7 valid      | 1.34  | 3.66  | ns   |



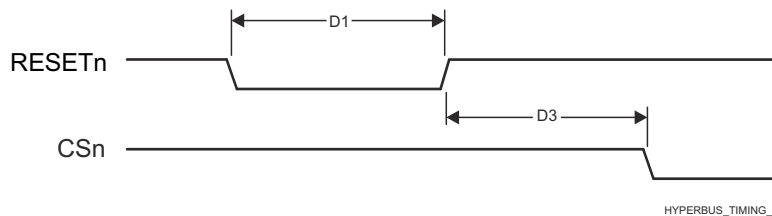
HYPERBUS\_TIMING\_01

**Figure 6-74. HyperBus Timing Diagrams – Transmitter Mode**



HYPERBUS\_TIMING\_02

**Figure 6-75. HyperBus Timing Diagrams – Receiver Mode**



HYPERBUS\_TIMING\_03

**Figure 6-76. HyperBus Timing Diagrams – Reset**

For more information, see *HyperBus Interface* section in *Peripherals* chapter in the device TRM.

#### 6.10.5.11 I2C

The device contains six multicontroller Inter-Integrated Circuit (I2C) controllers. Each I2C controller was designed to be compliant to the Philips I<sup>2</sup>C-bus™ specification version 2.1. However, the device IOs are not fully compliant to the I2C electrical specification. The speeds supported and exceptions are described per port below:

- MCU\_I2C1, I2C1, I2C2, I2C3, I2C4, I2C5 and I2C6
  - Speeds:

- Standard-mode (up to 100 Kbits/s)
  - 1.8 V
  - 3.3 V
- Fast-mode (up to 400 Kbits/s)
  - 1.8 V
  - 3.3 V
- Exceptions:
  - The IOs associated with these ports are not compliant to the fall time requirements defined in the I2C specification because they are implemented with higher performance LVCMOS push-pull IOs that were designed to support other signal functions that could not be implemented with I2C compatible IOs. The LVCMOS IOs being used on these ports are connected such they emulate open-drain outputs. This emulation is achieved by forcing a constant low output and disabling the output buffer to enter the Hi-Z state.
  - The I2C specification defines a maximum input voltage  $V_{IH}$  of  $(V_{DD_{max}} + 0.5 V)$ , which exceeds the absolute maximum ratings for the device IOs. The system must be designed to ensure the I2C signals never exceed the limits defined in the *Absolute Maximum Ratings* section of this datasheet.
- WAKEUP\_I2C0, MCU\_I2C0, and I2C0
  - Speeds:
    - Standard-mode (up to 100 Kbits/s)
      - 1.8 V
      - 3.3 V
    - Fast-mode (up to 400 Kbits/s)
      - 1.8 V
      - 3.3 V
    - Hs-mode (up to 3.4 Mbit/s)
      - 1.8 V
  - Exceptions:
    - The IOs associated with these ports were not design to support Hs-mode while operating at 3.3 V. So Hs-mode is limited to 1.8-V operation.
    - The rise and fall times of the I2C signals connected to these ports must not exceed a slew rate of 0.8 V/ns (or 8E+7 V/s). This limit is more restrictive than the minimum fall time limits defined in the I2C specification. Therefore, it may be necessary to add additional capacitance to the I2C signals to slow the rise and fall times such that they do not exceed a slew rate of 0.8 V/ns.
    - The I2C specification defines a maximum input voltage  $V_{IH}$  of  $(V_{DD_{max}} + 0.5 V)$ , which exceeds the absolute maximum ratings for the device IOs. The system must be designed to ensure the I2C signals never exceed the limits defined in the *Absolute Maximum Ratings* section of this datasheet.

Refer to the Philips I2C-bus specification version 2.1 for timing details.

For more details about features and additional description information on the device Inter-Integrated Circuit, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

#### 6.10.5.12 I3C

For more details about features and additional description information on the device Inter-Integrated Circuit, see the corresponding sections within [Section 5.3](#), *Signal Descriptions* and [Section 7](#), *Detailed Description*.

[Table 6-45](#), [Table 6-46](#), [Figure 6-77](#), [Table 6-47](#), and [Figure 6-78](#) assume testing over the recommended operating conditions and electrical characteristic conditions.

**Table 6-45. I3C Open Drain Timing Conditions**

| PARAMETER                |                 | MIN    | MAX | UNIT |
|--------------------------|-----------------|--------|-----|------|
| <b>INPUT CONDITIONS</b>  |                 |        |     |      |
| SR <sub>I</sub>          | Input slew rate | 0.2276 | 5   | V/ns |
| <b>OUTPUT CONDITIONS</b> |                 |        |     |      |

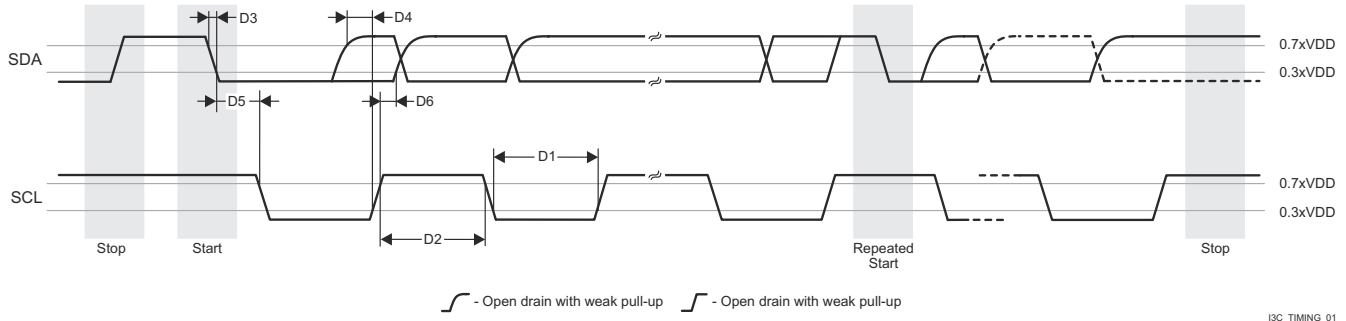
**Table 6-45. I3C Open Drain Timing Conditions (continued)**

| PARAMETER                     | MIN | MAX | UNIT |
|-------------------------------|-----|-----|------|
| $C_L$ Output load capacitance |     | 50  | pF   |

**Table 6-46. I3C Open Drain Timing Parameters**

| NO. | PARAMETER          | DESCRIPTION  | MODE               | MIN                                   | MAX     | UNIT |
|-----|--------------------|--|--------------------|---------------------------------------|---------|------|
| D1  | $t_{LOW\_OD}$      | Low Period of SCL Clock  | Controller         | 200                                   |         | ns   |
|     | $t_{DIG\_OD\_L}$   |  |                    | $t_{LOW\_OD\ MIN} + t_{FDA\_OD\ MIN}$ |         | ns   |
| D2  | $t_{HIGH}$         | High Period of SCL Clock   | Controller         |                                       | 41      | ns   |
|     | $t_{DIG\_H}$       |  |                    | $t_{HIGH} + t_{CF}$                   |         | ns   |
| D3  | $t_{rDA\_OD}$      | Fall Time of SDA Signal  | Controller, Target | $t_{CF}$                              | 12      | ns   |
| D4  | $t_{SU\_OD}$       | SDA Data Setup Time During Open Drain Mode                             | Controller, Target | 3                                     |         | ns   |
| D5  | $t_{CAS}$          | Clock After START (S) Condition  | Controller, ENTAS0 | 38.4                                  | 1000    | ns   |
|     |                    |  | Controller, ENTAS1 | 38.4                                  | 100000  | ns   |
|     |                    |  | Controller, ENTAS2 | 38.4                                  | 2000000 | ns   |
|     |                    |  | Controller, ENTAS3 | 38.4                                  | 5000000 | ns   |
| D6  | $t_{CBP}$          | Clock Before STOP (P) Condition  | Controller         | $t_{CAS\ MIN} / 2$                    |         | ns   |
| D7  | $t_{MMOVEOVERLAP}$ | Current Controller to Secondary Controller Overlap time during handoff | Controller         | $t_{DIG\_OD\_L\ min}$                 |         | ns   |
| D8  | $t_{AVAL}$         | Bus Available Condition  | Controller         | 1000                                  |         | ns   |
| D9  | $t_{IDLE}$         | Bus Idle Condition   | Controller         | 1000000                               |         | ns   |
| D10 | $t_{MMLOCK}$       | Time Internal Where New Controller Not Driving SDA Low                 | Controller         | $t_{AVAL\ min}$                       |         | ns   |

1. This is approximately equal to  $t_{LOW\ min} + t_{DS\_OD\ min} + t_{rDA\_OD\ typ} + t_{SU\_OD\ min}$ .
2. The Controller may use a shorter Low period if the Controller knows that this is safe, when SDA is already above  $V_{IH}$ .
3. Based on  $t_{SPIKE}$ , rise and fall times, and interconnect.
4. This maximum High period may be exceeded when the signals can be safely seen by Legacy I2C Devices, and/or in consideration of the interconnect (for example: a short Bus).
5. On a Legacy Bus where I2C Devices need to see Start, the  $t_{CAS}$  Min value is further constrained.
6. Targets that do not support the optional ENTASx CCCs shall use the  $t_{CAS}$  Max value shown for ENTAS3.
7. On a Mixed Bus with Fm Legacy I2C Devices,  $t_{AVAL}$  is 300ns shorter than the Fm Bus Free Condition time ( $t_{BUF}$ ).

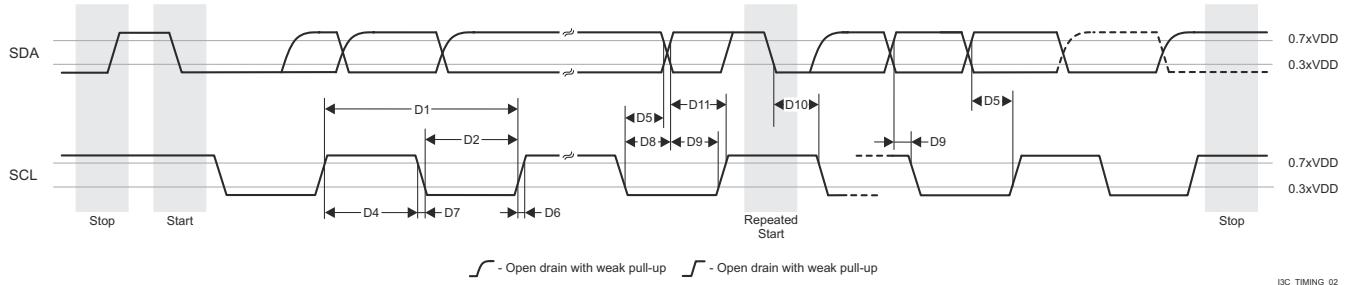


**Figure 6-77. I3C Open Drain Timing**

**Table 6-47. I3C Push-Pull Timing Parameters for SDR and HDR-DDR Modes**

| NO. | PARAMETER                | DESCRIPTION   | MODE                  | MIN  | MAX    | UNIT |
|-----|--------------------------|---|-----------------------|--|--------|------|
| D1  | f <sub>SCL</sub>         | SCL Clock Period  | Controller            | 80   | 100000 | ns   |
| D2  | t <sub>LOW</sub>         | SCL Clock Low Period  | Controller            | 24   |        | ns   |
|     | t <sub>DIG_L</sub>       |   |                       | 32   |        | ns   |
| D3  | t <sub>HIGH_MIXED</sub>  | SCL Clock High Period of Mixed Bus (Mixed Bus Topology Not Supported) | Controller            | 24   |        | ns   |
|     | t <sub>DIG_H_MIXED</sub> |   |                       | 32   | 45     | ns   |
| D4  | t <sub>HIGH</sub>        | SCL Clock High Period   | Controller            | 24   |        | ns   |
|     | t <sub>DIG_H</sub>       |   |                       | 32   |        | ns   |
| D5  | t <sub>SCO</sub>         | Clock in to Data Out for Target                                       | Target                | 12   |        | ns   |
| D6  | t <sub>CR</sub>          | SCL Clock Rise Time   | Controller            | 150 × 1 / f <sub>SCL</sub>                     | 60     | ns   |
| D7  | t <sub>CF</sub>          | SCL Clock Fall Time   | Controller            | 150 × 1 / f <sub>SCL</sub>                     | 60     | ns   |
| D8  | t <sub>HD_PP</sub>       | SDA Signal Data Hold in Push Pull Mode                                | Controller            | t <sub>CR</sub> + 3<br>and t <sub>CF</sub> + 3 |        | ns   |
|     |                          |   | Target                | 0  |        | ns   |
| D9  | t <sub>SU_PP</sub>       | SDA Signal Data Setup In Push-Pull Mode                               | Controller,<br>Target | 3  |        | ns   |
| D10 | t <sub>CASr</sub>        | Clock After Repeated START (Sr)                                       | Controller            | t <sub>CAS MIN</sub>                           |        | ns   |
| D11 | t <sub>CBSr</sub>        | Clock Before Repeated START (Sr)                                      | Controller            | t <sub>CAS MIN</sub> / 2                       |        | ns   |

1.  $f_{SCL} = 1 / (t_{DIG\_L} + t_{DIG\_H})$
2. t<sub>DIG\_L</sub> and t<sub>DIG\_H</sub> are the clock Low and High periods as seen at the receiver end of the I3C Bus using V<sub>IL</sub> and V<sub>IH</sub>.
3. When communicating with an I3C Device on a mixed Bus, the t<sub>DIG\_H\_MIXED</sub> period must be constrained to make sure that I2C Devices do not interpret I3C signaling as valid I2C signaling.
4. As both edges are used, the hold time needs to be satisfied for the respective edges; t<sub>CF</sub> + 3 for falling edge clocks, and t<sub>CR</sub> + 3 for rising edge clocks.
5. Clock Frequency Minimum 0.01 MHz, Maximum 12.5 MHz



**Figure 6-78. I3C Push-Pull Timing (SDR and HDR-DDR Modes)**

### 6.10.5.13 MCAN

Table 6-48 and Table 6-49 presents timing conditions and switching characteristics for MCAN.

For more details about features and additional description information on the device Controller Area Network Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

#### Note

The device has multiple MCAN modules. MCANn is a generic prefix applied to MCAN signal names, where n represents the specific MCAN module.

**Table 6-48. MCAN Timing Conditions**

| PARAMETER                |                         | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>INPUT CONDITIONS</b>  |                         |     |     |      |
| SR <sub>i</sub>          | Input slew rate         | 2   | 15  | V/ns |
| <b>OUTPUT CONDITIONS</b> |                         |     |     |      |
| C <sub>L</sub>           | Output load capacitance | 5   | 20  | pF   |

**Table 6-49. MCAN Switching Characteristics**

| NO.   | PARAMETER               | DESCRIPTION                                     | MIN | MAX | UNIT |
|-------|-------------------------|---|-----|-----|------|
| MCAN1 | t <sub>d(MCAN_TX)</sub> | Delay time, transmit shift register to MCANn_TX |     | 10  | ns   |
| MCAN2 | t <sub>d(MCAN_RX)</sub> | Delay time, MCANn_RX to receive shift register  |     | 10  | ns   |

For more information, see *Controller Area Network (MCAN)* section in *Peripherals* chapter in the device TRM.

### 6.10.5.14 MCASP

For more details about features and additional description information on the device Multichannel Audio Serial Port, see the corresponding sections within Section 5.3, *Signal Descriptions* and Section 7, *Detailed Description*.

Section 6.10.5.14.1 and Figure 6-79 present timing requirements for MCASP0 to MCASP11.

**Table 6-50. MCASP Timing Conditions**

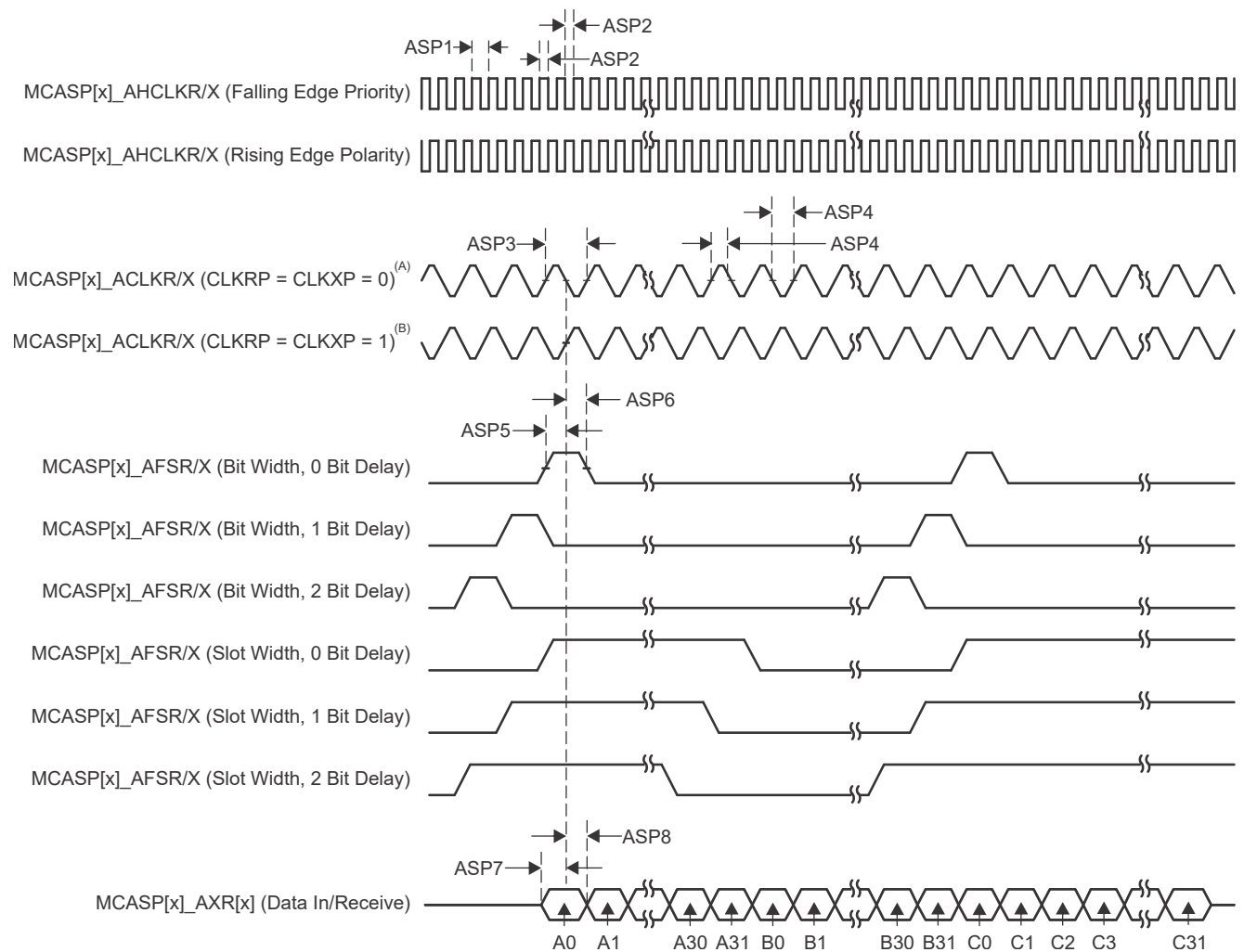
| PARAMETER                            | DESCRIPTION                            | MIN | MAX  | UNIT |
|--------------------------------------|--|-----|------|------|
| <b>Input Conditions</b>              |  |     |      |      |
| SR <sub>i</sub>                      | Input slew rate                        | 0.7 | 5    | V/ns |
| <b>Output Conditions</b>             |  |     |      |      |
| C <sub>L</sub>                       | Output load capacitance                | 1   | 10   | pF   |
| <b>PCB Connectivity Requirements</b> |  |     |      |      |
| t <sub>d(Trace Delay)</sub>          | Propagation delay of each trace        | 100 | 1100 | ps   |
| t <sub>d(Trace Mismatch Delay)</sub> | Propagation mismatch across all traces |     | 100  | ps   |

#### 6.10.5.14.1 Timing Requirements for MCASP

| NO.1 | PARAMETER                     | DESCRIPTION                                   | MODE               | MIN                       | MAX | UNIT |
|------|-------------------------------|---|--------------------|---------------------------|-----|------|
| ASP1 | t <sub>c(AHCLKRX)</sub>       | Cycle time, AHCLKR/X                          |                    | 15.26                     |     | ns   |
| ASP2 | t <sub>w(AHCLKRX)</sub>       | Pulse duration, AHCLKR/X high or low          |                    | -1.53 + 0.5P <sub>2</sub> |     | ns   |
| ASP3 | t <sub>c(ACLKRX)</sub>        | Cycle time, ACLKR/X                           |                    | 15.26                     |     | ns   |
| ASP4 | t <sub>w(ACLKRX)</sub>        | Pulse duration, ACLKR/X high or low           |                    | -1.53 + 0.5R <sub>3</sub> |     | ns   |
| ASP5 | t <sub>su(AFSRX-ACLKRX)</sub> | Setup time, AFSR/X input valid before ACLKR/X | ACLKR/X int        | 12.3                      |     | ns   |
|      |                               |   | ACLKR/X ext in/out | 4                         |     |      |

| NO.1 | PARAMETER             | DESCRIPTION                                 | MODE               | MIN  | MAX | UNIT |
|------|-----------------------|---|--------------------|------|-----|------|
| ASP6 | $t_{h(ACLKRX-AFSRX)}$ | Hold time, AFSR/X input valid after ACLKR/X | ACLKR/X int        | -1   |     | ns   |
|      |                       |   | ACLKR/X ext in/out | 1.6  |     |      |
| ASP7 | $t_{su(AXR-ACLKRX)}$  | Setup time, AXR input valid before ACLKR/X  | ACLKR/X int        | 12.3 |     | ns   |
|      |                       |   | ACLKR/X ext in/out | 4    |     |      |
| ASP8 | $t_{h(ACLKRX-AXR)}$   | Hold time, AXR input valid after ACLKR/X    | ACLKR/X int        | -1   |     | ns   |
|      |                       |   | ACLKR/X ext in/out | 1.6  |     |      |

1. ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1  
 ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0  
 ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1  
 ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1  
 ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0  
 ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1
2. P = AHCLKR/X period in ns.
3. R = ACLKR/X period in ns.



- A. For CLKRP = CLKXP = 0, the MCASP transmitter is configured for rising edge (to shift data out) and the MCASP receiver is configured for falling edge (to shift data in).

- B. For CLKRP = CLKXP = 1, the MCASP transmitter is configured for falling edge (to shift data out) and the MCASP receiver is configured for rising edge (to shift data in).

**Figure 6-79. MCASP Input Timing**

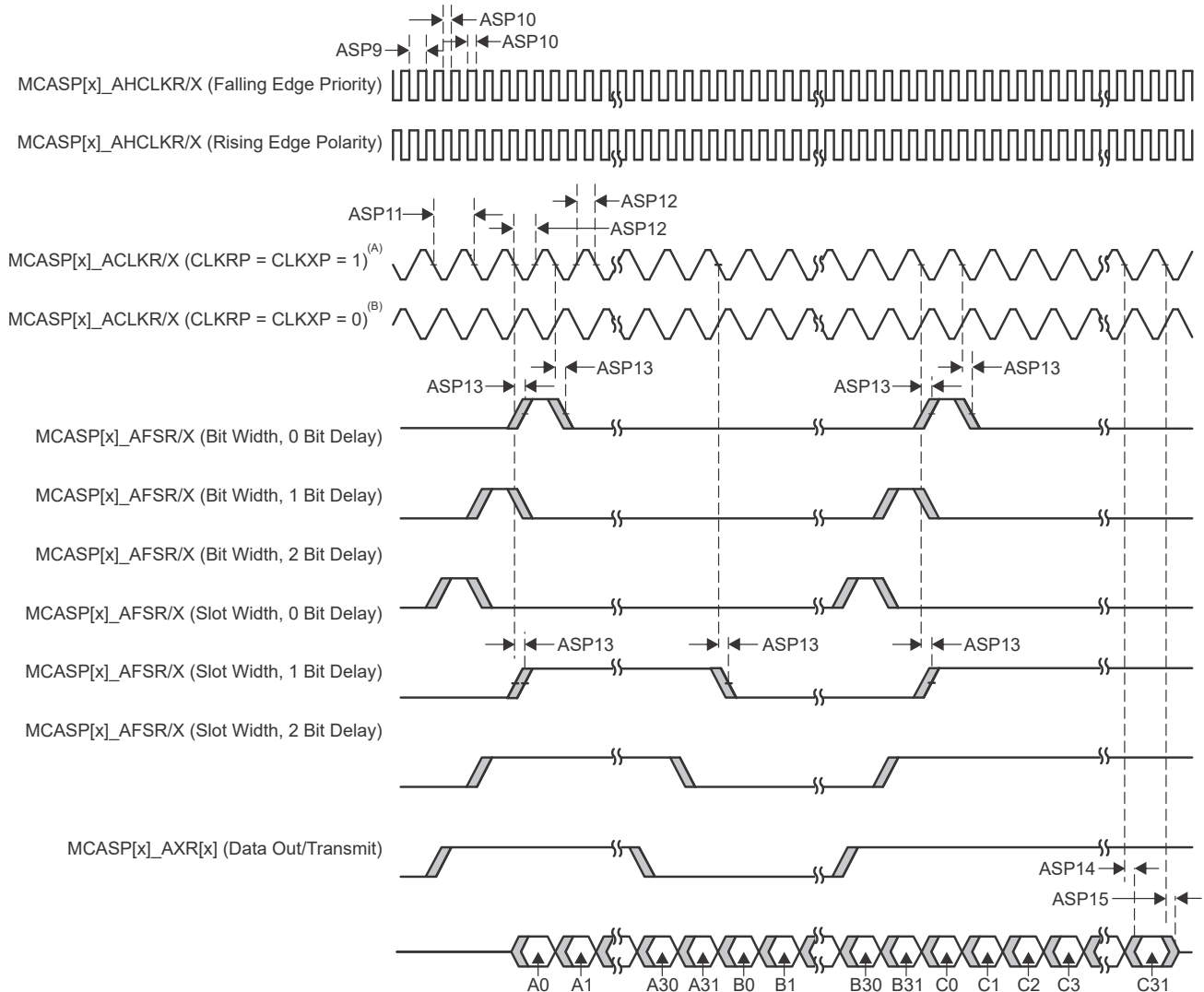
1. x in MCASP[x]\_\* is 0, 1 or 2

Table 6-51 and Figure 6-80 present switching characteristics over recommended operating conditions for MCASP0 to MCASP11.

**Table 6-51. Switching Characteristics Over Recommended Operating Conditions for MCASP**

| NO.1  | PARAMETER             | DESCRIPTION  | MODE               | MIN                    | MAX   | UNIT |
|-------|-----------------------|--|--------------------|------------------------|-------|------|
| ASP9  | $t_{c(AHCLKRX)}$      | Cycle time, AHCLKR/X   |                    | 20                     |       | ns   |
| ASP10 | $t_{w(AHCLKRX)}$      | Pulse duration, AHCLKR/X high or low                           |                    | -2 + 0.5P <sup>2</sup> |       | ns   |
| ASP11 | $t_{c(ACLKRX)}$       | Cycle time, ACLKR/X  |                    | 20                     |       | ns   |
| ASP12 | $t_{w(ACLKRX)}$       | Pulse duration, ACLKR/X high or low                            |                    | -2 + 0.5R <sup>3</sup> |       | ns   |
| ASP13 | $t_{d(ACLKRX-AFSRX)}$ | Delay time, ACLKR/X transmit edge to AFSR/X output valid       | ACLKR/X int        | 0                      | 7.25  | ns   |
|       |                       |  | ACLKR/X ext in/out | -15.28                 | 12.84 |      |
| ASP14 | $t_{d(ACLKX-AXR)}$    | Delay time, ACLKX transmit edge to AXR output valid            | ACLKR/X int        | 0                      | 7.25  | ns   |
|       |                       |  | ACLKR/X ext in/out | -15.28                 | 12.84 |      |
| ASP15 | $t_{dis(ACLKX-AXR)}$  | Disable time, ACLKX transmit edge to AXR output high impedance | ACLKR/X int        | 0                      | 7.25  | ns   |
|       |                       |  | ACLKR/X ext in/out | -14.9                  | 14    |      |

1. ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1  
 ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0  
 ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1  
 ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1  
 ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0  
 ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1
2. P = AHCLKR/X period in ns.
3. R = ACLKR/X period in ns.



- A. For CLKRP = CLKXP = 1, the MCASP transmitter is configured for falling edge (to shift data out) and the MCASP receiver is configured for rising edge (to shift data in).
- B. For CLKRP = CLKXP = 0, the MCASP transmitter is configured for rising edge (to shift data out) and the MCASP receiver is configured for falling edge (to shift data in).

**Figure 6-80. MCASP Output Timing**

1. x in MCASP[x]\_\* is 0, 1 or 2

For more information, see *Multichannel Audio Serial Port (MCASP)* section in *Peripherals* chapter in the device TRM.

### 6.10.5.15 MCSPI

For more details about features and additional description information on the device Serial Port Interface, see the corresponding sections within [Section 5.3, Signal Descriptions](#) and [Section 7, Detailed Description](#).

For more information, see *Multichannel Serial Peripheral Interface (MCSPI)* section in *Peripherals* chapter in the device TRM.

[Table 6-52](#) represents MCSPI timing conditions.

**Table 6-52. MCSPI Timing Conditions**

| PARAMETER                |                         | MIN       | MAX | UNIT |
|--------------------------|-------------------------|-----------|-----|------|
| <b>Input Conditions</b>  |                         |           |     |      |
| SR <sub>i</sub>          | Input slew rate         | 2         | 8.5 | V/ns |
| <b>Output Conditions</b> |                         |           |     |      |
| C <sub>L</sub>           | Output load capacitance | CLK       | 24  | pF   |
|                          |                         | D[x], CSi | 12  | pF   |

**6.10.5.15.1 MCSPI — Controller Mode**

Table 6-53, Figure 6-81, Table 6-54, and Figure 6-82 present timing requirements and switching characteristics for MCSPI – Controller Mode.

**Table 6-53. MCSPI Timing Requirements - Controller Mode**

see Figure 6-81

| PARAMETER |   | MIN | MAX | UNIT |
|-----------|---|-----|-----|------|
| SM4       | t <sub>su(misoV-spicklV)</sub><br>Setup time, SPI_D[x] valid before SPI_CLK active edge | 2.9 |     | ns   |
| SM5       | t <sub>h(spicklV-misoV)</sub><br>Hold time, SPI_D[x] valid after SPI_CLK active edge    | 2   |     | ns   |

**Table 6-54. MCSPI Switching Characteristics - Controller Mode**

see Figure 6-82

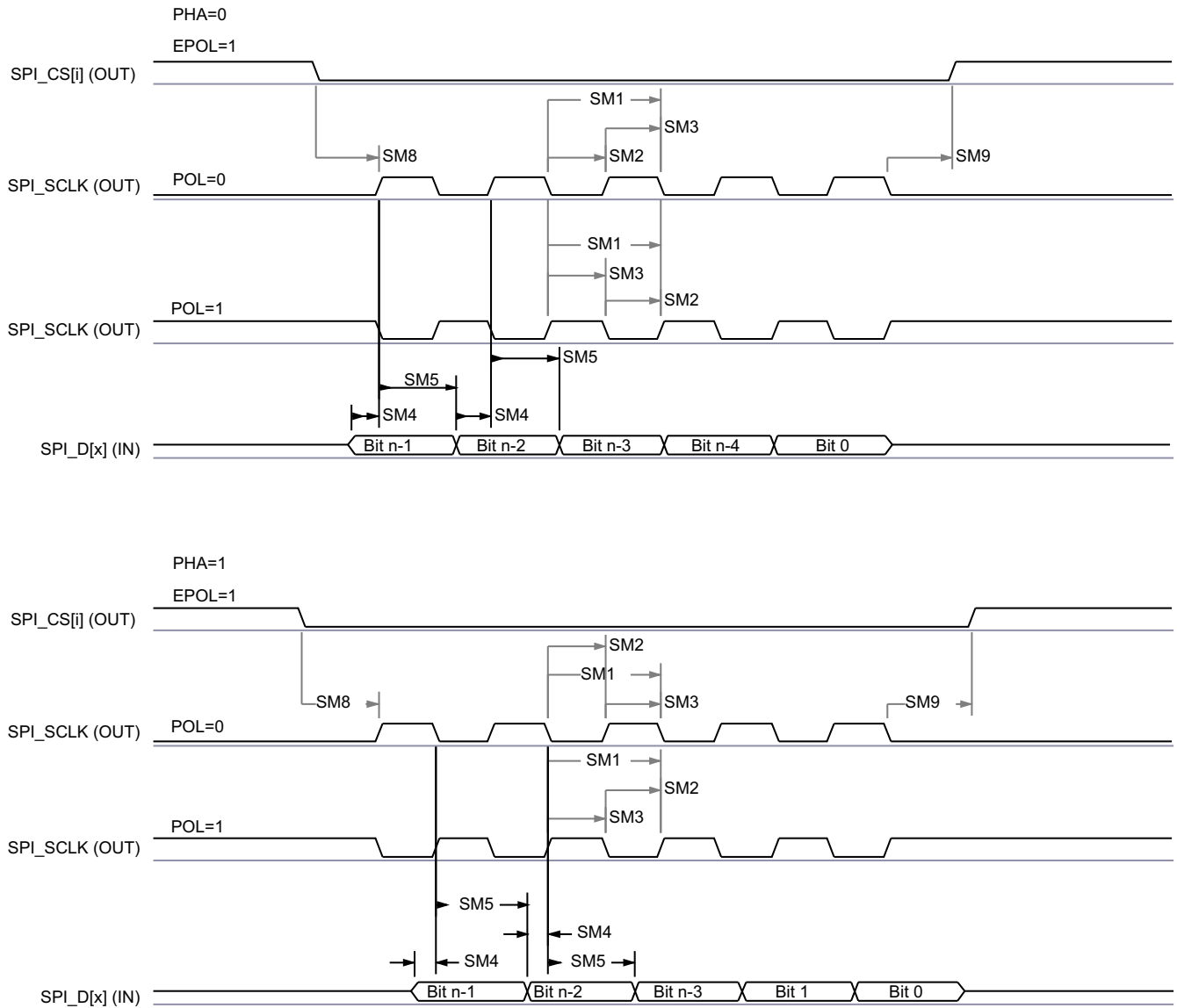
| PARAMETER |   | MODE                   | MIN                     | MAX | UNIT |
|-----------|---|------------------------|-------------------------|-----|------|
| SM1       | t <sub>c(spickl)</sub><br>Cycle time, SPI_CLK   |                        | 20                      |     | ns   |
| SM2       | t <sub>w(spicklL)</sub><br>Pulse duration, SPI_CLK low                                  |                        | 0.5P - 1 <sup>(1)</sup> |     | ns   |
| SM3       | t <sub>w(spicklH)</sub><br>Pulse duration, SPI_CLK high                                 |                        | 0.5P - 1 <sup>(1)</sup> |     | ns   |
| SM6       | t <sub>d(spicklV-simoV)</sub><br>Delay time, SPI_CLK active edge to SPI_D[x] transition |                        | -2                      | 2   | ns   |
| SM7       | t <sub>d(csV-simoV)</sub><br>Delay time, SPI_CSi active edge to SPI_D[x] transition     |                        | 5                       |     | ns   |
| SM8       | t <sub>d(csV-spickl)</sub><br>Delay time, SPI_CSi active to SPI_CLK first edge          | PHA = 0 <sup>(2)</sup> | B - 4 <sup>(3)</sup>    |     | ns   |
|           |   | PHA = 1 <sup>(2)</sup> | A - 4 <sup>(4)</sup>    |     | ns   |
| SM9       | t <sub>d(spicklV-csV)</sub><br>Delay time, SPI_CLK last edge to SPI_CSi inactive        | PHA = 0 <sup>(2)</sup> | A - 4 <sup>(4)</sup>    |     | ns   |
|           |   | PHA = 1 <sup>(2)</sup> | B - 4 <sup>(3)</sup>    |     | ns   |

(1) P = SPI\_CLK period in ns

(2) SPI\_CLK phase is programmable with the PHA bit of the MCSPI\_CHCONF\_0/1/2/3 register

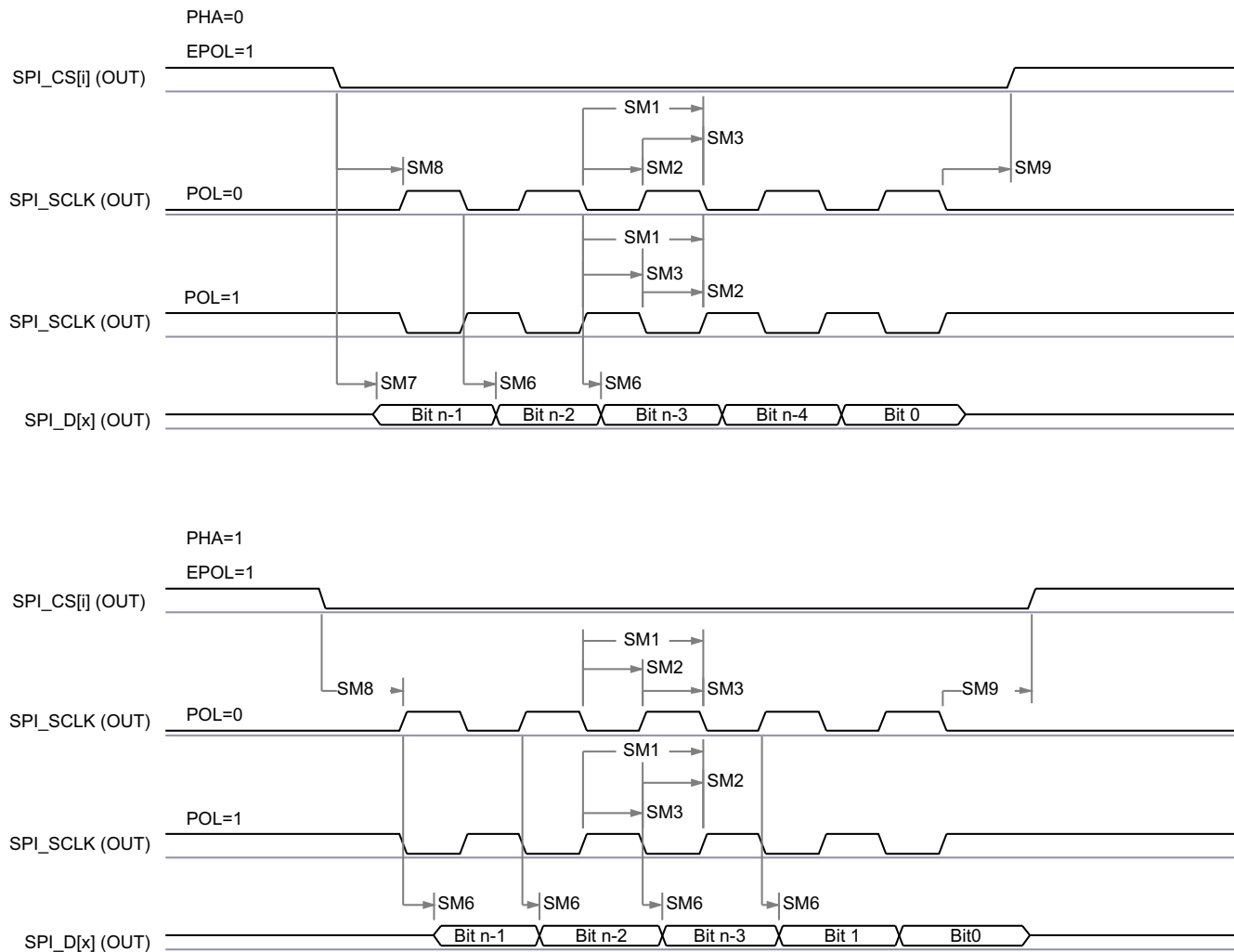
(3) B = (TCS + .5) \* TSPICKLREF, where TCSns a bit field of the MCSPI\_CHCONF\_0/1/2/3 register and Fratio = Even >= 2.

(4) When P = 20 ns, A = (TCS + 1) \* TSPICKLREF, where TCSns a bit field of the MCSPI\_CHCONF\_0/1/2/3 register.  
When P > 20 ns, A = (TCS + 0.5) \* Fratio \* TSPICKLREF, where TCSns a bit field of the MCSPI\_CHCONF\_0/1/2/3 register.



SPRSP08\_TIMING\_McSPI\_02

**Figure 6-81. SPI Controller Mode Receive Timing**



SPRSP08\_TIMING\_McSPI\_01

**Figure 6-82. MCSPI Controller Mode Transmit Timing**

### 6.10.5.15.2 MCSPI — Peripheral Mode

Table 6-55, Figure 6-83, Table 6-56, and Figure 6-84 present timing requirements and switching characteristics for MCSPI – Peripheral Mode.

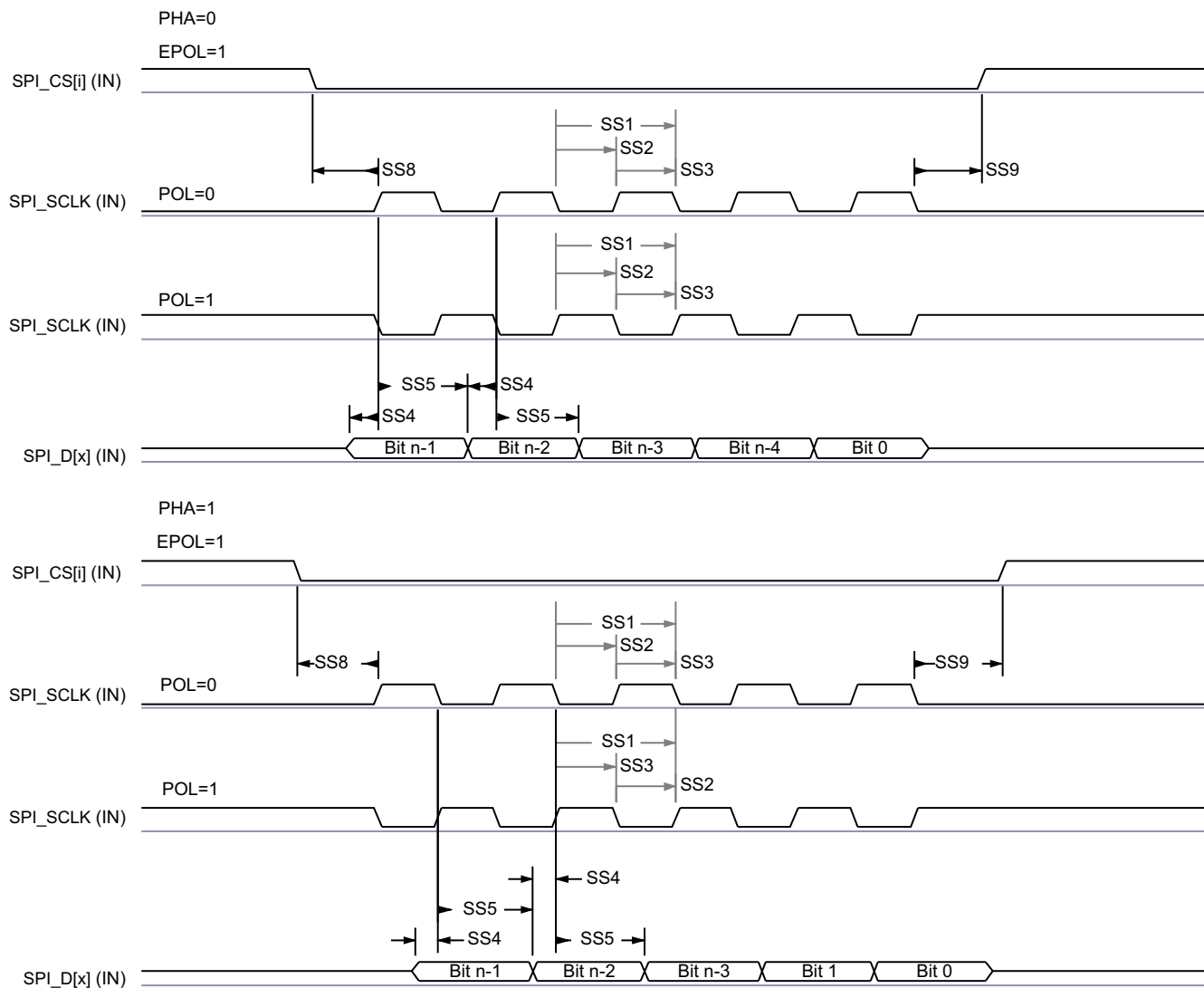
**Table 6-55. MCSPI Timing Requirements - Peripheral Mode**

| PARAMETER |                        |   | MIN                  | MAX | UNIT |
|-----------|------------------------|---|----------------------|-----|------|
| SS1       | $t_{c(spclk)}$         | Cycle time, SPI_CLK                                   | 20                   |     | ns   |
| SS2       | $t_{w(spclkL)}$        | Pulse duration, SPI_CLK low                           | 0.45P <sup>(1)</sup> |     | ns   |
| SS3       | $t_{w(spclkH)}$        | Pulse duration, SPI_CLK high                          | 0.45P <sup>(1)</sup> |     | ns   |
| SS4       | $t_{su(simoV-spclkV)}$ | Setup time, SPI_D[x] valid before SPI_CLK active edge | 5                    |     | ns   |
| SS5       | $t_{h(spclkV-simoV)}$  | Hold time, SPI_D[x] valid after SPI_CLK active edge   | 5                    |     | ns   |
| SS8       | $t_{su(csV-spclkV)}$   | Setup time, SPI_CSi valid before SPI_CLK first edge   | 5                    |     | ns   |
| SS9       | $t_{h(spclkV-csV)}$    | Hold time, SPI_CSi valid after SPI_CLK last edge      | 5                    |     | ns   |

**Table 6-56. MCSPI Switching Characteristics - Peripheral Mode**

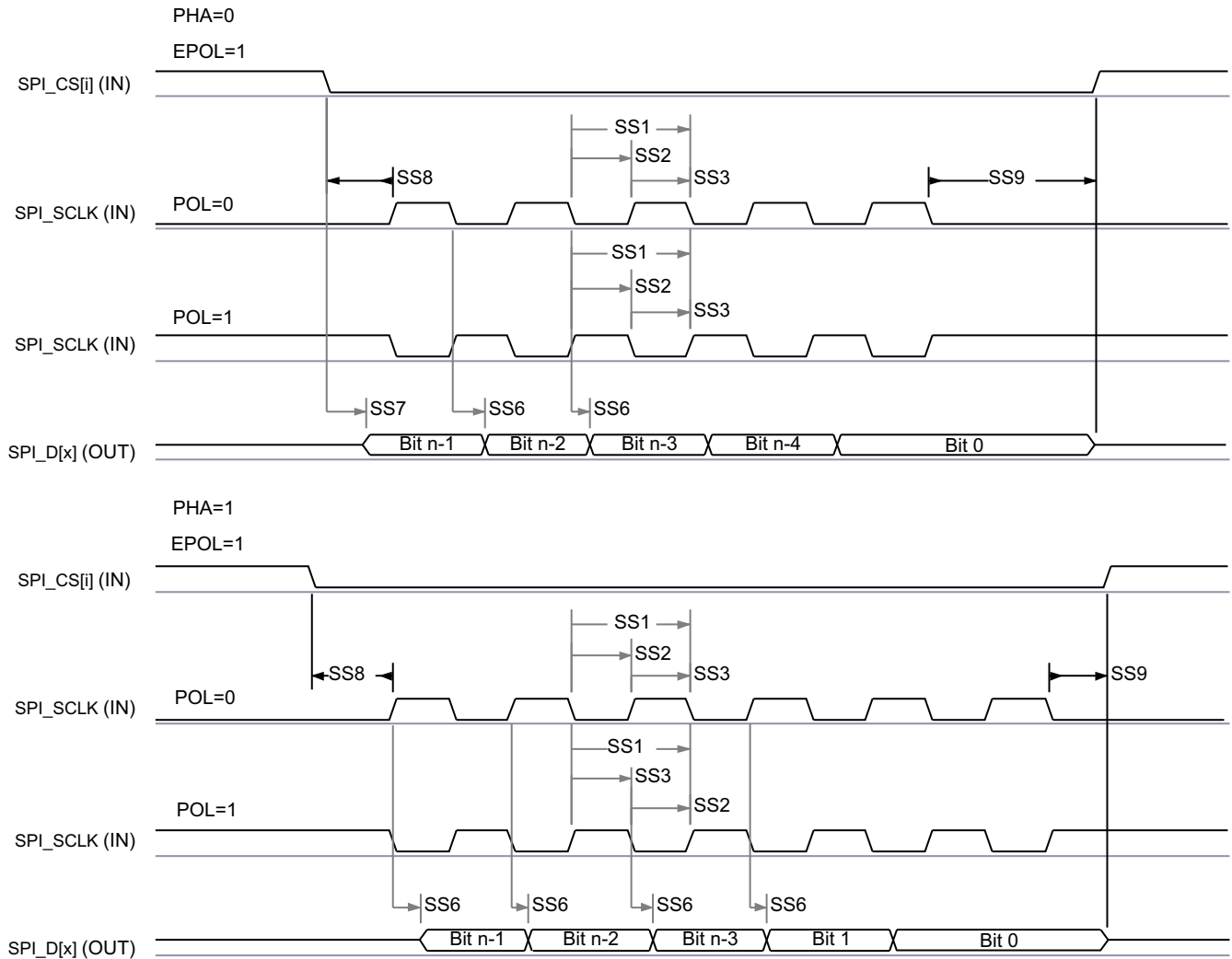
| PARAMETER |                       |  | MIN   | MAX   | UNIT |
|-----------|-----------------------|--|-------|-------|------|
| SS6       | $t_{d(spclkV-somiV)}$ | Delay time, SPI_CLK active edge to SPI_D[x] transition | 2     | 17.12 | ns   |
| SS7       | $t_{sk(csV-somiV)}$   | Delay time, SPI_CSi active edge to SPI_D[x] transition | 20.95 |       | ns   |

(1) P = SPI\_CLK period in ns.



SPRSP08\_TIMING\_McSPI\_04

**Figure 6-83. SPI Peripheral Mode Receive Timing**



SPRSP08\_TIMING\_McSPI\_03

**Figure 6-84. MCSPI Peripheral Mode Transmit Timing**

For more information, see *Multichannel Serial Peripheral Interface (MCSPi)* section in *Peripherals* chapter in the device TRM.

#### 6.10.5.16 eMMC/SD/SDIO

The MMCSD Host Controller provides an interface to eMMC 5.1 (embedded MultiMedia Card), SD 4.10 (Secure Digital), and SDIO 4.0 (Secure Digital IO) devices. The MMCSD Host Controller deals with MMC/SD/SDIO protocol at transmission level, data packing, adding cyclic redundancy checks (CRCs), start/end bit insertion, and checking for syntactical correctness.

For more details about features and additional description information on the device Multi Media Card, see the corresponding sections within [Section 5.3, Signal Descriptions](#) and [Section 7, Detailed Description](#).

#### Note

MMC modes require software configuration of the delay settings, as shown in [Table 6-57](#) and [Table 6-68](#).

Tuning algorithm should be implemented to meet input setup/hold time requirements for SDR50, DDR50 (only on MMCSD1), SDR104, HS200 and HS400 modes.

### 6.10.5.16.1 MMCSD0 - eMMC Interface

MMCSD0 interface is compliant with the JEDEC eMMC electrical standard v5.1 (JESD84-B51) and it supports the following eMMC applications:

- Default speed
- High speed SDR
- High speed DDR
- High speed HS200
- High speed HS400

Table 6-57 presents the required DLL software configuration settings for MMC0 timing modes.

**Table 6-57. MMC0 DLL Delay Mapping for All Timing Modes**

| REGISTER NAME        |  | MMCSD0_SS_PHY_CTRL_x_REG |                 |                           |                          |                          |                         |                                 |                      |                             |
|----------------------|--|--------------------------|-----------------|---------------------------|--------------------------|--------------------------|-------------------------|---------------------------------|----------------------|-----------------------------|
|                      |  | x=1                      | x=4             |                           |                          |                          | x=5                     |                                 |                      |                             |
| BIT FIELD            |  | [1]                      | [31:24]         | [20]                      | [15:12]                  | [8]                      | [4:0]                   | [17:16]                         | [10:8]               | [2:0]                       |
| BIT FIELD NAME       |  | ENDLL                    | STRBSEL         | OTAPDLYENA                | OTAPDLYSEL               | ITAPDLYENA               | ITAPDLYSEL              | SELDLYTXCLK<br>SELDLYRXCLK      | FRQSEL               | CLKBUFSEL                   |
| MODE                 | DESCRIPTION                              | ENABLE<br>DLL            | STROBE<br>DELAY | OUTPUT<br>DELAY<br>ENABLE | OUTPUT<br>DELAY<br>VALUE | INPUT<br>DELAY<br>ENABLE | INPUT<br>DELAY<br>VALUE | DLL/<br>DELAY CHAIN<br>SELECT   | DLL REF<br>FREQUENCY | DELAY<br>BUFFER<br>DURATION |
| Legacy<br>SDR        | 8-bit PHY<br>operating 1.8 V, 25<br>MHz  | 0x0                      | 0x0             | 0x0                       | NA <sup>(1)</sup>        | 0x1                      | 0x10                    | 0x1<br>or<br>0x3 <sup>(2)</sup> | NA <sup>(3)</sup>    | 0x7                         |
| High<br>Speed<br>SDR | 8-bit PHY<br>operating 1.8 V, 50<br>MHz  | 0x0                      | 0x0             | 0x0                       | NA <sup>(1)</sup>        | 0x1                      | 0xA                     | 0x1<br>or<br>0x3 <sup>(2)</sup> | NA <sup>(3)</sup>    | 0x7                         |
| High<br>Speed<br>DDR | 8-bit PHY<br>operating 1.8 V, 50<br>MHz  | 0x1                      | 0x0             | 0x1                       | 0x6                      | 0x1                      | Tuning <sup>(4)</sup>   | 0x0                             | 0x4                  | 0x7                         |
| HS200                | 8-bit PHY<br>operating 1.8 V,<br>200 MHz | 0x1                      | 0x0             | 0x1                       | 0x8                      | 0x1                      | Tuning <sup>(4)</sup>   | 0x0                             | 0x0                  | 0x7                         |
| HS400                | 8-bit PHY<br>operating 1.8 V,<br>200 MHz | 0x1                      | 0x77            | 0x1                       | 0x5                      | 0x1                      | Tuning <sup>(4)</sup>   | 0x0                             | 0x0                  | 0x7                         |

(1) NA means this register field has no function when operating with half-cycle timing, which is required for this mode.

(2) The SELDLYTXCLK bit has no function when operating with half-cycle timing, which is required for this mode.

(3) NA means this register field has no function when ENDLL is set to 0x0.

(4) Tuning means this mode requires a tuning algorithm to be used to determine optimal input timing

Table 6-58 represents MMCSD0 timing conditions.

**Table 6-58. MMCSD0 Timing Conditions**

| PARAMETER                            |                                 | MIN                                  | MAX  | UNIT |      |
|--------------------------------------|---------------------------------|--------------------------------------|------|------|------|
| <b>INPUT CONDITIONS</b>              |                                 |                                      |      |      |      |
| SR <sub>i</sub>                      | Input slew rate                 | Legacy SDR                           | 0.05 | 1.24 | V/ns |
|                                      |                                 | High Speed SDR                       | 0.3  | 1.65 | V/ns |
|                                      |                                 | High Speed DDR (CMD) [DDR52]         | 0.3  | 1.65 | V/ns |
|                                      |                                 | High Speed DDR (DAT[7:0])<br>[DDR52] | 0.3  | 1.65 | V/ns |
| <b>OUTPUT CONDITIONS</b>             |                                 |                                      |      |      |      |
| C <sub>L</sub>                       | Output load capacitance         | Legacy SDR                           | 1    | 18   | pF   |
|                                      |                                 | High Speed SDR                       | 1    | 18   | pF   |
|                                      |                                 | High Speed DDR                       | 1    | 18   | pF   |
|                                      |                                 | HS200                                | 1    | 12   | pF   |
|                                      |                                 | HS400                                | 1    | 6    | pF   |
| <b>PCB CONNECTIVITY REQUIREMENTS</b> |                                 |                                      |      |      |      |
| t <sub>d</sub> (Trace Delay)         | Propagation delay of each trace | All modes                            | 134  | 756  | ps   |

**Table 6-58. MMCSD0 Timing Conditions (continued)**

| PARAMETER                             |  | MIN                          | MAX | UNIT |
|---------------------------------------|--|------------------------------|-----|------|
| t <sub>d</sub> (Trace Mismatch Delay) | Propagation delay mismatch across all traces | Legacy SDR, High Speed SDR   | 100 | ps   |
|                                       |  | High Speed DDR, HS200, HS400 | 8   | ps   |

6.10.5.16.1.1 Legacy SDR Mode

Table 6-59 and Table 6-60 present Timing requirements and Switching characteristics in MMCSD0 - Legacy SDR Mode (see Figure 6-85 and Figure 6-86).

Table 6-59. MMCSD0 Timing Requirements - Legacy SDR Mode

| NO.   | PARAMETER           | DESCRIPTION   | MIN | MAX | UNIT |
|-------|---------------------|---|-----|-----|------|
| LSDR1 | $t_{su(cmdV-clkH)}$ | Setup time, MMC0_CMD valid before MMC0_CLK rising edge      | 2.5 |     | ns   |
| LSDR2 | $t_h(clkH-cmdV)$    | Hold time, MMC0_CMD valid after MMC0_CLK rising edge        | 6.5 |     | ns   |
| LSDR3 | $t_{su(dV-clkH)}$   | Setup time, MMC0_DAT[7:0] valid before MMC0_CLK rising edge | 2.5 |     | ns   |
| LSDR4 | $t_h(clkH-dV)$      | Hold time, MMC0_DAT[7:0] valid after MMC0_CLK rising edge   | 6.5 |     | ns   |

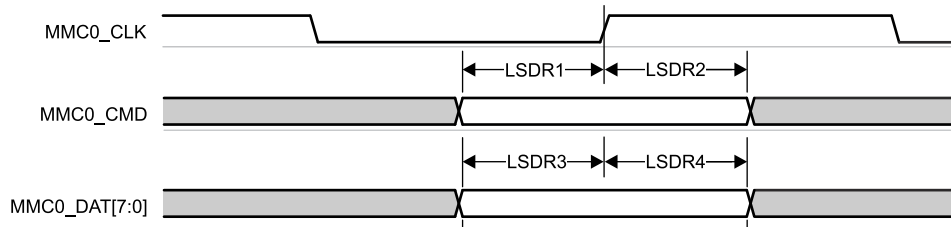


Figure 6-85. MMCSD0 - Legacy SDR - Receive Mode

Table 6-60. MMCSD0 Switching Characteristics - Legacy SDR Mode

| NO.   | PARAMETER        | DESCRIPTION   | MIN  | MAX | UNIT |
|-------|------------------|---|------|-----|------|
|       | $f_{op(clk)}$    | Operating frequency, MMC0_CLK                                 |      | 25  | MHz  |
| LSDR5 | $t_c(clk)$       | Cycle time, MMC0_CLK  | 40   |     | ns   |
| LSDR6 | $t_w(clkH)$      | Pulse duration, MMC0_CLK high                                 | 18.7 |     | ns   |
| LSDR7 | $t_w(clkL)$      | Pulse duration, MMC0_CLK low                                  | 18.7 |     | ns   |
| LSDR8 | $t_d(clkL-cmdV)$ | Delay time, MMC0_CLK falling edge to MMC0_CMD transition      | -3.2 | 3.8 | ns   |
| LSDR9 | $t_d(clkL-dV)$   | Delay time, MMC0_CLK falling edge to MMC0_DAT[7:0] transition | -3.2 | 3.8 | ns   |

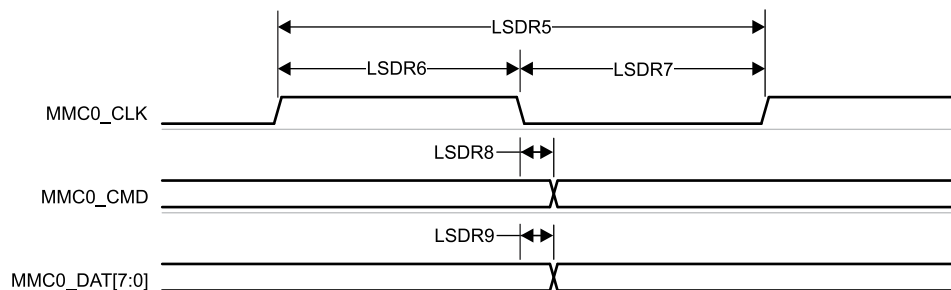


Figure 6-86. MMC0 - Legacy SDR - Transmit Mode

6.10.5.16.1.2 High Speed SDR Mode

Table 6-61 and Table 6-62 present Timing requirements and Switching characteristics for MMCSD0 – High Speed SDR Mode (see Figure 6-87 and Figure 6-88).

Table 6-61. MMCSD0 Timing Requirements - High Speed SDR Mode

| NO.    | PARAMETER           | DESCRIPTION   | MIN  | MAX | UNIT |
|--------|---------------------|---|------|-----|------|
| HSSDR1 | $t_{su(cmdV-clkH)}$ | Setup time, MMC0_CMD valid before MMC0_CLK rising edge      | 2.99 |     | ns   |
| HSSDR2 | $t_h(clkH-cmdV)$    | Hold time, MMC0_CMD valid after MMC0_CLK rising edge        | 2.67 |     | ns   |
| HSSDR3 | $t_{su(dV-clkH)}$   | Setup time, MMC0_DAT[7:0] valid before MMC0_CLK rising edge | 2.99 |     | ns   |
| HSSDR4 | $t_h(clkH-dV)$      | Hold time, MMC0_DAT[7:0] valid after MMC0_CLK rising edge   | 2.67 |     | ns   |

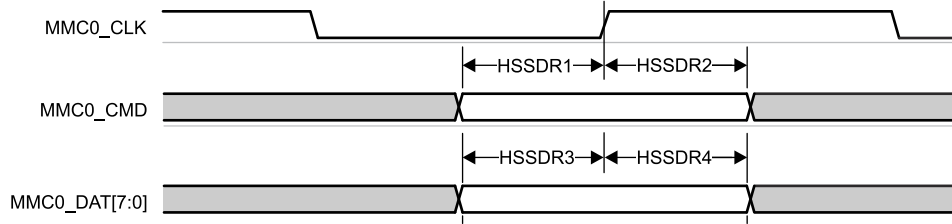


Figure 6-87. MMCSD0 – High Speed SDR Mode – Receive Mode

Table 6-62. MMCSD0 Switching Characteristics - High Speed SDR Mode

| NO.    | PARAMETER          | DESCRIPTION   | MIN  | MAX | UNIT |
|--------|--------------------|---|------|-----|------|
|        | $f_{op}(clk)$      | Operating frequency, MMC0_CLK                                 |      | 50  | MHz  |
| HSSDR5 | $t_{c}(clk)$       | Cycle time, MMC0_CLK  | 20   |     | ns   |
| HSSDR6 | $t_{w}(clkH)$      | Pulse duration, MMC0_CLK high                                 | 9.2  |     | ns   |
| HSSDR7 | $t_{w}(clkL)$      | Pulse duration, MMC0_CLK low                                  | 9.2  |     | ns   |
| HSSDR8 | $t_{d}(clkL-cmdV)$ | Delay time, MMC0_CLK falling edge to MMC0_CMD transition      | -3.2 | 3.8 | ns   |
| HSSDR9 | $t_{d}(clkL-dV)$   | Delay time, MMC0_CLK falling edge to MMC0_DAT[7:0] transition | -3.2 | 3.8 | ns   |

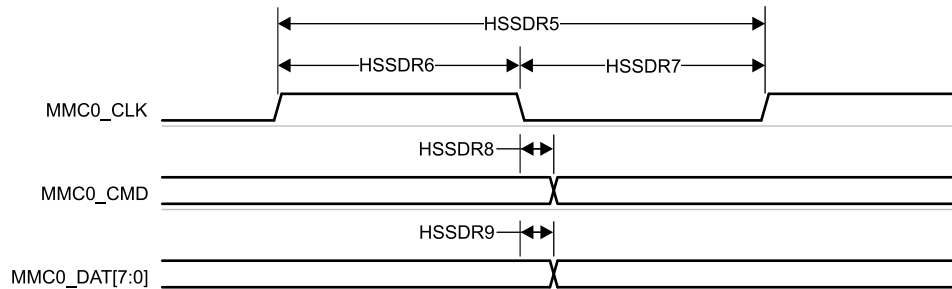


Figure 6-88. MMCSD0 – High Speed SDR Mode – Transmit Mode

#### 6.10.5.16.1.3 High Speed DDR Mode

Table 6-63 and Table 6-64 present Timing requirements and Switching characteristics for MMCSD0 – High Speed DDR Mode (see Figure 6-89 and Figure 6-90).

Table 6-63. MMCSD0 Timing Requirements - High Speed DDR Mode

| NO.    | PARAMETER           | DESCRIPTION  | MIN  | MAX | UNIT |
|--------|---------------------|--|------|-----|------|
| HSDDR1 | $t_{su}(cmdV-clkH)$ | Setup time, MMC0_CMD valid before MMC0_CLK rising edge     | 2.5  |     | ns   |
| HSDDR2 | $t_{h}(clkH-cmdV)$  | Hold time, MMC0_CMD valid after MMC0_CLK rising edge       | 2.67 |     | ns   |
| HSDDR3 | $t_{su}(dV-clkV)$   | Setup time, MMC0_DAT[7:0] valid before MMC0_CLK transition | 0.83 |     | ns   |
| HSDDR4 | $t_{h}(clkV-dV)$    | Hold time, MMC0_DAT[7:0] valid after MMC0_CLK transition   | 1.76 |     | ns   |

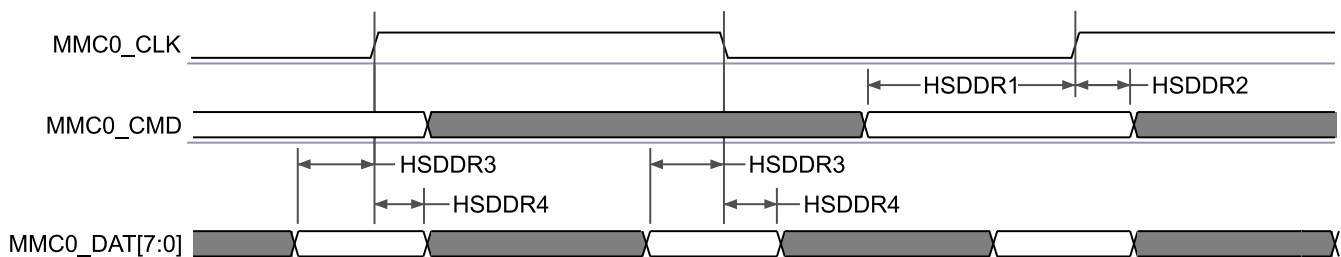
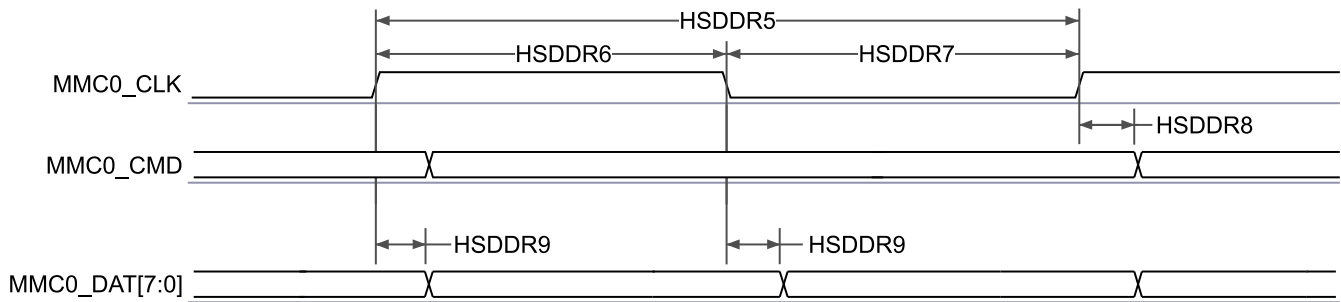


Figure 6-89. MMCSD0 – High Speed DDR Mode – Receive Mode

**Table 6-64. MMCSD0 Switching Characteristics - High Speed DDR Mode**

| NO.    | PARAMETER          | DESCRIPTION   | MIN  | MAX  | UNIT |
|--------|--------------------|---|------|------|------|
|        | $f_{op(clk)}$      | Operating frequency, MMC0_CLK                               |      | 50   | MHz  |
| HSDDR5 | $t_{c(clk)}$       | Cycle time, MMC0_CLK  | 20   |      | ns   |
| HSDDR6 | $t_{w(clkH)}$      | Pulse duration, MMC0_CLK high                               | 9.2  |      | ns   |
| HSDDR7 | $t_{w(clkL)}$      | Pulse duration, MMC0_CLK low                                | 9.2  |      | ns   |
| HSDDR8 | $t_{d(clkH-cmdV)}$ | Delay time, MMC0_CLK rising edge to MMC0_CMD transition     | 3.31 | 9.8  | ns   |
| HSDDR9 | $t_{d(clkV-dV)}$   | Delay time, MMC0_CLK transition to MMC0_DAT[7:0] transition | 2.81 | 6.94 | ns   |



**Figure 6-90. MMCSD0 – High Speed DDR Mode – Transmit Mode**

**6.10.5.16.1.4 HS200 Mode**

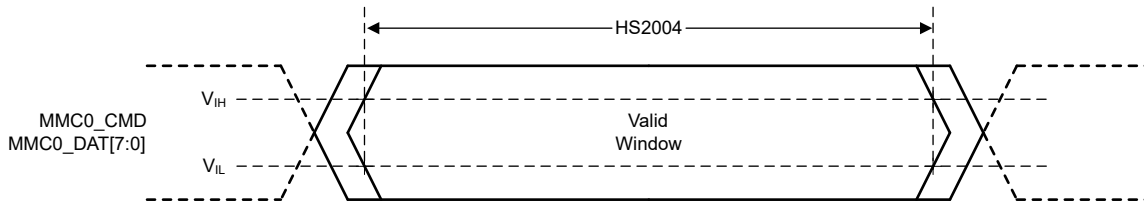
Table 6-65, Figure 6-91, Table 6-66 and Figure 6-92 present both timing requirements and switching characteristics for MMCSD0 – HS200 Mode.

**Table 6-65. MMCSD0 Timing Requirements – HS200 Mode**

see Figure 6-91

| NO.    |                  |   | MIN                | MAX | UNIT |
|--------|------------------|---|--------------------|-----|------|
| HS2004 | $t_{D\text{VW}}$ | Input data valid window, MMC0_CMD and MMC0_DAT[7:0] | 2.0 <sup>(1)</sup> |     | ns   |

- (1) This parameter defines the minimum data valid window required by the host, where any data valid window presented to the host greater than this value ensures the host is able to capture valid data. The value defined by this parameter is smaller than the smallest possible data valid window defined for any eMMC device operating in HS200 mode.

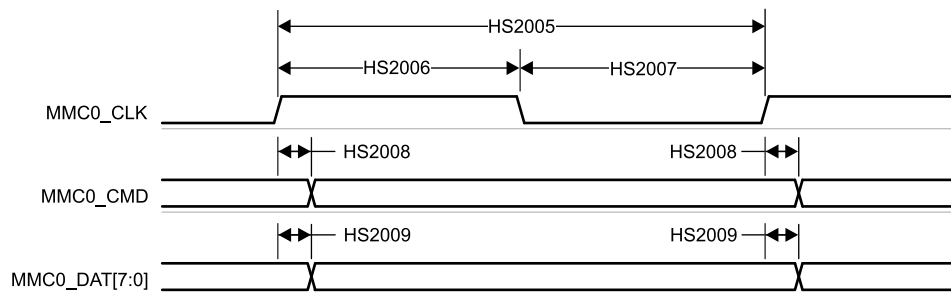


**Figure 6-91. MMCSD0 – HS200 – Receive Mode**

**Table 6-66. MMCSD0 Switching Characteristics – HS200 Mode**

see Figure 6-92

| NO.    | PARAMETER                 | MIN                           | MAX  | UNIT    |
|--------|---------------------------|-------------------------------|------|---------|
|        | $f_{op(\text{clk})}$      | Operating frequency, MMC0_CLK |      | 200 MHz |
| HS2005 | $t_{c(\text{clk})}$       | Cycle time, MMC0_CLK          |      | 5 ns    |
| HS2006 | $t_{w(\text{clkH})}$      | Pulse duration, MMC0_CLK high |      | 2.08 ns |
| HS2007 | $t_{w(\text{clkL})}$      | Pulse duration, MMC0_CLK low  |      | 2.08 ns |
| HS2008 | $t_{d(\text{clkL-cmdV})}$ | 0.99                          | 3.28 | ns      |
| HS2009 | $t_{d(\text{clkL-dV})}$   | 0.99                          | 3.28 | ns      |



**Figure 6-92. MMCSD0 – HS200 Mode – Transmit Mode**

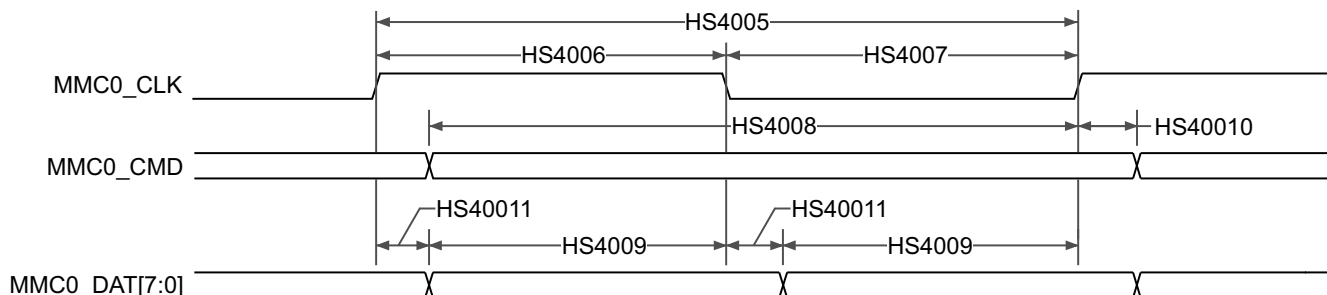
6.10.5.16.1.5 HS400 Mode

Table 6-67 presents Switching characteristics for MMCSD0 – HS400 Mode (see Figure 6-93).

**Table 6-67. MMCSD0 Switching Characteristics - HS400 Mode**

| NO.    | PARAMETER                        | DESCRIPTION   | MIN  | MAX | UNIT |
|--------|----------------------------------|---|------|-----|------|
|        | $f_{op}(clk)$                    | Operating frequency, MMC0_CLK   |      | 200 | MHz  |
| HS4005 | $t_{c}(clk)$                     | Operating period, MMC0_CLK  |      | 5   | ns   |
| HS4006 | $t_{w}(clkH)$                    | Pulse duration, MMC0_CLK high   | 2.23 |     | ns   |
| HS4007 | $t_{w}(clkL)$                    | Pulse duration, MMC0_CLK low  | 2.23 |     | ns   |
| HS4008 | $t_{osu}(cmdV-clkH)$             | Output setup time, MMC0_CMD valid to MMC0_CLK rising edge <sup>(1)</sup>                  | 2.54 |     | ns   |
| HS4009 | $t_{osu}(dV-clk) t_{d}(clkV-dV)$ | Output setup time, MMC0_DAT[7:0] valid to MMC0_CLK rising or falling edge <sup>(1)</sup>  | 0.63 |     | ns   |
| HS4010 | $t_{oh}(clkH-cmdIV)$             | Output hold time, MMC0_CLK rising edge to MMC0_CMD invalid <sup>(2)</sup>                 | 0.98 |     | ns   |
| HS4011 | $t_{oh}(clk-dIV)$                | Output hold time, MMC0_CLK rising or falling edge to MMC0_DAT[7:0] invalid <sup>(2)</sup> | 0.72 |     | ns   |

- (1) This parameter defines the output setup time provided to the attached device. This time is relative to the next capture clock edge. The timing references for this parameter are from mid-supply of the DAT or CMD signal transition to mid-supply of the CLK signal transition. The eMMC standard defines the setup timing references from VIL or VIH of the DAT or CMD signal transition to mid-supply of the CLK signal transition. Therefore, the system designer must consider the impact of the DAT signal slew rate when designing the PCB, and ensure the time it takes for the DAT signal to slew from mid-supply to VIL or VIH does not erode the setup time margin.
- (2) This parameter defines the output hold time provided to the attached device. This time is relative to the previous launch clock edge. The timing references for this parameter are from mid-supply of the CLK signal transition to mid-supply of the DAT or CMD signal transition. The eMMC standard defines the hold timing references from mid-supply of the CLK signal transition to VIL or VIH of the DAT or CMD signal transition. Therefore, the system designer must consider the impact of the DAT signal slew rate when designing the PCB, and ensure the time it takes for the DAT signal to slew from VIL or VIH to mid-supply does not erode the hold time margin.



**Figure 6-93. MMCSD0 – HS400 Mode – Transmit Mode**

6.10.5.16.2 MMCSDi — MMCS1 — SD/SDIO Interface

Note

The MMCSDi (i = 1) controller is also referred to as MMCi.

MMCSDi interface is compliant with the SD Host Controller Standard Specification 4.10 and SD Physical Layer Specification v3.01 as well as SDIO Specification v3.00 and it supports the following SD Card applications:

- Default speed
- High speed
- UHS-I SDR12
- UHS-I SDR25
- UHS-I SDR50
- UHS-I SDR104
- UHS-I DDR50

Table 6-68 presents the required delay software configuration settings for MMC1 timing modes.

Table 6-68. MMC1 Delay Mapping for All Timing Modes

| REGISTER NAME  |                                    | MMCS1_SS_PHY_CTRL_4_REG |                   |                    |                       |
|----------------|------------------------------------|-------------------------|-------------------|--------------------|-----------------------|
| BIT FIELD      |                                    | [20]                    | [15:12]           | [8]                | [4:0]                 |
| BIT FIELD NAME |                                    | OTAPDLYENA              | OTAPDLYSEL        | ITAPDLYENA         | ITAPDLYSEL            |
| MODE           | DESCRIPTION                        | DELAY ENABLE            | DELAY VALUE       | INPUT DELAY ENABLE | INPUT DELAY VALUE     |
| Default Speed  | 4-bit PHY operating 3.3 V, 25 MHz  | NA <sup>(1)</sup>       | NA <sup>(1)</sup> | 0x0                | 0x0                   |
| High Speed     | 4-bit PHY operating 3.3 V, 50 MHz  | NA <sup>(1)</sup>       | NA <sup>(1)</sup> | 0x0                | 0x0                   |
| UHS-I SDR12    | 4-bit PHY operating 1.8 V, 25 MHz  | 0x1                     | 0xF               | 0x0                | 0x0                   |
| UHS-I SDR25    | 4-bit PHY operating 1.8 V, 50 MHz  | 0x1                     | 0xF               | 0x0                | 0x0                   |
| UHS-I SDR50    | 4-bit PHY operating 1.8 V, 100 MHz | 0x1                     | 0xC               | 0x1                | Tuning <sup>(2)</sup> |
| UHS-I DDR50    | 4-bit PHY operating 1.8 V, 50 MHz  | 0x1                     | 0xC               | 0x1                | Tuning <sup>(2)</sup> |
| UHS-I SDR104   | 4-bit PHY operating 1.8, V 200 MHz | 0x1                     | 0x5               | 0x1                | Tuning <sup>(2)</sup> |

(1) NA means this register field has no function when operating with half-cycle timing, which is required for this mode.

(2) Tuning means this mode requires a tuning algorithm to be used to determine optimal input timing

Table 6-69 represents MMCS1 timing conditions.

Table 6-69. MMCS1 Timing Conditions

| PARAMETER                            | DESCRIPTION             | MODE                      | MIN  | MAX  | UNIT |
|--------------------------------------|-------------------------|---------------------------|------|------|------|
| <b>INPUT CONDITIONS</b>              |                         |                           |      |      |      |
| SR <sub>i</sub>                      | Input slew rate         | Default Speed, High Speed | 0.69 | 2.06 | V/ns |
|                                      |                         | UHS-I SDR12, UHS-I SDR25  | 0.34 | 1.34 | V/ns |
| <b>OUTPUT CONDITIONS</b>             |                         |                           |      |      |      |
| C <sub>L</sub>                       | Output load capacitance | All Speed Modes           | 1    | 10   | pF   |
| <b>PCB CONNECTIVITY REQUIREMENTS</b> |                         |                           |      |      |      |

**Table 6-69. MMCSD1 Timing Conditions (continued)**

| PARAMETER                    | DESCRIPTION                                  | MODE                      | MIN | MAX  | UNIT |
|------------------------------|--|---------------------------|-----|------|------|
| $t_d$ (Trace Delay)          | Propagation delay of each trace              | Default Speed, High Speed | 126 | 1200 | ps   |
|                              |  | UHS-I DDR50               | 255 | 1134 | ps   |
|                              |  | All Other Modes           | 134 | 1276 | ps   |
| $t_d$ (Trace Mismatch Delay) | Propagation delay mismatch across all traces | UHS-I DDR50               |     | 20   | ps   |
|                              |  | UHS-I SDR104              |     | 8    | ps   |
|                              |  | All Other Modes           |     | 100  | ps   |

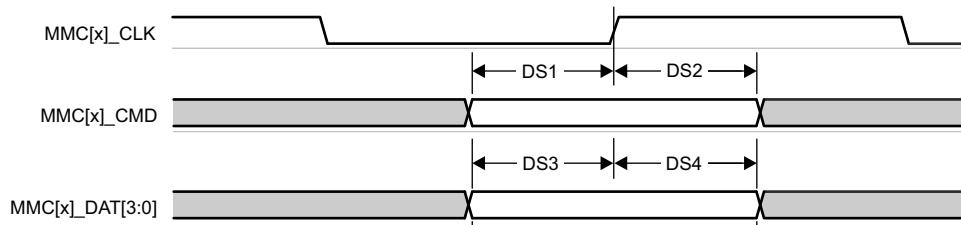
**6.10.5.16.2.1 Default speed Mode**

Table 6-70 and Table 6-71 present timing requirements and switching characteristics for MMCSDi – Default Speed Mode (see Figure 6-94 and Figure 6-95)

**Table 6-70. MMCSD1 Timing Requirements – Default Speed Mode**

| NO. | PARAMETER           | DESCRIPTION   | MIN  | MAX | UNIT |
|-----|---------------------|---|------|-----|------|
| DS1 | $t_{su}(cmdV-clkH)$ | Setup time, MMC[x]_CMD valid before MMC[x]_CLK rising edge      | 2.15 |     | ns   |
| DS2 | $t_h(clkH-cmdV)$    | Hold time, MMC[x]_CMD valid after MMC[x]_CLK rising edge        | 4.56 |     | ns   |
| DS3 | $t_{su}(dV-clkH)$   | Setup time, MMC[x]_DAT[3:0] valid before MMC[x]_CLK rising edge | 2.15 |     | ns   |
| DS4 | $t_h(clkH-dV)$      | Hold time, MMC[x]_DAT[3:0] valid after MMC[x]_CLK rising edge   | 4.56 |     | ns   |

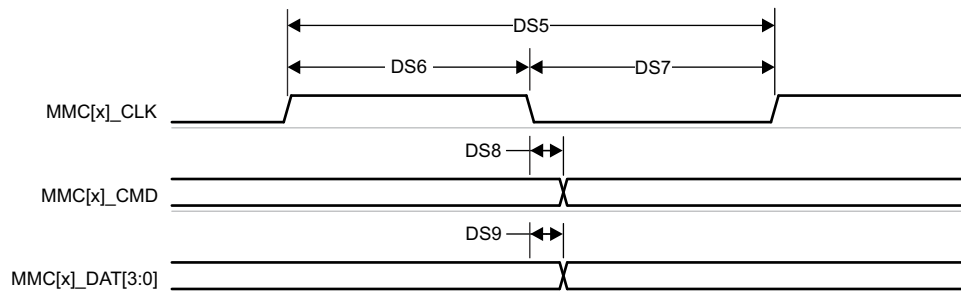
1. x = 1 for MMC1



**Figure 6-94. MMCSD1 – Default Speed – Receive Mode**

**Table 6-71. MMCSD1 Switching Characteristics – Default Speed Mode**

| NO. | PARAMETER        | DESCRIPTION   | MIN   | MAX  | UNIT |
|-----|------------------|---|-------|------|------|
|     | $f_{op}(clk)$    | Operating frequency, MMC[x]_CLK                                   |       | 25   | MHz  |
| DS5 | $t_c(clk)$       | Cycle time, MMC[x]_CLK  | 40    |      | ns   |
| DS6 | $t_w(clkH)$      | Pulse duration, MMC[x]_CLK high                                   | 18.7  |      | ns   |
| DS7 | $t_w(clkL)$      | Pulse duration, MMC[x]_CLK low                                    | 18.7  |      | ns   |
| DS8 | $t_d(clkL-cmdV)$ | Delay time, MMC[x]_CLK falling edge to MMC[x]_CMD transition      | -3.53 | 3.53 | ns   |
| DS9 | $t_d(clkL-dV)$   | Delay time, MMC[x]_CLK falling edge to MMC[x]_DAT[3:0] transition | -3.53 | 3.53 | ns   |



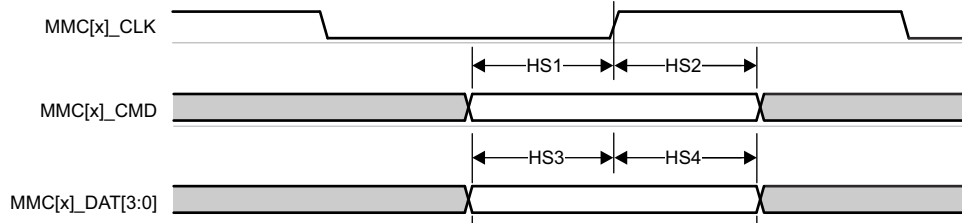
**Figure 6-95. MMCSD1 – Default Speed – Transmit Mode**

### 6.10.5.16.2.2 High Speed Mode

Table 6-72 and Table 6-73 present timing requirements and switching characteristics for MMCSDi – High Speed Mode (see Figure 6-96 and Figure 6-97).

**Table 6-72. MMCSD1 Timing Requirements – High Speed Mode**

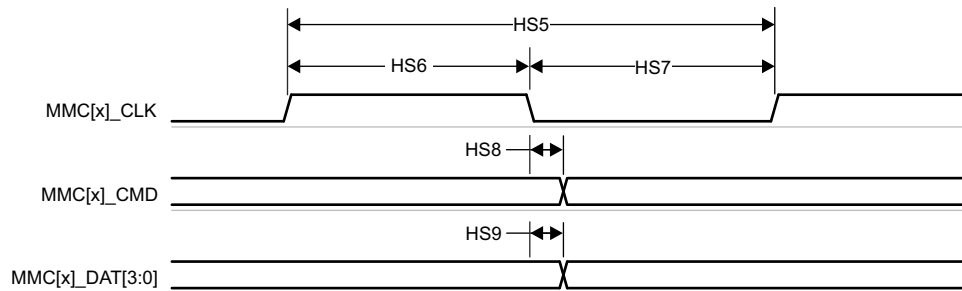
| NO. | PARAMETER           | DESCRIPTION   | MIN  | MAX | UNIT |
|-----|---------------------|---|------|-----|------|
| HS1 | $t_{su(cmdV-clkH)}$ | Setup time, MMC[x]_CMD valid before MMC[x]_CLK rising edge      | 2.15 |     | ns   |
| HS2 | $t_h(clkH-cmdV)$    | Hold time, MMC[x]_CMD valid after MMC[x]_CLK rising edge        | 2.26 |     | ns   |
| HS3 | $t_{su(dV-clkH)}$   | Setup time, MMC[x]_DAT[3:0] valid before MMC[x]_CLK rising edge | 2.15 |     | ns   |
| HS4 | $t_h(clkH-dV)$      | Hold time, MMC[x]_DAT[3:0] valid after MMC[x]_CLK rising edge   | 2.26 |     | ns   |



**Figure 6-96. MMCSD1 – High Speed – Receive Mode**

**Table 6-73. MMCSD1 Switching Characteristics – High Speed Mode**

| NO. | PARAMETER          | DESCRIPTION   | MIN   | MAX  | UNIT |
|-----|--------------------|---|-------|------|------|
|     | $f_{op(clk)}$      | Operating frequency, MMC[x]_CLK                                   |       | 50   | MHz  |
| HS5 | $t_{c(clk)}$       | Cycle time, MMC[x]_CLK  | 20    |      | ns   |
| HS6 | $t_w(clkH)$        | Pulse duration, MMC[x]_CLK high                                   | 9.2   |      | ns   |
| HS7 | $t_w(clkL)$        | Pulse duration, MMC[x]_CLK low                                    | 9.2   |      | ns   |
| HS8 | $t_{d(clkL-cmdV)}$ | Delay time, MMC[x]_CLK falling edge to MMC[x]_CMD transition      | -2.07 | 2.07 | ns   |
| HS9 | $t_{d(clkL-dV)}$   | Delay time, MMC[x]_CLK falling edge to MMC[x]_DAT[3:0] transition | -2.07 | 2.07 | ns   |



**Figure 6-97. MMCSD1 – High Speed – Transmit Mode**

### 6.10.5.16.2.3 UHS-I SDR12 Mode

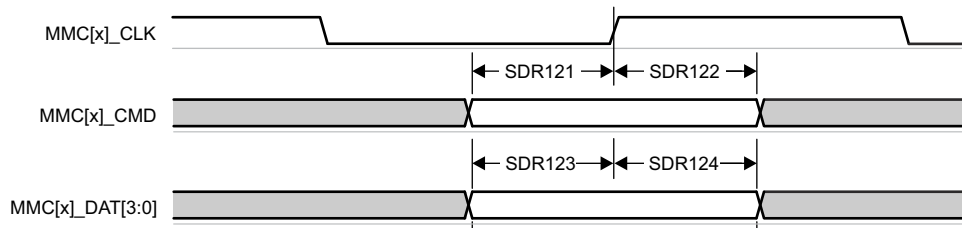
Table 6-74 and Table 6-75 present timing requirements and switching characteristics for MMCSDi – UHS-I SDR12 Mode (see Figure 6-98 and Figure 6-99).

**Table 6-74. MMCSD1 Timing Requirements – UHS-I SDR12 Mode**

| NO.    | PARAMETER           | DESCRIPTION   | MIN  | MAX | UNIT |
|--------|---------------------|---|------|-----|------|
| SDR121 | $t_{su(cmdV-clkH)}$ | Setup time, MMC[x]_CMD valid before MMC[x]_CLK rising edge      | 5.46 |     | ns   |
| SDR122 | $t_h(clkH-cmdV)$    | Hold time, MMC[x]_CMD valid after MMC[x]_CLK rising edge        | 1.67 |     | ns   |
| SDR123 | $t_{su(dV-clkH)}$   | Setup time, MMC[x]_DAT[3:0] valid before MMC[x]_CLK rising edge | 5.46 |     | ns   |

**Table 6-74. MMCSD1 Timing Requirements – UHS-I SDR12 Mode (continued)**

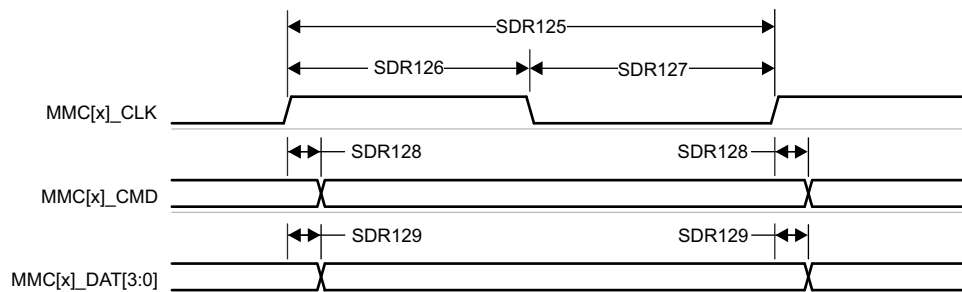
| NO.    | PARAMETER               | DESCRIPTION   | MIN  | MAX | UNIT |
|--------|-------------------------|---|------|-----|------|
| SDR124 | $t_{h(\text{clkH-dV})}$ | Hold time, MMC[x]_DAT[3:0] valid after MMC[x]_CLK rising edge | 1.67 |     | ns   |



**Figure 6-98. MMCSD1 – UHS-I SDR12 – Receive Mode**

**Table 6-75. MMCSD1 Switching Characteristics – UHS-I SDR12 Mode**

| NO.    | PARAMETER                        | DESCRIPTION  | MIN  | MAX   | UNIT |
|--------|----------------------------------|--|------|-------|------|
|        | $f_{\text{op}(\text{clk})}$      | Operating frequency, MMC[x]_CLK                                  |      | 25    | MHz  |
| SDR125 | $t_{\text{c}(\text{clk})}$       | Cycle time, MMC[x]_CLK   | 40   |       | ns   |
| SDR126 | $t_{\text{w}(\text{clkH})}$      | Pulse duration, MMC[x]_CLK high                                  | 18.7 |       | ns   |
| SDR127 | $t_{\text{w}(\text{clkL})}$      | Pulse duration, MMC[x]_CLK low                                   | 18.7 |       | ns   |
| SDR128 | $t_{\text{d}(\text{clkH-cmdV})}$ | Delay time, MMC[x]_CLK rising edge to MMC[x]_CMD transition      | 1.2  | 13.55 | ns   |
| SDR129 | $t_{\text{d}(\text{clkH-dV})}$   | Delay time, MMC[x]_CLK rising edge to MMC[x]_DAT[3:0] transition | 1.2  | 13.55 | ns   |



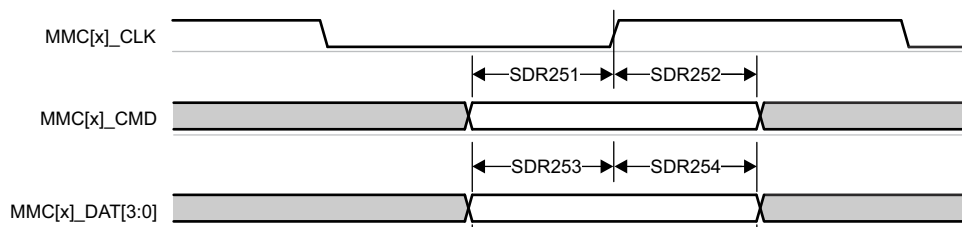
**Figure 6-99. MMCSD1 – UHS-I SDR12 – Transmit Mode**

#### 6.10.5.16.2.4 UHS-I SDR25 Mode

Table 6-76 and Table 6-77 present timing requirements and switching characteristics for MMCSDi – UHS-I SDR25 Mode (see Figure 6-100 and Figure 6-101).

**Table 6-76. MMCSD1 Timing Requirements – UHS-I SDR25 Mode**

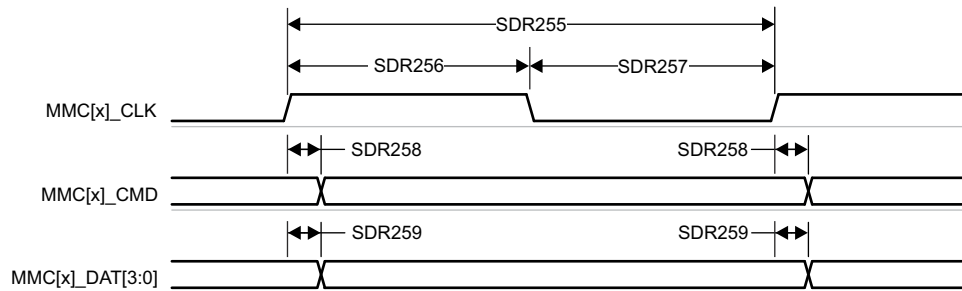
| NO.    | PARAMETER                         | DESCRIPTION   | MIN  | MAX | UNIT |
|--------|-----------------------------------|---|------|-----|------|
| SDR251 | $t_{\text{su}(\text{cmdV-clkH})}$ | Setup time, MMC[x]_CMD valid before MMC[x]_CLK rising edge      | 2.1  |     | ns   |
| SDR252 | $t_{\text{h}(\text{clkH-cmdV})}$  | Hold time, MMC[x]_CMD valid after MMC[x]_CLK rising edge        | 1.67 |     | ns   |
| SDR253 | $t_{\text{su}(\text{dV-clkH})}$   | Setup time, MMC[x]_DAT[3:0] valid before MMC[x]_CLK rising edge | 2.1  |     | ns   |
| SDR254 | $t_{\text{h}(\text{clkH-dV})}$    | Hold time, MMC[x]_DAT[3:0] valid after MMC[x]_CLK rising edge   | 1.67 |     | ns   |



**Figure 6-100. MMCSD1 – UHS-I SDR25 – Receive Mode**

**Table 6-77. MMCSD1 Switching Characteristics – UHS-I SDR25 Mode**

| NO.    | PARAMETER          | DESCRIPTION  | MIN | MAX  | UNIT |
|--------|--------------------|--|-----|------|------|
|        | $f_{op}(clk)$      | Operating frequency, MMC[x]_CLK                                  |     | 50   | MHz  |
| SDR255 | $t_{c}(clk)$       | Cycle time, MMC[x]_CLK   | 20  |      | ns   |
| SDR256 | $t_{w}(clkH)$      | Pulse duration, MMC[x]_CLK high                                  | 9.2 |      | ns   |
| SDR257 | $t_{w}(clkL)$      | Pulse duration, MMC[x]_CLK low                                   | 9.2 |      | ns   |
| SDR258 | $t_{d}(clkH-cmdV)$ | Delay time, MMC[x]_CLK rising edge to MMC[x]_CMD transition      | 2.4 | 9.37 | ns   |
| SDR259 | $t_{d}(clkH-dV)$   | Delay time, MMC[x]_CLK rising edge to MMC[x]_DAT[3:0] transition | 2.4 | 9.37 | ns   |



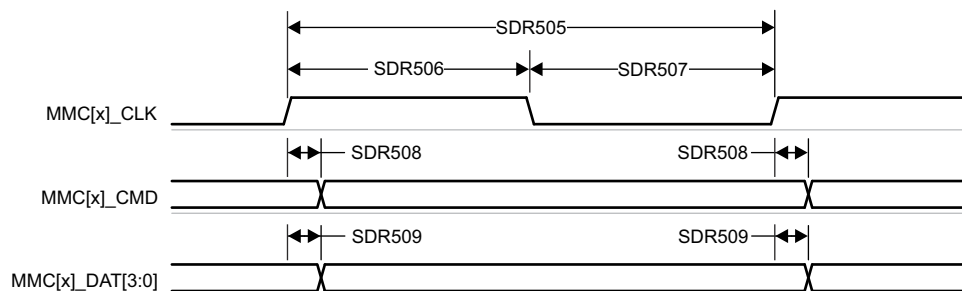
**Figure 6-101. MMCSD1 – UHS-I SDR25 – Transmit Mode**

#### 6.10.5.16.2.5 UHS-I SDR50 Mode

Table 6-78 presents timing requirements and switching characteristics for MMCSDi – UHS-I SDR50 Mode (see and Figure 6-102).

**Table 6-78. MMCSD1 Switching Characteristics – UHS-I SDR50 Mode**

| NO.    | PARAMETER          | DESCRIPTION  | MIN  | MAX  | UNIT |
|--------|--------------------|--|------|------|------|
|        | $f_{op}(clk)$      | Operating frequency, MMC[x]_CLK                                  |      | 100  | MHz  |
| SDR505 | $t_{c}(clk)$       | Cycle time, MMC[x]_CLK   | 10   |      | ns   |
| SDR506 | $t_{w}(clkH)$      | Pulse duration, MMC[x]_CLK high                                  | 4.45 |      | ns   |
| SDR507 | $t_{w}(clkL)$      | Pulse duration, MMC[x]_CLK low                                   | 4.45 |      | ns   |
| SDR508 | $t_{d}(clkH-cmdV)$ | Delay time, MMC[x]_CLK rising edge to MMC[x]_CMD transition      | 1.2  | 6.35 | ns   |
| SDR509 | $t_{d}(clkH-dV)$   | Delay time, MMC[x]_CLK rising edge to MMC[x]_DAT[3:0] transition | 1.2  | 6.35 | ns   |



**Figure 6-102. MMCSD1 – UHS-I SDR50 – Transmit Mode**

#### 6.10.5.16.2.6 UHS-I DDR50 Mode

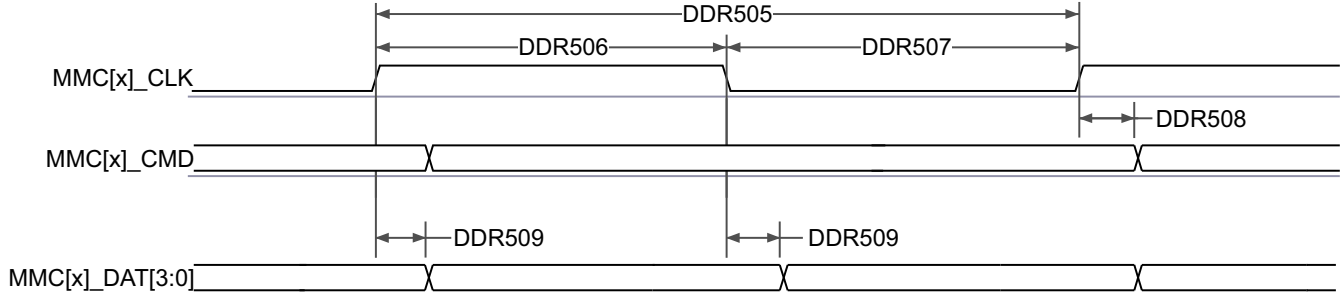
Table 6-79 present switching characteristics for MMCSDi – UHS-I DDR50 Mode (see Figure 6-103).

**Table 6-79. MMCSD1 Switching Characteristics – UHS-I DDR50 Mode**

| NO.    | PARAMETER     | DESCRIPTION                     | MIN | MAX | UNIT |
|--------|---------------|---------------------------------|-----|-----|------|
|        | $f_{op}(clk)$ | Operating frequency, MMC[x]_CLK |     | 50  | MHz  |
| DDR505 | $t_{c}(clk)$  | Cycle time, MMC[x]_CLK          | 20  |     | ns   |
| DDR506 | $t_{w}(clkH)$ | Pulse duration, MMC[x]_CLK high | 9.2 |     | ns   |

**Table 6-79. MMCSD1 Switching Characteristics – UHS-I DDR50 Mode (continued)**

| NO.    | PARAMETER                 | DESCRIPTION   | MIN | MAX  | UNIT |
|--------|---------------------------|---|-----|------|------|
| DDR507 | $t_{w(\text{clkL})}$      | Pulse duration, MMC[x]_CLK low                                  | 9.2 |      | ns   |
| DDR508 | $t_{d(\text{clkH-cmdV})}$ | Delay time, MMC[x]_CLK rising edge to MMC[x]_CMD transition     | 1.2 | 3.46 | ns   |
| DDR509 | $t_{d(\text{clk-dV})}$    | Delay time, MMC[x]_CLK transition to MMC[x]_DAT[3:0] transition | 1.2 | 6.12 | ns   |



**Figure 6-103. MMCSD1 – UHS-I DDR50 – Transmit Mode**

6.10.5.16.2.7 UHS-I SDR104 Mode

Table 6-80 presents timing requirements and switching characteristics for MMCSDi – UHS-I SDR104 Mode (see Figure 6-104)

Table 6-80. MMCSD1 Switching Characteristics – UHS-I SDR104 Mode

| NO.     | PARAMETER          | DESCRIPTION  | MIN  | MAX | UNIT |
|---------|--------------------|--|------|-----|------|
|         | $f_{op}(clk)$      | Operating frequency, MMC[x]_CLK                                  |      | 200 | MHz  |
| SDR1045 | $t_{c}(clk)$       | Cycle time, MMC[x]_CLK   | 5    |     | ns   |
| SDR1046 | $t_{w}(clkH)$      | Pulse duration, MMC[x]_CLK high                                  | 2.12 |     | ns   |
| SDR1047 | $t_{w}(clkL)$      | Pulse duration, MMC[x]_CLK low                                   | 2.12 |     | ns   |
| SDR1048 | $t_{d}(clkH-cmdV)$ | Delay time, MMC[x]_CLK rising edge to MMC[x]_CMD transition      | 2.12 | 3.2 | ns   |
| SDR1049 | $t_{d}(clkH-dV)$   | Delay time, MMC[x]_CLK rising edge to MMC[x]_DAT[3:0] transition | 2.12 | 3.2 | ns   |

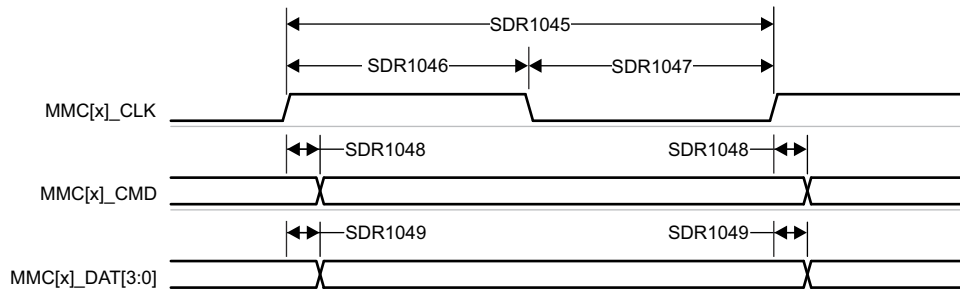


Figure 6-104. MMCSD1 – UHS-I SDR104 – Transmit Mode

6.10.5.17 NAVSS

Table 6-81 represents CPTS timing conditions.

Table 6-81. CPTS Timing Conditions

| PARAMETER                | DESCRIPTION             | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----|-----|------|
| <b>Input Conditions</b>  |                         |     |     |      |
| $t_{SR}$                 | Input slew rate         | 0.5 | 5   | V/ns |
| <b>Output Conditions</b> |                         |     |     |      |
| $C_{LOAD}$               | Output load capacitance | 2   | 10  | pF   |

Section 6.10.5.17.1, Section 6.10.5.17.2, Figure 6-105, and Figure 6-106 present timing requirement and switching characteristics of the CPTS interface.

6.10.5.17.1 Timing Requirements for CPTS Input

| NO. | PARAMETER               | DESCRIPTION                      | MIN                           | MAX | UNIT |
|-----|-------------------------|----------------------------------|-------------------------------|-----|------|
| T1  | $t_{w}(HWn\_TS\_PUSHH)$ | HWn_TS_PUSH Pulse duration, high | $2.1 + 12P^{(1)}$             |     | ns   |
| T2  | $t_{w}(HWn\_TS\_PUSHL)$ | HWn_TS_PUSH pulse duration, low  | $2.1 + 12P^{(1)}$             |     | ns   |
| T3  | $t_{c}(RFT\_CLK)$       | RFT_CLK cycle time               | 5                             | 8   | ns   |
| T4  | $t_{w}(RFT\_CLKH)$      | RFT_CLK pulse duration, high     | $0.45 \times t_{c}(RFT\_CLK)$ |     | ns   |
| T5  | $t_{w}(RFT\_CLKL)$      | RFT_CLK pulse duration, low      | $0.45 \times t_{c}(RFT\_CLK)$ |     | ns   |

(1) P = functional clock period in ns.

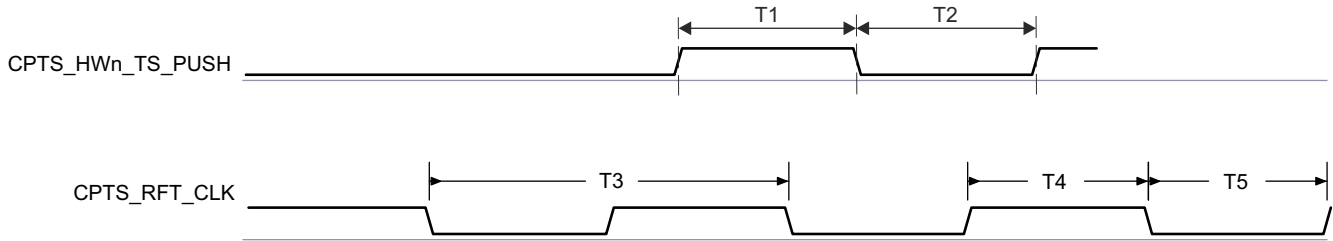


Figure 6-105. CPTS Input Timing

6.10.5.17.2 Switching Characteristics for CPTS Output

| NO.   | PARAMETER         | DESCRIPTION                      | MIN                     | MAX | UNIT |
|-------|-------------------|----------------------------------|-------------------------|-----|------|
| T6    | $t_w(TS\_COMPH)$  | NAVSS-CPTS TS_COMP, high         | -2.1+36P <sup>(1)</sup> |     | ns   |
| T7    | $t_w(TS\_COMPL)$  | NAVSS-CPTS TS_COMP, low          | -2.1+36P <sup>(1)</sup> |     | ns   |
| T8    | $t_w(TS\_COMPH)$  | CPSW-CPTS TS_COMP, high          | -2.1+36P <sup>(1)</sup> |     | ns   |
| T9    | $t_w(TS\_COMPL)$  | CPSW-CPTS TS_COMP, low           | -2.1+36P <sup>(1)</sup> |     | ns   |
| T10   | $t_w(TS\_SYNCH)$  | NAVSS-CPTS TS_SYNC, high         | -2.1+36P <sup>(1)</sup> |     | ns   |
| T11   | $t_w(TS\_SYNCL)$  | NAVSS-CPTS TS_SYNC, low          | -2.1+36P <sup>(1)</sup> |     | ns   |
| T12.1 | $t_w(TS\_SYNCH)$  | CPSW-CPTS TS_SYNC, high          | -2.1+36P <sup>(1)</sup> |     | ns   |
| T13   | $t_w(TS\_SYNCL)$  | CPSW-CPTS TS_SYNC, low           | -2.1+36P <sup>(1)</sup> |     | ns   |
| T14   | $t_w(SYNC\_OUTH)$ | TS_SYNC sourcing SYNCn_OUT, high | -2.1+36P <sup>(1)</sup> |     | ns   |
| T15   | $t_w(SYNC\_OUTL)$ | TS_SYNC sourcing SYNCn_OUT, low  | -2.1+36P <sup>(1)</sup> |     | ns   |
| T16   | $t_w(SYNC\_OUTH)$ | GENF sourcing SYNCn_OUT, high    | -2.1+5P <sup>(1)</sup>  |     | ns   |
| T17   | $t_w(SYNC\_OUTL)$ | GENF sourcing SYNCn_OUT, low     | -2.1+5P <sup>(1)</sup>  |     | ns   |

(1) P = functional clock period in ns.

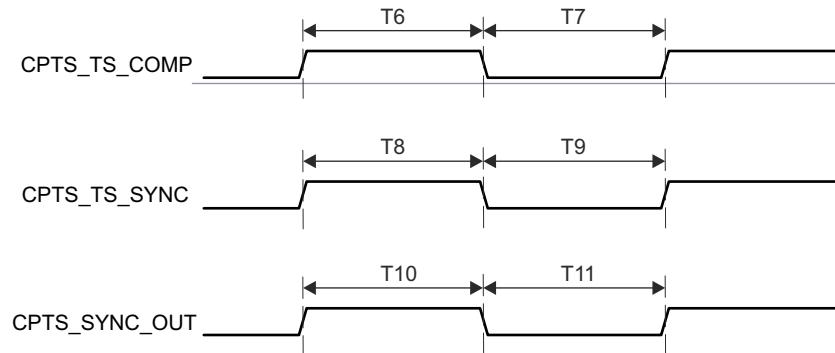


Figure 6-106. CPTS Output Switching Characteristics

For more information, see *Navigator Subsystem (NAVSS)* section in *Data Movement Architecture (DMA)* chapter in the device TRM.

6.10.5.18 OSPI

For more details about features and additional description information on the device Octal Serial Peripheral Interface, see the corresponding sections within [Section 5.3, Signal Descriptions](#) and [Section 7, Detailed Description](#).

[Table 6-82](#) represents OSPI timing conditions.

Table 6-82. OSPIx Timing Conditions

| PARAMETER               | MODE | MIN | MAX | UNIT |
|-------------------------|------|-----|-----|------|
| <b>INPUT CONDITIONS</b> |      |     |     |      |

**Table 6-82. OSPIx Timing Conditions (continued)**

| PARAMETER                             |  | MODE  | MIN                    | MAX                    | UNIT |
|---------------------------------------|--|---|------------------------|------------------------|------|
| SR <sub>I</sub>                       | Input slew rate  | 1.8V, PHY Data Training DDR with DQS                          | 0.75                   | 6                      | V/ns |
| <b>OUTPUT CONDITIONS</b>              |  |   |                        |                        |      |
| C <sub>L</sub>                        | Output load capacitance  |   | 3                      | 10                     | pF   |
| <b>PCB CONNECTIVITY REQUIREMENTS</b>  |  |   |                        |                        |      |
| t <sub>d</sub> (Trace Delay)          | Propagation delay of OSPI0_CLK traces  | No Loopback<br>Internal PHY Loopback<br>Internal Pad Loopback |                        | 450                    | ps   |
|                                       | Propagation delay of OSPI0_LBCLKO traces   | External Board Loopback                                       | 2L <sup>(1)</sup> - 30 | 2L <sup>(1)</sup> + 30 | ps   |
|                                       | Propagation delay of OSPI0_DQS traces  | DQS   | L <sup>(1)</sup> - 30  | L <sup>(1)</sup> + 30  | ps   |
| t <sub>d</sub> (Trace Mismatch Delay) | Propagation delay mismatch of OSPIx_D[7:0] and OSPIx_CS <sub>n</sub> [3:0] relative to OSPIx_CLK | All modes   |                        | 60                     | ps   |

(1) L = Propagation delay of OSPIx\_CLK trace

For more information, see *Octal Serial Peripheral Interface (OSPI)* section in *Peripherals* chapter in the device TRM.

### 6.10.5.18.1 OSPI With Data Training

#### 6.10.5.18.1.1 OSPI Switching Characteristics – Data Training

| PARAMETER            | DESCRIPTION     | MODE      | MIN  | MAX | UNIT |
|----------------------|-----------------|-----------|------|-----|------|
| t <sub>c</sub> (CLK) | Cycle time, CLK | DDR, 1.8V | 6.02 | 7.5 | ns   |
|                      |                 | DDR, 3.3V | 7.52 | 7.5 | ns   |
| t <sub>c</sub> (CLK) | Cycle time, CLK | SDR, 1.8V | 6.02 | 7.5 | ns   |
|                      |                 | SDR, 3.3V | 7.52 | 7.5 | ns   |

#### 6.10.5.18.2 OSPI Without Data Training

##### Note

The I/O Timings provided in this section are only applicable when data training is not implemented. Additionally, the I/O Timings are valid only for some OSPI usage modes when the corresponding DLL Delays are configured as described in [Table 6-83](#) found in this section.

[Section 6.10.5.18.2.1](#), [Section 6.10.5.18.2.2](#), [Figure 6-107](#), and [Figure 6-108](#) present switching characteristics for OSPI DDR and SDR Mode.

#### 6.10.5.18.2.1 OSPI Switching Characteristics – DDR Mode

| NO. <sup>(1)</sup> | PARAMETER                             | DESCRIPTION  | MODE                                      | MIN  | MAX   | UNIT |
|--------------------|---------------------------------------|--|---|--|---|------|
| O1                 | t <sub>c</sub> (CLK)                  | Cycle time, CLK  | 1.8V                                      | 19   |   | ns   |
|                    |                                       |  | 3.3V                                      | 19   |   | ns   |
| O2                 | t <sub>w</sub> (CLKL)                 | Pulse duration, CLK low  |   | -0.3+0.475*P<br>(2)                            |   | ns   |
| O3                 | t <sub>w</sub> (CLKH)                 | Pulse duration, CLK high   |   | -0.3+0.475*P<br>(2)                            |   | ns   |
| O4                 | t <sub>d</sub> (CLK-CS <sub>n</sub> ) | Delay time, CS <sub>n</sub> [3:0] active edge to CLK rising edge | 1.8V, OSPI0 DDR TX;<br>1.8V, OSPI1 DDR TX | -7-0.475 * P –<br>0.975 * N * R<br>(3) (4) (5) | 0.525 * P +<br>1.025 * M * R<br>+ 1 (3) (4) (5) | ns   |
|                    |                                       |  | 3.3V, OSPI0 DDR TX;<br>3.3V, OSPI1 DDR TX | -7-0.475 * P –<br>0.975 * N * R<br>(3) (4) (5) | 0.525 * P +<br>1.025 * M * R<br>+ 1 (3) (4) (5) | ns   |

| NO. (1) | PARAMETER        | DESCRIPTION                                      | MODE                                      | MIN   | MAX  | UNIT |
|---------|------------------|--|---|---|--|------|
| O5      | $t_{d(CLK-CSn)}$ | Delay time, CLK rising edge to CSn inactive edge | 1.8V, OSPI0 DDR TX;<br>1.8V, OSPI1 DDR TX | $-7+0.475 * P$<br>$+ 0.975 * N * R$<br><small>R (3) (4) (5)</small> | $0.525 * P +$<br>$1.025 * N * R$<br><small>+ 1 (3) (4) (5)</small> | ns   |
|         |                  |  | 3.3V, OSPI0 DDR TX;<br>3.3V, OSPI1 DDR TX | $-7+0.475 * P$<br>$+ 0.975 * N * R$<br><small>R (3) (4) (5)</small> | $0.525 * P +$<br>$1.025 * N * R$<br><small>+ 1 (3) (4) (5)</small> | ns   |
| O6      | $t_{d(CLK-D)}$   | Delay time, CLK active edge to D[i:0] transition | 1.8V, OSPI0 DDR TX;<br>1.8V, OSPI1 DDR TX | -7.7  | -1.56  | ns   |
|         |                  |  | 3.3V, OSPI0 DDR TX;<br>3.3V, OSPI1 DDR TX | -7.7  | -1.56  | ns   |

- (1) i in [i:0] = 7 for OSPI0, i in [i:0] = 3 for OSPI1
- (2) P = CLK cycle time
- (3) P = SCLK period
- (4) M = OSPI\_DEV\_DELAY\_REG[D\_INIT\_FLD], N = OSPI\_DEV\_DELAY\_REG[D\_AFTER\_FLD]
- (5) R = reflck

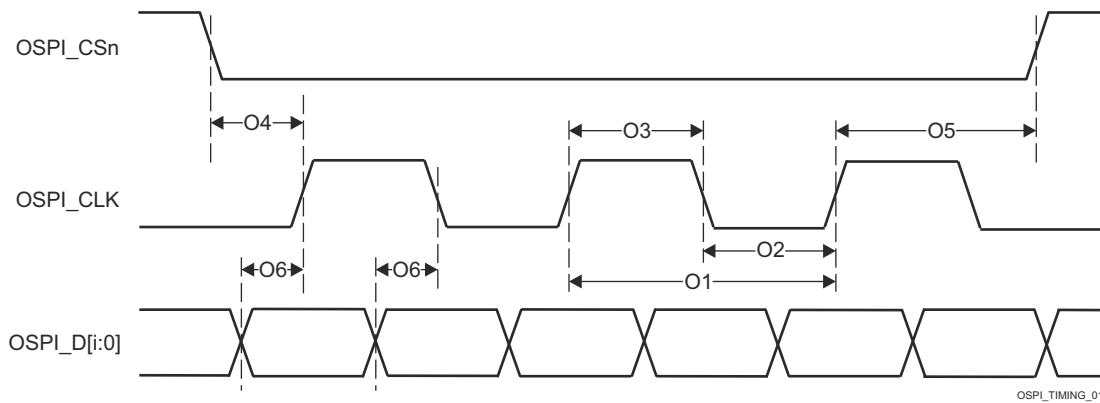


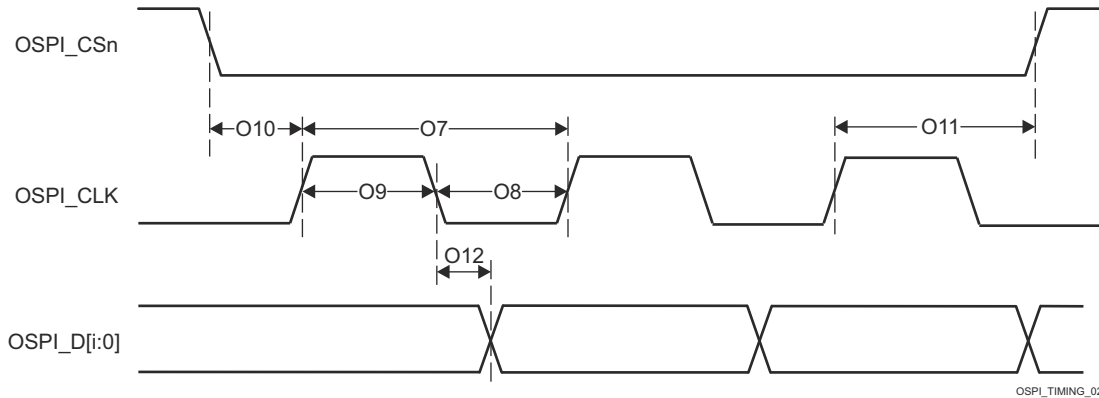
Figure 6-107. OSPI Switching Characteristics – DDR

6.10.5.18.2.2 OSPI Switching Characteristics – SDR Mode

| NO. (1) | PARAMETER        | DESCRIPTION   | MODE | MIN   | MAX  | UNIT |
|---------|------------------|---|------|---|--|------|
| O7      | $t_{c(CLK)}$     | Cycle time, CLK                                     | 1.8V | 7   |  | ns   |
|         |                  |   | 3.3V | 7.52  |  | ns   |
| O8      | $t_{w(CLKL)}$    | Pulse duration, CLK low                             |      | $-0.3+0.475 * P$<br><small>(2)</small>                              |  | ns   |
| O9      | $t_{w(CLKH)}$    | Pulse duration, CLK high                            |      | $-0.3+0.475 * P$<br><small>(2)</small>                              |  | ns   |
| O10     | $t_{d(CLK-CSn)}$ | Delay time, CSn[3:0] active edge to CLK rising edge | 1.8V | $-1-0.475 * P -$<br>$0.975 * N * R$<br><small>(3) (4) (5)</small>   | $0.525 * P +$<br>$1.025 * M * R$<br><small>+ 1 (3) (4) (5)</small> | ns   |
|         |                  |   | 3.3V | $-1-0.475 * P -$<br>$0.975 * N * R$<br><small>(3) (4) (5)</small>   | $0.525 * P +$<br>$1.025 * M * R$<br><small>+ 1 (3) (4) (5)</small> | ns   |
| O11     | $t_{d(CLK-CSn)}$ | Delay time, CLK rising edge to CSn inactive edge    | 1.8V | $-1+0.475 * P$<br>$+ 0.975 * N * R$<br><small>R (3) (4) (5)</small> | $0.525 * P +$<br>$1.025 * N * R$<br><small>+ 1 (3) (4) (5)</small> | ns   |
|         |                  |   | 3.3V | $-1+0.475 * P$<br>$+ 0.975 * N * R$<br><small>R (3) (4) (5)</small> | $0.525 * P +$<br>$1.025 * N * R$<br><small>+ 1 (3) (4) (5)</small> | ns   |
| O12     | $t_{d(CLK-D)}$   | Delay time, CLK active edge to D[i:0] transition    | 1.8V | -1.15   | 1.25   | ns   |
|         |                  |   | 3.3V | -1.33   | 1.51   | ns   |

- (1) i in [i:0] = 7 for OSPI0, i in [i:0] = 3 for OSPI1
- (2) P = CLK cycle time

- (3) P = SCLK period
- (4) M = OSPI\_DEV\_DELAY\_REG[D\_INIT\_FLD], N = OSPI\_DEV\_DELAY\_REG[D\_AFTER\_FLD]
- (5) R = refclk



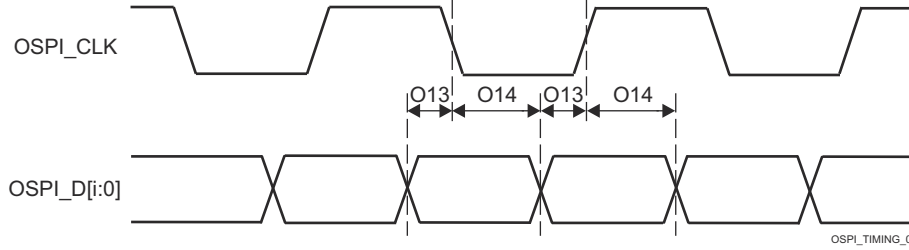
**Figure 6-108. OSPI Switching Characteristics – SDR**

Section 6.10.5.18.2.3, Section 6.10.5.18.2.4, Figure 6-109, Figure 6-110, Figure 6-111, and Figure 6-112 presents timing requirements for OSPI DDR and SDR Mode.

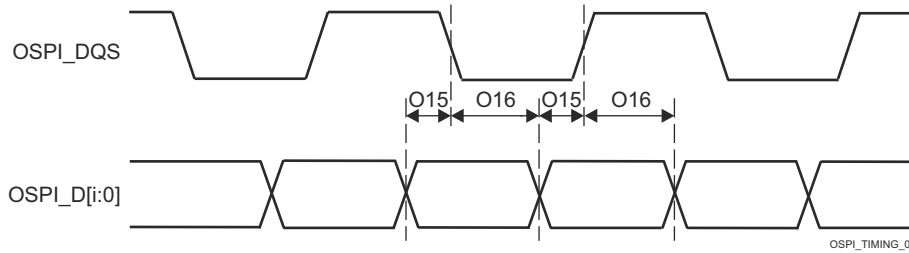
**6.10.5.18.2.3 OSPI Timing Requirements – DDR Mode**

| NO. (1) | PARAMETER         | DESCRIPTION   | MODE   | MIN      | MAX | UNIT |
|---------|-------------------|---|--|----------|-----|------|
| O13     | $t_{su(D-CLK)}$   | Setup time, D[i:0] valid before active CLK edge         | 1.8V, No Loopback Clock; 1.8V, Internal Pad Loopback Clock | 5.23     |     | ns   |
|         |                   |   | 3.3V, No Loopback Clock; 3.3V, Internal Pad Loopback Clock | 6.19     |     | ns   |
| O14     | $t_{h(CLK-D)}$    | Hold time, D[i:0] valid after active CLK edge           | 1.8V, No Loopback Clock; 1.8V, Internal Pad Loopback Clock | 1.84     |     | ns   |
|         |                   |   | 3.3V, No Loopback Clock; 3.3V, Internal Pad Loopback Clock | 2.34     |     | ns   |
| O15     | $t_{su(D-LBCLK)}$ | Setup time, D[i:0] valid before active LBCLK (DQS) edge | 1.8V, External Board Loopback Clock                        | 0.52     |     | ns   |
|         |                   |   | 3.3V, External Board Loopback Clock                        | 1.97     |     | ns   |
| O16     | $t_{h(LBCLK-D)}$  | Hold time, D[i:0] valid after active LBCLK (DQS) edge   | 1.8V, External Board Loopback Clock                        | 1.2 (2)  |     | ns   |
|         |                   |   | 3.3V, External Board Loopback Clock                        | 1.44 (2) |     | ns   |
|         | $t_{DVW}$         | Data valid window (O15 + O16)                           | 1.8V, DDR with DQS   | 1.4      |     | ns   |
| O17     | $t_{su(D-DQS)}$   | Setup time, DQS edge to D[i:0] transition               | 1.8V, OSPI0 DQS; 1.8V, OSPI1 DQS                           | -0.46    |     | ns   |
|         |                   |   | 3.3V, OSPI0 DQS; 3.3V, OSPI1 DQS                           | -0.66    |     | ns   |
| O18     | $t_{h(DQS-D)}$    | Hold time, DQS edge to D[i:0] transition                | 1.8V, OSPI0 DQS; 1.8V, OSPI1 DQS                           | 3.59     |     | ns   |
|         |                   |   | 3.3V, OSPI0 DQS; 3.3V, OSPI1 DQS                           | 7.92     |     | ns   |

- (1) i in [i:0] = 7 for OSPI0, i in [i:0] = 3 for OSPI1
- (2) This Hold time requirement is larger than the Hold time provided by a typical flash device. Therefore, the trace length between the SoC and flash device must be sufficiently long enough to ensure that the Hold time is met at the SoC. The length of the SoC's external loopback clock (OSPI\_LBCLKO to OSPI\_DQS) may need to be shortened to compensate.



**Figure 6-109. OSPI Timing Requirements – DDR, No Loopback Clock and Internal Pad Loopback Clock**

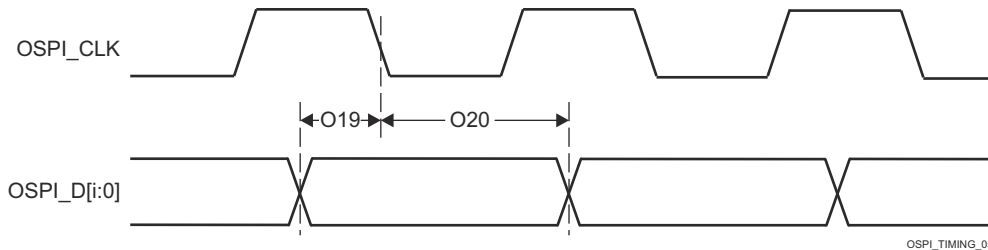


**Figure 6-110. OSPI Timing Requirements – DDR, External Loopback Clock and DQS**

**6.10.5.18.2.4 OSPI Timing Requirements – SDR Mode**

| NO.<br>(1) | PARAMETER         | DESCRIPTION   | MODE                                   | MIN  | MAX | UNIT |
|------------|-------------------|---|--|------|-----|------|
| O19        | $t_{su}(D-CLK)$   | Setup time, D[i:0] valid before active CLK edge               | 1.8V, No Loopback Clock                | 4.8  |     | ns   |
|            |                   |   | 3.3V, No Loopback Clock                | 5.39 |     | ns   |
| O20        | $t_h(CLK-D)$      | Hold time, D[i:0] valid after active CLK edge                 | 1.8V, No Loopback Clock                | -0.5 |     | ns   |
|            |                   |   | 3.3V, No Loopback Clock                | -0.5 |     | ns   |
| O21        | $t_{su}(D-LBCLK)$ | Setup time, D[i:0] valid before active LBCLK input (DQS) edge | 1.8V, External Board Loopback Clock    | 0.6  |     | ns   |
|            |                   |   | 3.3V, External Board Loopback Clock    | 0.9  |     | ns   |
| O22        | $t_h(LBCLK-D)$    | Hold time, D[i:0] valid after active LBCLK input (DQS) edge   | 1.8V, External Board Loopback Clock    | 1.7  |     | ns   |
|            |                   |   | 3.3V, External Board Loopback Clock    | 2    |     | ns   |
|            | $t_{DVW}$         | Data valid window (O21 + O22)                                 | 1.8V, SDR with External Board Loopback | 1.7  |     | ns   |

(1) i in [i:0] = 7 for OSPI0, i in [i:0] = 3 for OSPI1



**Figure 6-111. OSPI Timing Requirements – SDR, No Loopback Clock and Internal Pad Loopback Clock**

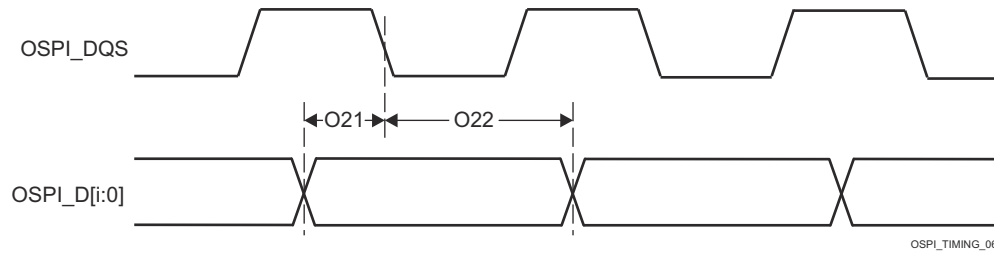


Figure 6-112. OSPI Timing Requirements – SDR, External Loopback Clock

Table 6-83. OSPI DLL Delay Mapping for Timing Modes

| MODE            | OSPI_PHY_CONFIGURATION_REG BIT FIELD | DELAY VALUE |
|-----------------|--------------------------------------|-------------|
| <b>TRANSMIT</b> |                                      |             |
| 1.8 V           | PHY_CONFIG_TX_DLL_DELAY_FLD          | 0x54        |
| 3.3 V           | PHY_CONFIG_TX_DLL_DELAY_FLD          | 0x55        |
| <b>RECEIVE</b>  |                                      |             |
| 1.8 V, DQS      | PHY_CONFIG_RX_DLL_DELAY_FLD          | 0x2D        |
| 3.3 V, DQS      | PHY_CONFIG_RX_DLL_DELAY_FLD          | 0x29        |
| All other modes | PHY_CONFIG_RX_DLL_DELAY_FLD          | 0x0         |

For more information, see *Octal Serial Peripheral Interface (OSPI)* section in *Peripherals* chapter in the device TRM.

#### 6.10.5.19 PCIe

The PCI-Express Subsystem is compliant with the PCIe® Base Specification, Revision 4.0. Refer to the specification for timing details.

For more details about features and additional description information on the device Peripheral Component Interconnect Express, see the corresponding sections within [Section 5.3, Signal Descriptions](#) and [Section 7, Detailed Description](#).

For more information, see *Peripheral Component Interconnect Express (PCIe) Subsystem* section in *Peripherals* chapter in the device TRM.

#### 6.10.5.20 Timers

For more details about features and additional description information on the device Timers, see the corresponding sections within [Section 5.3, Signal Descriptions](#) and [Section 7, Detailed Description](#).

[Table 6-84](#) represents Timers timing conditions.

Table 6-84. Timers Timing Conditions

| PARAMETER                | DESCRIPTION             | MODE    | MIN | MAX | UNIT |
|--------------------------|-------------------------|---------|-----|-----|------|
| <b>Input Conditions</b>  |                         |         |     |     |      |
| $t_{SR}$                 | Input slew rate         | CAPTURE | 0.5 | 5   | V/ns |
| <b>Output Conditions</b> |                         |         |     |     |      |
| $C_{LOAD}$               | Output load capacitance | PWM     | 2   | 10  | pF   |

[Section 6.10.5.20.1](#), [Section 6.10.5.20.2](#) and [Figure 6-113](#) present timings and switching characteristics of the Timers.

**6.10.5.20.1 Timing Requirements for Timers**

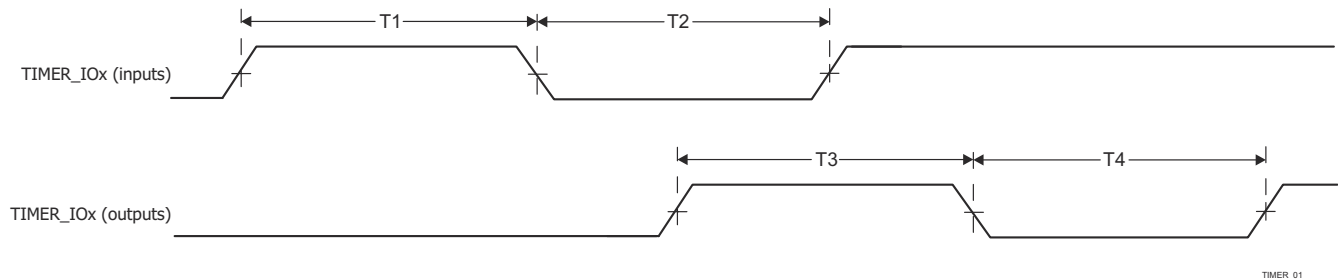
| NO. | PARAMETER      | DESCRIPTION          | MODE    | MIN              | MAX | UNIT |
|-----|----------------|----------------------|---------|------------------|-----|------|
| T1  | $t_{w(TINPH)}$ | Pulse duration, high | CAPTURE | $2.5 + 4P^{(1)}$ |     | ns   |
| T2  | $t_{w(TINPL)}$ | Pulse duration, low  | CAPTURE | $2.5 + 4P^{(1)}$ |     | ns   |

(1) P = functional clock period in ns.

**6.10.5.20.2 Switching Characteristics for Timers**

| NO. | PARAMETER       | DESCRIPTION          | MODE | MIN               | MAX | UNIT |
|-----|-----------------|----------------------|------|-------------------|-----|------|
| T3  | $t_{w(TOOUTH)}$ | Pulse duration, high | PWM  | $-2.5 + 4P^{(1)}$ |     | ns   |
| T4  | $t_{w(TOOUTL)}$ | Pulse duration, low  | PWM  | $-2.5 + 4P^{(1)}$ |     | ns   |

(1) P = functional clock period in ns.



**Figure 6-113. Timer Timing**

For more information, see *Timers* section in *Peripherals* chapter in the device TRM.

**6.10.5.21 UART**

For more details about features and additional description information on the device Universal Asynchronous Receiver Transmitter, see the corresponding sections within [Section 5.3, Signal Descriptions](#) and [Section 7, Detailed Description](#).

[Table 6-85](#) represents UART timing conditions.

**Table 6-85. UART Timing Conditions**

| PARAMETER                | DESCRIPTION             | MIN | MAX        | UNIT |
|--------------------------|-------------------------|-----|------------|------|
| <b>Input Conditions</b>  |                         |     |            |      |
| $t_{SR}$                 | Input slew rate         | 0.5 | 5          | V/ns |
| <b>Output Conditions</b> |                         |     |            |      |
| $C_{LOAD}$               | Output load capacitance | 1   | $30^{(1)}$ | pF   |

(1) This value represents an absolute maximum load capacitance. As the UART baud rate increases, it may be necessary to reduce the load capacitance to a value less than this maximum limit to provide enough timing margin for the attached device. The output rise/fall times increase as capacitive load increases, which decreases the time data is valid for the receiver of the attached devices. Therefore, it is important to understand the minimum data valid time required by the attached device at the operating baud rate. Then use the device IBIS models to verify the actual load capacitance on the UART signals does not increase the rise/fall times beyond the point where the minimum data valid time of the attached device is violated.

[Section 6.10.5.21.1](#), [Section 6.10.5.21.2](#), and [Figure 6-114](#) present timing requirements and switching characteristics for UART interface.

### 6.10.5.21.1 UART Timing Requirements

| NO. | PARAMETER    | DESCRIPTION                                 | MIN                         | MAX                         | UNIT |
|-----|--------------|---|-----------------------------|-----------------------------|------|
| 4   | $t_{w(RX)}$  | Pulse width, receive data bit, high or low  | 0.95U <sup>(1)</sup><br>(2) | 1.05U <sup>(1)</sup><br>(2) | ns   |
| 5   | $t_{w(CTS)}$ | Pulse width, receive start bit, high or low | 0.95U <sup>(1)</sup><br>(2) |                             | ns   |

(1) U = UART baud time = 1/Programmed baud rate

(2) This value defines the data valid time, where the input voltage is required to be above  $V_{IH}$  or below  $V_{IL}$ .

### 6.10.5.21.2 UART Switching Characteristics

| NO. | PARAMETER    | DESCRIPTION                                  | MIN                  | MAX                  | UNIT |
|-----|--------------|--|----------------------|----------------------|------|
|     | $f_{(baud)}$ | Maximum programmable baud rate               |                      | 12                   | Mbps |
| 2   | $t_{w(TX)}$  | Pulse width, transmit data bit, high or low  | U - 2 <sup>(1)</sup> | U + 2 <sup>(1)</sup> | ns   |
| 3   | $t_{w(RTS)}$ | Pulse width, transmit start bit, high or low | U - 2 <sup>(1)</sup> |                      | ns   |

(1) U = UART baud time = 1/Programmed baud rate

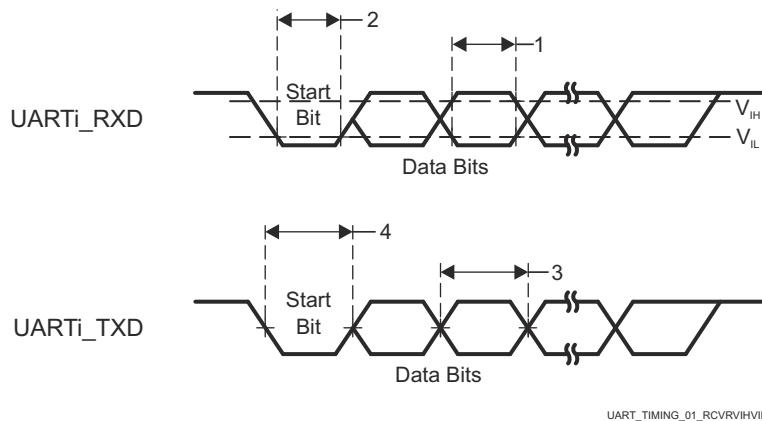


Figure 6-114. UART Timing

For more information, see *Universal Asynchronous Receiver/Transmitter (UART)* section in *Peripherals* chapter in the device TRM.

### 6.10.5.22 USB

The USB 2.0 subsystem is compliant with the Universal Serial Bus (USB) Specification, revision 2.0. Refer to the specification for timing details.

The USB 3.1 GEN1 Dual-Role Device Subsystem is compliant with the Universal Serial Bus (USB) 3.1 Specification, revision 1.0. Refer to the specification for timing details.

For more details about features and additional description information on the device Universal Serial Bus Subsystem (USB), see the corresponding sections within [Section 5.3, Signal Descriptions](#) and [Section 7, Detailed Description](#).

For more information, see *Universal Serial Bus (USB) Subsystem* section in *Peripherals* chapter in the device TRM.

## 6.10.6 Emulation and Debug

### 6.10.6.1 Debug Trace

[Table 6-87](#) represents Debug Trace timing conditions.

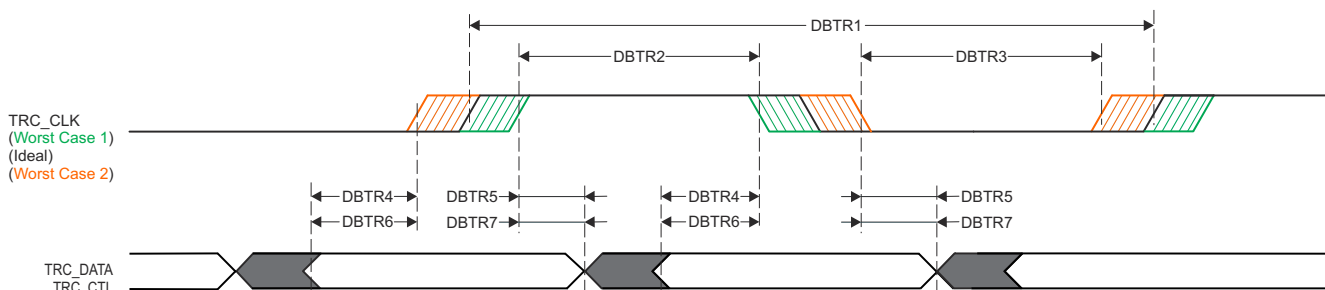
**Table 6-86. Debug Trace Timing Conditions**

| PARAMETER                            |  | MIN | MAX | UNIT |
|--------------------------------------|--|-----|-----|------|
| <b>Output Conditions</b>             |  |     |     |      |
| $C_L$                                | Output load capacitance                      | 2   | 5   | pF   |
| <b>PCB CONNECTIVITY REQUIREMENTS</b> |  |     |     |      |
| $t_d(\text{Trace Mismatch})$         | Propagation delay mismatch across all traces |     | 200 | ps   |

Table 6-87 and Figure 6-115 assume testing over the recommended operating conditions and electrical characteristic conditions.

**Table 6-87. Debug Trace Switching Characteristics**

| NO.               | PARAMETER                             | DESCRIPTION  | MIN  | MAX | UNIT |
|-------------------|---------------------------------------|--|------|-----|------|
| <b>1.8 V Mode</b> |                                       |  |      |     |      |
| DBTR1             | $t_c(\text{TRC\_CLK})$                | Cycle time, TRC_CLK                                | 6.50 |     | ns   |
| DBTR2             | $t_w(\text{TRC\_CLKH})$               | Pulse width, TRC_CLK high                          | 2.50 |     | ns   |
| DBTR3             | $t_w(\text{TRC\_CLKL})$               | Pulse width, TRC_CLK low                           | 2.50 |     | ns   |
| DBTR4             | $t_{osu}(\text{TRC\_DATAV-TRC\_CLK})$ | Output setup time, TRC_DATA valid to TRC_CLK edge  | 0.81 |     | ns   |
| DBTR5             | $t_{oh}(\text{TRC\_CLK-TRC\_DATAI})$  | Output hold time, TRC_CLK edge to TRC_DATA invalid | 0.81 |     | ns   |
| DBTR6             | $t_{osu}(\text{TRC\_CTLV-TRC\_CLK})$  | Output setup time, TRC_CTL valid to TRC_CLK edge   | 0.81 |     | ns   |
| DBTR7             | $t_{oh}(\text{TRC\_CLK-TRC\_CTLI})$   | Output hold time, TRC_CLK edge to TRC_CTL invalid  | 0.81 |     | ns   |
| <b>3.3 V Mode</b> |                                       |  |      |     |      |
| DBTR1             | $t_c(\text{TRC\_CLK})$                | Cycle time, TRC_CLK                                | 9.75 |     | ns   |
| DBTR2             | $t_w(\text{TRC\_CLKH})$               | Pulse width, TRC_CLK high                          | 4.13 |     | ns   |
| DBTR3             | $t_w(\text{TRC\_CLKL})$               | Pulse width, TRC_CLK low                           | 4.13 |     | ns   |
| DBTR4             | $t_{osu}(\text{TRC\_DATAV-TRC\_CLK})$ | Output setup time, TRC_DATA valid to TRC_CLK edge  | 1.22 |     | ns   |
| DBTR5             | $t_{oh}(\text{TRC\_CLK-TRC\_DATAI})$  | Output hold time, TRC_CLK edge to TRC_DATA invalid | 1.22 |     | ns   |
| DBTR6             | $t_{osu}(\text{TRC\_CTLV-TRC\_CLK})$  | Output setup time, TRC_CTL valid to TRC_CLK edge   | 1.22 |     | ns   |
| DBTR7             | $t_{oh}(\text{TRC\_CLK-TRC\_CTLI})$   | Output hold time, TRC_CLK edge to TRC_CTL invalid  | 1.22 |     | ns   |



SPRSP08\_Debug\_01

**Figure 6-115. Debug Trace Timing**

**6.10.6.2 IEEE 1149.1 Standard–Test–Access Port (JTAG)**

For more details about features and additional description information on the device IEEE 1149.1 Standard–Test–Access Port, see the corresponding sections within [Section 5.3, Signal Descriptions](#) and [Section 7, Detailed Description](#).

Table 6-88 represents JTAG timing conditions.

**Note**

The JTAG signals are split across two IO power domains on the device. Timings parameters defined in this section only apply when the two IO power domains are operating at the same voltage and level-shifters are not inserted into the signal path. Values for the following timing parameters are not defined when operating the two IO power domains at different voltages since propagation delay through the device IO buffers differ when some are operating at 1.8V while others are operating at 3.3V. This effectively reduces timing margin beyond the values defined in this section. The JTAG interface is still expected to function when the two IO power domains are operated at different voltages, assuming the system designer has implemented appropriate level-shifters and the operating frequency is reduced to accommodate additional delay inserted by the level-shifters and IO buffers operating at different voltages

**Table 6-88. JTAG Timing Conditions**

| PARAMETER                            |  | MIN  | MAX                 | UNIT |
|--------------------------------------|--|------|---------------------|------|
| <b>Input Conditions</b>              |  |      |                     |      |
| $t_{SR}$                             | Input slew rate                              | 0.50 | 2.00                | V/ns |
| <b>Output Conditions</b>             |  |      |                     |      |
| $C_L$                                | Output load capacitance                      | 5    | 15                  | pF   |
| <b>PCB CONNECTIVITY REQUIREMENTS</b> |  |      |                     |      |
| $t_d(\text{Trace Delay})$            | Propagation delay of each trace              | 83.5 | 1000 <sup>(1)</sup> | ps   |
| $t_d(\text{Trace Mismatch Delay})$   | Propagation delay mismatch across all traces |      | 100                 | ps   |

- (1) Maximum propagation delay associated with the JTAG signal traces has a significant impact on maximum TCK operating frequency. It may be possible to increase the trace delay beyond this value, but the operating frequency of TCK must be reduced to account for the additional trace delay.

**6.10.6.2.1 JTAG Electrical Data and Timing**

Section 6.10.6.2.1.1, Section 6.10.6.2.1.2, and Figure 6-116 assume testing over the recommended operating conditions and electrical characteristic conditions.

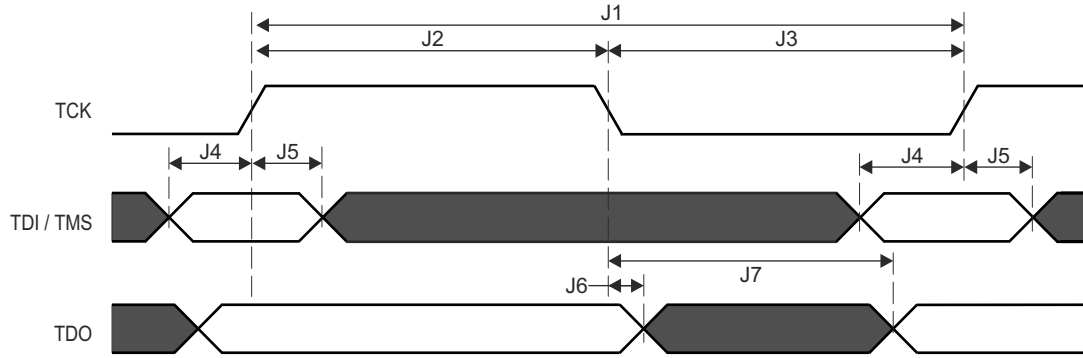
**6.10.6.2.1.1 Timing Requirements for IEEE 1149.1 JTAG**

| NO. | PARAMETER                | DESCRIPTION                                      | MIN                 | MAX | UNIT |
|-----|--------------------------|--|---------------------|-----|------|
| J1  | $t_c(\text{TCK})$        | Cycle time minimum, TCK                          | 46.5 <sup>(1)</sup> |     | ns   |
| J2  | $t_w(\text{TCKH})$       | Pulse width minimum, TCK high                    | 0.4P <sup>(2)</sup> |     | ns   |
| J3  | $t_w(\text{TCKL})$       | Pulse width minimum, TCK low                     | 0.4P <sup>(2)</sup> |     | ns   |
| J4  | $t_{su}(\text{TDI-TCK})$ | Input setup time minimum, TDI valid to TCK high  | 4.5                 |     | ns   |
|     | $t_{su}(\text{TMS-TCK})$ | Input setup time minimum, TMS valid to TCK high  | 4.5                 |     | ns   |
| J5  | $t_h(\text{TCK-TDI})$    | Input hold time minimum, TDI valid from TCK high | 2                   |     | ns   |
|     | $t_h(\text{TCK-TMS})$    | Input hold time minimum, TMS valid from TCK high | 2                   |     | ns   |

- (1) The maximum TCK operating frequency assumes the following timing requirements and switching characteristics for the attached debugger. The operating frequency of TCK must be reduced to provide appropriate timing margin if the debugger exceeds any of these assumptions.
- Minimum TDO setup time of 4.6 ns relative to the rising edge of TCK
  - TDI and TMS output delay in the range of -16.5 ns to 14.0 ns relative to the falling edge of TCK
- (2) P = TCK cycle time in ns

**6.10.6.2.1.2 Switching Characteristics Over Recommended Operating Conditions for IEEE 1149.1 JTAG**

| NO. | PARAMETER               | DESCRIPTION                                | MIN | MAX | UNIT |
|-----|-------------------------|--|-----|-----|------|
| J6  | $t_d(\text{TCKL-TDOI})$ | Delay time minimum, TCK low to TDO invalid | 0   |     | ns   |
| J7  | $t_d(\text{TCKL-TDOV})$ | Delay time maximum, TCK low to TDO valid   |     | 12  | ns   |



**Figure 6-116. JTAG Test-Port Timing**

## 7 Detailed Description

### 7.1 Overview

Jacinto™ DRA821x processors, based on the Armv8 64-bit architecture, are System-on-Chip (SoCs) that provide lower system cost through integration of features including system MCU, Ethernet switch, safety, security. Multi-core system enables ECU consolidation for automotive applications such as automotive gateway and vehicle compute systems. The integrated diagnostics and functional safety features are targeted to ASIL-D certification/requirements. The Integrated Microcontroller (MCU) island eliminates the need for an external system MCU. In addition to the PCIe hub, the device features up to four Gigabit Ethernet ports with integrated switch to meet networking use cases that require heavy data bandwidth and also includes PCIe hub functionality. Twenty CAN-FD and up to twelve UART interfaces are available on the device. Up to four general purpose Arm® Cortex®-R5F subsystems can handle low level, timing critical processing tasks and leave the Arm® Cortex®-A72's unencumbered for advanced applications.

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#### Note

For more information on features, subsystems, and architecture of superset device System on Chip (SoC), see the device TRM.

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## 7.2 Processor Subsystems

### 7.2.1 Arm Cortex-A72

The device implements one dual-core Arm® Cortex®-A72 MPU, which is integrated inside the Compute Cluster, along with other modules. The Cortex-A72 cores are general-purpose processors that can be used for running customer applications.

The A72SS is built around the Arm Cortex-A72 MPCore (A72 cluster), which is provided by Arm and configured by TI. It is based on the symmetric multiprocessor (SMP) architecture, and thus it delivers high performance and optimal power management and debug capabilities.

The A72 processor is a multi-issue out-of-order superscalar execution engine with integrated L1 instruction and data caches, compatible with Armv8-A architecture. The Armv8-A architecture brings a number of new features. These include 64-bit data processing, extended virtual addressing and 64-bit general purpose registers.

For more information, see *Dual-A72 MPU Subsystem* section in *Processors and Accelerators* chapter in the device TRM.

### 7.2.2 Arm Cortex-R5F

The MCU\_ARMSS is a dual-core implementation of the Arm® Cortex®-R5F processor configured for split/lock operation. It also includes accompanying memories (L1 caches and tightly-coupled memories), standard Arm® CoreSight™ debug and trace architecture, integrated Vectored Interrupt Manager (VIM), ECC Aggregators, and various wrappers for protocol conversion and address translation for easy integration into the SoC.

For more information, see *Dual-R5F MCU Subsystem* section in *Processors and Accelerators* chapter in the device TRM.

## 7.3 Other Subsystems

### 7.3.1 MSMC

The Multicore Shared Memory Controller (MSMC) forms the heart of the compute cluster (COMPUTE\_CLUSTER0) providing high-bandwidth resource access both to and from all of the connected processing elements and the rest of the system. MSMC serves as the data-movement backbone of the compute cluster.

For more information, see *Multicore Shared Memory Controller (MSMC)* section in *Device Configuration* chapter in the device TRM.

### 7.3.2 NAVSS

#### 7.3.2.1 NAVSS0

Main SoC Navigator Subsystem (NAVSS0) consists of DMA/Queue Management components – UDMA and Ring Accelerator (UDMASS), Peripherals (Module subsystem [MODSS]), Virtualization translation (VirtSS), and a North Bridge (NBSS).

#### 7.3.2.2 MCU\_NAVSS

MCU Navigator Subsystem (MCU NAVSS) has a subset of the modules of the main NAVSS and is instantiated in the MCU domain.

MCU Navigator Subsystem consists of DMA/Queue Management components – UDMA and Ring Accelerator (UDMASS), and Peripherals (Module subsystem [MODSS]).

For more information, see *Main Navigator Subsystem (NAVSS)* and *MCU Navigator Subsystem (MCU NAVSS)* sections in *Data Movement Architecture (DMA)* chapter in the device TRM.

### 7.3.3 PDMA Controller

The Peripheral DMA is a simple DMA which has been architected to specifically meet the data transfer needs of peripherals, which perform data transfers using memory mapped registers accessed via a standard non-coherent bus fabric. The PDMA module is intended to be located close to one or more peripherals which

require an external DMA for data movement and is architected to reduce cost by using VBUSP interfaces and supporting only statically configured Transfer Request (TR) operations.

The PDMA is only responsible for performing the data movement transactions which interact with the peripherals themselves. Data which is read from a given peripheral is packed by a PDMA source channel into a PSI-L data stream which is then sent to a remote peer UDMA-P destination channel which then performs the movement of the data into memory. Likewise, a remote UDMA-P source channel fetches data from memory and transfers it to a peer PDMA destination channel over PSI-L which then performs the writes to the peripheral.

The PDMA architecture is intentionally heterogeneous (UDMA-P + PDMA) to right size the data transfer complexity at each point in the system to match the requirements of whatever is being transferred to or from. Peripherals are typically FIFO based and do not require multi-dimensional transfers beyond their FIFO dimensioning requirements, so the PDMA transfer engines are kept simple with only a few dimensions (typically for sample size and FIFO depth), hardcoded address maps, and simple triggering capabilities.

Multiple source and destination channels are provided within the PDMA which allow multiple simultaneous transfer operations to be ongoing. The DMA controller maintains state information for each of the channels and employs round-robin scheduling between channels in order to share the underlying DMA hardware.

For more information, see *PDMA Controller* section in *DMA Controllers* chapter in the device TRM.

### **7.3.4 Peripherals**

#### **7.3.4.1 ADC**

The Analog-to-Digital Converter (ADC) module contains a single 12-bit ADC which can be multiplexed to any 1 of 8 analog inputs (channels).

For more information, see *Analog-to-Digital Converter (ADC)* section in *Peripherals* chapter in the device TRM.

#### **7.3.4.2 ATL**

The Audio Tracking Logic (ATL) is used by HD Radio™ applications to synchronize the digital audio output to the baseband clock. This same IP can also be used generically to track errors between two reference signals (such as frame syncs) and generate a modulated clock output (using software-controlled cycle stealing) which averages to some desired frequency. This process can be used as a hardware assist for asynchronous sample rate conversion algorithms.

For more information, see *Audio Tracking Logic (ATL)* section in *Peripherals* chapter in the device TRM.

#### **7.3.4.3 CPSW2G**

The two-port Gigabit Ethernet MAC (MCU\_CPSW0) subsystem provides Ethernet packet communication for the device and is configured in a similar manner as an Ethernet switch. MCU\_CPSW0 features the Reduced Gigabit Media Independent Interface (RGMII), Reduced Media Independent Interface (RMII), and the Management Data Input/Output (MDIO) interface for physical layer device (PHY) management.

For more information, see *Gigabit Ethernet Switch (CPSW0)* section in *Peripherals* chapter in the device TRM.

#### **7.3.4.4 CPSW5G**

The 5-port Gigabit Ethernet Switch (CPSW0) subsystem provides Ethernet packet communication for the device and can be configured as an Ethernet switch. CPSW0 features the 1G and 2.5G Serial Gigabit Media Independent Interface (SGMII), Universal Serial 10G Media Independent Interface (USXGMII), 10G Form-factor Interface (XFI), Reduced Gigabit Media Independent Interface (RGMII), Reduced Media Independent Interface (RMII) and the Management Data Input/Output (MDIO) interface for physical layer device (PHY) management.

For more information, see *Gigabit Ethernet Switch (MCU\_CPSW0)* section in *Peripherals* chapter in the device TRM.

#### **7.3.4.5 DCC**

The Dual Clock Comparator (DCC) is used to determine the accuracy of a clock signal during the time execution of an application. Specifically, the DCC is designed to detect drifts from the expected clock frequency.

The desired accuracy can be programmed based on calculation for each application. The DCC measures the frequency of a selectable clock source using another input clock as a reference.

For more information, see *Dual Clock Comparator (DCC)* section in *Peripherals* chapter in the device TRM.

#### 7.3.4.6 DDRSS

The DDR subsystem in this device comprises DDR controller, DDR PHY and wrapper logic to integrate these blocks in the device. The DDR subsystem is referred to as DDRSS0 and is used to provide an interface to external SDRAM devices which can be utilized for storing program or data. Specifically, the DDR subsystem supports LPDDR4 devices compliant to the JEDEC JESD209-4B standard. DDRSS0 is accessed via MSMC, and not directly through the system interconnect.

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#### Note

The DDRSS does not support byte mode LPDDR4 memories, or memories with more than 17 row address bits.

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For more information, see *DDR Subsystem (DDRSS)* section in *Peripherals* chapter in the device TRM.

#### 7.3.4.7 ECAP

The enhanced Capture (ECAP) module can be used for:

- Sample rate measurements of audio inputs
- Speed measurements of rotating machinery (for example, toothed sprockets sensed via Hall sensors)
- Elapsed time measurements between position sensor pulses
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors.

For more information, see *Enhanced Capture (ECAP) Module* section in *Peripherals* chapter in the device TRM.

#### 7.3.4.8 EPWM

An effective PWM peripheral must be able to generate complex pulse width waveforms with minimal CPU overhead or intervention. It needs to be highly programmable and very flexible while being easy to understand and use. The EPWM unit described here addresses these requirements by allocating all needed timing and control resources on a per PWM channel basis. Cross coupling or sharing of resources has been avoided; instead, the EPWM is built up from smaller single channel modules with separate resources and that can operate together as required to form a system. This modular approach results in an orthogonal architecture and provides a more transparent view of the peripheral structure, helping users to understand its operation quickly.

In the further description the letter x within a signal or module name is used to indicate a generic EPWM instance on a device. For example, output signals EPWMxA and EPWMxB refer to the output signals from the EPWM\_x instance. Thus, EPWM1A and EPWM1B belong to EPWM1, EPWM2A and EPWM2B belong to EPWM2, and so forth.

Additionally, the EPWM integration allows this synchronization scheme to be extended to the capture peripheral modules (ECAP). The number of modules is device-dependent and based on target application needs. Modules can also operate stand-alone.

For more information, see *Enhanced Pulse Width Modulation (EPWM) Module* section in *Peripherals* chapter in the device TRM.

#### 7.3.4.9 ELM

The Error Location Module (ELM) is used with the GPMC. Syndrome polynomials generated on-the-fly when reading a NAND flash page and stored in GPMC registers are passed to the ELM. A host processor can then correct the data block by flipping the bits to which the ELM error-location outputs point.

When reading from NAND flash memories, some level of error-correction is required. In the case of NAND modules with no internal correction capability, sometimes referred to as *bare NANDs*, the correction process is delegated to the memory controller. ELM can be also used to support parallel NOR flash or NAND flash.

For more information, see *Error Location Module (ELM)* section in *Peripherals* chapter in the device TRM.

#### **7.3.4.10 ESM**

The Error Signaling Module (ESM) aggregates events and/or errors from throughout the device into one location. It can signal both low and high priority interrupts to a processor to deal with an event and/or manipulate an I/O error pin to signal an external hardware that an error has occurred. Therefore an external controller is able to reset the device or keep the system in a safe, known state.

For more information, see *Error Signaling Module (ESM)* section in *Peripherals* chapter in the device TRM.

#### **7.3.4.11 EQEP**

The Enhanced Quadrature Encoder Pulse (EQEP) peripheral is used for direct interface with a linear or rotary incremental encoder to get position, direction and speed information from a rotating machine for use in high performance motion and position control system. The disk of an incremental encoder is patterned with a single track of slots patterns. These slots create an alternating pattern of dark and light lines. The disk count is defined as the number of dark/light line pairs that occur per revolution (lines per revolution). As a rule, a second track is added to generate a signal that occurs once per revolution (index signal: QEPI), which can be used to indicate an absolute position. Encoder manufacturers identify the index pulse using different terms such as index, marker, home position and zero reference.

For more information, see *Enhanced Quadrature Encoder Pulse (EQEP) Module* section in *Peripherals* chapter in the device TRM.

#### **7.3.4.12 GPIO**

The General-Purpose Input/Output (GPIO) peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an output, the user can write to an internal register to control the state driven on the output pin. When configured as an input, user can obtain the state of the input by reading the state of an internal register.

In addition, the GPIO peripheral can produce host CPU interrupts and DMA synchronization events in different interrupt/event generation modes.

For more information, see *General-Purpose Interface (GPIO)* section in *Peripherals* chapter in the device TRM.

#### **7.3.4.13 GPMC**

The General-Purpose Memory Controller is a unified memory controller dedicated for interfacing with external memory devices like:

- Asynchronous SRAM-like memories and application-specific integrated circuit (ASIC) devices
- Asynchronous, synchronous, and page mode (available only in non-multiplexed mode) burst NOR flash devices
- NAND flash
- Pseudo-SRAM devices

For more information, see *General-Purpose Memory Controller (GPMC)* section in *Peripherals* chapter in the device TRM.

#### **7.3.4.14 Hyperbus**

The Hyperbus module is a part in the device Flash Subsystem (FSS).

The Hyperbus module is a low pin count memory interface that provides high read/write performance. The Hyperbus module connects to Hyperbus memory (HyperFlash or HyperRAM) and uses simple Hyperbus protocol for read and write transactions.

There is one Hyperbus™ module inside the device. The Hyperbus module includes one Hyperbus Memory Controller (HBMC).

For more information, see *Hyperbus Interface* section in *Peripherals* chapter in the device TRM.

#### 7.3.4.15 I2C

The device contains ten multimaster Inter-Integrated Circuit (I2C) controllers each of which provides an interface between a local host (LH), such as an Arm or a Digital Signal Processor (DSP), and any I<sup>2</sup>C-bus-compatible device that connects via the I<sup>2</sup>C serial bus. External components attached to the I<sup>2</sup>C bus can serially transmit and receive up to 8 bits of data to and from the LH device through the 2-wire I<sup>2</sup>C interface.

Each multimaster I2C module can be configured to act like a slave or master I<sup>2</sup>C-compatible device.

The WKUP\_I2C0, MCU\_I2C0, I2C0, and I2C1 controllers have dedicated I<sup>2</sup>C compliant open drain buffers, and support high speed mode (up to 3.4 Mbps in 1.8 V mode and up to 400 kbps in 3.3 V mode). The MCU\_I2C1, I2C2, I2C3, I2C4, I2C5, and I2C6 controllers are multiplexed with standard LVCMOS I/O, connected to emulate open drain, and support fast mode (up to 400 kbps in 1.8 V/3.3 V mode). The I2C emulation is achieved by configuring the LVCMOS buffers to output Hi-Z instead of driving high when transmitting logic 1.

For more information, see *Inter-Integrated Circuit (I2C) Interface* section in *Peripherals* chapter in the device TRM.

#### 7.3.4.16 I3C

The device contains three Improved Inter-Integrated Circuit (I3C) controllers each of which provides an interface between a local host (LH), such as an Arm, and any I3C-bus-compatible device that connects via the I3C serial bus.

For more information, see *Improved Inter-Integrated Circuit (I3C) Interface* section in *Peripherals* chapter in the device TRM.

#### 7.3.4.17 MCAN

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control. CAN has high immunity to electrical interference. In a CAN network, many short messages are broadcast to the entire network, which provides for data consistency in every node of the system.

The MCAN module supports both classic CAN and CAN FD (CAN with Flexible Data-Rate) specifications. CAN FD feature allows high throughput and increased payload per data frame. The classic CAN and CAN FD devices can coexist on the same network without any conflict.

For more information, see *Modular Controller Area Network (MCAN)* section in *Peripherals* chapter in the device TRM.

#### 7.3.4.18 MCASP

The MCASP functions as a general-purpose audio serial port are optimized to the requirements of various audio applications. The MCASP module can operate in both transmit and receive modes. The MCASP is useful for time-division multiplexed (TDM) stream, Inter-IC Sound (I2S) protocols reception and transmission as well as for an inter-component digital audio interface transmission (DIT). The MCASP has the flexibility to gluelessly connect to a Sony/Philips digital interface (S/PDIF) transmit physical layer component.

Although inter-component digital audio interface reception (DIR) mode (this is, S/PDIF stream receiving) is not natively supported by the MCASP module, a specific TDM mode implementation for the MCASP receivers allows an easy connection to external DIR components (for example, S/PDIF to I2S format converters).

For more information, see *Multichannel Audio Serial Port (MCASP)* section in *Peripherals* chapter in the device TRM.

#### 7.3.4.19 MCRC Controller

VBUSM CRC controller is a module which is used to perform CRC (Cyclic Redundancy Check) to verify the integrity of a memory system. A signature representing the contents of the memory is obtained when the contents of the memory are read into MCRC Controller. The responsibility of MCRC controller is to calculate the signature for a set of data and then compare the calculated signature value against a predetermined good signature value. MCRC controller provides four channels to perform CRC calculation on multiple memories in

parallel and can be used on any memory system. Channel 1 can also be put into data trace mode, where MCRC controller compresses each data being read through CPU read data bus.

For more information, see *MCRC Controller* section in *Interprocessor Communication* chapter in the device TRM.

#### **7.3.4.20 MCSPI**

The MCSPI module is a multichannel transmit/receive, master/slave synchronous serial bus.

There are total of eleven MCSPI modules in the device.

For more information, see *Multichannel Serial Peripheral Interface (MCSPI)* section in *Peripherals* chapter in the device TRM.

#### **7.3.4.21 MMC/SD**

The MMCS Host Controller provides an interface to eMMC 5.1 (embedded MultiMedia Card), SD 4.10 (Secure Digital), and SDIO 4.0 (Secure Digital IO) devices. The MMCS Host Controller deals with MMC/SD/SDIO protocol at transmission level, data packing, adding cyclic redundancy checks (CRCs), start/end bit insertion, and checking for syntactical correctness.

For more information, see *Multimedia Card/Secure Digital (MMC/SD) Interface* section in *Peripherals* chapter in the device TRM.

#### **7.3.4.22 OSPI**

The Octal Serial Peripheral Interface (OSPI™) module is a kind of Serial Peripheral Interface (SPI) module which allows single, dual, quad or octal read and write access to external flash devices.

The OSPI module is used to transfer data, either in a memory mapped direct mode (for example a processor wishing to execute code directly from external flash memory), or in an indirect mode where the module is set-up to silently perform some requested operation, signaling its completion via interrupts or status registers.

For more information, see *Octal Serial Peripheral Interface (OSPI)* section in *Peripherals* chapter in the device TRM.

#### **7.3.4.23 PCIE**

The Peripheral Component Interconnect Express (PCIe) subsystem is built around a multi-lane dual-mode PCIe controller that provides low pin-count, high reliability, and high-speed data transfers at rates of up to 8.0 Gbps per lane for serial links on backplanes and printed wiring boards.

For more information, see *Peripheral Component Interconnect Express (PCIe) Subsystem* section in *Peripherals* chapter in the device TRM.

#### **7.3.4.24 SerDes**

SerDes'es goal is to convert device (SoC) parallel data into serialized data that can be output over a highspeed electrical interface. In the opposite direction, SerDes converts high-speed serial data into parallel data that can be processed by the device. To this end, the SerDes contains a variety of functional blocks to handle both the external analog interface as well as the internal digital logic.

For more information, see *Serializer/Deserializer (SerDes)* section in *Peripherals* chapter in the device TRM.

#### **7.3.4.25 WWDT**

The Windowed Watchdog Timer provides timer functionality for operating systems and for benchmarking code. The module incorporates several counters, which define the timebases needed for scheduling in the operating system. The module is implemented with an RTI module, but only WWDT is supported.

This module is specifically designed to fulfill the requirements for OSEK (“Offene Systeme und deren Schnittstellen für die Elektronik im Kraftfahrzeug”; “Open Systems and the Corresponding Interfaces for Automotive Electronics”) as well as OSEK/Time compliant operating systems.

For more information, see *Real Time Interrupt (RTI) Module* section in *Peripherals* chapter in the device TRM.

#### 7.3.4.26 Timers

All timers include specific functions to generate accurate tick interrupts to the operating system.

Each timer can be clocked from several different independent clocks. The selection of clock source is made from registers in the MCU\_CTRL\_MMR0/CTRL\_MMR0.

In the MCU domain the device provides 10 timer pins to be used as MCU Timer Capture inputs or as MCU Timer PWM outputs. In order to provide maximum flexibility, these 10 pins may be used with any of MCU\_TIMER0 through MCU\_TIMER9 instances. System level muxes are used to control the capture source pin for each MCU\_TIMER[9-0] and the MCU\_TIMER[9-0] source for each MCU\_TIMER\_IO[9-0] PWM output.

In the MAIN domain the device provides 8 timer pins to be used as Timer Capture inputs or as Timer PWM outputs. For maximum flexibility, these 8 pins may be used with any of TIMER0 through TIMER19 instances. System level muxes are used to control the capture source pin for each TIMER[19-0] and the TIMER[19-0] source for each TIMER\_IO[7-0] PWM output.

Each odd numbered timer instance from each of the domains may be optionally cascaded with the previous even numbered timer instance from the same domain to form up to a 64-bit timer. For example, TIMER1 may be cascaded to TIMER0, MCU\_TIMER1 may be cascaded to MCU\_TIMER0, etc.

When cascaded, TIMER<sub>i</sub> acts as a 32-bit prescaler to TIMER<sub>i+1</sub>, as well as MCU\_TIMER<sub>n</sub> acts as a 32-bit prescaler to MCU\_TIMER<sub>n+1</sub>. TIMER<sub>i</sub> / MCU\_TIMER<sub>n</sub> must be configured to generate a PWM output edge at the desired rate to increment the TIMER<sub>i+1</sub> / MCU\_TIMER<sub>n+1</sub> counter.

For more information, see *Timers* section in *Peripherals* chapter in the device TRM.

#### 7.3.4.27 UART

The UART is a slave peripheral that utilizes the DMA for data transfer or interrupt polling via host CPU. There are twelve UART modules in the device. All UART modules support IrDA and CIR modes when 48 MHz function clock is used. Each UART can be used for configuration and data exchange with a number of external peripheral devices or interprocessor communication between devices.

For more information, see *Universal Synchronous/Asynchronous Receiver/Transmitter (UART)* section in *Peripherals* chapter in the device TRM.

#### 7.3.4.28 USB

Similar to earlier versions of USB bus, USB 3.0 is a general-purpose cable bus, supporting data exchange between a host device and a wide range of simultaneously accessible peripherals.

The device supports one USB subsystem:

- USB3SS0 is SuperSpeed (SS) USB 3.0 Dual-Role-Device (DRD) subsystem with on-chip SS (USB3.0) PHY and HS/FS/LS (1) (USB2.0) PHY

For more information, see *Universal Serial Bus (USB) Subsystem* section in *Peripherals* chapter in the device TRM.

## 8 Applications, Implementation, and Layout

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### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test design implementation to confirm system functionality.

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### 8.1 Power Supply Mapping

TPS6594x and LP8764x are the Power Management ICs (PMIC) that should be used for Power Distribution Network (PDN) designs to support this device. TI requires use of these PMICs for the following reasons:

- TI has validated their use with the Device
- Board level margins including transient response and output accuracy are analyzed and optimized for the entire system
- Support for power sequencing requirements (refer to [Section 6.10.2, Power Supply Sequences](#))
- Support for Adaptive Voltage Scaling (AVS) Class 0 requirements, including TI provided software

When combining device voltage domains into a common power rail is allowed, the most stringent voltage domain PDN guideline must be implemented for the common power rail.

It is possible that some device voltage domains may be unused in some systems. In such cases, all unused voltage domain supply pins must still be connected to a valid power rail with a proper voltage level in order to ensure device reliability (refer to Section 4.3, Signal Descriptions). For example, if MCU is not used, then vdd\_mcu domain can be combined with the CORE domain (vdd\_core) that has the same voltage specifications. A buck converter power stage connected to the common power rail would then supply both CORE and MCU domains.

For the combined rail, the following relaxations apply:

- The AVS voltage of active rail in the combined rail needs to be used to set the power supply
- The decoupling capacitance should be set according to the active rail in the combined rail

[Figure 8-1](#) shows an example of the detailed power mapping between the processor and TPS659414-Q1 and LP876441-Q1 PMICs. In this configuration, both PMIC devices use a 3.3V input voltage. For more details, refer to the appnote titled "[User's Guide for Powering DRA821 with the TPS6594-Q1 and LP8764-Q1 PMICs](#)".

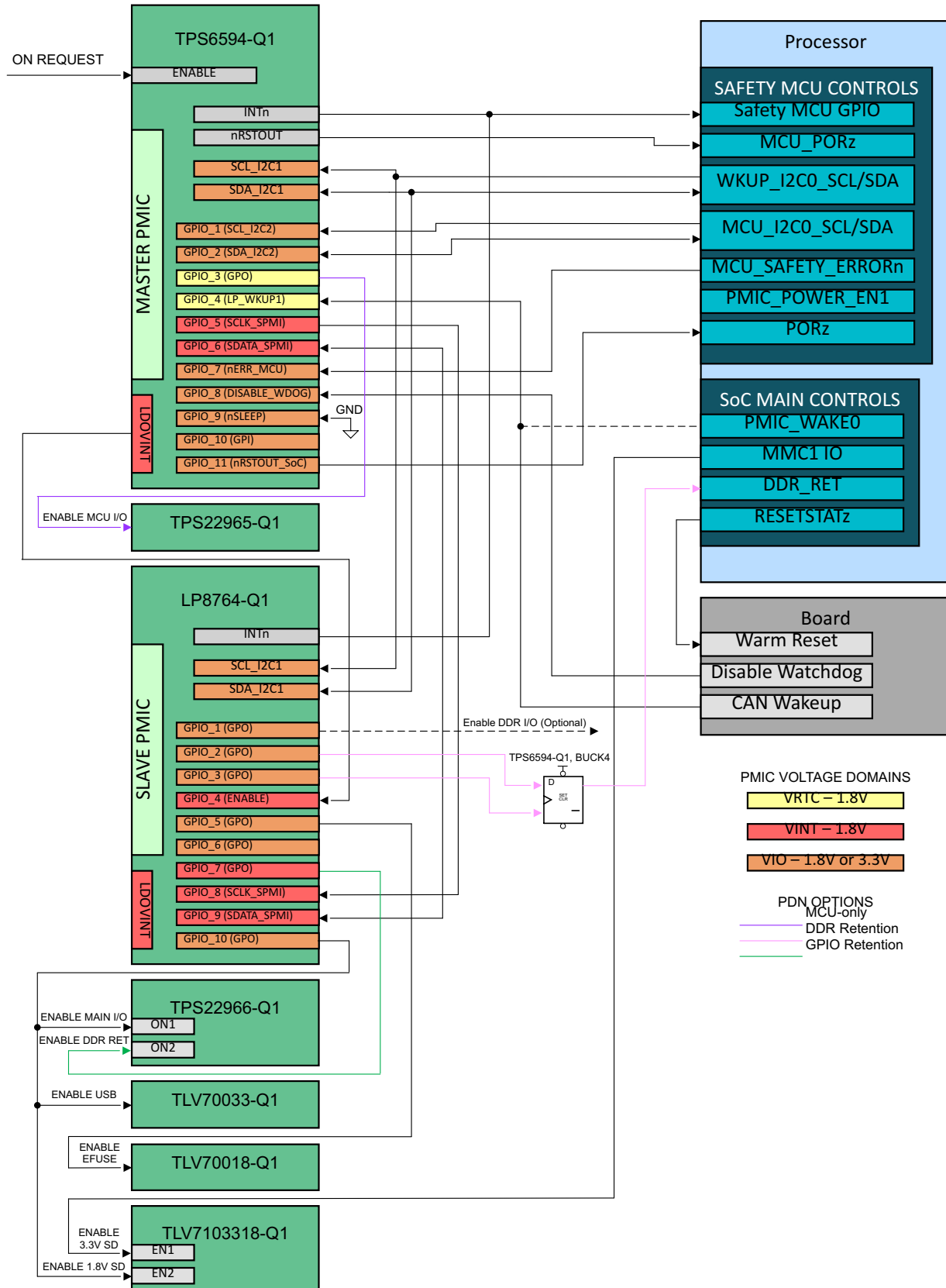


Figure 8-1. TPS6594-Q1 and LP8764-Q1 Digital Connections

**Table 8-1. Combined MCU and Main Voltage Domain Power Rail Mapping**

| TYPES                    | VOLTAGE [V] | DOMAIN NAMES  | DOMAIN TYPES  | POWER RAILS                    | # |
|--------------------------|-------------|---|---|--------------------------------|---|
| Digital IO               | 3.3         | (VDDSHV0_MCU, VDDSHV1_MCU, VDDSHV2_MCU, VDDSHV0, VDDSHV2, VDDSHV5 <sup>(3)</sup> ) <sup>(1)</sup> , VDDA_3P3_USB <sup>(4)</sup>   | VDDSHVn_MCU, VDDSHVn, VDDA_3P3_USB <sup>(1)</sup>                   | VDD_IO_3V3                     | 1 |
| Digital IO               | 1.8         | (VDDSHV0_MCU, VDDSHV1_MCU, VDDSHV2_MCU, VDDSHV0, VDDSHV2, VDDSHV5 <sup>(3)</sup> ) <sup>(2)</sup> , VDDS_MMC0   | VDDSHVn_MCU3 VDDSHVn <sup>(2), (3)</sup>                            | VDD_IO_1V8                     | 2 |
| Analog PHY               | 1.8         | (VDDA_MCU_PLLGRP0, VDDA_MCU_TEMP, VDDA_ADC_MCU, VDDA_POR_WKUP, VDDA_WKUP, VDDA_OSC1, VDDA_PLLGRP8,6,4,0, VDDA_TEMP1:0) <sup>(5)</sup> , VDDA_1P8_USB, VDDA_1P8_SERDES) <sup>(6)</sup> | VDDA_1P8_<clk/meas> <sup>(5)</sup><br>VDDA_1P8_<phy> <sup>(6)</sup> | VDA_LN_1V8 <sup>(6), (7)</sup> | 3 |
| Analog, low voltage      | 0.80        | (VDDA_0P8_PLL_DDR, VDDA_0P8_DLL_MMC0) <sup>(7)</sup>  | VDDA_0P8_DPLL   | VDA_DPLL_0V8                   | 4 |
| Digital, AVS low voltage | 0.77 – 0.84 | VDD_CPU   | VDD_CPU   | VDD_CPU_AVS                    | 5 |
| Digital, low voltage     | 0.80        | VDD_MCU9, VDD_MCU_WAKE1, VDD_CORE, VDD_WAKE0, (VDDA_0P8_SERDES, VDDA_0P8_USB)   | VDD_MCU<br>VDD_CORE<br>VDDA_0P8_<phy>                               | VDD_CORE_0V8                   | 6 |
| Digital, low voltage     | 0.85        | VDDAR_MCU, VDDAR_CORE, VDDAR_CPU  | VDDAR   | VDD_RAM_0V85                   | 7 |
| Digital, low voltage     | 1.1         | VDDS_DDR_BIAS, VDDS_DDR, VDDS_DDR_C   | VDDS_DDR  | VDD_DDR_1V1                    | 8 |

- (1) Any MCU or Main dual voltage IO domains (VDDSHVn\_MCU or VDDSHVn) being supplied by 3.3V to support 3.3V digital interfaces
- (2) Any MCU or Main dual voltage IO domains (VDDSHVn\_MCU or VDDSHVn) being supplied by 1.8V to support 1.8V digital interfaces
- (3) VDDSHV5 supports MMC1 signaling for SD memory cards. A dual voltage (3.3/1.8V) power rail is required for compliant, high-speed SD card operations. If SD card is not needed or standard data rates with fixed 3.3V operation is acceptable, then domain can be grouped with digital IO 3.3V power rail. If a SD card is capable of operating with fixed 1.8V, then domain can be grouped with digital IO 1.8V power rail.
- (4) VDDA\_3P3\_USB is 3.3V analog domain used for USB 2.0 differential interface signaling. A low noise, analog supply is recommended to provide best signal integrity for USB data eye mask compliance. If USB interface is not needed or data bit errors can be tolerated, then domain can be grouped with 3.3V digital IO power rail either directly or through a supply filter.
- (5) VDDA\_1P8\_<clk/pll/ana> are 1.8V analog domains supporting clock oscillator, PLL and analog circuitry needing a low noise supply for optimal performance. It is not recommended to combine digital VDDSHVn\_MCU and VDDSHVn IO domains since high frequency switching noise could negatively impact jitter performance of clock, PLL and DLL signals. Combining analog VDDA\_1p8\_<phy> domains should be avoided but if grouped, then in-line ferrite bead supply filtering is required.
- (6) VDDA\_1P8\_<phy> are 1.8V analog domains supporting multiple serial PHY interfaces. A low noise, analog supply is recommended to provide best signal integrity, interface performance and spec compliance. If any of these interfaces are not needed, data bit errors or non-compliant operation can be tolerated, then domains can be grouped with digital IO 1.8V power rail either directly or through an in-line supply filter is allowed.
- (7) VDDA\_0P8\_<dll/pll> are 0.8V analog domains supporting PLL and DLL circuitry needing a low noise supply for optimal performance. It is not recommended to combine these domains with any other 0.8V domains since high frequency switching noise could negatively impact jitter performance of PLL and DLL signals.

**Table 8-2. Independent MCU and Main Voltage Domain Power Rail Mapping**

| TYPES                    | VOLTAGE [V] | DOMAIN NAMES   | DOMAIN GROUPS                         | POWER RAILS                | #  |
|--------------------------|-------------|--|---------------------------------------|----------------------------|----|
| Digital IO               | 3.3         | (VDDSHV0_MCU, VDDSHV1_MCU, VDDSHV2_MCU) <sup>(1)</sup>                                   | VDDSHVn_MCU                           | VDD_MCUIO_3V3              | 1  |
| Digital IO               | 3.3         | (VDDSHV0, VDDSHV2, VDDSHV5 <sup>(3)</sup> ) <sup>(2)</sup> , VDDA_3P3_USB <sup>(4)</sup> | VDDSHVn, VDDA_3P3_USB <sup>(1)</sup>  | VDD_IO_3V3                 | 2  |
| Digital IO               | 1.8         | (VDDSHV0_MCU, VDDSHV1_MCU, VDDSHV2_MCU) <sup>(2)</sup>                                   | VDDSHVn_MCU <sup>(2)</sup>            | VDD_MCUIO_1V8              | 3  |
| Digital IO               | 1.8         | (VDDSHV0, VDDSHV2, VDDSHV5 <sup>(3)</sup> ) <sup>(2)</sup> , VDDS_MMC0                   | VDDSHVn <sup>(2)</sup> <sup>(3)</sup> | VDD_IO_1V8                 | 4  |
| Analog Clk, Meas         | 1.8         | (VDDA_MCU_PLLGRP0, VDDA_MCU_TEMP, VDDA_ADC_MCU, VDDA_POR_WKUP, VDDA_WKUP) <sup>(2)</sup> | VDDA_MCU1P8_<clk/meas>                | VDA_MCU_1V8                | 5  |
| Analog Clk, Meas         | 1.8         | VDDA_OSC1, VDDA_PLLGRP8,6,4,0, VDDA_TEMP1:0  | VDDA_1P8_<clk/meas>                   | VDA_PLL_1V8                | 6  |
| Analog PHY               | 1.8         | (VDDA_1P8_USB, VDDA_1P8_SERDES) <sup>(5)</sup>   | VDDA_1P8_<phy> <sup>(5)</sup>         | VDA_PHY_1V8 <sup>(6)</sup> | 7  |
| Analog, low voltage      | 0.80        | (VDDA_0P8_PLL_DDR, VDDA_0P8_DLL_MMC0) <sup>(6)</sup>                                     | VDDA_0P8_DPLL                         | VDA_DLL_0V8                | 8  |
| Digital, low voltage     | 0.85        | VDD_MCU <sup>(7)</sup> , VDD_MCU_WAKE1, VDDAR_MCU  | VDD_MCU<br>VDDAR_MCU                  | VDD_MCU_0V8                |    |
| Digital, AVS low voltage | 0.77 – 0.84 | VDD_CPU  | VDD_CPU                               | VDD_CPU_AVS                | 9  |
| Digital, low voltage     | 0.80        | VDD_CORE, VDD_WAKE0, (VDDA_0P8_SERDES, VDDA_0P8_USB)                                     | VDD_CORE<br>VDDA_0P8_<phy>            | VDD_CORE_0V8               | 10 |
| Digital, low voltage     | 0.85        | VDDAR_CORE, VDDAR_CPU  | VDDAR                                 | VDD_RAM_0V85               | 11 |
| Digital, low voltage     | 1.1         | VDDS_DDR_BIAS, VDDS_DDR, VDDS_DDR_C  | VDDS_DDR                              | VDD_DDR_1V1                | 12 |

- (1) Any MCU or Main dual voltage IO domains (VDDSHVn\_MCU or VDDSHVn) being supplied by 3.3V to support 3.3V digital interfaces
- (2) Any MCU or Main dual voltage IO domains (VDDSHVn\_MCU or VDDSHVn) being supplied by 1.8V to support 1.8V digital interfaces
- (3) VDDSHV5 supports MMC1 signaling for SD memory cards. A dual voltage (3.3/1.8V) power rail is required for compliant, high-speed SD card operations. If SD card is not needed or standard data rates with fixed 3.3V operation is acceptable, then domain can be grouped with digital IO 3.3V power rail. If a SD card is capable of operating with fixed 1.8V, then domain can be grouped with digital IO 1.8V power rail.
- (4) VDDA\_3P3\_USB is 3.3V analog domain used for USB 2.0 differential interface signaling. A low noise, analog supply is recommended to provide best signal integrity for USB data eye mask compliance. If USB interface is not needed or data bit errors can be tolerated, then domain can be grouped with 3.3V digital IO power rail either directly or through a supply filter.
- (5) VDDA\_1P8\_<phy> are 1.8V analog domains supporting multiple serial PHY interfaces. A low noise, analog supply is recommended to provide best signal integrity, interface performance and spec compliance. If any of these interfaces are not needed, data bit errors or non-compliant operation can be tolerated, then domains can be grouped with digital IO 1.8V power rail either directly or through an in-line supply filter is allowed.
- (6) VDDA\_0P8\_<dll/pll> are 0.8V analog domains supporting PLL and DLL circuitry needing a low noise supply for optimal performance. It is not recommended to combine these domains with any other 0.8V domains since high frequency switching noise could negatively impact jitter performance of PLL and DLL signals.
- (7) VDD\_MCU is a digital voltage domain with a wide operational voltage range enabling it to be grouped either with VDDAR\_MCU domain or with VDD\_CORE; for the "Isolated MCU and Main Domains Power-Up Sequencing," VDD\_MCU can be grouped with VDDAR\_MCU; VDD\_MCU must be ramped-up before T2. If VDDAR\_MCU is not grouped with VDD\_MCU, it must be ramped at T3.

## 8.2 Device Connection and Layout Fundamentals

### 8.2.1 Power Supply Decoupling and Bulk Capacitors

#### 8.2.1.1 Power Distribution Network Implementation Guidance

The [Sitara Processor Power Distribution Networks: Implementation and Analysis](#) provides guidance for successful implementation of the power distribution network. This includes PCB stackup guidance as well as guidance for optimizing the selection and placement of the decoupling capacitors. TI supports *only* designs that follow the board design guidelines contained in the application report.

#### 8.2.2 External Oscillator

For more information about External Oscillators, see [Section 6.10.4, Clock Specifications](#)

#### 8.2.3 JTAG and EMU

Texas Instruments supports a variety of eXtended Development System (XDS) JTAG controllers with various debug capabilities beyond only JTAG support. A summary of this information is available in the [XDS Target Connection Guide](#).

For more recommendations on EMU routing, see [Emulation and Trace Headers Technical Reference Manual](#)

#### 8.2.4 Reset

The device incorporates four external reset pins (MCU\_PORz, MCU\_RESETz, PORz, and RESET\_REQz) and two reset status pins (MCU\_RESETSTATz and RESETSTATz). These pins can be driven by an external power good circuitry or Power Management IC (PMIC). MCU\_PORz and Main PORz pins should be held active low during the entire power-up phase, and until all power supplies as well as the HFOSC0 clock are stable.

All MCU domain resets act as master resets to the whole device, whereas Main domain resets only reset Main domain (MCU domain is reset isolated from all Main domain resets).

#### 8.2.5 Unused Pins

For more information about Unused Pins, see [Section 5.5, Connections for Unused Pins](#)

#### 8.2.6 Hardware Design Guide for Jacinto™ 7 Devices

The Hardware Design Guide for Jacinto™ 7 Devices document describes hardware system design considerations for the Jacinto™ 7 family of processors. This design guide is intended to be used as an aid during the development of application hardware.

## 8.3 Peripheral- and Interface-Specific Design Information

### 8.3.1 LPDDR4 Board Design and Layout Guidelines

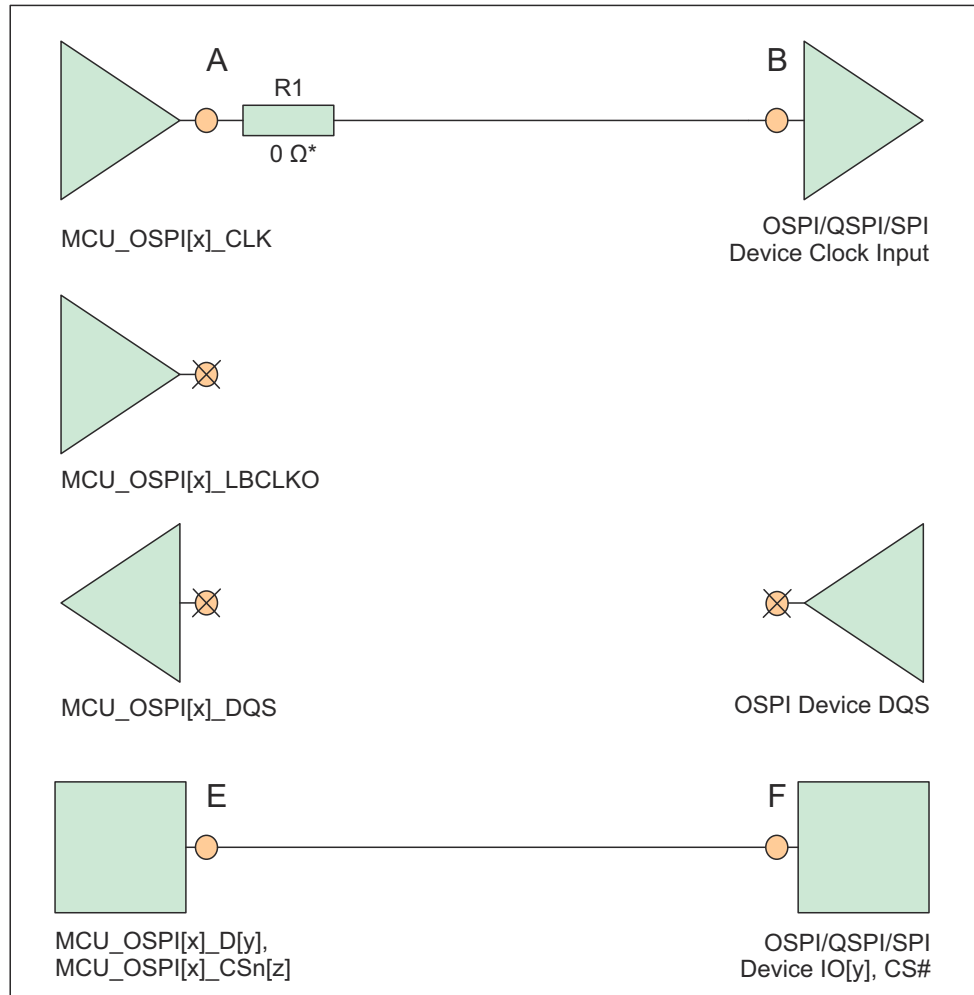
The goal of the [Jacinto 7 DDR Board Design and Layout Guidelines](#) is to make the LPDDR4 system implementation straightforward for all designers. Requirements have been distilled down to a set of layout and routing rules that allow designers to successfully implement a robust design for the topologies that TI supports. TI only supports board designs using LPDDR4 memories that follow the guidelines in this document.

### 8.3.2 OSPI and QSPI Board Design and Layout Guidelines

The following section details the routing guidelines that must be observed when routing the OSPI and QSPI interfaces.

#### 8.3.2.1 No Loopback and Internal Pad Loopback

- The MCU\_OSPI[x]\_CLK output signal must be connected to the CLK pin of the flash device
- The signal propagation delay from the MCU\_OSPI[x]\_CLK signal to the flash device must be < 450 ps (~7cm as stripline or ~8cm as microstrip)
- 50 Ω PCB routing is recommended along with series terminations, as shown in [Figure 8-2](#)
- Propagation delays and matching:
  - A to B < 450 ps
  - Matching skew: < 60 ps



\* 0 Ω resistor (R1), located as close as possible to the MCU\_OSPI[x]\_CLK pin, is placeholder for fine tuning, if needed.

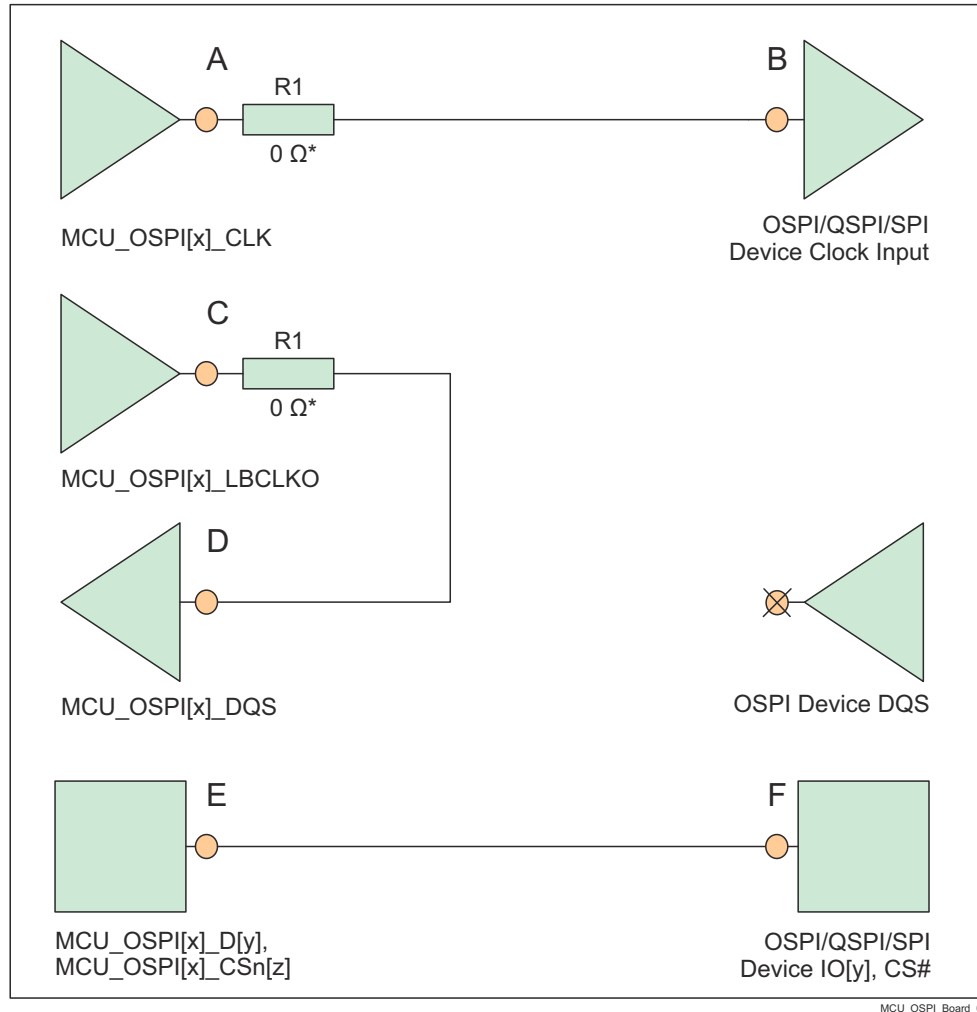
**Figure 8-2. OSPI Interface High Level Schematic**

### 8.3.2.2 External Board Loopback

- The MCU\_OSPI[x]\_CLK output signal must be connected to the CLK pin of the flash device
- The MCU\_OSPI[x]\_LBCLKO output signal must be looped back into the MCU\_OSPI[x]\_DQS input
- The signal propagation delay from the MCU\_OSPI[x]\_CLK pin to the flash device CLK input pin (A to B) should be approximately equal to half of the signal propagation delay from the MCU\_OSPI[x]\_LBCLKO pin to the MCU\_OSPI[x]\_DQS pin ((C to D)/2). See the note below.
- The signal propagation delay from the MCU\_OSPI[x]\_CLK pin to the flash device CLK input pin (A to B) must be approximately equal to the signal propagation delay of the control and data signals between the flash device and the SoC device (E to F, or F to E)
- 50 Ω PCB routing is recommended along with series terminations, as shown in [Figure 8-3](#)
- Propagation delays and matching:
  - A to B = E to F = (C to D) / 2
  - Matching skew: < 60 ps

**Note**

The OSPI Board Loopback Hold time requirement (described in [Section 6.10.5.18, OSPI](#)) is larger than the Hold time provided by a typical flash device. Therefore, the length of MCU\_OSPI[x]\_LBCLKO pin to the MCU\_OSPI[x]\_DQS pin (C to D) can be shortened to compensate.

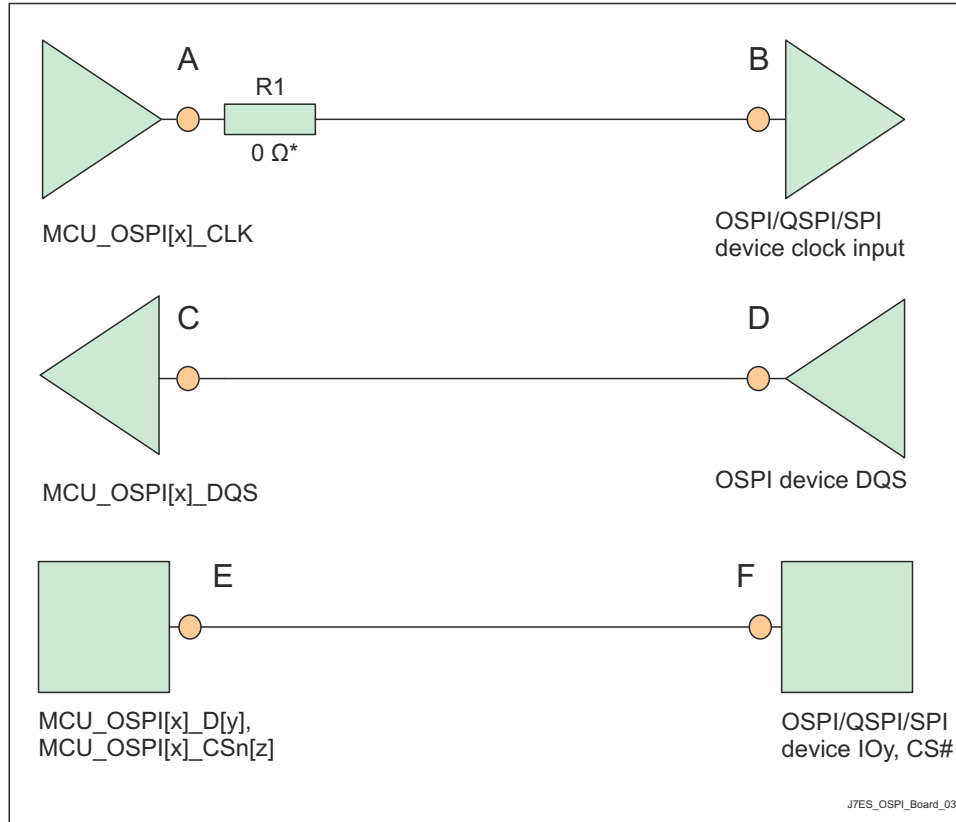


\* 0 Ω resistor (R1), located as close as possible to the MCU\_OSPI[x]\_CLK and MCU\_OSPI[x]\_LBCLKO pins, is a placeholder for fine tuning, if needed.

**Figure 8-3. OSPI Interface High Level Schematic**

**8.3.2.3 DQS (only available in Octal Flash devices)**

- The MCU\_OSPI[x]\_CLK output signal must be connected to the CLK pin of the flash device
- The DQS pin of the flash devices must be connected to MCU\_OSPI[x]\_DQS signal
- The signal propagation delay from the MCU\_OSPI[x]\_CLK pin to the flash device CLK input pin (A to B) should be approximately equal to the signal propagation delay from the MCU\_OSPI[x]\_DQS pin to the DQS output pin (C to D)
- 50 Ω PCB routing is recommended along with series terminations, as shown in [Figure 8-4](#)
- Propagation delays and matching:
  - A to B = C to D
  - Matching skew: < 60 ps



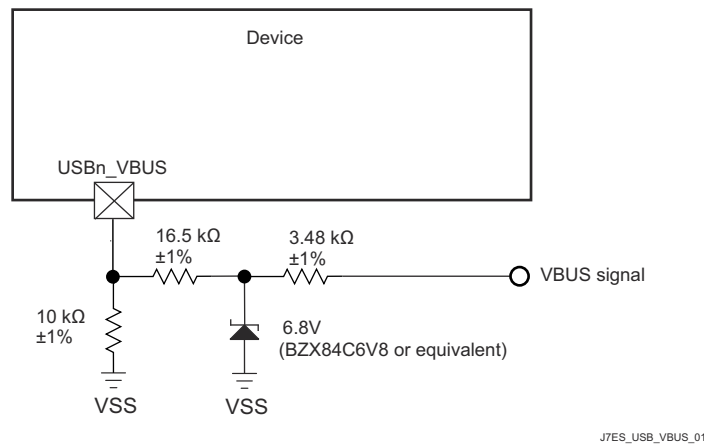
\* 0 Ω resistor (R1), located as close as possible to the MCU\_OSPI[x]\_CLK pin, is a placeholder for fine tuning, if needed.

**Figure 8-4. OSPI Interface High Level Schematic**

**8.3.3 USB VBUS Design Guidelines**

The USB 3.1 specification allows the VBUS voltage to be as high as 5.5 V for normal operation, and as high as 20 V when the Power Delivery addendum is supported. Some automotive applications require a max voltage to be 30 V.

The device requires the VBUS signal voltage be scaled down using an external resistor divider (as shown in the Figure 8-5), which limits the voltage applied to the actual device pin (USB0\_VBUS). The tolerance of these external resistors should be equal to or less than 1%, and the leakage current of zener diode at 5 V should be less than 100 nA.<sup>(1)</sup>



**Figure 8-5. USB VBUS Detect Voltage Divider / Clamp Circuit**

The USB0\_VBUS pin can be considered to be fail-safe because the external circuit in [Figure 8-5](#) limits the input current to the actual device pin in a case where VBUS is applied while the device is powered off.

### 8.3.4 System Power Supply Monitor Design Guidelines

The VMON1\_ER\_VSYS pin provides a way to monitor a system power supply. This system power supply is typically a single pre-regulated power source for the entire system. This supply is monitored by comparing the output of an external voltage divider circuit sourced by this supply with an internal voltage reference, with a power fail event being triggered when the voltage applied to VMON1\_ER\_VSYS drops below the internal reference voltage. The actual system power supply voltage trip point is determined by the system designer when selecting component values used to implement the external resistor voltage divider circuit. When designing the resistor divider circuit it is important to understand various factors which contribute to variability in the system power supply monitor trip point. The first thing to consider is the initial accuracy of the VMON1\_ER\_VSYS input threshold which has a nominal value of 0.45 V, with a variation of  $\pm 3\%$ . Precision 1% resistors with similar thermal coefficient are recommended for implementing the resistor voltage divider. This minimizes variability contributed by resistor value tolerances. Input leakage current associated with VMON1\_ER\_VSYS must also be considered since any current flowing into the pin creates a loading error on the voltage divider output. The VMON1\_ER\_VSYS input leakage current may be in the range of 10 nA to 2.5  $\mu\text{A}$  when applying 0.45 V.

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#### Note

The resistor voltage divider shall be designed such that its output voltage never exceeds the maximum value defined in [Section 6.3, Recommended Operating Conditions](#) during normal operating conditions.

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[Figure 8-6](#) presents an example, where the system power supply is nominally 5 V and the maximum trigger threshold is 5 V - 10%, or 4.5 V.

For this example, it is important to understand which variables effect the maximum trigger threshold when selecting resistor values. It is obvious a device which has a VMON1\_ER\_VSYS input threshold of 0.45 V + 3% needs to be considered when trying to design a voltage divider that doesn't trip until the system supply drops 10%. The effect of resistor tolerance and input leakage also needs to be considered, but how these contributions effect the maximum trigger point may not be obvious. When selecting component values which produce a maximum trigger voltage, the system designer must consider a condition where the value of R1 is 1% low and the value of R2 is 1% high combined with a condition where input leakage current for the VMON1\_ER\_VSYS pin is 2.5  $\mu\text{A}$ . When implementing a resistor divider where R1 = 4.81 K $\Omega$  and R2 = 40.2 K $\Omega$ , the result is a maximum trigger threshold of 4.523 V.

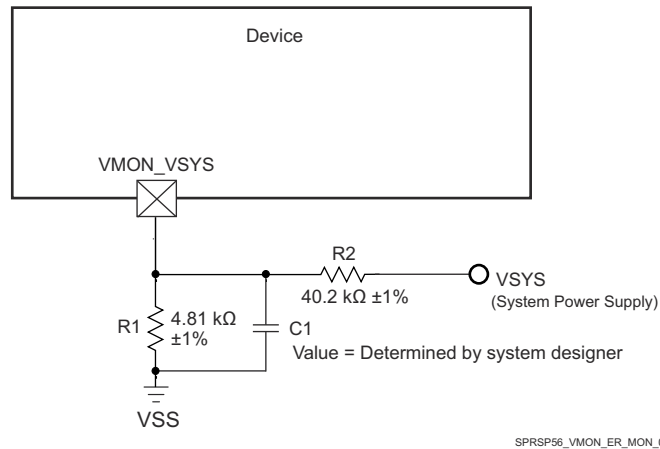
Once component values have been selected to satisfy the maximum trigger voltage as described above, the system designer can determine the minimum trigger voltage by calculating the applied voltage that produces an output voltage of 0.45 V - 3% when the value of R1 is 1% high and the value of R2 is 1% low, and the input leakage current is 10 nA, or zero. Using an input leakage of zero with the resistor values given above, the result is a minimum trigger threshold of 4.008 V.

This example demonstrates a system power supply voltage trip point that ranges from 4.008 V to 4.523 V. Approximately 250 mV of this range is introduced by VMON1\_ER\_VSYS input threshold accuracy of  $\pm 3\%$ , approximately 150 mV of this range is introduced by resistor tolerance of  $\pm 1\%$ , and approximately 100 mV of this range is introduced by loading error when VMON1\_ER\_VSYS input leakage current is 2.5  $\mu\text{A}$ .

The resistor values selected in this example produces approximately 100  $\mu\text{A}$  of bias current through the resistor divider when the system supply is 4.5 V. The 100 mV of loading error mentioned above could be reduced to about 10 mV by increasing the bias current through the resistor divider to approximately 1 mA. So resistor divider bias current vs loading error is something the system designer needs to consider when selecting component values.

The system designer should also consider implementing a noise filter on the voltage divider output since VMON1\_ER\_VSYS has minimum hysteresis and a high-bandwidth response to transients. This could be done by installing a capacitor across R1 as shown in [Figure 8-6](#). However, the system designer must determine the response time of this filter based on system supply noise and expected response to transient events.

Figure 8-6 presents an example, when the system power supply voltage is nominally 5 V and the desired trigger threshold is -10% or 4.5 V.



**Figure 8-6. System Supply Monitor Voltage Divider Circuit**

The **VMON2\_IR\_VCPU** pin provides a way to monitor VDD\_CPU power supply. TI recommends that VMON2\_IR\_VCPU pin be externally connected as close as possible to VDD\_CPU pin on the board.

The **VMON3\_IR\_VEXT1P8** and **VMON4\_IR\_VEXT1P8** pins provide a way to monitor an external 1.8V power supply. The **VMON5\_IR\_VEXT3P3** pin provides a way to monitor an external 3.3V power supply. An internal resistor divider with software control is implemented inside the SoC. Software can program the internal resistor divider to create appropriate under voltage and over voltage interrupts. These pins should not be sourced from an external resistor divider. If the monitored voltage requires adjustment, be sure to buffer the divided voltage prior connecting to monitor pin.

### 8.3.5 High Speed Differential Signal Routing Guidance

The [High Speed Interface Layout Guidelines](#) provides guidance for successful routing of the high speed differential signals. This includes PCB stackup and materials guidance as well as routing skew, length and spacing limits. TI supports *only* designs that follow the board design guidelines contained in the application report.

### 8.3.6 Thermal Solution Guidance

The [Thermal Design Guide for DSP and ARM Application Processors](#) provides guidance for successful implementation of a thermal solution for system designs containing this device. This document provides background information on common terms and methods related to thermal solutions. TI only supports designs that follow system design guidelines contained in the application report.

## 9 Device and Documentation Support

### 9.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, DRA821). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

- X** Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.
- P** Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.
- null** Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

- TMDX** Development-support product that has not yet completed Texas Instruments internal qualification testing.
- TMDS** Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

For orderable part numbers of DRA821 devices in the ALM package type, see the Package Option Addendum of this document, the TI website ([ti.com](http://ti.com)), or contact your TI sales representative.

### 9.1.1 Standard Package Symbolization

#### Note

Some devices can have a cosmetic circular marking visible on the top of the device package which results from the production test process. In addition, some devices can also show a color variation in the package substrate which results from the substrate manufacturer. These differences are cosmetic only with no reliability impact.

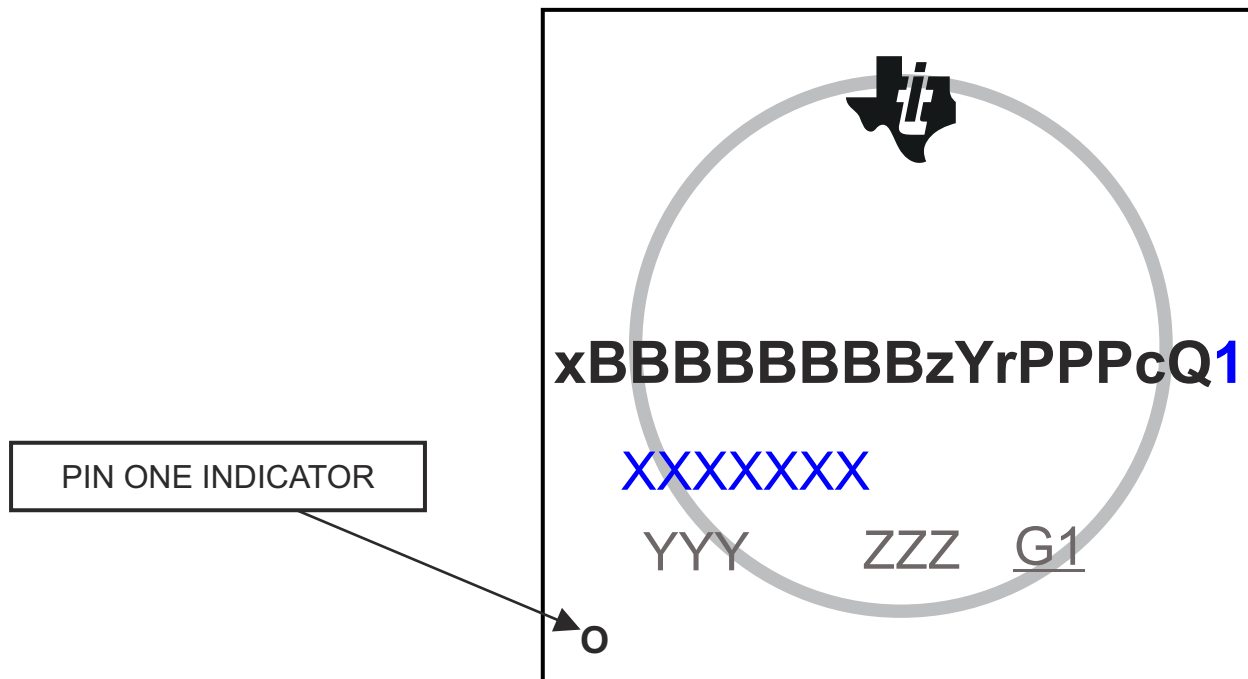


Figure 9-1. Printed Device Reference

### 9.1.2 Device Naming Convention

**Table 9-1. Nomenclature Description**

| FIELD<br>PARAMETER     | FIELD<br>DESCRIPTION        | VALUE      |           | DESCRIPTION   |
|------------------------|-----------------------------|------------|-----------|---|
|                        |                             | MARKING    | ORDERABLE |   |
| x <sup>(1)</sup>       | Device Evolution Stage      | X          |           | Prototype   |
|                        |                             | P          |           | Preproduction (production test flow, no reliability data)   |
|                        |                             | BLANK      |           | Production  |
| BBBBBBB <sup>(3)</sup> | Base Production Part Number | J7200      |           | See <a href="#">Table 4-1, Device Comparison</a>  |
|                        |                             | DRA821U4   |           |   |
|                        |                             | DRA821U2   |           |   |
| z                      | Device Speed                | T          |           | See <a href="#">Table 6-1, Speed Grade Maximum Frequency</a>  |
|                        |                             | L          |           |   |
|                        |                             | E          |           |   |
|                        |                             | C          |           |   |
|                        |                             | OTHER      |           |   |
| Y                      | Device Type <sup>(4)</sup>  | G          |           | General purpose   |
|                        |                             | C          |           | General purpose, R5F Lockstep capable   |
|                        |                             | 0          |           | High Security capable   |
|                        |                             | 5          |           | High Security capable, R5F Lockstep capable   |
|                        |                             | R          |           | High Security Prime <sup>(4)</sup> capable, R5F Lockstep capable  |
|                        |                             | D          |           | High Security capable, R5F Lockstep capable, Customer Dev Keys (Preview) <sup>(5)</sup>   |
| r                      | Device Revision             | A or BLANK |           | SR 1.0  |
|                        |                             | B          |           | SR 2.0  |
| PPP                    | Package Designator          | ALM        |           | ALM FCBGA-N433 (17.2 mm × 17.2 mm) Package  |
| c                      | Carrier Designator          | N/A        | BLANK     | Tray  |
|                        | Carrier Designator          | N/A        | R         | Tape and Reel   |
| Q1 <sup>(2)</sup>      | Automotive Designator       | BLANK      |           | Not automotive qualified.<br>Supports T <sub>J</sub> = –40 °C to 105 °C   |
|                        |                             | Q1         |           | Meets AEC-Q100 qualification requirements, with exceptions as specified in this document (data sheet)<br>Supports T <sub>J</sub> = –40 °C to 125 °C |
| XXXXXXX                | Lot Trace Code              | As Marked  | N/A       | Lot Trace Code (LTC)  |
| YYY                    | Production Code             | As Marked  | N/A       | Production Code; For TI use only  |
| ZZZ                    | Production Code             | As Marked  | N/A       | Production Code; For TI use only  |
| O                      | Pin one                     | As Marked  | N/A       | Pin one designator  |
| G1                     | ECAT                        | As Marked  | N/A       | ECAT—Green package designato  |

- (1) To designate the stages in the product development cycle, TI assigns prefixes to the part numbers. These prefixes represent evolutionary stages of product development from engineering prototypes through fully qualified production devices. Prototype devices are shipped against the following disclaimer:  
"This product is still in development and is intended for internal evaluation purposes."  
Notwithstanding any provision to the contrary, TI makes no warranty expressed, implied, or statutory, including any implied warranty of merchantability or fitness for a specific purpose, of this device.
- (2) Applies to device max junction temperature.
- (3) XJ7200GALM base part number with X speed grade indicator is the part number for the superset device. Software should constrain the features and speed used to match the intended production device.
- (4) For High Security (HS) device support, TI recommends the 0, 5 or D device types. The R and P (*High Security Prime*) device types are not recommended for most applications, as extra steps are required in the manufacturing process and, therefore, these device types are offered at a higher price point.

- (5) Only available on preproduction J7200 devices. (Advance Information/Preview)

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**Note**

BLANK in the symbol or part number is collapsed so there are no gaps between characters.

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## 9.2 Tools and Software

The following products support development for DRA821 platforms:

### Development Tools

**Code Composer Studio™ Integrated Development Environment** Code Composer Studio (CCS) Integrated Development Environment (IDE) is a development environment that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

**SYSCONFIG Tool** System Configuration Tool: To help simplify configuration challenges and accelerate software development, TI created SysConfig, an intuitive and comprehensive collection of graphical utilities for configuring pins, peripherals, radios, subsystems, and other components. SysConfig helps you manage, expose, and resolve conflicts visually so that you have more time to create differentiated applications. The SysConfig tool is integrated in Code Composer Studio™ (CCS) IDE, as a standalone installer, or can be used via the [dev.ti.com](https://dev.ti.com) cloud tools portal.

For a complete listing of development-support tools for the processor platform, visit the Texas Instruments website at [ti.com](https://ti.com). For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

## 9.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The following documents describe the DRA821 devices.

### Technical Reference Manual

**J7200 DRA821 Processor Silicon Revision 1.0 Texas Instruments Families of Products Technical Reference Manual** Details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the DRA821 family of devices.

### Errata

**J7200 DRA821 Processor Silicon Revision 1.0 Silicon Errata** Describes the known exceptions to the functional specifications for the device.

## 9.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

## 9.5 Trademarks

I2C™ is a trademark of NXP Semiconductors.

eMMC™ is a trademark of MultiMediaCard Association.

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HyperBus™ is a trademark of Mobiveil Inc.

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## 9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

### Changes from June 30, 2023 to June 9, 2026 (from Revision E (June 2023) to Revision F (June 2026))

|  | <b>Page</b> |
|--|-------------|
| • <b>Global</b> :: Updated/Changed signal type "OD" to "O" and deleted the "n" suffix on the PMIC_WAKE0 and PMIC_WAKE1 signals, where applicable.....  | 1           |
| • (Features): Removed "DMIPS" references .....   | 1           |
| • (Functional Block Diagram): Added SDK software build sheet Note.....   | 2           |
| • (Device Comparison): Added SDK software build sheet Note.....  | 5           |
| • (Device Comparison): Added the JTAG User ID register bit field [CTRLMMR_WKUP_JTAG_USER_ID[31:16] "DEVICE_ID"]; associated the DEVICE_ID bit field values per GPN; plus, added/changed the associated footnotes.....  | 5           |
| • (Pin Attributes): Added reset states to the BALL RESET STATE column for MMC0_* pins in the <i>Pin Attributes</i> table.....  | 9           |
| • (System Signal Descriptions): Updated OBSCLK signal descriptions.....  | 75          |
| • (VMON Signal Descriptions): Updated VMON2_IR_VCPU signal description.....  | 76          |
| • (SERDES Electrical Characteristics): Updated the "USXGMII supports ... "Note.....  | 103         |
| • (Recommended Operating Conditions for OTP eFuse Programming): Removed the OPP NOM (BOOT) reference from the VDD_CORE and VDD_MCU parameter descriptions.....   | 104         |
| • (Impact to Your Hardware Warranty): Updated/Changed the "Consequently, TI will have no ..." sentence in the paragraph.....   | 105         |
| • (Temperature Sensor Characteristics): Added new section to define Voltage and Temperature Module (VTM) on die temperature sensor characteristics.....  | 106         |
| • (Combined MCU and Main Domains Power- Up Sequencing): Updated note that starts with "VDD_MCU is a digital voltage domain ..." to clarify VDD_MCU grouping and sequence constraints.....  | 109         |
| • (Combined MCU and Main Domains Power- Down Sequencing - Option 1): Added "Option 1".....   | 111         |
| • (Combined MCU and Main Domains Power- Down Sequencing - Option 2): Added "Option 2" section ( <i>new</i> ).....  | 111         |
| • (Independent MCU and Main Domains Power- Up Sequencing): Updated note that starts with "VDD_MCU is a digital voltage domain ..." to clarify VDD_MCU grouping and sequence constraints.....   | 114         |
| • (Independent MCU and Main Domains Power- Down Sequencing - Option 1): Added "Option 1".....  | 117         |
| • (Independent MCU and Main Domains Power- Down Sequencing - Option 2): Added "Option 2" section ( <i>new</i> ).....   | 117         |
| • (Independent MCU and Main Domains, Entry and Exit of MCU Only Sequencing): Updated waveforms for oscillators labeled "WKUP_*" to indicate that these signals remain active. Updated the MCU_PORz waveform to reflect that it stays asserted, as no boot-mode re-latching occurs on the MCU side.....       | 119         |
| • (Independent MCU and Main Domains, Entry and Exit of DDR Retention State): Updated waveforms for oscillators labeled "WKUP_*" to indicate that these signals remain active. Updated the MCU_PORz waveform to reflect that it stays asserted, as no boot-mode re-latching occurs on the MCU side.....       | 120         |
| • (Independent MCU and Main Domains, Entry and Exit of GPIO Retention Sequencing): Updated waveforms for oscillators labeled "WKUP_*" to indicate that these signals remain active. Updated the MCU_PORz waveform to reflect that it stays asserted, as no boot-mode re-latching occurs on the MCU side..... | 121         |
| • (System Timing): Removed the System Timing Conditions table and introduced dedicated Timing Conditions tables for Reset, Safety Signals, and Clock Timing.....   | 123         |
| • (WKUP_OSC0 Internal Oscillator Clock Source): Updated/Changed the C <sub>shunt</sub> , Crystal Circuit Shunt Capacitance content in the <i>WKUP_OSC0 Crystal Electrical Characteristics</i> table.....   | 134         |
| • (OSC1 Switching Characteristics – Crystal Mode [Table]): Updated/Changed the XI and XO capacitance MAX values.....   | 139         |
| • (Auxiliary OSC1 Internal Oscillator Clock Source): Updated/Changed the C <sub>shunt</sub> , Crystal Circuit Shunt Capacitance content in the <i>OSC1 Crystal Electrical Characteristics</i> table.....   | 139         |
| • (MCSPI Timing Requirements - Controller Mode): Updated/Changed the MIN value of SM1, tc(spick), Cycle time, SPI_CLK from "20.8" to "20" ns.....  | 194         |

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|   |     |
|---|-----|
| • (MCSPi Switching Characteristics - Peripheral Mode): Updated/Changed the MIN value of SS1, tc(spick), Cycle time, SPI_CLK from "20.8" to "20" ns.....   | 197 |
| • (MMC0 DLL Delay Mapping for All Timing Modes): Added a new column for MMCS0_SS_PHY_CTRL_1_REG [x=1] and associated values for all operating modes. Updated ITAPDLYSEL bit-field value for <i>HS DDR</i> mode. Updated SELDLYTXCLK, SELDLYRXCLK, and FRQSEL bit-fields for <i>Legacy SDR</i> and <i>HS SDR</i> modes. Added footnotes defining the different <i>NA</i> options, <i>0x1</i> or <i>0x3</i> , and <i>Tuning</i> values..... | 200 |
| • (HS200 Mode): Added MMC0 Timing Requirements.....   | 205 |
| • (HS400 Mode): Updated/Changed the MMC0 HS400 Mode timing parameters to use Output Setup times and Output Hold times.....  | 206 |
| • (MMC1/2 DLL Delay Mapping for All Timing Modes): Removed MMCS12_SS_PHY_CTRL_5_REG register column. Updated OTAPDLYENA and OTAPDLYSEL bit-field values for <i>Default Speed</i> and <i>High Speed</i> modes. Added footnotes defining <i>NA</i> and <i>Tuning</i> values.....  | 207 |
| • (OSPIx Timing Conditions): Updated minimum input slew rate time from 1ns to 0.75ns. Added 1.8 V, PHY Data Training DDR with DQS label which is valid for this mode.....   | 214 |
| • (OSPI Switching Characteristics – Data Training): Added MAX values to the t <sub>c(CLK)</sub> , Cycle time, CLK for DDR 1.8 V, 3.3 V and SDR 1.8 V, 3.3 V modes.....  | 215 |
| • (OSPI Timing Requirements – DDR Mode): Added minimum input data valid window of 1.4ns for OSPI timing requirements in DDR mode.....   | 217 |
| • (OSPI Timing Requirements – SDR Mode): Added minimum input data valid window of 1.7ns for OSPI timing requirements in SDR mode.....   | 218 |
| • (Power Supply Mapping): Updated note that starts with "VDD_MCU is a digital voltage domain ..." to clarify VDD_MCU grouping and sequence constraints.....   | 233 |
| • (System Power Supply Monitor Design Guidelines): Updated VMON2_IR_VCPU design guidelines.....   | 241 |

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## **11 Mechanical, Packaging, and Orderable Information**

### **11.1 Packaging Information**

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable part number             | Status<br>(1) | Material type<br>(2) | Package   Pins    | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)               |
|-----------------------------------|---------------|----------------------|-------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|-----------------------------------|
| DRA821U2CGBALM                    | Active        | Production           | FCBGA (ALM)   433 | 84   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 125   | DRA821U2CGBALM<br>357<br>357 G1   |
| DRA821U2CGBALM.B                  | Active        | Production           | FCBGA (ALM)   433 | 84   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 125   | DRA821U2CGBALM<br>357<br>357 G1   |
| <a href="#">DRA821U2CGBALMR</a>   | Active        | Production           | FCBGA (ALM)   433 | 500   LARGE T&R       | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 125   | DRA821U2CGBALM<br>357<br>357 G1   |
| DRA821U2CGBALMR.B                 | Active        | Production           | FCBGA (ALM)   433 | 500   LARGE T&R       | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 125   | DRA821U2CGBALM<br>357<br>357 G1   |
| <a href="#">DRA821U4TCBALMQ1</a>  | Active        | Production           | FCBGA (ALM)   433 | 84   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 125   | DRA821U4TCBALMQ1<br>357<br>357 G1 |
| DRA821U4TCBALMQ1.B                | Active        | Production           | FCBGA (ALM)   433 | 84   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 125   | DRA821U4TCBALMQ1<br>357<br>357 G1 |
| <a href="#">DRA821U4TCBALMRQ1</a> | Active        | Production           | FCBGA (ALM)   433 | 500   LARGE T&R       | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 125   | DRA821U4TCBALMQ1<br>357<br>357 G1 |
| DRA821U4TCBALMRQ1.B               | Active        | Production           | FCBGA (ALM)   433 | 500   LARGE T&R       | Yes         | Call TI                              | Level-3-250C-168 HR               | -40 to 125   | DRA821U4TCBALMQ1<br>357<br>357 G1 |
| <a href="#">DRA821U4TGBALM</a>    | Active        | Production           | FCBGA (ALM)   433 | 84   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 125   | DRA821U4TGBALM<br>357<br>357 G1   |
| DRA821U4TGBALM.B                  | Active        | Production           | FCBGA (ALM)   433 | 84   JEDEC TRAY (5+1) | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 125   | DRA821U4TGBALM<br>357<br>357 G1   |
| <a href="#">DRA821U4TGBALMR</a>   | Active        | Production           | FCBGA (ALM)   433 | 500   LARGE T&R       | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 125   | DRA821U4TGBALM<br>357<br>357 G1   |

| Orderable part number | Status<br>(1) | Material type<br>(2) | Package   Pins    | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)             |
|-----------------------|---------------|----------------------|-------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------------------|
| DRA821U4TGBALMR.B     | Active        | Production           | FCBGA (ALM)   433 | 500   LARGE T&R       | Yes         | Call TI                              | Level-3-260C-168 HR               | -40 to 125   | DRA821U4TGBALM<br>357<br>357 G1 |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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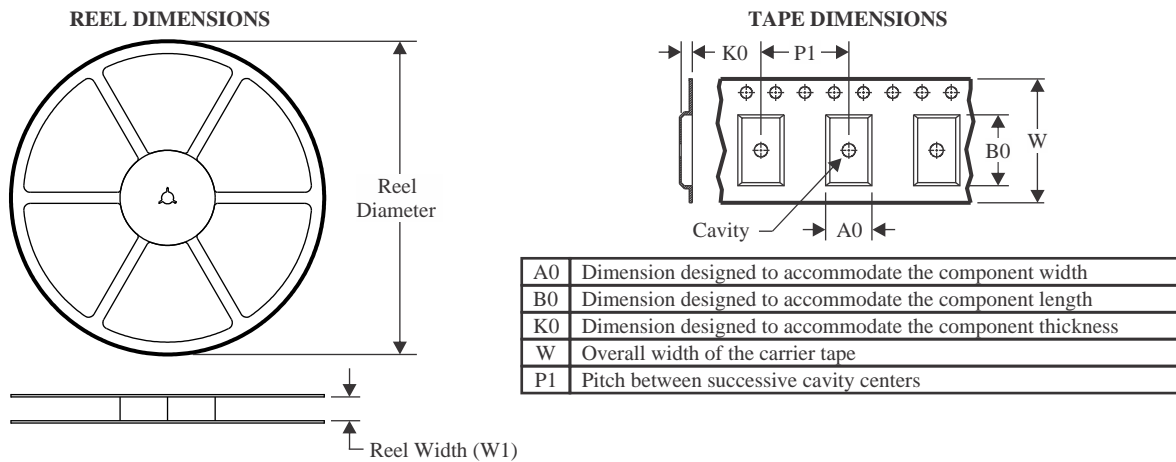
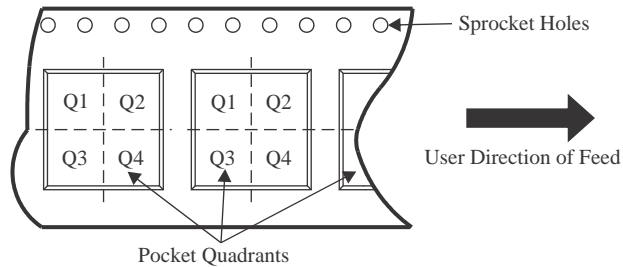
#### OTHER QUALIFIED VERSIONS OF DRA821U, DRA821U-Q1 :

- Catalog : [DRA821U](#)

- Automotive : [DRA821U-Q1](#)

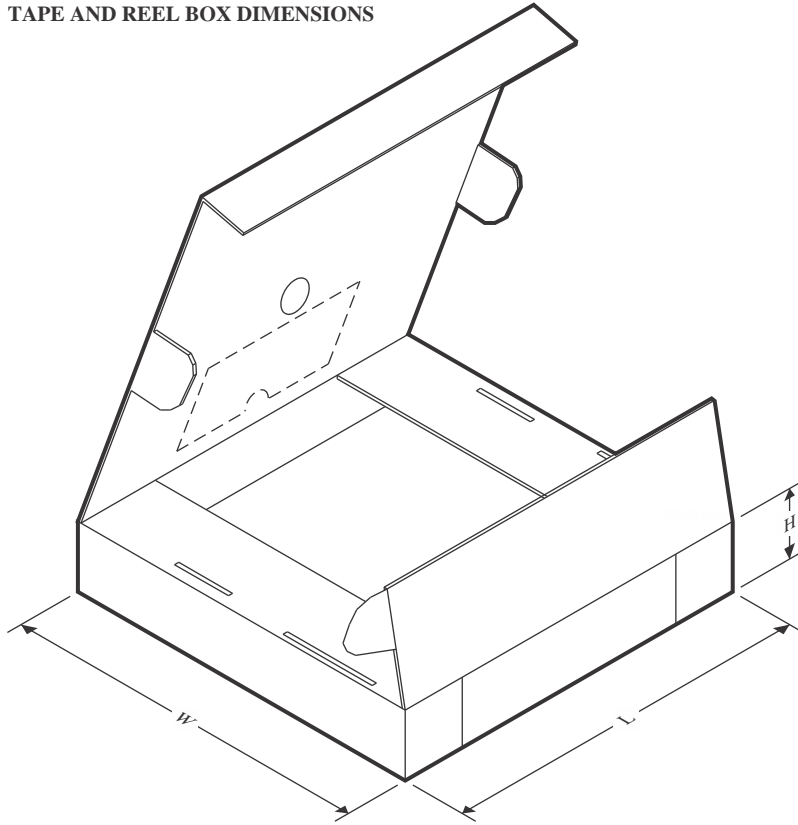
**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


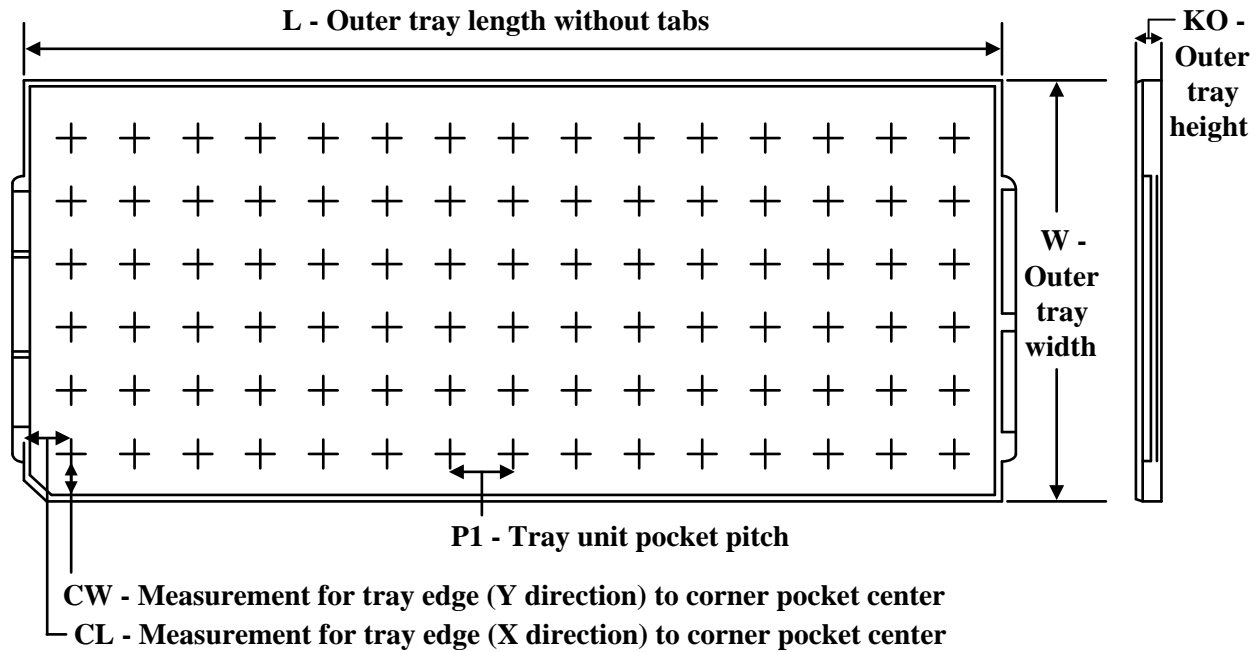
\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|-----|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DRA821U2CGBALMR | FCBGA        | ALM             | 433  | 500 | 330.0              | 32.4               | 17.6    | 17.6    | 3.74    | 24.0    | 32.0   | Q1            |
| DRA821U4TGBALMR | FCBGA        | ALM             | 433  | 500 | 330.0              | 32.4               | 17.6    | 17.6    | 3.74    | 24.0    | 32.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|-----|-------------|------------|-------------|
| DRA821U2CGBALMR | FCBGA        | ALM             | 433  | 500 | 336.6       | 336.6      | 41.3        |
| DRA821U4TGBALMR | FCBGA        | ALM             | 433  | 500 | 336.6       | 336.6      | 41.3        |

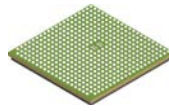
**TRAY**


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

\*All dimensions are nominal

| Device             | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|--------------------|--------------|--------------|------|-----|-------------------|----------------------|--------|--------|---------|---------|---------|---------|
| DRA821U2CGBALM     | ALM          | FCBGA        | 433  | 84  | 6 X 14            | 150                  | 315    | 135.9  | 7620    | 22      | 14.5    | 14.45   |
| DRA821U2CGBALM.B   | ALM          | FCBGA        | 433  | 84  | 6 X 14            | 150                  | 315    | 135.9  | 7620    | 22      | 14.5    | 14.45   |
| DRA821U4TCBALMQ1   | ALM          | FCBGA        | 433  | 84  | 6 X 14            | 150                  | 315    | 135.9  | 7620    | 22      | 14.5    | 14.45   |
| DRA821U4TCBALMQ1.B | ALM          | FCBGA        | 433  | 84  | 6 X 14            | 150                  | 315    | 135.9  | 7620    | 22      | 14.5    | 14.45   |
| DRA821U4TGBALM     | ALM          | FCBGA        | 433  | 84  | 6 X 14            | 150                  | 315    | 135.9  | 7620    | 22      | 14.5    | 14.45   |
| DRA821U4TGBALM.B   | ALM          | FCBGA        | 433  | 84  | 6 X 14            | 150                  | 315    | 135.9  | 7620    | 22      | 14.5    | 14.45   |

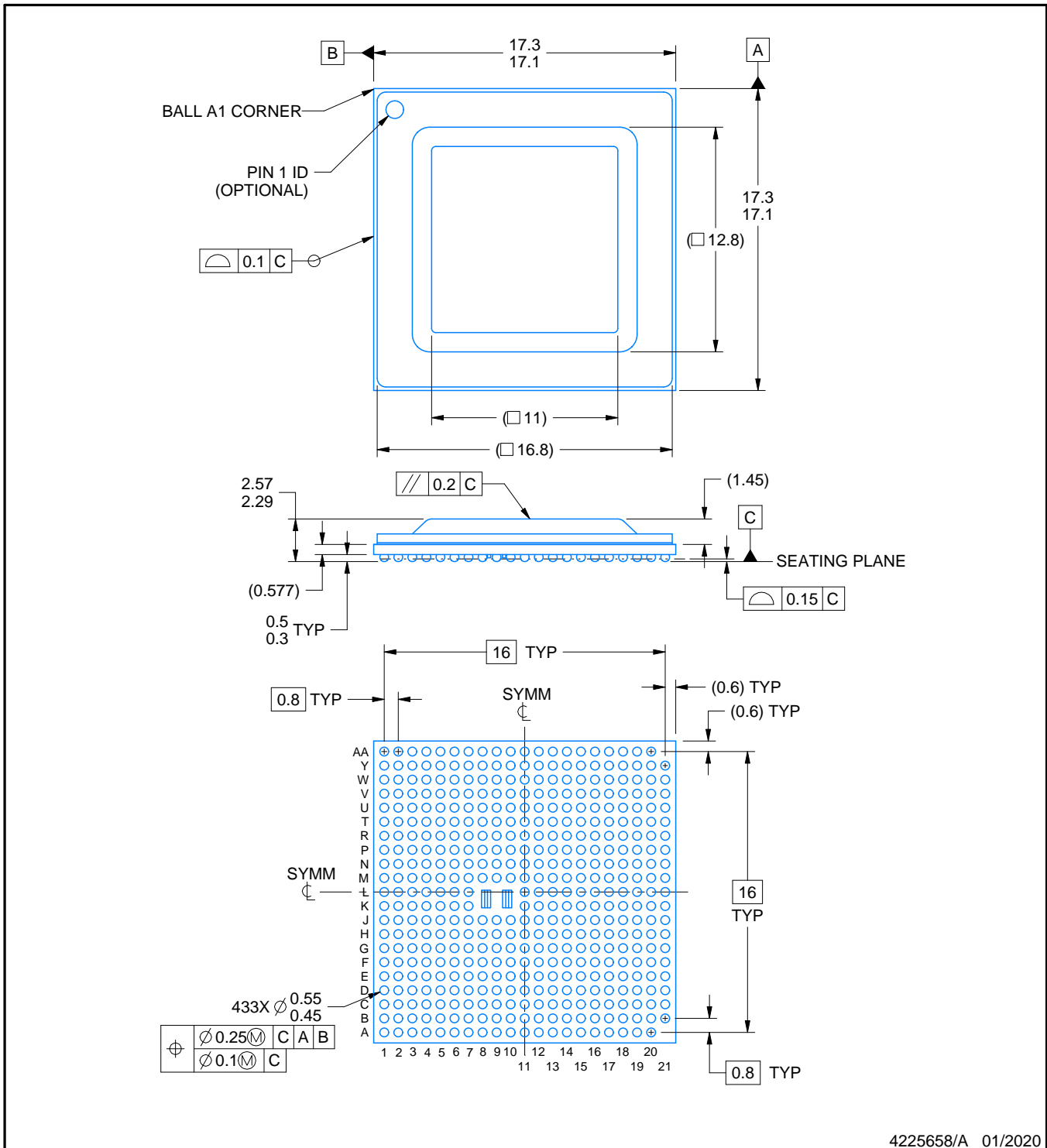
# ALM0433A



# PACKAGE OUTLINE

## FCBGA - 2.57 mm max height

BALL GRID ARRAY



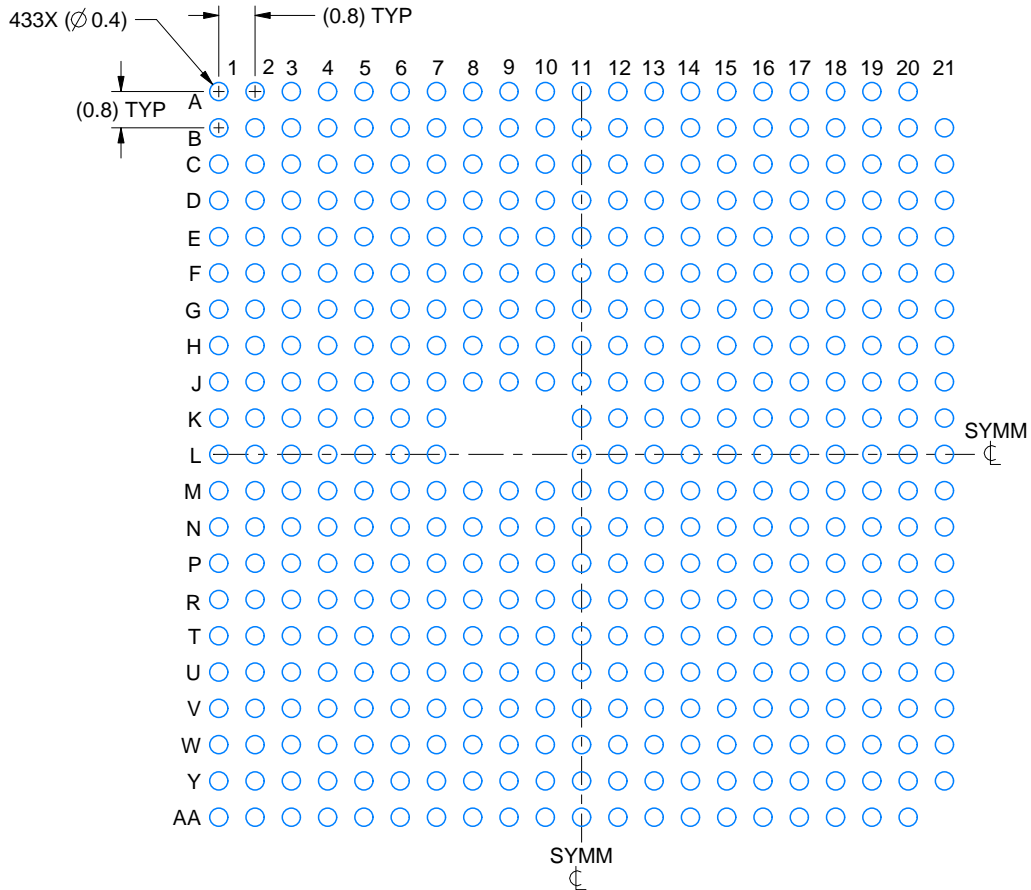
4225658/A 01/2020

# EXAMPLE BOARD LAYOUT

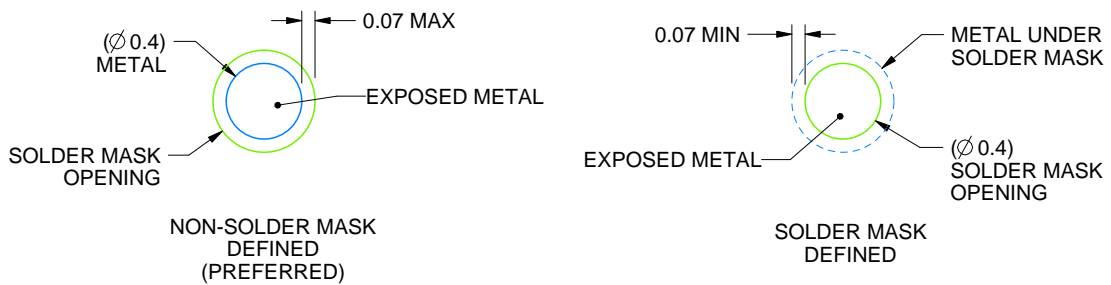
**ALM0433A**

**FCBGA - 2.57 mm max height**

BALL GRID ARRAY



**LAND PATTERN EXAMPLE**  
EXPOSED METAL SHOWN  
SCALE:6X



**SOLDER MASK DETAILS**  
NOT TO SCALE

4225658/A 01/2020

NOTES: (continued)

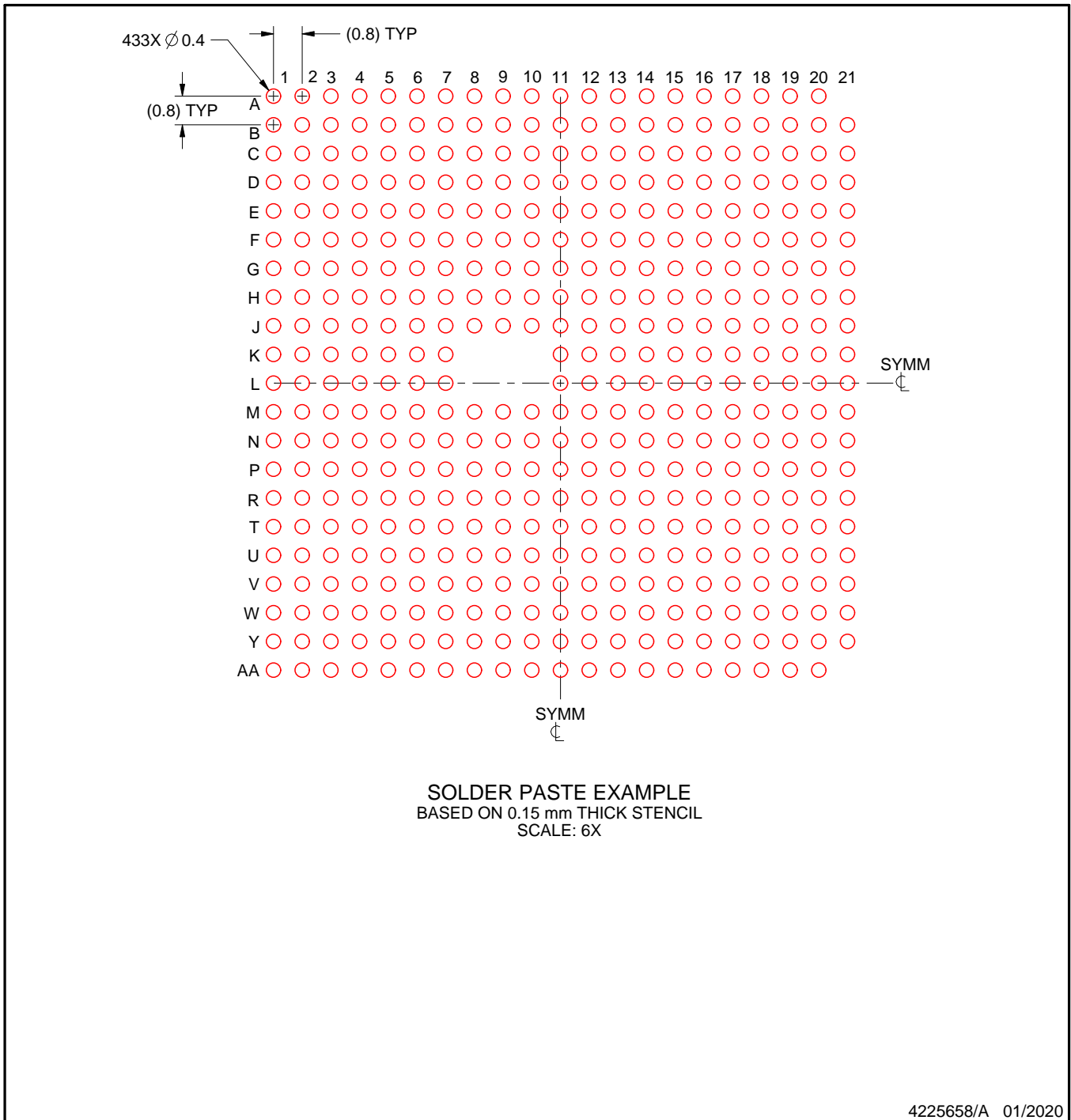
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 ([www.ti.com/lit/spru811](http://www.ti.com/lit/spru811)).

# EXAMPLE STENCIL DESIGN

## ALM0433A

## FCBGA - 2.57 mm max height

BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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Last updated 10/2025