# DRV8218 11V 8A H-Bridge Motor Driver with PWM, PH/EN, and Half-Bridge Control Interfaces and Low-Power Sleep Mode

## 1 Features

- N-Channel H-bridge motor driver
- **1.8V to 11V** operating supply voltage range
- High output current capability: **8A** peak
- **80mΩ** $R_{DS(ON)}$ (High-Side + Low-Side)
  - 40mΩ per FET
  - Parallel ½ Bridge Mode $R_{DS(on)}$: 20mΩ (HS1|| HS2)
- 120nA Ultra low-power sleep mode
  - <120nA at $V_{VM}$ = 5V, $V_{VCC}$ = 3.3V, $T_J$ = 25°C
  - Timed autosleep mode to reduce GPIO
- Supports 1.8V, 3.3V, and 5V logic inputs
- PWM, PH/EN, independent ½ bridge, parallel ½ bridge for flexibility and reduced GPIO
- Protection features
  - Undervoltage lockout (UVLO)
  - Overcurrent protection (OCP)
  - Thermal shutdown (TSD)
- Can drive various types of loads:
  - One bidirectional brushed DC motor
  - Two unidirectional brushed DC motors
  - Single-coil or dual-coil latching relays
  - Push-pull and bistable solenoids
  - Other resistive, inductive, or LED loads
- Family of devices. See Device Comparison for details.
  - DRV8210: 1.65-11V, 1Ω, multiple interfaces
  - DRV8210P: Sleep pin, PWM interface
  - DRV8212: 1.65-11V, 280mΩ, multiple interfaces
  - DRV8212P: Sleep pin, PWM interface
  - DRV8218**: 1.8-11V, 80mΩ, multiple interfaces**
  - DRV8220: 4.5-18V, 1Ω, multiple interfaces

## 2 Applications

- Brushed DC motor, solenoid, & relay driving
- Electric toothbrush
- Beauty & grooming
- Electronic smart lock
- Water, gas, & electricity meters
- Electronic and robotic toys
- IP network camera IR cut filter
- Video doorbell
- Blood pressure monitors
- Infusion pumps

## 3 Description

The DRV8218 is an integrated H-bridge motor driver featuring four N-Channel power FETs, a charge pump regulator, and built-in protection circuitry. A tripler charge pump architecture enables operation down to 1.8V, maintaining stable $R_{DS(on)}$ even at low battery voltages. All capacitors are integrated, minimizing PCB footprint and enabling 100% duty cycle operation.

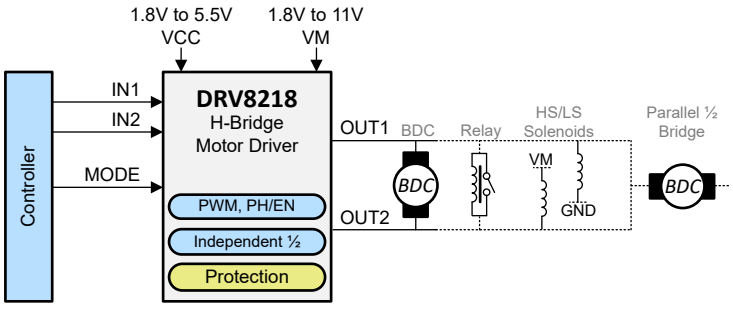
The device supports three control interface modes - PWM (IN1/IN2), phase/enable (PH/EN), and independent half-bridge - as well as a parallel half-bridge mode. Each interface includes a low-power sleep mode that reduces quiescent current to under 120nA by shutting down most internal circuitry.

Output current reaches up to 8A peak, with a logic supply range of 1.8V to 5.5V and a motor supply range of 1.8V to 11V. Built-in protection includes undervoltage lockout (UVLO), overcurrent protection (OCP), and thermal shutdown (TSD). The DRV8218 is part of a pin-to-pin compatible family with scalable $R_{DS(on)}$ and supply voltage options. See Device Comparison for details, or explore TI's full portfolio of brushed motor drivers at ti.com.

**Device Information**

| PART NUMBER (1) | PACKAGE | PACKAGE SIZE(2) |
|---|---|---|
| DRV8218DSG | WSON (8) | 2.00mm × 2.00mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




**Simplified Schematic**

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# 4 Device Comparison

**Table 4-1. Device Comparison Table**

| Device name | Supply voltage (V) | $R_{DS(on)}$ (mΩ) | $I_{OCP}$ (A) | Interface options | Sleep mode entry | Pin-to-pin devices | Packages |
|---|---|---|---|---|---|---|---|
| DRV8210 | 1.65 to 11 | 950 (DRL), 1050 (DSG) | 1.76 | **PWM, PH/EN, Half Bridge** | **Autosleep, VCC** | DRV8210, DRV8212, DRV8218 , DRV8220 | SOT563 (DRL), WSON (DSG) |
| DRV8212 | 1.65 to 11 | 280 | 4 | | | | |
| DRV8218 | **1.8 to 11** | **80** | **8** | | | | **WSON (DSG)** |
| DRV8220 | 4.5 to 18 | 1000 | 1.76 | | Autosleep, nSLEEP pin | | SOT563 (DRL), WSON (DSG) |
| DRV8210P | 1.65 to 11 | 1050 | 1.76 | PWM | nSLEEP pin | DRV8837, DRV8837C, DRV8210P, DRV8212P | WSON (DSG) |
| DRV8212P | 1.65 to 11 | 280 | 4 | | | | WSON (DSG) |

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## 5 Pin Configuration and Functions

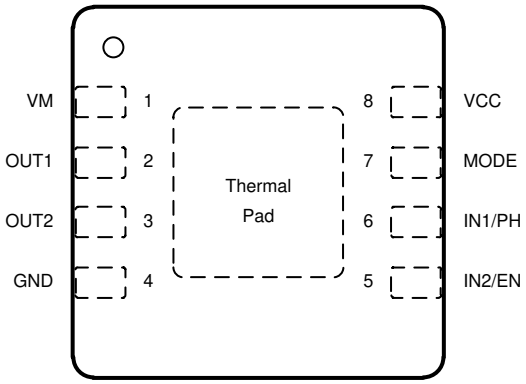


**Figure 5-1. DRV8218 DSG Package 8-Pin WSON Top View**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| **POWER AND GROUND** | | | |
| VM | 1 | PWR | Motor power supply.<br>Bypass this pin to the GND pin with a 0.1µF ceramic capacitor as well as sufficient bulk capacitance rated for VM. |
| GND | 4 | PWR | Device ground.<br>Connect to system ground. |
| VCC | 8 | PWR | Logic power supply.<br>Bypass this pin to the GND pin with a 0.1µF ceramic capacitor rated for VCC. |
| THERMAL PAD | — | — | Thermal pad. Connect to system ground. |
| **CONTROL** | | | |
| IN1/PH | 6 | I | IN1 input. See Section 7.4.1. Internal pulldown resistor. |
| IN2/EN | 5 | I | IN2 input. See Section 7.4.1. Internal pulldown resistor. |
| MODE | 7 | I | H-bridge control input mode. See Section 7.4.1. Tri-level input referenced to VCC pin voltage. |
| **OUTPUT** | | | |
| OUT1 | 2 | O | H-bridge output.<br>Connect to the motor or other load. |
| OUT2 | 3 | O | |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

Over operating temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Power supply pin voltage | VM | -0.3 | 12 | V |
| Logic power supply pin voltage | VCC | -0.3 | 5.75 | V |
| Power supply transient voltage ramp | VM, VCC | 0 | 2 | V/µs |
| Logic pin voltage | IN1/PH, IN2/EN | -0.3 | 5.75 | V |
| Tri-level pin voltage | MODE | -0.3 | $V_{VCC}$+0.3 | V |
| Output pin voltage | OUT1, OUT2 | $-V_{SD}$ | $V_{VM}+V_{SD}$ | V |
| Output current | OUT1, OUT2 | Internally Limited by OCP | Internally Limited by OCP | A |
| Ambient temperature, $T_A$ | | –40 | 125 | °C |
| Junction temperature, $T_J$ | | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | | –60 | 150 | °C |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101(2) | ±500 | |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

Over operating temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{VM}$ | Motor power supply voltage | VM | 1.8 | | 11 | V |
| $V_{VCC}$ | Logic power supply voltage | VCC | 1.8 | | 5.5 | V |
| $V_{IN}$ | Logic pin voltage | IN1/PH, IN2/EN, MODE | 0 | | 5.5 | V |
| $f_{PWM}$ | PWM frequency | IN1/PH, IN2/EN | 0 | | 100 | kHz |
| $I_{OUT}$ (1) | Peak output current | OUT1, OUT2 | | | 8 | A |
| $T_A$ | Operating ambient temperature | | –40 | | 125 | °C |
| $T_J$ | Operating junction temperature | | –40 | | 150 | °C |

(1) Power dissipation and thermal limits must be observed.

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## 6.4 Thermal Information

| THERMAL METRIC(1) | | DRV8218 DSG (WSON) 8 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 60.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 71.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 32.2 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 1.6 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 32.8 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 9.8 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.5 Electrical Characteristics

$1.8V \le V_{VM} \le 11V$ and $1.8V \le V_{VCC} \le 5.5V$, $–40°C \le T_J \le 150°C$ (unless otherwise noted).
Typical values are at $T_J = 25°C$, $V_{VCC} = 3.3V$, and $V_{VM} = 5V$.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLIES (VM, VCC)** | | | | | | |
| $I_{VM}$ | VM active mode current | IN1 = 0V, IN2 = 3.3V | | 0.7 | 2 | mA |
| | | IN1 = 0V, IN2 = 50kHz PWM | | 2 | 7.5 | mA |
| $I_{VMQ}$ | VM sleep mode current | $V_{VM}$ = 5V, $T_J$ = 25°C; INx = 0V after waiting $t_{AUTOSLEEP}$ | | 5 | 100 | nA |
| $I_{VMQ\_UV}$ | VM sleep mode current in $V_{CC}$ undervoltage | INx = 0V after waiting $t_{AUTOSLEEP}$, $V_{VM}$ = 5V, $V_{VCC}$ < 0.35V, $T_J$ = 25°C | | 10 | 120 | nA |
| $I_{VCC}$ | VCC active mode current | $V_{VM}$ = 5V, $V_{VCC}$ = 3.3V; IN1 = 0V, IN2 = 3.3V, No PWM | | 0.45 | 0.6 | mA |
| | | $V_{VM}$ = 5V, $V_{VCC}$ = 3.3V; IN1 = 0V, IN2 = 50kHz PWM | | 0.5 | 1 | mA |
| $I_{VCCQ}$ | VCC sleep mode current | $V_{VM}$ = 5V, $V_{VCC}$ = 3.3V, $T_J$ = 25°C; INx = 0V after waiting $t_{AUTOSLEEP}$ | | | 800 | nA |
| $I_{VCCQ\_UV}$ | VCC sleep mode current in $V_{CC}$ undervoltage | $V_{VM}$ = 5V, $V_{VCC}$ < 0.35V, $T_J$ = 25°C; INx = 0V after waiting $t_{AUTOSLEEP}$ | | | 35 | nA |
| $t_{WAKE}$ | Turnon time | Sleep mode to active mode delay | | | 100 | µs |
| $t_{AUTOSLEEP}$ | Autosleep turnoff time | Active mode to autosleep mode delay | 7.0 | 10 | 14 | ms |
| **LOGIC-LEVEL INPUTS (IN1/PH, IN2/EN)** | | | | | | |
| $V_{IL}$ | Input logic low voltage | | 0 | | 0.4 | V |
| $V_{IH}$ | Input logic high voltage | | 1.45 | | 5.5 | V |
| $V_{HYS}$ | Input logic hysteresis | | 50 | | | mV |
| $I_{IL}$ | Input logic low current | $V_{IN}$ = 0V | -5 | | 5 | µA |
| $I_{IH}$ | Input logic high current | $V_{IN}$ = 3.3V | | | 50 | µA |
| $R_{PD}$ | Input pulldown resistance | To GND | | 100 | | kΩ |
| **TRI-LEVEL INPUTS (MODE)** | | | | | | |
| $V_{TIL}$ | Tri-level input logic low voltage | | 0 | | 0.22 × $V_{VCC}$ | V |
| $V_{TIZ}$ | Tri-level input Hi-Z voltage | | 0.60 × $V_{VCC}$ | | 0.675 × $V_{VCC}$ | V |
| $V_{TIH}$ | Tri-level input logic high voltage | | 0.75 × $V_{VCC}$ | | 5.5 | V |
| $R_{TPD}$ | Tri-level pulldown resistance | to GND, sleep mode | | 1 | | MΩ |
| | | to GND, active mode | | 130 | | kΩ |

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1.8V ≤ $V_{VM}$ ≤ 11V and 1.8V ≤ $V_{VCC}$ ≤ 5.5V, –40°C ≤ $T_J$ ≤ 150°C (unless otherwise noted).
Typical values are at $T_J$ = 25°C, $V_{VCC}$ = 3.3V, and $V_{VM}$ = 5V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $R_{TPU}$ | Tri-level pullup resistance | to VCC | | 75 | | kΩ |
| **DRIVER OUTPUTS (OUT1, OUT2)** | | | | | | |
| $R_{DS(on)\_HS}$ | High-side MOSFET on resistance | $T_A$ = 25°C, $V_{VM}$ = 5V, $V_{VCC}$ = 3.3V, $I_O$ = 1.0A | | 40 | | mΩ |
| | | $T_A$ = 85°C, $V_{VM}$ = 5V, $V_{VCC}$ = 3.3V, $I_O$ = 1.0A | | 50 | | mΩ |
| $R_{DS(on)\_LS}$ | Low-side MOSFET on resistance | $T_A$ = 25°C, $V_{VM}$ = 5V, $V_{VCC}$ = 3.3V, $I_O$ = -1.0A | | 40 | | mΩ |
| | | $T_A$ = 85°C, $V_{VM}$ = 5V, $V_{VCC}$ = 3.3V, $I_O$ = -1.0A | | 50 | | mΩ |
| $V_{SD}$ | Body diode forward voltage | $I_O$ = –1.5A | | 1 | | V |
| $t_{RISE}$ | Output rise time | $V_{VM}$ = 5V, $V_{VCC}$ = 3.3V, $R_L$ = 20Ω OUT1 to OUT2<br>$V_{OUTx}$ rising from 10% to 90% of $V_{VM}$ | | 320 | 450 | ns |
| $t_{FALL}$ | Output fall time | $V_{VM}$ = 5V, $V_{VCC}$ = 3.3V, $R_L$ = 20Ω OUT1 to OUT2<br>$V_{OUTx}$ falling from 90% to 10% of $V_{VM}$ | | 35 | 100 | ns |
| $t_{PD}$ | Input to output propagation delay | INx edge at 50% to output 10% change<br>Load = 200mA | | 25 | | ns |
| $t_{DEAD}$ | Output dead time | Internal dead time | | 320 | | ns |
| $I_{LEAK\_VM}$ | Off-state leakage current into OUTx with load connected to VM | OUTx is Hi-Z, $R_{LOAD}$ = 20Ω to VM<br>$V_{VM}$ = 5V, $V_{VCC}$ = 3.3V | | 20 | | μA |
| $I_{LEAK\_GND}$ | | OUTx is Hi-Z, $R_{LOAD}$ = 20Ω to GND<br>$V_{VM}$ = 5V, $V_{VCC}$ = 3.3V | | -1 | | nA |
| **PROTECTION CIRCUITS** | | | | | | |
| $V_{UVLO,VCC}$ | VCC supply undervoltage lockout (UVLO) | Supply rising | | | 1.8 | V |
| | | Supply falling | 1.5 | | 1.7 | V |
| $V_{UVLO\_HYS}$ | Supply UVLO hysteresis | Rising to falling threshold | | 100 | | mV |
| $t_{UVLO}$ | Supply undervoltage deglitch time | $V_{VCC}$ falling to OUTx disabled | | 4.5 | | μs |
| $I_{OCP}$ | Overcurrent protection trip point | | 8 | | | A |
| $t_{OCP}$ | Overcurrent protection deglitch time | | | 2.5 | | μs |
| $t_{RETRY}$ | Overcurrent protection retry time | | | 1.7 | | ms |
| $T_{TSD}$ | Thermal shutdown temperature | Die temperature $T_J$ | 150 | | 190 | °C |
| $T_{HYS}$ | Thermal shutdown hysteresis | | | 35 | | °C |

## 6.6 Transient Current Capability

**Table 6-1. Transient Current Capability - Full-Bridge**

| PART NUMBER | PKG. | Current [A] without PWM(1) | | | |
|---|---|---|---|---|---|
| | | 0.1 sec | 1 sec | 10 sec | DC |
| **DRV8218** | **DSG** | **7.9** | **5.7** | **5.3** | **4.6** |
| DRV8212 | DSG | 3.6 | 2.8 | 2.6 | 2.4 |
| DRV8210 | DSG | 1.4 | 1.1 | 1.0 | 1.0 |

(1) Based on bench testing at 25°C using DRV8212EVM form factor - 35mm x 60mm x 1.6mm 2 layer PCB with 2-oz Cu on top and bottom layers. Electronic load connected across OUT1 and OUT2, increased the load current until thermal shutdown (TSD) triggered during the pulse duration.

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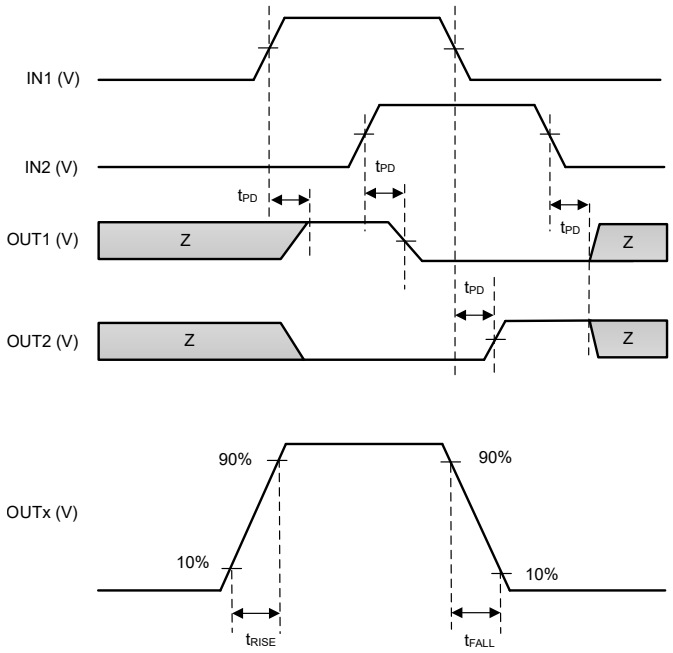



**Figure 6-1. Input-to-Output Timing**

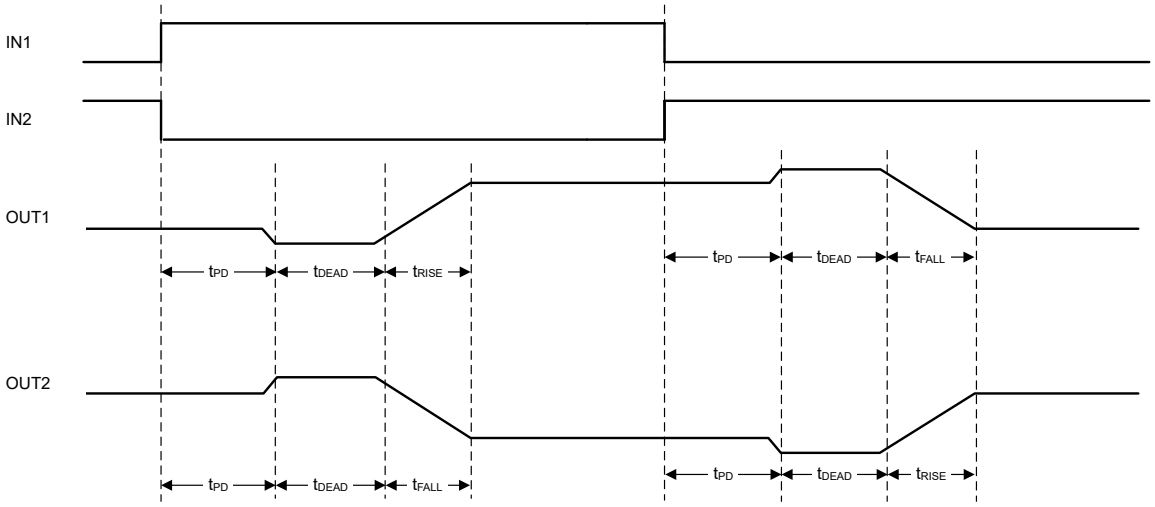
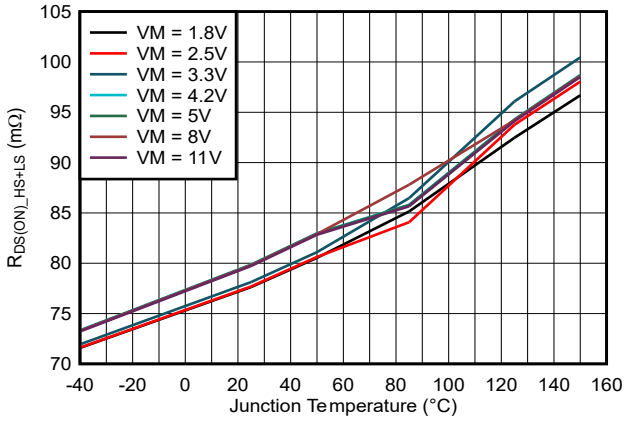


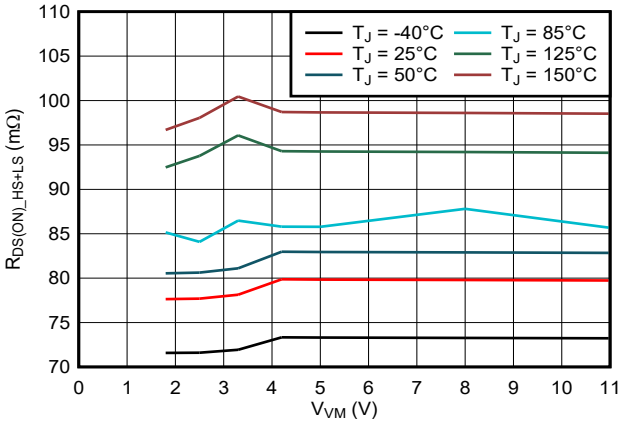

**Figure 6-2. Propagation Delay and Dead Time**

## 6.8 Typical Characteristics



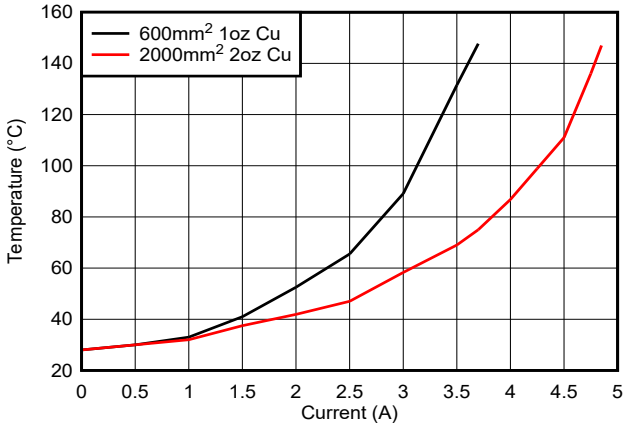

A. $V_{VCC}$ = 3.3V. Preliminary data from simulations.

**Figure 6-3. High-Side + Low-Side $R_{DS(on)}$ vs. Junction Temperature ($T_J$)**




A. $V_{VCC}$ = 3.3V. Preliminary data from simulations.

**Figure 6-4. High-Side + Low-Side $R_{DS(on)}$ vs. Supply Voltage**




A. The 600mm$^2$ data is tested with DRV8837EVM (19mm × 33mm) which has 1oz outer copper thickness. The 2000mm$^2$ data is tested with DRV8212EVM (35mm × 60mm) which has 2oz outer copper thickness.

**Figure 6-5. Device Temperature vs. DC Current per PCB size**

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# 7 Detailed Description

## 7.1 Overview

The DRV8218 is a fully integrated H-bridge motor driver delivering over 4A DC current in a compact 2×2mm WSON package. Four integrated N-Channel power MOSFETs provide a combined $R_{DS(on)}$ of just 80mΩ, saving up to 93% board area compared to equivalent discrete FET solutions while eliminating external gate resistors, flyback diodes, and bootstrap capacitors.

A tripler charge pump architecture with all capacitors integrated on-chip maintains stable $R_{DS(on)}$ across the full 1.8V to 11V motor supply range, even at low battery voltages where discrete solutions degrade. The 1.8V minimum supply makes the DRV8218 well suited for single-cell Li-ion, multi-cell alkaline, and other battery-powered applications. The fully integrated charge pump also enables 100% PWM duty cycle operation and supports PWM frequencies up to 100kHz.

The device supports three control interface modes - PWM (IN1/IN2), phase/enable (PH/EN), and independent half-bridge - selected via the tri-level MODE pin. PH/EN mode enables bidirectional motor control from a single microcontroller timer peripheral. In half-bridge mode, both outputs can be paralleled to achieve 20mΩ effective $R_{DS(on)}$ for high-current single-load applications. Automatic dead-time generation in all modes simplifies firmware and speeds time to market by removing the need for manually matched FET timing to prevent shoot-through.

Rather than requiring a dedicated sleep GPIO, the device automatically enters sleep after inputs remain inactive for $t_{AUTOSLEEP}$ (7–14 ms), reducing quiescent current to under 120nA to extend battery life. Alternatively, the VCC pin can be driven from a microcontroller GPIO to enter sleep via UVLO.

On-chip protection - including overcurrent protection (OCP), thermal shutdown (TSD), and undervoltage lockout (UVLO) - guards against short circuits, overheating, and supply drops, increasing system reliability and potentially eliminating the need for an external fuse. All faults recover automatically. In half-bridge mode, OCP operates independently per output, allowing the unaffected channel to continue normal operation during a single-channel fault.

The DRV8218 is part of a pin-to-pin compatible family of drivers with scalable $R_{DS(on)}$ and supply voltage options. See Section 4 for a full device comparison.

## 7.2 Functional Block Diagram

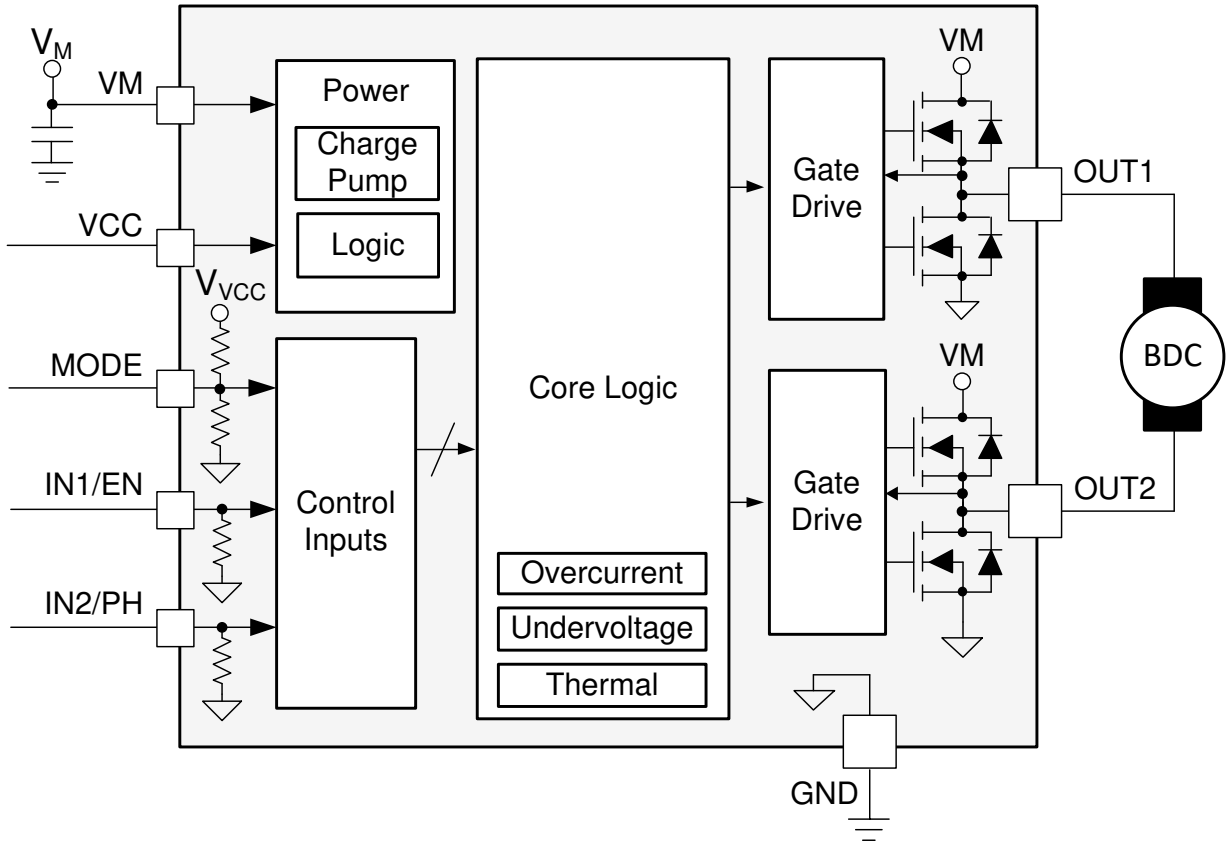


**Figure 7-1. DRV8218 Functional Block Diagram**

## 7.3 External Components

Table 7-1 lists the recommended external components for the device.

**Table 7-1. Recommended external components**

| COMPONENT | PIN 1 | PIN 2 | RECOMMENDED |
|---|---|---|---|
| $C_{VM}$ | VM | GND | 0.1µF, low ESR ceramic capacitor, VM-rated. |
| $C_{BULK}$ | VM | GND | VM-rated. See Section 8.4.1 section for capacitance guidelines. |
| $C_{VCC}$ | VCC | GND | 0.1µF, low ESR ceramic capacitor, VCC-rated. |

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## 7.4 Feature Description

### 7.4.1 Control Modes

The DRV8218 provides three modes to support different control schemes with the PH/IN1 and EN/IN2 pins. The MODE pin selects the control interface mode by setting the pin either logic low, logic high, or Hi-Z as shown in Table 7-2. The MODE pin state is not latching, so the mode can be changed during operation.

**Table 7-2. MODE pin functions**

| MODE STATE | CONTROL MODE |
|---|---|
| MODE = Logic Low | PWM |
| MODE = Logic High | PH/EN |
| MODE = Hi-Z | Independent Half-Bridge |

The inputs can accept DC or pulse-width modulated (PWM) voltage signals with duty cycles from 0% to 100%. The PH/IN1, and EN/IN2 pins have internal pulldown resistors to keep the outputs Hi-Z if no inputs are present (the only exception is half-bridge mode, where OUTx = LOW if INx is floating).

The following sections show the truth tables for each control mode. Additionally, the DRV8218 automatically handles the dead-time generation when switching between the high-side and low-side MOSFET of a half-bridge. Figure 7-2 describes the naming and configuration for the various H-bridge states described in the following sections.

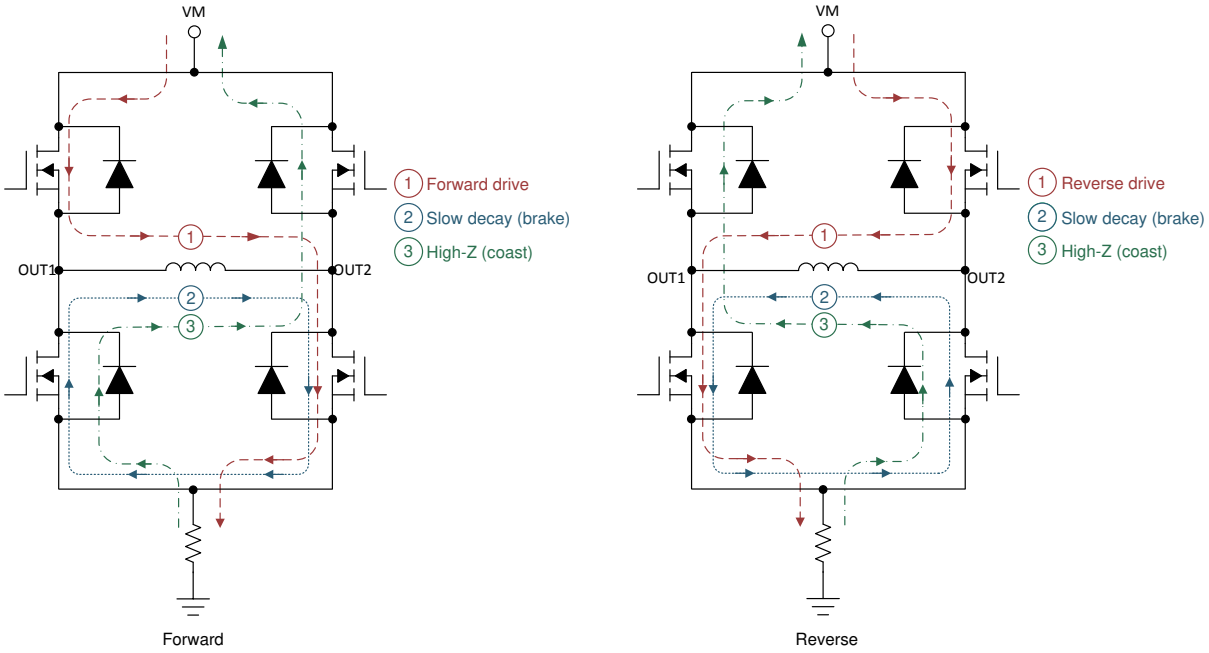


**Figure 7-2. H-bridge states**

#### 7.4.1.1 PWM Control Mode (MODE = 0)

The PWM interface (IN1/IN2) controls the OUTx pins according to the logic table in Table 7-3. In the DSG package, setting the MODE pin logic low selects PWM mode. The coast/Hi-Z state doubles as an automatic sleep mode. After staying in the coast/Hi-Z state for $t_{AUTOSLEEP}$, the device automatically goes into low-power sleep mode (autosleep).

**Table 7-3. PWM control mode with automatic sleep**

| IN1 | IN2 | OUT1 | OUT2 | DESCRIPTION |
|---|---|---|---|---|
| 0 | 0 | Hi-Z | Hi-Z | Coast (H-bridge Hi-Z)/ low-power automatic sleep mode |
| 0 | 1 | L | H | Reverse (OUT2 → OUT1) |
| 1 | 0 | H | L | Forward (OUT1 → OUT2) |
| 1 | 1 | L | L | Brake (low-side slow decay) |

#### 7.4.1.2 PH/EN Control Mode (MODE = 1)

When the MODE pin is logic high, the device selects "phase-enable" mode (PH/EN). PH/EN mode allows for the H-bridge to be controlled with a speed and direction type of interface. Table 7-4 shows the truth table for PH/EN mode. When the EN pin is low, the device enters brake mode. This allows the controller to use a single PWM generator peripheral on the EN pin while a standard GPIO pin controls direction using the PH pin.

If the EN pin remains low for longer than $t_{AUTOSLEEP}$, the device goes into low-power sleep mode and the outputs are disabled. This can be avoided by instead using Half-Bridge Control Mode where the device does not enter automatic sleep mode.

**Table 7-4. PH/EN control mode**

| EN | PH | OUT1 | OUT2 | DESCRIPTION |
|---|---|---|---|---|
| 0 | X | L → Hi-Z | L → Hi-Z | Brake (low-side slow decay) for $t_{AUTOSLEEP}$, then autosleep mode (H-bridge Hi-Z) |
| 1 | 0 | L | H | Reverse (OUT2 → OUT1) |
| 1 | 1 | H | L | Forward (OUT1 → OUT2) |

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#### 7.4.1.3 Independent Half-Bridge Control Mode (MODE = Hi-Z)

When the MODE pin is floating (Hi-Z), the device is in half-bridge control mode. This mode allows for each half-bridge to be directly controlled to support high-side slow decay (or brake), driving two independent loads, or paralleling the outputs for higher current capability for a single load. Table 7-5 shows the truth table for independent half-bridge mode. The Hi-Z state for the MODE pin can be implemented by setting the microcontroller GPIO pin as an *Input* for the MODE pin.

The half-bridge control mode does not support autosleep mode. One way to enter autosleep mode is to set the MODE, IN1, and IN2 pins to logic low, which puts the device into PWM mode and autosleep entry. Alternatively, the VCC pin can be supplied from a microcontroller GPIO pin where setting the GPIO pin low brings the device into undervoltage lockout (UVLO) condition with the outputs all Hi-Z. See Section 7.5.2 for more details.

To wake up the DRV8218 in half-bridge mode, bring VCC high, then set IN1 or IN2 high for longer than $t_{WAKE}$ before returning low or sending a PWM signal. Figure 8-18 and Figure 8-19 show this wake-up procedure.

**Table 7-5. Half-bridge control mode**

| VCC | MODE | IN1 | IN2 | OUT1 | OUT2 | DESCRIPTION |
|---|---|---|---|---|---|---|
| 0V | X | X | X | Hi-Z | Hi-Z | Low-power sleep mode in UVLO |
| 1.8 - 5.5V | 0 | 0 | 0 | Hi-Z | Hi-Z | (Not Independent half-bridge mode) H-bridge disabled/low-power automatic sleep mode |
| 1.8 - 5.5V | Hi-Z | 0 | X | L | X | OUT1 low-side On |
| 1.8 - 5.5V | Hi-Z | 1 | X | H | X | OUT1 high-side On |
| 1.8 - 5.5V | Hi-Z | X | 0 | X | L | OUT2 low-side On |
| 1.8 - 5.5V | Hi-Z | X | 1 | X | H | OUT2 high-side On |

### *7.4.2 Pin Diagrams*

#### 7.4.2.1 Logic-Level Inputs

Figure 7-3 shows the input structure for the logic-level input pins IN1/PH, and IN2/EN.

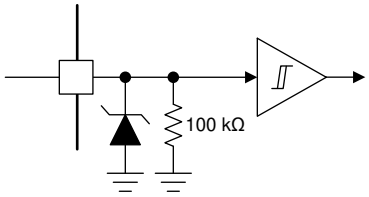


**Figure 7-3. Logic-level input**

#### 7.4.2.2 Tri-Level Input

Figure 7-4 shows the input structure for the tri-level input pin, MODE.

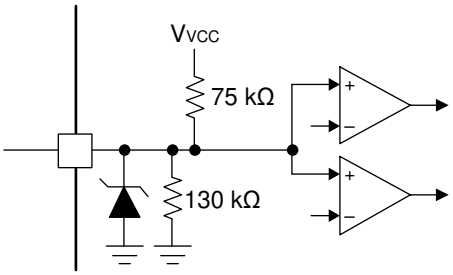


**Figure 7-4. MODE tri-level input in DRV8218**

### 7.4.3 Protection Circuits

The DRV8218 is fully protected against supply undervoltage, output overcurrent, and device overtemperature events.

#### 7.4.3.1 Supply Undervoltage Lockout (UVLO)

If at any time the VCC supply voltage falls below the undervoltage lockout threshold voltage, all MOSFETs in the H-bridge are disabled, the charge pump is disabled, and device logic is disabled. Normal operation resumes when the supply voltage rises above the $V_{UVLO}$ rising threshold. Table 7-6 summarizes the conditions when the device enters UVLO.

**Table 7-6. UVLO response conditions**

| FAULT | $V_{VM}$ | $V_{VCC}$ | Device response |
|---|---|---|---|
| VCC undervoltage | Any 1.8V to 12V | <1.8V | UVLO, H-Bridge Disabled |
| Normal operation | > 1.8V | > 1.8V | Normal operation |

#### 7.4.3.2 OUTx Overcurrent Protection (OCP)

An analog current limit circuit on each MOSFET limits the peak current out of the device even in hard short circuit events. If the output current exceeds the overcurrent threshold, $I_{OCP}$, for longer than the overcurrent deglitch time, $t_{OCP}$, all MOSFETs in the H-bridge are disabled. After $t_{RETRY}$, the MOSFETs are re-enabled according to the state of the PH/IN1 and EN/IN2 pins. If the overcurrent condition is still present, the cycle repeats; otherwise normal device operation resumes.

In half-bridge control mode, the OCP behavior is slightly modified. If an overcurrent event is detected, only the corresponding half-bridge is disabled. The other half-bridge continues normal operation. This allows for the device to manage independent fault events when driving independent loads. If an overcurrent event is detected in both half-bridges, both half-bridges are disabled. Both half-bridges share the same overcurrent retry timer. If an overcurrent event occurs first in OUT1, that output is disabled for the duration of $t_{RETRY}$. If OUT2 experiences an overcurrent event after OUT1, but before $t_{RETRY}$ has expired, then both OUTx pins remain disabled for a full duration of $t_{RETRY}$.

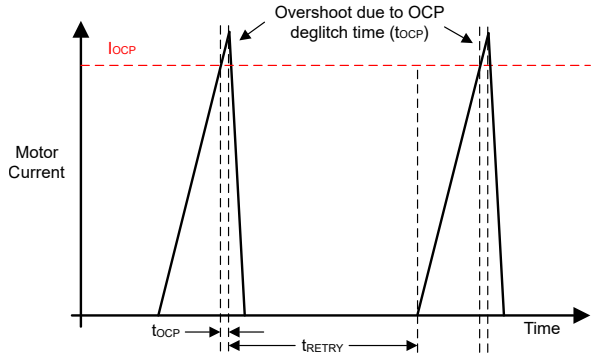


**Figure 7-5. OCP Operation**

#### 7.4.3.3 Thermal Shutdown (TSD)

If the die temperature exceeds the overtemperature limit $T_{TSD}$, all MOSFETs in the H-bridge are disabled. Normal operation resumes when the overtemperature condition is removed and the die temperature drops below the $T_{TSD}$ threshold.

## 7.5 Device Functional Modes

DRV8218 has several different modes of operation depending on the system inputs and conditions.

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### 7.5.1 Active Mode

In active mode, the H-bridge, charge pump, and internal logic are active and the device is ready to receive inputs. The device leaves active mode when entering low-power sleep mode or fault mode. When waking from autosleep, the INx pins (when MODE = 0) or EN pin (when MODE = 1) must be held high for the duration of $t_{WAKE}$ to enable the device. After the $t_{WAKE}$ time has elapsed, the device is awake, and the INx pins or EN pin can receive a PWM signal.

When $V_{VCC} < V_{VM}$, the DRV8218 draws active current from the VM pin rather than the VCC pin. During this operating condition, $I_{VCC}$ is typically less than 500µA.

### 7.5.2 Low-Power Sleep Mode

The DRV8218 supports a low-power sleep mode to reduce current consumption from VM and VCC when the driver is not active. There are two ways to enter low-power sleep mode: autosleep and using the VCC pin. In autosleep mode, the device draws minimal current denoted by $I_{VCCQ}$ and $I_{VMQ}$. In VCC sleep mode, the device draws minimal current denoted by $I_{VMQ\_UV}$ and $I_{VCCQ\_UV}$ since the device is in undervoltage lockout (UVLO) with VCC below the UVLO threshold.

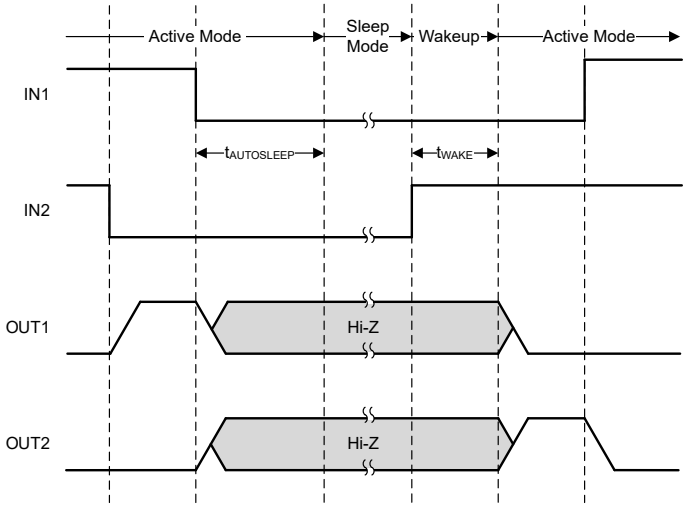


**Figure 7-6. Sleep Mode Entry and Wakeup Timing Diagram**

#### Autosleep

Table 7-7 describes how to enter low-power sleep mode for PWM control mode and PH/EN control mode.

**Table 7-7. Autosleep mode summary**

| Input pin state | OUT1 | OUT2 | Description | Exit/Wake |
|---|---|---|---|---|
| MODE = 0, IN1 = IN2 = 0 | Hi-Z | Hi-Z | **Autosleep for PWM or half-bridge interface:** Upon entering this state, the outputs are disabled. The device remains in Active Mode for $t_{AUTOSLEEP}$, then goes into low-power mode. | IN1 = 1 or IN2 = 1 |
| MODE = 1, EN = 0 | L → Hi-Z | L → Hi-Z | **Autosleep for PH/EN interface:** Upon entering this state, both outputs go into brake mode by turning the low-side FETs on. The device remains in this state for $t_{AUTOSLEEP}$, then goes into low-power mode. Once in low-power mode, the outputs are disabled. | EN = 1 |

The device returns to active mode when the input pins move to a state other than the ones in Table 7-7. To wake up the device from autosleep mode, the INx pins or EN pin (depending on MODE state) must be asserted high for longer than $t_{WAKE}$ before receiving PWM input signals.

#### VCC = 0V UVLO Sleep Mode

**Table 7-8. VCC supply as sleep pin summary**

| Input pin state | OUT1 | OUT2 | Description | Exit/Wake |
|---|---|---|---|---|
| VCC = 0V, MODE = 0 (PWM) | UVLO (Hi-Z) | UVLO (Hi-Z) | The VCC pin can be powered from a GPIO pin to control device sleep. Driving the GPIO low pulls VCC below the UVLO threshold, placing the device into low-power mode and setting all outputs to Hi-Z. See Section 8.2.2.2 for details. | VCC > $V_{UVLO}$, then IN1 or IN2 = 1 for $t_{WAKE}$ |
| VCC = 0V, MODE = 1 (PH/EN) | UVLO (Hi-Z) | UVLO (Hi-Z) | | VCC > $V_{UVLO}$, then EN = 1 for $t_{WAKE}$ |
| VCC = 0V, MODE = Hi-Z (Half-Bridge) | UVLO (Hi-Z) | UVLO (Hi-Z) | | VCC > $V_{UVLO}$, then IN1 or IN2 = 1 for $t_{WAKE}$. |

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To wake up the device from VCC sleep mode, the VCC pin voltage must be greater than $V_{UVLO,VCC}$. Once the VCC pin has a valid voltage, either or both INx pins must be asserted high for longer than $t_{WAKE}$ to fully wake up the device. To protect the microcontroller GPIO pin from excess current due to the decoupling capacitor charging current, a resistor can be added between the GPIO and the decoupling capacitor on the VCC pin. See Section 8.2.2.2 for more information on designing this limiting resistor.

For the lowest supply current draw, set all input pins to logic low to eliminate current draw through the pulldown resistors in sleep mode. If the MODE pin is set to Hi-Z or logic low, the pin does not draw current in sleep mode. However, the MODE pin draws some current in sleep mode when set to logic high.

### *7.5.3 Fault Mode*

The DRV8218 enters a fault mode when a fault is encountered. This protects the device and the output load. The device behavior in the fault mode is described in Section 7.4.3 and depends on the fault condition. The device leaves the fault mode and re-enters the active mode once the recovery condition is met. Table 7-9 summarizes the fault conditions, response, and recovery.

**Table 7-9. Fault condition summary**

| FAULT | CONDITION | H-BRIDGE | RECOVERY |
|---|---|---|---|
| Undervoltage Lockout (UVLO) | VCC < $V_{UVLO,VCC}$ falling | Disabled | VCC > $V_{UVLO,VCC}$ rising |
| Overcurrent (OCP) | $I_{OUT} > I_{OCP}$ | PWM or PH/EN Mode: H-Bridge disabled<br>Half-bridge Mode: Affected half-bridge disabled | $t_{RETRY}$ |
| Thermal Shutdown (TSD) | $T_J > T_{TSD}$ | Disabled | $T_J < T_{TSD} – T_{HYS}$ |

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# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant the accuracy or completeness of this information. Customers are responsible for determining the appropriateness of components for the intended purposes, as well as validating and testing the design implementation to confirm system functionality.

## 8.1 Application Information

The DRV8218 can be used in a variety of applications that require either a half-bridge or H-bridge power stage configuration. Common application examples include brushed DC motors, solenoids, bistable latching relays, and actuators. These devices can also drive many common passive loads such as LEDs, resistive elements, relays, etc. This section highlights some application examples for the DRV8218.

## 8.2 Typical Application

### *8.2.1 Full-Bridge Driving*

A typical application for the DRV8218 is to drive a brushed DC motor or single-coil latching relay bidirectionally (in forward and reverse) using the outputs as a full-bridge, or H-bridge configuration. Figure 8-1 shows examples driving a motor with the PWM interface. Figure 8-2 shows an example of driving a single-coil latching relay with the PWM interface. Figure 8-3 shows an example of driving a motor with the PH/EN interface.

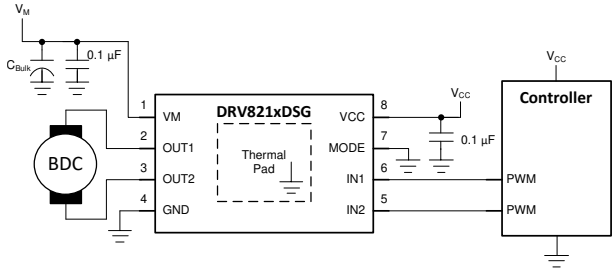


**Figure 8-1. PWM interface motor-driving application**

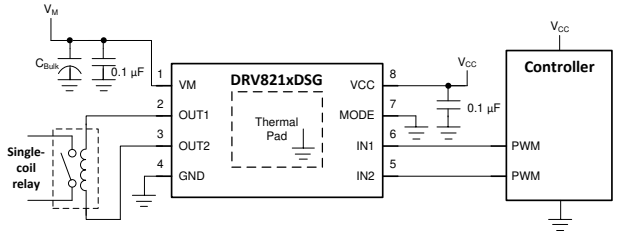


**Figure 8-2. PWM interface single-coil latching relay application**

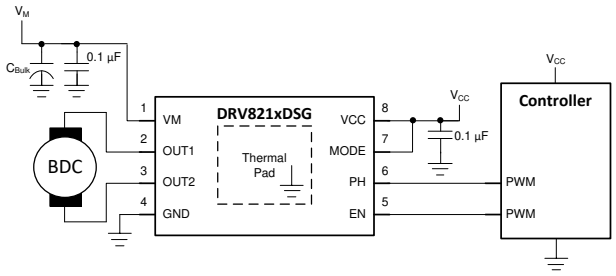


**Figure 8-3. PH/EN interface motor-driving application**

#### 8.2.1.1 Supply Voltage

The appropriate supply voltage depends on the ratings of the load (motor, solenoid, relay, etc.). In the case of a brushed DC motor, the supply voltage impacts the desired RPM. A higher voltage spins a brushed dc motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive windings of a motor, solenoid, or relay.

#### 8.2.1.2 Control Interface - Full Bridge

Section 7.4.1.1 describes the PWM control interface depending on selected package. TI recommends connecting the MODE pin directly to the GND net as shown in Figure 8-1. However, if other interface states

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are required in the application, the MODE pin can be connected to a GPIO pin to select the other interface options during operation. The autosleep feature allows for bidirectional control of the motor and low-power mode using only two pins. This eliminates the need for another GPIO to control a sleep pin. Figure 8-4 and Figure 8-5 show waveform examples of driving a motor with the PWM interface.

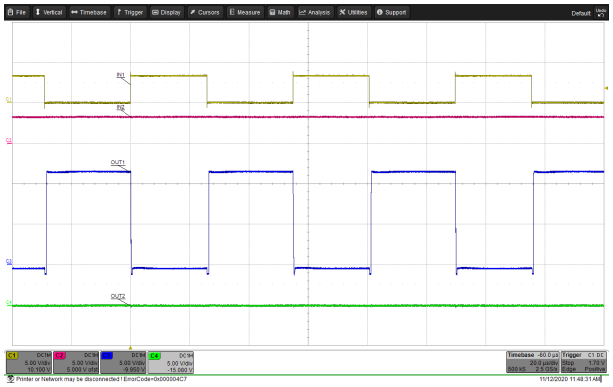
Figure 8-6 and Figure 8-7 show waveform examples of driving a single coil relay with the PWM interface. The relay can be driven between the forward/reverse states and the brake/coast states as shown in the figures.

Section 7.4.1.2 describes the PH/EN control interface. Connecting the MODE pin to the microcontroller supply selects the PH/EN interface. PH/EN mode helps to reduce the number of microcontroller PWM generators needed for motor driving by toggling only the EN pin. The PH pin controls the direction of motor driving with this interface. The device enters sleep mode if EN is held low for longer than $t_{AUTOSLEEP}$.

#### 8.2.1.3 Low-Power Operation

Section 7.5.2 describes how to enter low-power sleep mode. When entering sleep mode, TI recommends setting all inputs as a logic low to minimize system power.

#### 8.2.1.4 Application Curves

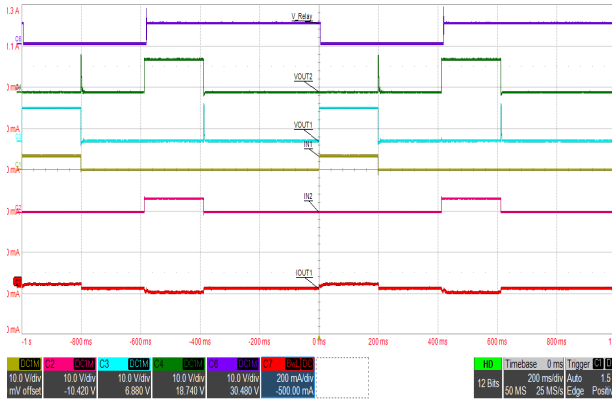


A. Channel 1 = IN1 Channel 2 = IN2 Channel 3 = OUT1 Channel 4 = OUT2

**Figure 8-4. PWM driving for a motor with 50% duty cycle, INx and OUTx voltages**

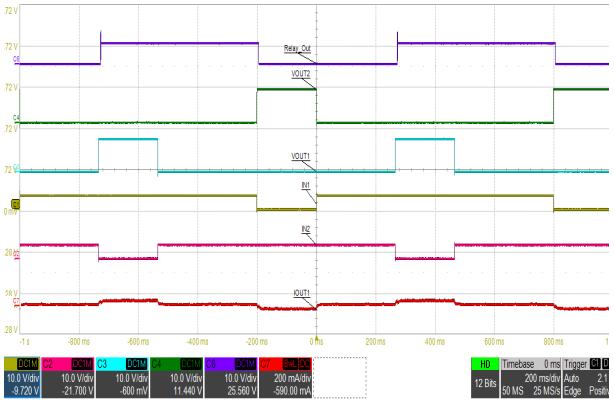
A. Channel 1 = IN1 Channel 2 = Motor Current Channel 3 = OUT1 Channel 4 = OUT2

**Figure 8-5. PWM driving for a motor with 50% duty cycle, signals and motor current**



A. Channel 1 = IN1 Channel 2 = IN2 Channel 3 = $V_{OUT1}$ Channel 4 = $V_{OUT2}$ Channel 6 = Relay Switch Channel 7 = Relay Coil Current

**Figure 8-6. PWM driving for a single-coil latching relay with driving profile FORWARD → COAST → REVERSE → COAST**



A. Channel 1 = IN1 Channel 2 = IN2 Channel 3 = $V_{OUT1}$ Channel 4 = $V_{OUT2}$ Channel 6 = Relay Switch Channel 7 = Relay Coil Current

**Figure 8-7. PWM driving for a single-coil latching relay with driving profile FORWARD → BRAKE → REVERSE → BRAKE**

### *8.2.2 Half-Bridge Driving*

The DRV8218 can be configured to half-bridge mode by leaving the MODE pin floating. In this mode, the device outputs can be used as low-side or high-side drivers. This allows the device to drive various loads such as one or two motors unidirectionally (only in one direction), solenoids, valves, and relays. Figure 8-8 shows the device used as a low-side driver on OUT1 and high-side driver on OUT2. Both loads can also be driven from the high-side or from the low-side. By tying the INx pins together and OUTx pins together, as shown in Figure 8-9 and Figure 8-10, the device can drive a single load with half of the $R_{DS(on)}$. This can accommodate larger current requirements. This configuration is called "parallel half-bridge mode."

In half-bridge mode, the other FETs and body diodes in the half-bridge recirculate freewheeling current during the off-time of the PWM duty cycle, so extra external diodes are not needed.

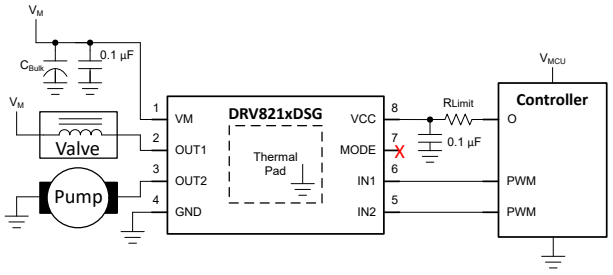



**Figure 8-8. Half-bridge mode used as a high-side and low-side driver for two loads**

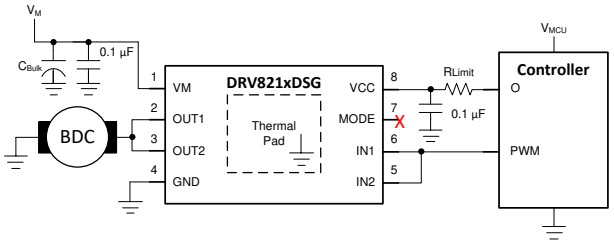



**Figure 8-9. Half-bridge mode used as a high-side driver with outputs paralleled**

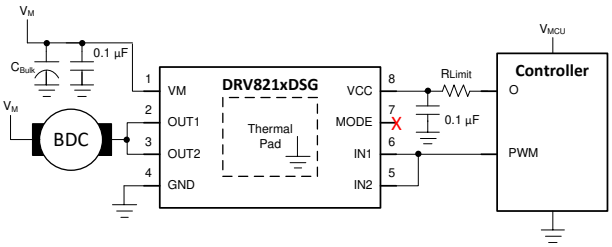



**Figure 8-10. Half-bridge mode used as a low-side driver with outputs paralleled**

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#### 8.2.2.1 Control Interface

Section 7.4.1.3 describes the half-bridge control interface for the DSG package.

#### 8.2.2.2 Low-Power Operation

Bringing VCC to 0V puts the DRV8218 to sleep in half-bridge mode. Section 7.5.2 describes how to enter low-power sleep mode in detail. When entering sleep mode, TI recommends setting all inputs as a logic low to minimize system power. To wake up the DRV8218 in half-bridge mode, bring VCC high, then set IN1 or IN2 high for longer than $t_{WAKE}$ before returning low or sending a PWM signal. Figure 8-18 and Figure 8-19 show this wake-up procedure.

Because of the decoupling capacitor on the VCC pin, TI recommends adding a resistor between the GPIO pin of the controller and the VCC pin as shown in Figure 8-8, Figure 8-9, and Figure 8-10. The purpose of this resistor is to protect the GPIO pin from large currents from the capacitor when switching the GPIO pin. However, this resistor must be sized appropriately to allow the operating current, $I_{VCC}$, to flow into the VCC pin. Table 8-1 shows the design considerations for the $R_{LIMIT}$ resistor. $V_{OL}$ is the GPIO voltage when logic low, $V_{OH}$ is the GPIO voltage when logic high, and $I_{OL}$ is the maximum current that the GPIO can sink. The microcontroller data sheet specifies $V_{OL}$, $V_{OH}$ and $I_{OL}$ for the GPIO pin.

**Table 8-1. GPIO pin current limiting resistor design requirements**

| Design consideration | Equation | Example |
|---|---|---|
| Minimum resistance needed to protect GPIO pin. Here, $V_{Cap}$ is the voltage on the capacitor when the GPIO pin switches from high to low. To simplify calculation and assume a worst-case condition, $V_{Cap}$ is assumed to be equivalent to the controller supply voltage, $V_{MCU}$. See Figure 8-11 for example circuit. | $R_{Limit} \geq (V_{Cap} - V_{OL}) / I_{OL}$ | $R_{Limit} \geq (3.3V - 0.3V) / 24mA = 125\Omega$ |
| Keep the VCC pin voltage high enough so device does not go into undervoltage lockout. See Figure 8-12 for example circuit. | $V_{OH} - (I_{VCC} \times R_{Limit}) = V_{VCC} \geq 1.8V$ | $3.0V - (3.6mA \times 125\Omega) = 2.55V \geq 1.8V$ |

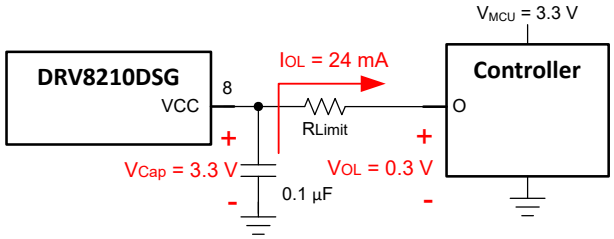



**Figure 8-11. GPIO current when switching output from logic high to logic low**

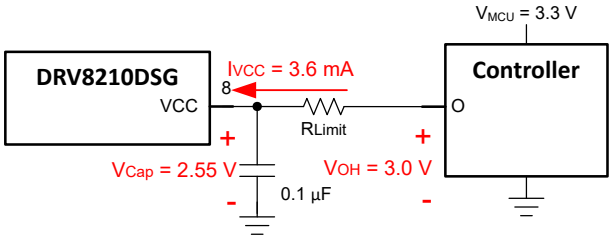



**Figure 8-12. GPIO current with logic high output when $V_{VCC} > V_{VM}$**

In cases where the specified GPIO current is too small, there are a few other options to put the device to sleep. One option is to parallel multiple GPIO to supply the appropriate current. A second option is to set MODE = IN1 = IN2 = 0 to put the device into the autosleep state. This requires the GPIO pin that controls MODE to be configured as an input during operation and an output low during sleep. A third option is to place a GPIO-controlled transistor between the supply and the VCC pin as shown in Figure 8-13.

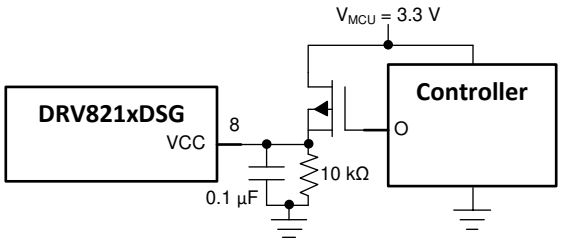
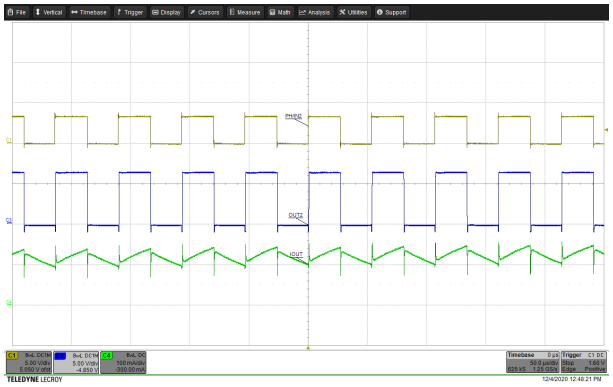



**Figure 8-13. GPIO with transistor**

To minimize leakage current into the OUTx pins (especially in battery-powered applications), connect the load from OUTx to GND. As mentioned earlier, connecting the load from OUTx to VM is also possible, but there can be some small leakage current into OUTx when the outputs are disabled. No leakage current is expected if loads are connected in H-bridge configuration.

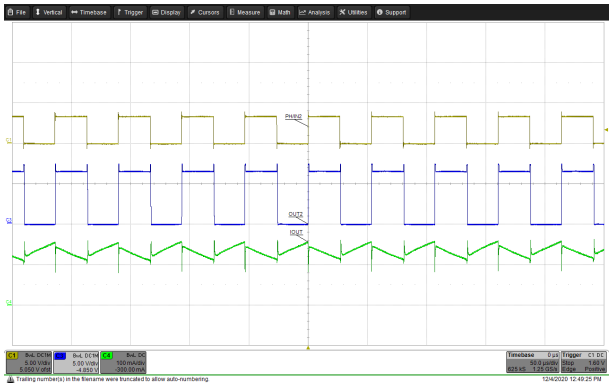
#### 8.2.2.3 Application Curves

The figures below show waveform examples of high-side and low-side driving in half-bridge mode. Figure 8-14 and Figure 8-15 show example waveforms of driving a motor uni-directionally using high-side and low-side driving. Figure 8-16 and Figure 8-17 show example waveforms of driving a solenoid using high-side and low-side driving. Figure 8-18 and Figure 8-19 show examples of driving a motor using high-side and low-side driving when the OUTx pins are paralleled together to create a single half bridge.



A. Channel 1 = IN2 Channel 2 = $V_{OUT2}$ Channel 4 = Motor Current

**Figure 8-14. Driving a motor in half-bridge mode with 50% duty cycle using the high-side FET**



A. Channel 1 = IN2 Channel 2 = $V_{OUT2}$ Channel 4 = Motor Current

**Figure 8-15. Driving a motor in half-bridge mode with 50% duty cycle using the low-side FET**

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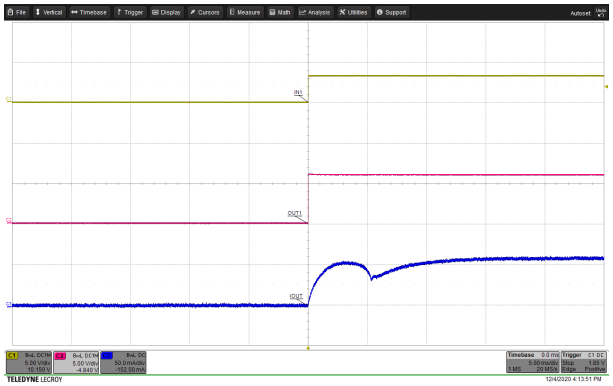
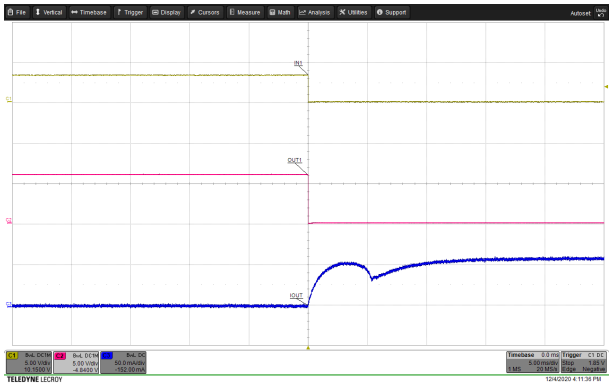


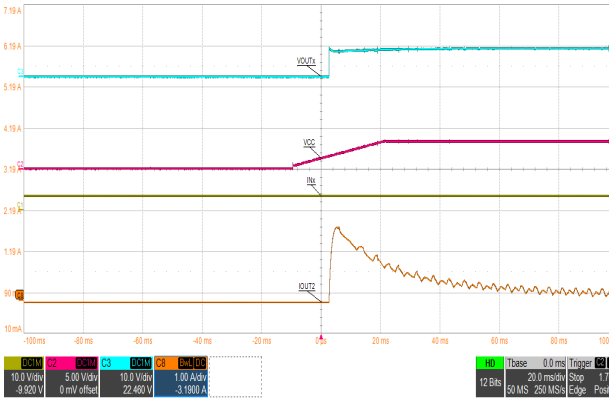
A. Channel 1 = IN1 Channel 2 = $V_{OUT1}$ Channel 4 = Solenoid Current

**Figure 8-16. Driving a solenoid in half-bridge mode using the high-side FET**



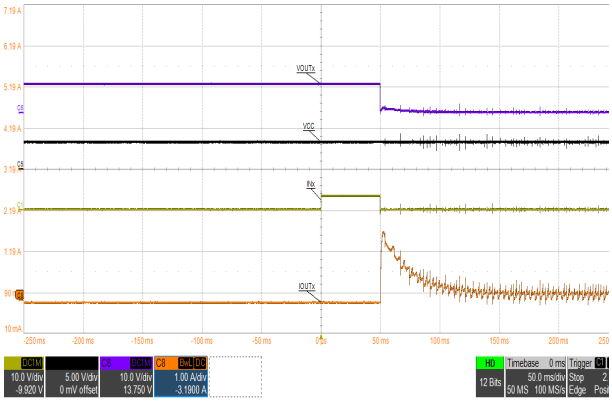
A. Channel 1 = IN1 Channel 2 = $V_{OUT1}$ Channel 4 = Solenoid Current

**Figure 8-17. Driving a solenoid in half-bridge mode using the low-side FET**



A. Channel 1 = IN1, IN2 (paralleled) Channel 8 = Motor Current Channel 2 = $V_{VCC}$ Channel 3 = $V_{OUT}$ (OUT1/2 paralleled)

**Figure 8-18. Driving a motor in parallel half-bridge mode using the high-side FETs**



A. Channel 1 = IN1, IN2 (paralleled) Channel 8 = Motor Current Channel 5 = $V_{VCC}$ Channel 6 = $V_{OUT}$ (OUT1/2 paralleled)

**Figure 8-19. Driving a motor in parallel half-bridge mode using the low-side FETs**

### *8.2.3 Parallel Multiple Drivers*

Multiple DRV8218 can be paralleled to drive one load with significantly lower $R_{DS(on)}$ than a single driver. The rise time, fall time, and propagation delay are sufficiently smaller than the dead time to account for device variations between two parts. The small form factor of the DSG package results in a smaller footprint for two DRV8218 than using a single higher current motor driver such as DRV8850.

PWM or PH/EN mode is recommended for when using multiple DRV8218 in parallel so that the devices can automatically handle the dead time. If half-bridge mode is used the dead time must be manually inserted between turning off a high-side FET and turning on the low-side FETs to avoid shoot-through.

Multiple devices naturally balance the load current between the devices because the FET resistance increases with temperature. However, a spike in current can cause a device's overcurrent protection to trip faster than this heating effect can balance the load between devices.

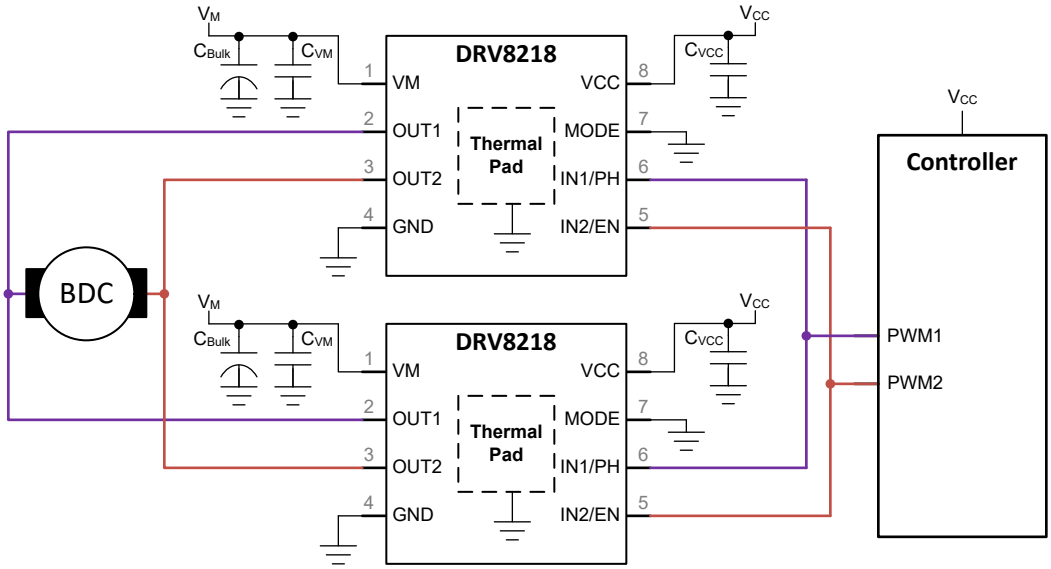



**Figure 8-20. Two DRV8218 driving one load in parallel, PWM mode**

### *8.2.4 Dual-Coil Relay Driving*

The PWM interface can also be used to drive a dual-coil latching relay. The figure in this section shows example schematics.

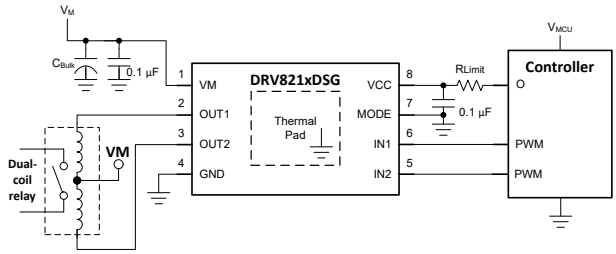



**Figure 8-21. Dual-coil relay driving**

#### 8.2.4.1 Control Interface

The PWM interface can be used to drive dual-coil relays. Section 7.4.1.1 describes the PWM control interface. Figure 8-22 and Figure 8-23 show a schematic and timing diagram for driving a dual-coil relay with the PWM interface.

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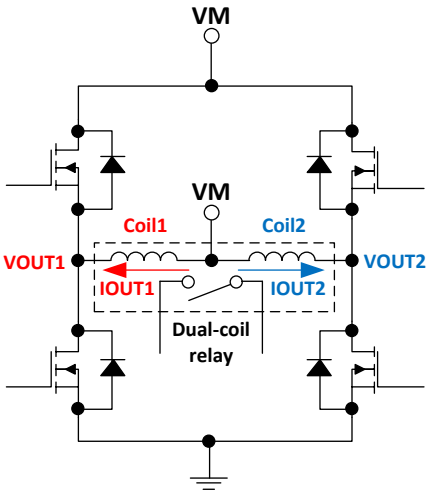



**Figure 8-22. Schematic of dual-coil relay driven by the OUTx H-bridge**

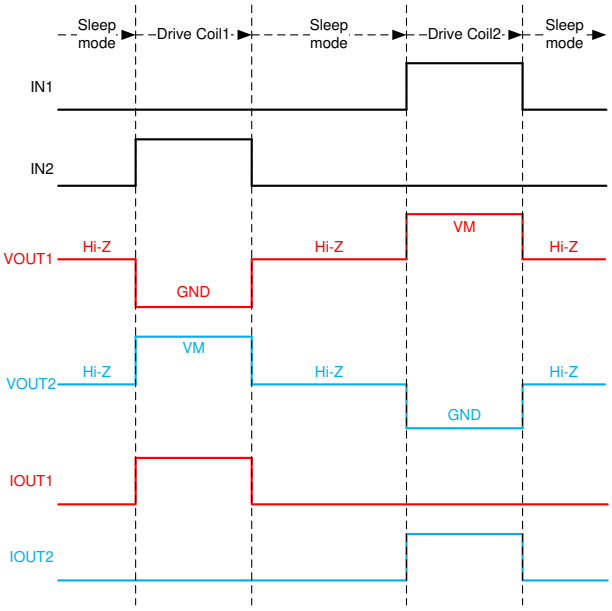



**Figure 8-23. Timing diagram for driving a dual-coil relay with PWM interface**

Table 8-2 shows the logic table for the PWM interface. The descriptions in this table reflect how the input and output states drive the dual coil relay. When Coil1 is driven (OUT1 voltage is at GND), The voltage at OUT2 goes to VM. Because the center tap of the relay is also at VM, no current flows through Coil2. The same is true when Coil2 is driven; Coil1 shorts to VM. The body diodes of the high-side FETs act as freewheeling diodes, so extra external diodes are not needed. Figure 8-24 shows oscilloscope traces for this application.

**Table 8-2. PWM control table for dual-coil relay driving**

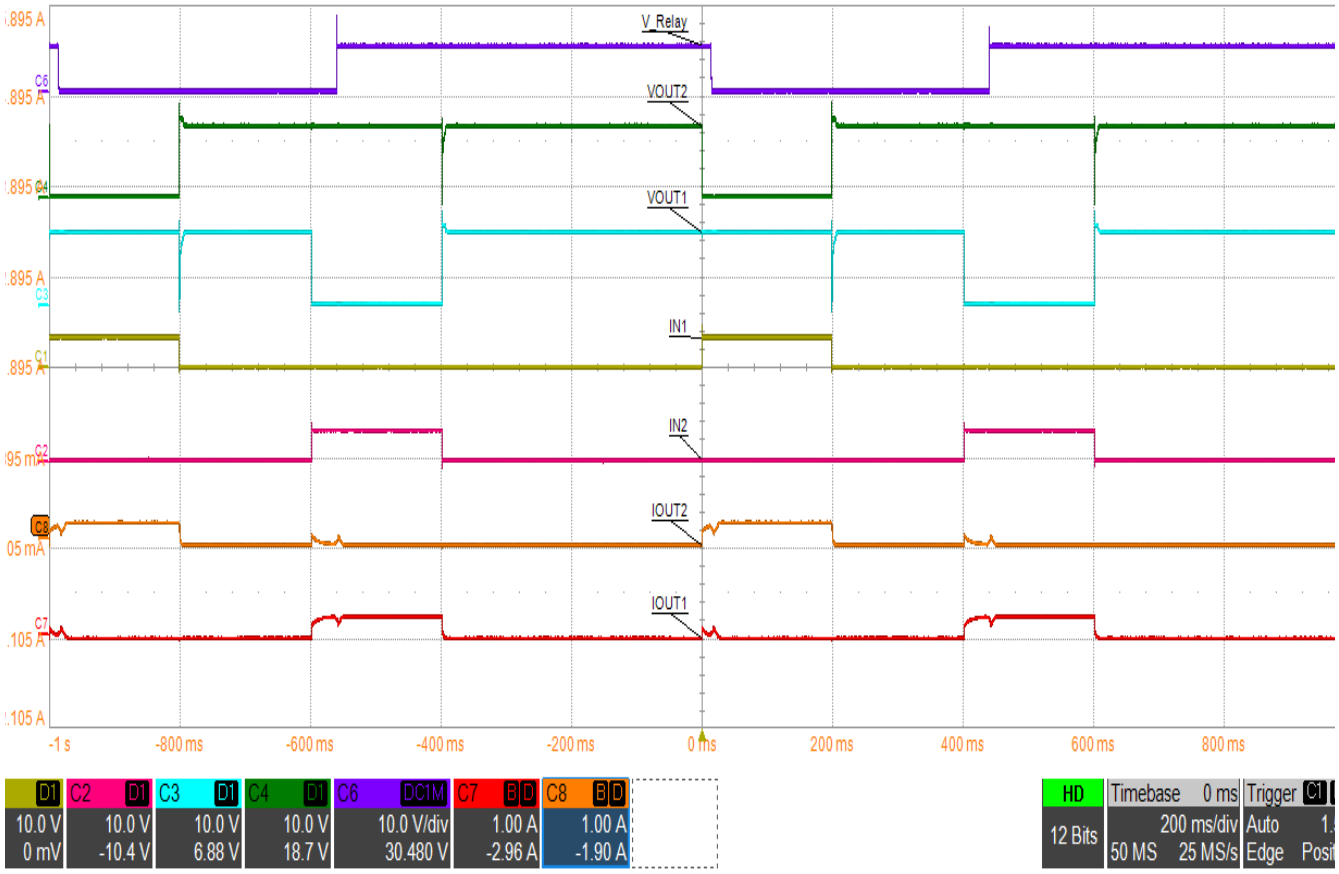
| IN1 | IN2 | OUT1 | OUT2 | DESCRIPTION |
|---|---|---|---|---|
| 0 | 0 | Hi-Z | Hi-Z | Outputs disabled (H-Bridge Hi-Z) |
| 0 | 1 | L | H | Drive Coil1 |
| 1 | 0 | H | L | Drive Coil2 |
| 1 | 1 | L | L | Drive Coil1 and Coil2 (invalid state for a dual-coil latching relay) |

#### 8.2.4.2 Low-Power Operation

Section 7.5.2 describes how to enter low-power sleep mode. When entering sleep mode, TI recommends setting all inputs as a logic low to minimize system power.

To minimize leakage current into the OUTx pins (especially in battery-powered applications), connect the load from OUTx to GND. As shown in the previous section, connecting the load from OUTx to VM is also possible, but there can be some small leakage current into OUTx when the output is disabled.

### 8.2.4.3 Application Curves




A. Channel 1 = IN1 Channel 2 = IN2 Channel 3 = $V_{OUT1}$ Channel 4 = $V_{OUT2}$ Channel 6 = Relay Switch Channel 7 = Relay Coil1 Current Channel 8 = Relay Coil2 Current

**Figure 8-24. PWM driving for dual-coil relay**

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### 8.2.5 Current Sense

A small shunt resistor on the GND pin can provide current sense information back to the microcontroller ADC. The microcontroller can use this information to detect motor load conditions, such as stall. If better current sensing dynamic range is needed, an amplifier can be added as shown in Figure 8-26.

The thermal pad can be connected to the board ground net or the GND pin/sense signal net.

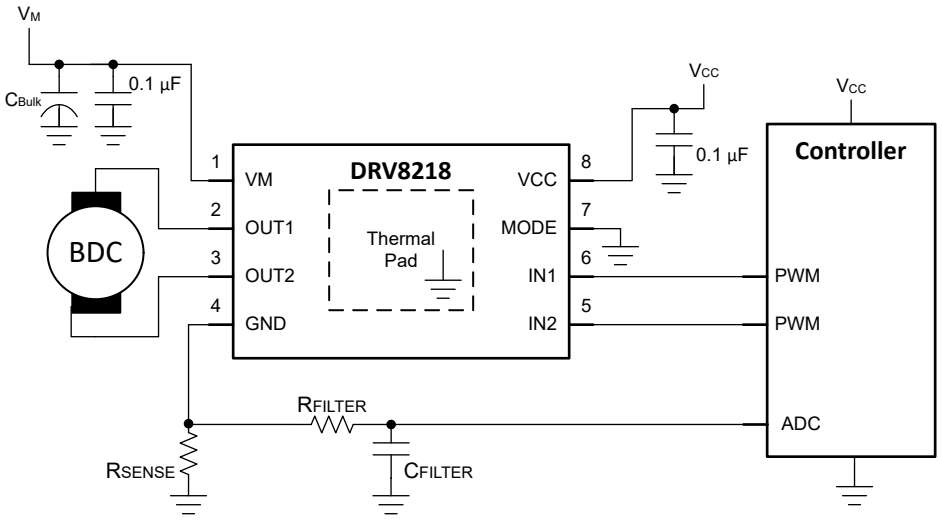


**Figure 8-25. Shunt resistor on GND pin**

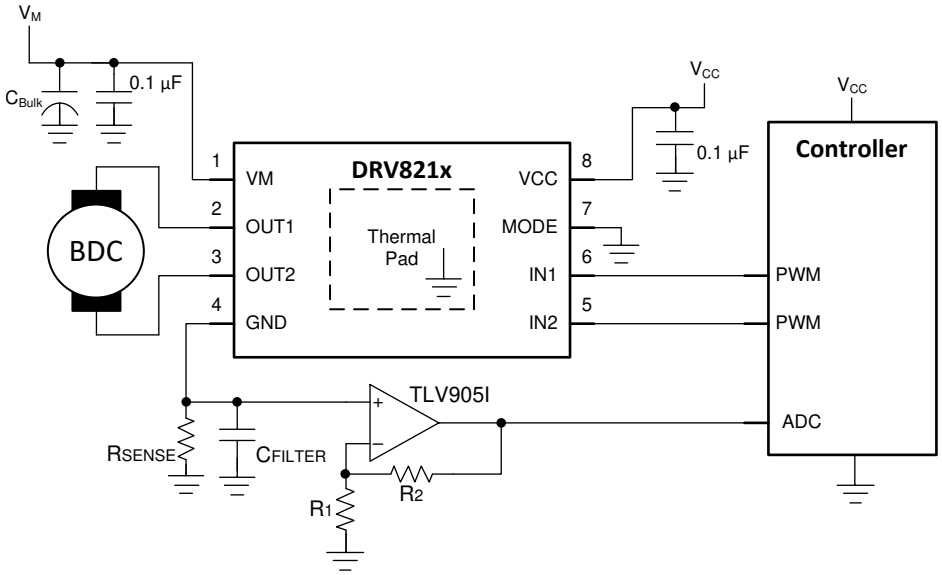


**Figure 8-26. Current sense amplifier with shunt resistor on GND pin example**

#### 8.2.5.1 Design Requirements

Table 8-3 provides example requirements for a current sensing application.

**Table 8-3. System design requirements**

| DESIGN PARAMETER | REFERENCE | EXAMPLE VALUE |
|---|---|---|
| Motor supply voltage | $V_M$ | 5V |
| Logic supply voltage | $V_{CC}$ | 3.3V |
| Maximum voltage across $R_{SENSE}$ | $V_{SENSE}$ | 150mV |

**Table 8-3. System design requirements (continued)**

| DESIGN PARAMETER | REFERENCE | EXAMPLE VALUE |
|---|---|---|
| Motor RMS current | $I_{OUT1}$, $I_{OUT2}$ | 2.0A |
| Motor stall current | $I_{OUT1,stall}$, $I_{OUT2,stall}$ | 6.0A |

#### 8.2.5.2 Detailed Design Procedure

##### *8.2.5.2.1 Shunt Resistor Sizing*

The Absolute Maximum Ratings for the INx pins set the maximum voltage across the shunt resistor. If the signal on the INx pin is low, referenced at the board ground, then the INx pins are at a negative voltage with respect to the GND pin voltage. This sets the maximum sense voltage/GND pin voltage to 0.5V. Figure 8-27 shows the relative pin voltages.

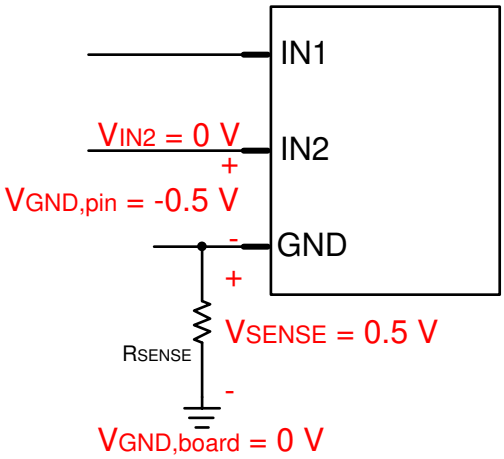


**Figure 8-27. Pin voltages with respect to board ground using current sense resistor**

This example uses 150mV for the maximum $V_{SENSE}$, which is less than 0.5V and provides some margin for safety or error. The maximum current through the motor is the stall current, which is 6.0A for this example. With this information, the sense resistance $R_{SENSE}$ can be calculated from the equation below.

$$R_{SENSE} = V_{SENSE} / I_{STALL} = 0.15V / 6.0A = 0.025\Omega \quad (1)$$

Because the device GND pin voltage varies with current through the sense resistor, the sense resistor must be selected such that the logic pins meet $V_{IL}$ and $V_{IH}$ parameters, the MODE pin meets the $V_{TIL}$, $V_{TIZ}$, and $V_{TIH}$ parameters, and the supply remains above $V_{UVLO}$ for proper operation.

##### *8.2.5.2.2 RC Filter*

The RC filter shown in Figure 8-25 is used to filter noise and transients from the sense signal. TI recommends $R_{FILTER}$ = 1kΩ and $C_{FILTER}$ = 100nF. Different values can be chosen depending on the specific system conditions.

## 8.3 Current Capability and Thermal Performance

The output current and power dissipation capabilities of the driver depends heavily on the PCB design and external system conditions. See the Application Note *Understanding Motor Driver Current Ratings* for the meaning of different current ratings applied to TI motor drivers and PCB layout techniques.

The motor driver can experience different transient driving conditions that cause large currents to flow for a short duration of time. These can include

- Motor start-up when the rotor is initially stationary.
- Fault conditions when there is a supply or ground short to one of the motor outputs, and the overcurrent protection triggers.
- Briefly energizing a motor or solenoid for a limited time, then de-energizing.

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### 8.3.1 Power Dissipation and Output Current Capability

Total power dissipation for the device consists of three main components: quiescent supply current dissipation ($P_{VM}$ and $P_{VCC}$), the power MOSFET switching losses ($P_{SW}$), and the power MOSFET $R_{DS(on)}$ (conduction) losses ($P_{RDS}$). While other factors can contribute additional power losses, these other losses are typically insignificant compared to the three main items.

$$P_{TOT} = P_{VM} + P_{VCC} + P_{SW} + P_{RDS} \quad (2)$$

$P_{VM}$ can be calculated from the nominal motor supply voltage ($V_{VM}$) and the $I_{VM}$ active mode current specification. $P_{VCC}$ can be calculated from the nominal logic supply voltage ($V_{VCC}$) and the $I_{VCC}$ active mode current specification. When $V_{VCC} < V_{VM}$, the DRV8218 draws active current from the VM pin rather than the VCC pin. During this operating condition, $I_{VCC}$ is typically less than 500nA.

$$P_{VM} = V_{VM} \times I_{VM} \quad (3)$$

$$P_{VM} = 7.5mW = 5V \times 1.5mA \quad (4)$$

$$P_{VCC} = V_{VCC} \times I_{VCC} \quad (5)$$

$$P_{VCC} = 1.0mW = 3.3V \times 0.3mA \quad (6)$$

$P_{SW}$ can be calculated from the nominal motor supply voltage ($V_{VM}$), average output current ($I_{RMS}$), switching frequency ($f_{PWM}$) and the device output rise ($t_{RISE}$) and fall ($t_{FALL}$) time specifications.

$$P_{SW} = P_{SW\_RISE} + P_{SW\_FALL} \quad (7)$$

$$P_{SW\_RISE} = 0.5 \times V_M \times I_{RMS} \times t_{RISE} \times f_{PWM} \quad (8)$$

$$P_{SW\_FALL} = 0.5 \times V_M \times I_{RMS} \times t_{FALL} \times f_{PWM} \quad (9)$$

$$P_{SW\_RISE} = 15mW = 0.5 \times 5V \times 2.0A \times 150ns \times 20kHz \quad (10)$$

$$P_{SW\_FALL} = 15mW = 0.5 \times 5V \times 2.0A \times 150ns \times 20kHz \quad (11)$$

$$P_{SW} = 30mW = 15mW + 15mW \quad (12)$$

$P_{RDS}$ can be calculated from the device $R_{DS(on)}$ and average output current ($I_{RMS}$).

$$P_{RDS} = I_{RMS}^{2} \times (R_{DS(ON)\_HS} + R_{DS(ON)\_LS}) \quad (13)$$

$R_{DS(ON)}$ has a strong correlation with the device temperature. Assuming a device junction temperature of 85°C, $R_{DS(on)}$ can increase approximately 1.5x based on the normalized temperature data. The calculation below shows this derating factor. Alternatively, the Section 6.8 section shows curves that plot how $R_{DS(on)}$ changes with temperature.

$$P_{RDS} = 480mW = (2.0A)^2 \times (40m\Omega \times 1.5 + 40m\Omega \times 1.5) \quad (14)$$

Based on the example calculations above, the expressions below calculate the total expected power dissipation for the device.

$$P_{TOT} = P_{VM} + P_{VCC} + P_{SW} + P_{RDS} \quad (15)$$

$$P_{TOT} = 518mW = 7.5mW + 1.0mW + 30mW + 480mW \quad (16)$$

The driver junction temperature can be estimated using $P_{TOT}$, device ambient temperature ($T_A$), and package thermal resistance ($R_{\theta JA}$). The value for $R_{\theta JA}$ depends heavily on the PCB design and copper heat sinking around the device.

$$T_J = (P_{TOT} \times R_{\theta JA}) + T_A \quad (17)$$

$$T_J = 117°C = (0.518W \times 60.9°C/W) + 85°C \quad (18)$$

The device junction temperature must remain below the absolute maximum rating for all system operating conditions. The calculations in this section provide reasonable estimates for junction temperature. However, other methods based on temperature measurements taken during system operation are more realistic and reliable. Additional information on motor driver current ratings and power dissipation can be found in Section 9.1.1.

The motor driver can experience different transient driving conditions that cause large currents to flow for a short duration of time. These can include

- Motor start-up when the rotor is initially stationary.
- Fault conditions when there is a supply or ground short to one of the motor outputs, and the overcurrent protection triggers.
- Briefly energizing a motor or solenoid for a limited time, then de-energizing.

See *Understanding Motor Driver Current Ratings* Application Report for a deeper explanation of the meaning of different current ratings on TI motor drivers and PCB layout techniques.

ADVANCE INFORMATION

## 8.4 Power Supply Recommendations

### *8.4.1 Bulk Capacitance*

Appropriate local bulk capacitance is an important factor in motor drive system design. Having more bulk capacitance is generally beneficial, although the disadvantages include increased cost and physical size. Bulk capacitors near the motor driver act as a local reservoir of electrical charge to smooth out the motor current variation.

Experienced engineers often use general guidelines about bulk capacitance to select the capacitor values. One such guideline says to use at least 1 to 4µF of capacitance for each Watt of motor power. For example, a motor which draws 3 Amps from a 5V supply has a power of 15 Watts, leading to bulk capacitance of 15 to 60µF, using this general guideline.

The voltage rating for bulk capacitors must be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

A large value of bulk capacitance is desired to provide a constant motor supply voltage during current transitions, such as motor start-up, changes in load torque, or PWM operation. A working estimate of the required capacitance for consistent supply is essential to reduce complexity, cost and size of board electronics. We can use a general guideline method to find an appropriate capacitor size based on the expected load current variation and allowable motor supply voltage variation:

$$C_{BULK} > k \quad \times \quad \Delta I_{MOTOR} \times T_{PWM} / \Delta V_{SUPPLY} \tag{19}$$

Where:

$C_{BULK}$ is the bulk capacitance

$k$ is a scale factor to account for the ESR for typical capacitors in this type of application; based on the lab measurements with DRV8718-Q1EVM, k ≈ 3 is practical for these cases.

$\Delta I_{MOTOR}$ is the expected variation in motor current, $i_{max} - i_{min}$

$T_{PWM}$ is the PWM period which is the reciprocal of the PWM frequency

$\Delta V_{SUPPLY}$ is the allowable variation in the motor supply voltage

Figure 8-28 plots several data points and applies this general guideline, showing relatively good agreement.

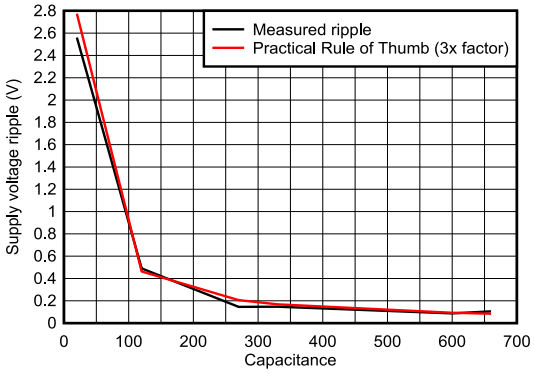


**Figure 8-28. Measured Results and 3x General Guideline, Accounting for Real-World Non-Zero ESR Values of Electrolytic Capacitors**

For more information please see the Application Note SLVAFT0.

## 8.5 Layout

### 8.5.1 Layout Guidelines

Since the DRV8218 device has integrated power MOSFETs capable of driving high current, careful attention must be paid to the layout design and external component placement. Some design and layout guidelines are provided below. For more information on layout recommendations, please see the application note *Best Practices for Board Layout of Motor Drivers*.

- Bypass the VM and VCC pins to GND using low-ESR ceramic bypass capacitors. A capacitance of 0.1uF and X5R and X7R types are recommended. For best results, place these capacitors as close to the device as possible to minimize the loop inductance.
- The VM power supply bulk capacitor can be of ceramic or electrolytic type, and is also recommended to be placed as close as possible to the device to minimize the loop inductance.
- VM, OUT1, OUT2, and GND carry the high current from the power supply to the outputs and back to ground. Utilize thick metal routing or custom polygon pours for these traces if feasible.
- Connect the device thermal pad to the PCB top layer ground plane and internal ground plane (when available) through thermal vias to maximize the PCB heat sinking.
- Maximize the copper plane area attached to the thermal pad for heat sinking.
- See Application Note - Best Practices for Board Layout of Motor Drivers for more information on thermal management, routing techniques, capacitor placement, and grounding optimization for motor drivers.

### 8.5.2 Layout Example

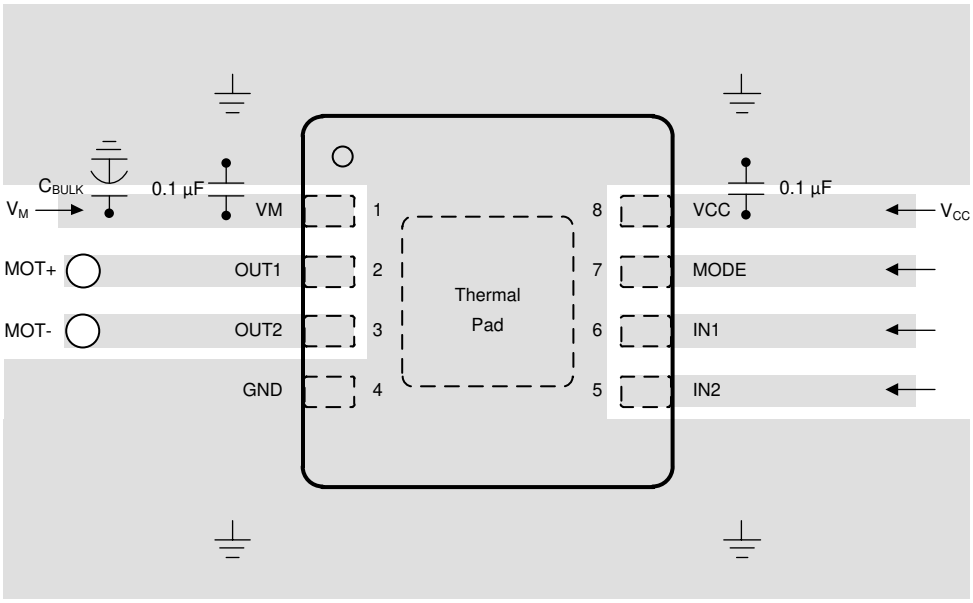


**Figure 8-29. Simplified Layout Example for DSG package**

ADVANCE INFORMATION

# 9 Device and Documentation Support

## 9.1 Documentation Support

### *9.1.1 Related Documentation*

For related documentation see the following:

- Texas Instruments, *Calculating Motor Driver Power Dissipation* application report
- Texas Instruments, *PowerPAD™ Made Easy application report* application report
- Texas Instruments, *PowerPAD™ Thermally Enhanced Package* application report
- Texas Instruments, *Understanding Motor Driver Current Ratings* application report
- Texas Instruments, *Best Practices for Board Layout of Motor Drivers* application report

## 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 Support Resources

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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

ADVANCE INFORMATION

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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