DRV832x 6 to 60-V Three-Phase Smart Gate Driver

1 Features

- Triple Half-Bridge Gate Driver
  - Drives 3 High-Side and 3 Low-Side N-Channel MOSFETs (NMOS)
- Smart Gate Drive Architecture
  - Adjustable Slew Rate Control
  - 10-mA to 1-A Peak Source Current
  - 20-mA to 2-A Peak Sink Current
- Integrated Gate Driver Power Supplies
  - Supports 100% PWM Duty Cycle
  - High-Side Charge Pump
  - Low-Side Linear Regulator
- 6 to 60-V Operating Voltage Range
- Optional Integrated DC/DC Buck Regulator
  - LMR16006X SIMPLE SWITCHER®
  - 4 to 60-V Operating Voltage Range
  - 0.8 to 60-V, 600-mA Output Capability
- Optional Integrated Triple Low-Side Current Sense Amplifiers (CSAs)
  - Adjustable Gain (5, 10, 20, 40 V/V)
  - Bidirectional or Unidirectional Support
- SPI and Hardware Interface Available
- 6x, 3x, 1x, and Independent PWM Modes
- Supports 1.8-V, 3.3-V, and 5-V Logic Inputs
- Low-Power Sleep Mode (12 µA)
- Linear Voltage Regulator, 3.3 V, 30 mA
- Compact QFN Packages and Footprints
- Efficient System Design With Power Blocks
- Integrated Protection Features
  - VM Undervoltage Lockout (UVLO)
  - Charge Pump Undervoltage (CPUV)
  - MOSFET Overcurrent Protection (OCP)
  - Gate Driver Fault (GDF)
  - Thermal Warning and Shutdown (OTW/OTSD)
  - Fault Condition Indicator (nFAULT)

2 Applications

- Brushless-DC (BLDC) Motor Modules and PMSM
- Fans, Pumps, and Servo Drives
- E-Bikes, E-Scooters, and E-Mobility
- Cordless Garden and Power Tools, Lawnmowers
- Cordless Vacuum Cleaners
- Drones, Robotics, and RC Toys
- Industrial and Logistics Robots

3 Description

The DRV832x family of devices is an integrated gate driver for three-phase applications. The devices provide three half-bridge gate drivers, each capable of driving high-side and low-side N-channel power MOSFETs. The DRV832x generates the correct gate drive voltages using an integrated charge pump for the high-side MOSFETs and a linear regulator for the low-side MOSFETs. The Smart Gate Drive architecture supports peak gate drive currents up to 1A source and 2A. The DRV832x can operate from a single power supply and supports a wide input supply range of 6 to 60 V for the gate driver and 4 to 60 V for the optional buck regulator.

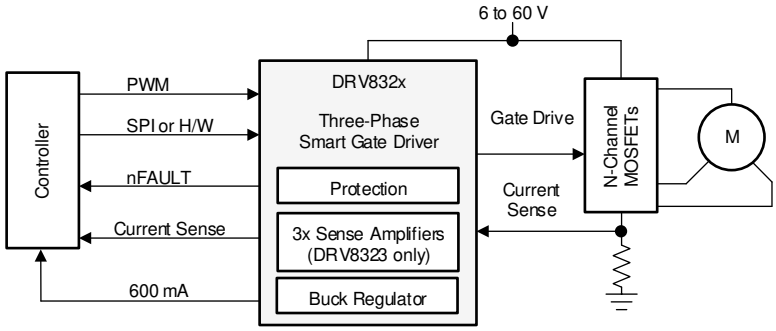
The 6x, 3x, 1x, and independent input PWM modes allow for simple interfacing to controller circuits. The configuration settings for the gate driver and device are highly configurable through the SPI or hardware (H/W) interface. The DRV8323 and DRV8323R devices integrate three low-side current sense amplifiers that allow bidirectional current sensing on all three phases of the drive stage. The DRV8320R and DRV8323R devices integrate a 600mA DC/DC buck regulator.

A low-power sleep mode is provided to achieve low quiescent current draw by shutting down most of the internal circuitry. Internal protection functions are provided for undervoltage lockout, charge pump fault, MOSFET overcurrent, MOSFET short circuit, gate driver fault, and overtemperature. Fault conditions are indicated on the nFAULT pin with details through the device registers for SPI device variants.

Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
DRV8320	WQFN (32)	5.00mm × 5.00mm
DRV8320R	VQFN (40)	6.00mm × 6.00mm
DRV8323	WQFN (40)	6.00mm × 6.00mm
DRV8323R	VQFN (48)	7.00mm × 7.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (August 2018) to Revision D (March 2022)	Page
• Added information in the Sleep Mode section on the behavior of GHx and GLx w hen Enable is pulled low..	51

Changes from Revision B (December 2017) to Revision C (August 2018)	Page
• Changed the *Applications*	1
• Updated input labels for the INLx and INHx signals in the *Layout Example* imags	77
• Added the DRV835x device options to the image in the *Device Nomenclature* section	78

Changes from Revision A (April 2017) to Revision B (December 2017)	Page
• Changed the low-power sleep mode supply current from the maximum value (20 µA) to the typical value (12 µA) in the *Features*	1
• Changed the *Applications*	1
• Changed the GAIN value from 45kΩ to 47kΩ in the test condition of the amplifier gain for the H/W device in the *Electrical Characteristics* table	14
• Deleted t_{EN_nSCS} from the *SPI Secondary Mode Timing Diagram*	19
• Added a note to the *Synchronous 1x PWM Mode* to define *!PWM*	32
• Updated the *Auto Offset Calibration* section	45
• Updated the V_{DS} *Latched Shutdown* and V_{DS} *Automatic Retry* sections	49
• Updated the *Sleep Mode* section	51
• Changed the address listed in the title for the *Gate Drive LS Register* section to the correct register address, 0x04	60
• Changed the maximum Q_g value for both trapezoidal and sinusoidal commutation the V_{VM} = 8 V example of the *Detailed Design Procedure*	65
• Changed I_{DRIVEP} and I_{DRIVEN} equations in the *IDRIVE Configuration* section	65

Changes from Revision * (February 2017) to Revision A (April 2017) **Page**

- Changed the test condition for the I_{BIAS} parameter in the *Electrical Characteristics* table 14
- Changed the GHx values in the *3x PWM Mode Truth Table* 32
- Changed the calibration description and added auto calibration feature description 45

5 Device Comparison Table

DEVICE	VARIANT(1)	CURRENT SENSE AMPLIFIERS	BUCK REGULATOR(1)	INTERFACE(1)
DRV8320	DRV8320H	0	None	Hardware
	DRV8320S			SPI
DRV8320R	DRV8320RH		600 mA	Hardware
	DRV8320RS			SPI
DRV8323	DRV8323H	3	None	Hardware
	DRV8323S			SPI
DRV8323R	DRV8323RH		600 mA	Hardware
	DRV8323RS			SPI

(1) For more information on the device name and device options, see *Section 12.1.1*. For additional details, see the *Architecture for Brushless-DC Gate Drive Systems* application report.

6 Pin Configuration and Functions

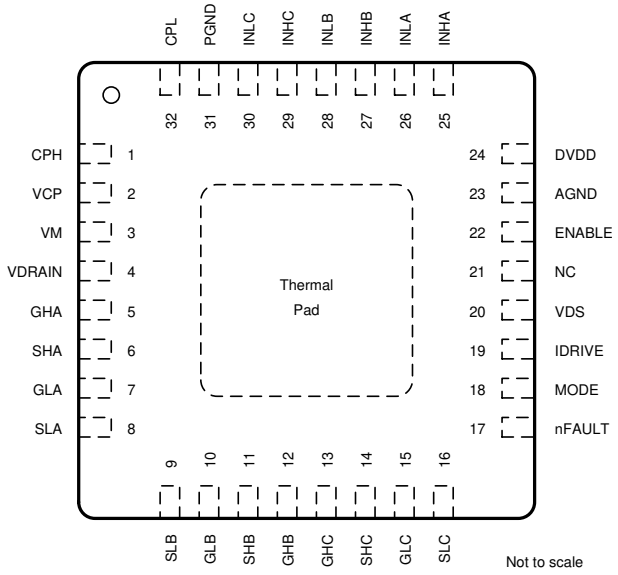


Figure 6-1. DRV8320H RTV Package 32-Pin WQFN With Exposed Thermal Pad Top View

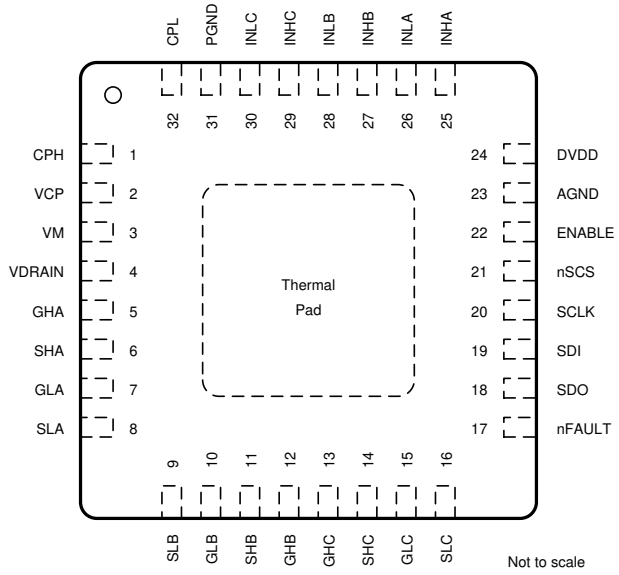


Figure 6-2. DRV8320S RTV Package 32-Pin WQFN With Exposed Thermal Pad Top View

Table 6-1. Pin Functions—32-Pin DRV8320 Devices

PIN			TYPE(1)	DESCRIPTION
NAME	NO.			
	DRV8320H	DRV8320S		
AGND	23	23	PWR	Device analog ground. Connect to system ground. AGND must be connected to PGND externally.
CPH	1	1	PWR	Charge pump switching node. Connect an X5R or X7R, 47nF, VM-rated ceramic capacitor between the CPH and CPL pins. For example, in a 24V system the capacitor should be rated 50V (2x margin).
CPL	32	32	PWR	
DVDD	24	24	PWR	3.3V internal regulator output. Connect an X5R or X7R, 1µF, 6.3V ceramic capacitor between the DVDD and AGND pins. This regulator can source up to 30 mA externally.
ENABLE	22	22	I	Gate driver enable. When this pin is logic low the device goes to a low-power sleep mode. An 8 to 40µs pulse can be used to reset fault conditions without entering sleep mode.
GHA	5	5	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHB	12	12	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHC	13	13	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GLA	7	7	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GLB	10	10	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.

Table 6-1. Pin Functions—32-Pin DRV8320 Devices (continued)

PIN			TYPE[1]	DESCRIPTION
NAME	NO.			
	DRV8320H	DRV8320S		
GLC	15	15	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
IDRIVE	19	—	I	Gate drive output current setting. This pin is a 7 level input pin set by an external resistor.
INHA	25	25	I	High-side gate driver control input. This pin controls the output of the high-side gate driver when using 6x PWM mode.
INHB	27	27	I	High-side gate driver control input. This pin controls the output of the high-side gate driver when using 6x PWM mode.
INHC	29	29	I	High-side gate driver control input. This pin controls the output of the high-side gate driver when using 6x PWM mode.
INLA	26	26	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver when using 6x PWM mode.
INLB	28	28	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver when using 6x PWM mode.
INLC	30	30	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver when using 6x PWM mode.
MODE	18	—	I	PWM input mode setting. This pin is a 4 level input pin set by an external resistor.
NC	21	—	NC	No internal connection. This pin can be left floating or connected to system ground.
nFAULT	17	17	OD	Fault indicator output. This open drain pin pulls logic low during a fault condition and requires an external pullup resistor.
nSCS	—	21	I	Serial chip select. A logic low on this pin enables serial interface communication.
PGND	31	31	PWR	Device power ground. Also used as the gate drive sink path for the low side MOSFETs. Connect to system ground. PGND must be connected to AGND externally.
SCLK	—	20	I	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin.
SDI	—	19	I	Serial data input. Data is captured on the falling edge of the SCLK pin.
SDO	—	18	OD	Serial data output. Data is shifted out on the rising edge of the SCLK pin. This open drain pin requires an external pullup resistor.
SHA	6	6	I/O	High-side source pin. Connect to the high-side power MOSFET source. This pin is an input for the VDS monitor and the output for the high-side gate driver sink.
SHB	11	11	I/O	High-side source pin. Connect to the high-side power MOSFET source. This pin is an input for the VDS monitor and the output for the high-side gate driver sink.
SHC	14	14	I/O	High-side source pin. Connect to the high-side power MOSFET source. This pin is an input for the VDS monitor and the output for the high-side gate driver sink.
SLA	8	8	I	Low-side source input. Connect to the low-side power MOSFET source. This pin is an input for the VDS monitor.
SLB	9	9	I	Low-side source input. Connect to the low-side power MOSFET source. This pin is an input for the VDS monitor.
SLC	16	16	I	Low-side source input. Connect to the low-side power MOSFET source. This pin is an input for the VDS monitor.
VCP	2	2	PWR	Charge pump output. Connect an X5R or X7R, 1µF, 25V ceramic capacitor between the VCP and VM pins.
VDRAIN	4	4	I	High-side MOSFET drain input. Connect to the common point of the high-side MOSFET drains. This pin is an input for the VDS monitor.
VDS	20	—	I	VDS monitor trip point setting. This pin is a 7 level input pin set by an external resistor.
VM	3	3	PWR	Gate driver power supply input. Connect to the motor power supply and VDRAIN. Connect an X5R or X7R, 0.1µF, VM-rated ceramic and greater then or equal to 10-uF local capacitance between the VM and PGND pins.
Thermal Pad	PAD	PAD	PWR	Must be connected to ground

(1) PWR = power, I = input, O = output, NC = no connection, OD = open-drain output

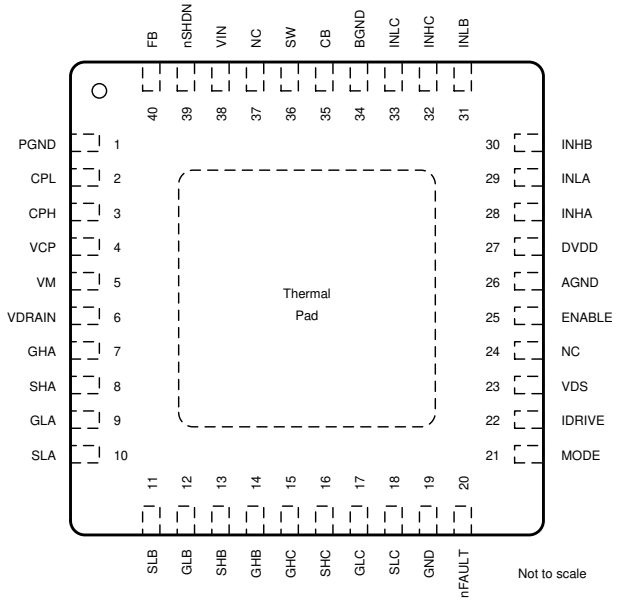


Figure 6-3. DRV8320RH RHA Package 40-Pin VQFN With Exposed Thermal Pad Top View

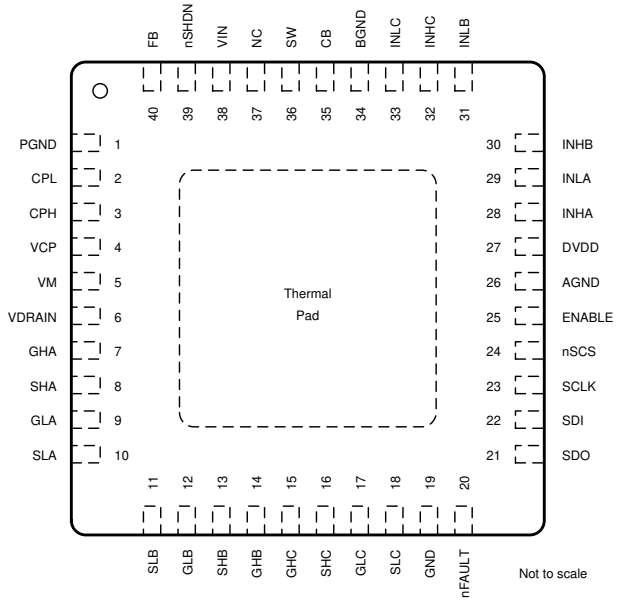


Figure 6-4. DRV8320RS RHA Package 40-Pin VQFN With Exposed Thermal Pad Top View

Table 6-2. Pin Functions—40-Pin DRV8320R Devices

PIN			TYPE[1]	DESCRIPTION
NAME	NO.			
	DRV8320RH	DRV8320RS		
AGND	26	26	PWR	Device analog ground. Connect to system ground. AGND must be connected to BGND and PGND externally.
BGND	34	34	PWR	Buck regulator ground. Connect to system ground. BGND must be connected to AGND and PGND externally.
CB	35	35	PWR	Buck regulator bootstrap input. Connect an X5R or X7R, 0.1µF, 16V, capacitor between the CB and SW pins.
CPH	3	3	PWR	Charge pump switching node. Connect an X5R or X7R, 47nF, VM-rated ceramic capacitor between the CPH and CPL pins. For example, in a 24V system the capacitor should be rated 50V (2x margin).
CPL	2	2	PWR	
DVDD	27	27	PWR	3.3V internal regulator output. Connect an X5R or X7R, 1µF, 6.3V ceramic capacitor between the DVDD and AGND pins. This regulator can source up to 30mA externally.
ENABLE	25	25	I	Gate driver enable. When this pin is logic low the device goes to a low-power sleep mode. An 8 to 40µs low pulse can be used to reset fault conditions without entering sleep mode.
FB	40	40	I	Buck feedback input. A resistor divider from the buck post inductor output to this pin sets the buck output voltage.
GHA	7	7	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHB	14	14	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHC	15	15	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GLA	9	9	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GLB	12	12	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GLC	17	17	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GND	19	19	PWR	Device ground. Connect to system ground.
IDRIVE	22	—	I	Gate drive output current setting. This pin is a 7 level input pin set by an external resistor.
INHA	28	28	I	High-side gate driver control input. This pin controls the output of the high-side gate driver when using 6x PWM mode.
INHB	30	30	I	High-side gate driver control input. This pin controls the output of the high-side gate driver when using 6x PWM mode.
INHC	32	32	I	High-side gate driver control input. This pin controls the output of the high-side gate driver when using 6x PWM mode.
INLA	29	29	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver when using 6x PWM mode.
INLB	31	31	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver when using 6x PWM mode.
INLC	33	33	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver when using 6x PWM mode.
MODE	21	—	I	PWM input mode setting. This pin is a 4 level input pin set by an external resistor.
NC	24	—	NC	No internal connection. This pin can be left floating or connected to system ground.
NC	37	37	NC	No internal connection. This pin can be left floating or connected to system ground.
nFAULT	20	20	OD	Fault indicator output. This open drain pin pulls logic low during a fault condition and requires an external pullup resistor.
nSCS	—	24	I	Serial chip select. A logic low on this pin enables serial interface communication.
nSHDN	39	39	I	Buck shutdown input. Enable and disable input (high voltage tolerant). Internal pullup current source. Pull lower than 1.25V to disable. Float to enable. Establish input undervoltage lockout with two resistor divider.

Table 6-2. Pin Functions—40-Pin DRV8320R Devices (continued)

PIN			TYPE(1)	DESCRIPTION
NAME	NO.			
	DRV8320RH	DRV8320RS		
PGND	1	1	PWR	Device power ground. Also used as the gate drive sink path for the low side MOSFETs. Connect to system ground. PGND mut be connected to AGND and BGND externally.
SCLK	—	23	I	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin.
SDI	—	22	I	Serial data input. Data is captured on the falling edge of the SCLK pin.
SDO	—	21	OD	Serial data output. Data is shifted out on the rising edge of the SCLK pin. This open drain pin requires an external pullup resistor.
SHA	8	8	I/O	High-side source pin. Connect to the high-side power MOSFET source. This pin is an input for the VDS monitor and the output for the high-side gate driver sink.
SHB	13	13	I/O	High-side source pin. Connect to the high-side power MOSFET source. This pin is an input for the VDS monitor and the output for the high-side gate driver sink.
SHC	16	16	I/O	High-side source pin. Connect to the high-side power MOSFET source. This pin is an input for the VDS monitor and the output for the high-side gate driver sink.
SLA	10	10	I	Low-side source input. Connect to the low-side power MOSFET source. This pin is an input for the VDS monitor.
SLB	11	11	I	Low-side source input. Connect to the low-side power MOSFET source. This pin is an input for the VDS monitor.
SLC	18	18	I	Low-side source input. Connect to the low-side power MOSFET source. This pin is an input for the VDS monitor.
SW	36	36	O	Buck switch node. Connect this pin to an inductor, diode, and the CB bootstrap capacitor.
VCP	4	4	PWR	Charge pump output. Connect an X5R or X7R, 1µF, 25V ceramic capacitor between the VCP and VM pins.
VDRAIN	6	6	I	High-side MOSFET drain input. Connect to the common point of the high-side MOSFET drains. This pin is an input for the VDS monitor.
VDS	23	—	I	VDS monitor trip point setting. This pin is a 7 level input pin set by an external resistor.
VIN	38	38	PWR	Buck regulator power supply input. Place an X5R or X7R, VM-rated ceramic capacitor between the VIN and BGND pins.
VM	5	5	PWR	Gate driver power supply input. Connect to the motor power supply and VDRAIN. Connect an X5R or X7R, 0.1µF, VM-rated ceramic and greater then or equal to 10-uF local capacitance between the VM and PGND pins.
Thermal Pad	PAD	PAD	PWR	Must be connected to ground

(1) PWR = power, I = input, O = output, NC = no connection, OD = open-drain output

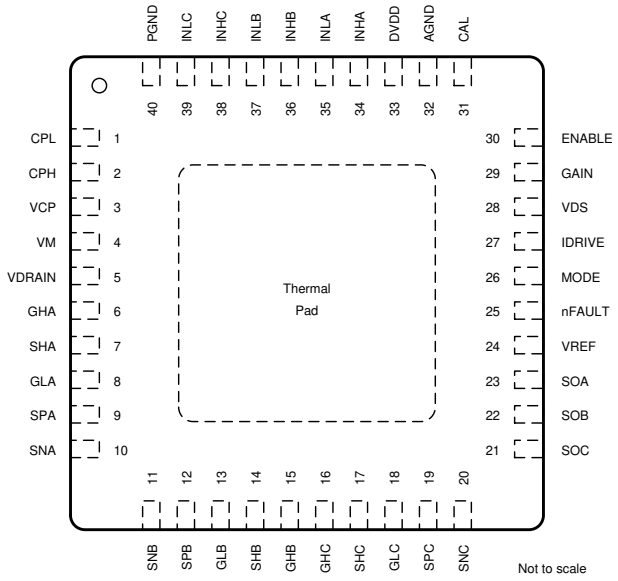


Figure 6-5. DRV8323H RTA Package 40-Pin WQFN With Exposed Thermal Pad Top View

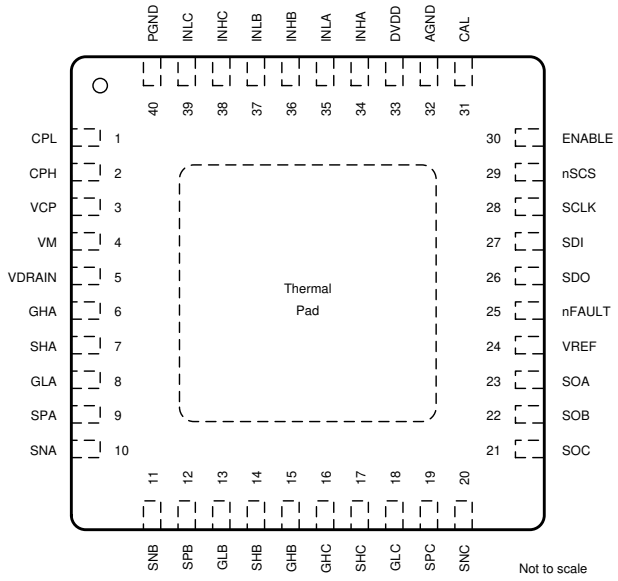


Figure 6-6. DRV8323S RTA Package 40-Pin WQFN With Exposed Thermal Pad Top View

Table 6-3. Pin Functions—40-Pin DRV8323 Devices

PIN			TYPE(1)	DESCRIPTION
NAME	NO.			
	DRV8323H	DRV8323S		
AGND	32	32	PWR	Device analog ground. Connect to system ground. AGND must be connected to PGND externally.

Table 6-3. Pin Functions—40-Pin DRV8323 Devices (continued)

PIN			TYPE[1]	DESCRIPTION
NAME	NO.			
	DRV8323H	DRV8323S		
CAL	31	31	I	Amplifier calibration input. Set logic high to internally short amplifier inputs and perform auto offset calibration.
CPH	2	2	PWR	Charge pump switching node. Connect an X5R or X7R, 47nF, VM-rated ceramic capacitor between the CPH and CPL pins. For example, in a 24V system the capacitor should be rated 50V (2x margin).
CPL	1	1	PWR	
DVDD	33	33	PWR	3.3V internal regulator output. Connect an X5R or X7R, 1µF, 6.3V ceramic capacitor between the DVDD and AGND pins. This regulator can source up to 30mA externally.
ENABLE	30	30	I	Gate driver enable. When this pin is logic low the device goes to a low-power sleep mode. An 8 to 40µs low pulse can be used to reset fault conditions without entering sleep mode.
GAIN	29	—	I	Amplifier gain setting. The pin is a 4 level input pin set by an external resistor.
GHA	6	6	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHB	15	15	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHC	16	16	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GLA	8	8	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GLB	13	13	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GLC	18	18	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
IDRIVE	27	—	I	Gate drive output current setting. This pin is a 7 level input pin set by an external resistor.
INHA	34	34	I	High-side gate driver control input. This pin controls the output of the high-side gate driver when using 6x PWM mode.
INHB	36	36	I	High-side gate driver control input. This pin controls the output of the high-side gate driver when using 6x PWM mode.
INHC	38	38	I	High-side gate driver control input. This pin controls the output of the high-side gate driver when using 6x PWM mode.
INLA	35	35	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver when using 6x PWM mode.
INLB	37	37	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver when using 6x PWM mode.
INLC	39	39	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver when using 6x PWM mode.
MODE	26	—	I	PWM input mode setting. This pin is a 4 level input pin set by an external resistor.
nFAULT	25	25	OD	Fault indicator output. This open drain pin pulls logic low during a fault condition and requires an external pullup resistor.
nSCS	—	29	I	Serial chip select. A logic low on this pin enables serial interface communication.
PGND	40	40	PWR	Device power ground. Also used as the gate drive sink path for the low side MOSFETs. Connect to system ground. PGND must be connected to AGND externally.
SCLK	—	28	I	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin.
SDI	—	27	I	Serial data input. Data is captured on the falling edge of the SCLK pin.
SDO	—	26	OD	Serial data output. Data is shifted out on the rising edge of the SCLK pin. This open drain pin requires an external pullup resistor.
SHA	7	7	I/O	High-side source pin. Connect to the high-side power MOSFET source. This pin is an input for the VDS monitor and the output for the high-side gate driver sink.
SHB	14	14	I/O	High-side source pin. Connect to the high-side power MOSFET source. This pin is an input for the VDS monitor and the output for the high-side gate driver sink.
SHC	17	17	I/O	High-side source pin. Connect to the high-side power MOSFET source. This pin is an input for the VDS monitor and the output for the high-side gate driver sink.
SNA	10	10	I	Current sense amplifier input. Connect to the low-side of the current shunt resistor. If CSA is not used tie to PGND.
SNB	11	11	I	Current sense amplifier input. Connect to the low-side of the current shunt resistor. If CSA is not used tie to PGND.
SNC	20	20	I	Current sense amplifier input. Connect to the low-side of the current shunt resistor. If CSA is not used tie to PGND.
SOA	23	23	O	Current sense amplifier output. If CSA is not used leave this pin disconnected.
SOB	22	22	O	Current sense amplifier output. If CSA is not used leave this pin disconnected.
SOC	21	21	O	Current sense amplifier output. If CSA is not used leave this pin disconnected.
SPA	9	9	I	Low-side current shunt amplifier input. Also VDS monitor negative input for low side MOSFET. Connect to the low-side power MOSFET source and high-side of the current shunt resistor. If CSA is not used tie to SNA.
SPB	12	12	I	Low-side current shunt amplifier input. Also VDS monitor negative input for low side MOSFET. Connect to the low-side power MOSFET source and high-side of the current shunt resistor. If CSA is not used tie to SNB.
SPC	19	19	I	Low-side current shunt amplifier input. Also VDS monitor negative input for low side MOSFET. Connect to the low-side power MOSFET source and high-side of the current shunt resistor. If CSA is not used tie to SNC.
VCP	3	3	PWR	Charge pump output. Connect an X5R or X7R, 1µF, 25V ceramic capacitor between the VCP and VM pins.
VDRAIN	5	5	I	High-side MOSFET drain input. Connect to the common point of the high-side MOSFET drains. This pin is an input for the VDS monitor.
VDS	28	—	I	VDS monitor trip point setting. This pin is a 7 level input pin set by an external resistor.
VM	4	4	PWR	Gate driver power supply input. Connect to the motor power supply and VDRAIN. Connect an X5R or X7R, 0.1µF, VM-rated ceramic and greater then or equal to 10uF local capacitance between the VM and PGND pins.
VREF	24	24	PWR	Current sense amplifier power supply input and reference. Connect an X5R or X7R, 0.1µF, 6.3V ceramic capacitor between the VREF and AGND pins.

Table 6-3. Pin Functions—40-Pin DRV8323 Devices (continued)

PIN			TYPE[1]	DESCRIPTION
NAME	NO.			
	DRV8323H	DRV8323S		
Thermal Pad	PAD	PAD	PWR	Must be connected to ground

(1) PWR = power, I = input, O = output, NC = no connection, OD = open-drain output

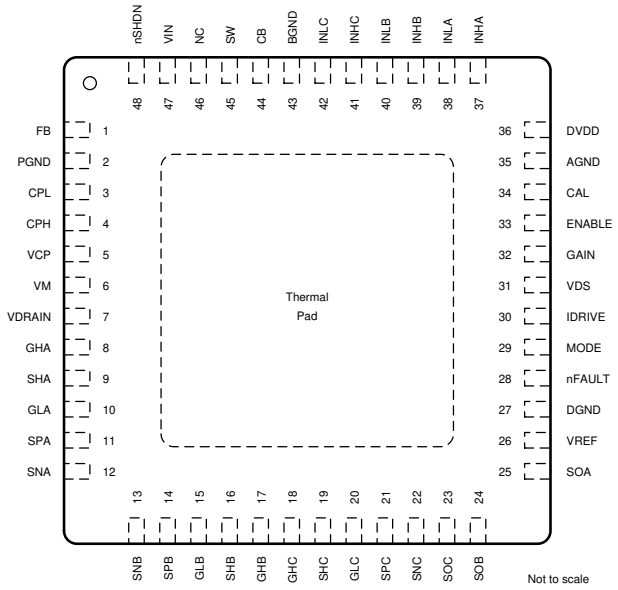


Figure 6-7. DRV8323RH RGZ Package 48-Pin VQFN With Exposed Thermal Pad Top View

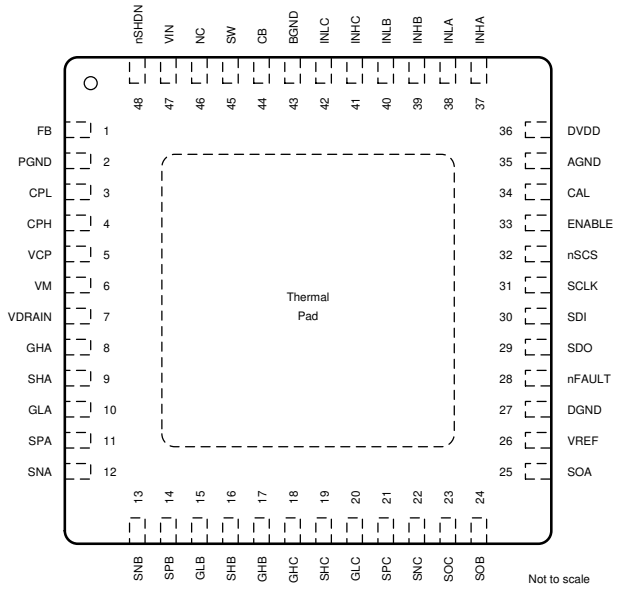


Figure 6-8. DRV8323RS RGZ Package 48-Pin VQFN With Exposed Thermal Pad Top View

Table 6-4. Pin Functions—48-Pin DRV8323R Devices

PIN			TYPE[1]	DESCRIPTION
NAME	NO.			
	DRV8323RH	DRV8323RS		
AGND	35	35	PWR	Device analog ground. Connect to system ground. AGND must be connected to BGND and PGND externally.
BGND	43	43	PWR	Buck regulator ground. Connect to system ground. BGND must be connected to AGND and PGND externally.
CAL	34	34	I	Amplifier calibration input. Set logic high to internally short amplifier inputs and perform auto offset calibration.
CB	44	44	PWR	Buck regulator bootstrap input. Connect an X5R or X7R, 0.1µF, 16V, capacitor between the CB and SW pins.
CPH	4	4	PWR	Charge pump switching node. Connect an X5R or X7R, 47-nF, VM-rated ceramic capacitor between the CPH and CPL pins. For example, in a 24V system the capacitor should be rated 50V (2x margin).
CPL	3	3	PWR	
DGND	27	27	PWR	Device ground. Connect to system ground.
DVDD	36	36	PWR	3.3V internal regulator output. Connect an X5R or X7R, 1µF, 6.3V ceramic capacitor between the DVDD and AGND pins. This regulator can source up to 30mA externally.
ENABLE	33	33	I	Gate driver enable. When this pin is logic low the device goes to a low-power sleep mode. An 8 to 40µs low pulse can be used to reset fault conditions without entering sleep mode.
FB	1	1	I	Buck feedback input. A resistor divider from the buck post inductor output to this pin sets the buck output voltage.
GAIN	32	—	I	Amplifier gain setting. The pin is a 4 level input pin set by an external resistor.
GHA	8	8	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHB	17	17	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GHC	18	18	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET.
GLA	10	10	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GLB	15	15	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
GLC	20	20	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
IDRIVE	30	—	I	Gate drive output current setting. This pin is a 7 level input pin set by an external resistor.
INHA	37	37	I	High-side gate driver control input. This pin controls the output of the high-side gate driver when using 6x PWM mode.
INHB	39	39	I	High-side gate driver control input. This pin controls the output of the high-side gate driver when using 6x PWM mode.

Table 6-4. Pin Functions—48-Pin DRV8323R Devices (continued)

PIN			TYPE[1]	DESCRIPTION
NAME	NO.			
	DRV8323RH	DRV8323RS		
INHC	41	41	I	High-side gate driver control input. This pin controls the output of the high-side gate driver when using 6x PWM mode.
INLA	38	38	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver when using 6x PWM mode.
INLB	40	40	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver when using 6x PWM mode.
INLC	42	42	I	Low-side gate driver control input. This pin controls the output of the low-side gate driver when using 6x PWM mode.
MODE	29	—	I	PWM input mode setting. This pin is a 4 level input pin set by an external resistor.
NC	46	46	NC	No internal connection. This pin can be left floating or connected to system ground.
nFAULT	28	28	OD	Fault indicator output. This open drain pin pulls logic low during a fault condition and requires an external pullup resistor.
nSCS	—	32	I	Serial chip select. A logic low on this pin enables serial interface communication.
nSHDN	48	48	I	Buck shutdown input. Enable and disable input (high voltage tolerant). Internal pullup current source. Pull lower than 1.25V to disable. Float to enable. Establish input undervoltage lockout with two resistor divider.
PGND	2	2	PWR	Device power ground. Also used as the gate drive sink path for the low side MOSFETs. Connect to system ground. PGND must be connected to AGND and BGND externally.
SCLK	—	31	I	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin.
SDI	—	30	I	Serial data input. Data is captured on the falling edge of the SCLK pin.
SDO	—	29	OD	Serial data output. Data is shifted out on the rising edge of the SCLK pin. This open drain pin requires an external pullup resistor.
SHA	9	9	I/O	High-side source pin. Connect to the high-side power MOSFET source. This pin is an input for the VDS monitor and the output for the high-side gate driver sink.
SHB	16	16	I/O	High-side source pin. Connect to the high-side power MOSFET source. This pin is an input for the VDS monitor and the output for the high-side gate driver sink.
SHC	19	19	I/O	High-side source pin. Connect to the high-side power MOSFET source. This pin is an input for the VDS monitor and the output for the high-side gate driver sink.
SNA	12	12	I	Current sense amplifier input. Connect to the low-side of the current shunt resistor. If CSA is not used tie to PGND.
SNB	13	13	I	Current sense amplifier input. Connect to the low-side of the current shunt resistor. If CSA is not used tie to PGND.
SNC	22	22	I	Current sense amplifier input. Connect to the low-side of the current shunt resistor. If CSA is not used tie to PGND.
SOA	25	25	O	Current sense amplifier output. If CSA is not used leave this pin disconnected.
SOB	24	24	O	Current sense amplifier output. If CSA is not used leave this pin disconnected.
SOC	23	23	O	Current sense amplifier output. If CSA is not used leave this pin disconnected.
SPA	11	11	I	Low-side current shunt amplifier input. Also VDS monitor negative input for low side MOSFET. Connect to the low-side power MOSFET source and high-side of the current shunt resistor. If CSA is not used tie to SNA.
SPB	14	14	I	Low-side current shunt amplifier input. Also VDS monitor negative input for low side MOSFET. Connect to the low-side power MOSFET source and high-side of the current shunt resistor. If CSA is not used tie to SNB.
SPC	21	21	I	Low-side current shunt amplifier input. Also VDS monitor negative input for low side MOSFET. Connect to the low-side power MOSFET source and high-side of the current shunt resistor. If CSA is not used tie to SNC.
SW	45	45	O	Buck switch node. Connect this pin to an inductor, diode, and the CB bootstrap capacitor.
VCP	5	5	PWR	Charge pump output. Connect an X5R or X7R, 1µF, 25V ceramic capacitor between the VCP and VM pins.
VDRAIN	7	7	I	High-side MOSFET drain input. Connect to the common point of the high-side MOSFET drains. This pin is an input for the VDS monitor.
VDS	31	—	I	VDS monitor trip point setting. This pin is a 7 level input pin set by an external resistor.
VIN	47	47	PWR	Buck regulator power supply input. Place an X5R or X7R, VM-rated ceramic capacitor between the VIN and BGND pins.
VM	6	6	PWR	Gate driver power supply input. Connect to the motoro power supply and VDRAIN. Connect an X5R or X7R, 0.1µF, VM-rated ceramic and greater then or equal to 10uF local capacitance between the VM and PGND pins.
VREF	26	26	PWR	Current sense amplifier power supply input and reference. Connect an X5R or X7R, 0.1µF, 6.3V ceramic capacitor between the VREF and AGND pins.
Thermal Pad	PAD	PAD	PWR	Must be connected to ground

(1) PWR = power, I = input, O = output, NC = no connection, OD = open-drain output

7 Specifications

7.1 Absolute Maximum Ratings

at T_A = –40°C to +125°C (unless otherwise noted)(1)

	MIN	MAX	UNIT
GATE DRIVER			
Power supply pin voltage (VM)	–0.3	65	V
Voltage differential between ground pins (AGND, BGND, DGND, PGND)	–0.3	0.3	V
MOSFET drain sense pin voltage (VDRAIN)	–0.3	65	V
Charge pump pin voltage (CPH, VCP)	–0.3	V_{VM} + 15.5	V
Continuous charge pump negative-switching pin voltage (CPL)	–0.3	V_{VM} + 1	V
Transient 1-us charge pump negative-switching pin voltage (CPL)	–1		V
Internal logic regulator pin voltage (DVDD)	–0.3	3.8	V
Digital pin voltage (CAL, ENABLE, GAIN, IDRIVE, INHx, INLx, MODE, nFAULT, nSCS, SCLK, SDI, SDO, VDS)	–0.3	5.75	V
Continuous high-side gate driver output pin voltage (GHx)	–5(2)	V_{VCP} + 1	V
Transient 200ns high-side gate driver output pin voltage (GHx)	–7	V_{VCP} + 1	V
High-side gate driver output pin voltage with respect to SHx (GHx)	–1.6	18	V
Continuous high-side source pin voltage (SHx)	–5(2)	V_{VM} + 5	V
Transient 200ns high-side source pin voltage (SHx)	–7	V_{VM} + 7	V
Transient 1-us high-side source pin voltage (SHx)		V_{VCP} - 2	V
Continuous low-side gate driver output pin voltage (GLx)	–0.5	18	V
Transient 200ns low-side gate driver output pin voltage (GLx)	–1.5		V
Gate driver output pin source current (GHx, GLx)	Internally limited		A
Gate driver output pin sink current (GHx, GLx)	Internally limited		A
Continuous voltage at low-side source pin (SLx) and current sense amplifier input pin (SPx, SNx)	–1	1	V
Transient 200ns voltage at low-side source pin (SLx) and current sense amplifier input pin (SPx, SNx)	–3	3	V
Current sense amplifier power supply input and reference pin voltage (VREF)	–0.3	5.75	V
Current sense amplifier output pin voltage (SOx)	–0.3	V_{VREF} + 0.3	V
BUCK REGULATOR			
Power supply pin voltage (VIN)	–0.3	65	V
Shutdown control pin voltage (nSHDN)	–0.3	V_{VIN}	V
Voltage feedback pin voltage (FB)	–0.3	7	V
Bootstrap pin voltage with respect to SW (CB)	–0.3	7	V
Switching node pin voltage (SW)	–0.3	V_{VIN}	V
Switching node pin voltage less than 30ns transients (SW)	–2	V_{VIN}	V
DRV832x			
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Continuous high-side gate driver output pin (GHx) and high-side source pin voltage (SHx) should be limited to –2V minimum for an absolute maximum of 65V on VM or VDRAIN. At 60V and lower, the full specification of –5V continuous on GHx and SHx is allowable.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000V may actually have higher performance.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±500V may actually have higher performance.

7.3 Recommended Operating Conditions

at T_A = –40°C to +125°C (unless otherwise noted)

		MIN	MAX	UNIT
GATE DRIVER				
V_{VM}	Power supply voltage (VM)	6	60	V
V_I	Input voltage (CAL, ENABLE, GAIN, IDRIVE, INHx, INLx, MODE, nSCS, SCLK, SDI, VDS)	0	5.5	V
f_{PWM}	Applied PWM signal (INHx, INLx)	0	200(1)	kHz
I_{GATE_HS}	High-side average gate drive current (GHx)	0	25(1)	mA
I_{GATE_LS}	Low-side average gate drive current (GLx)	0	25(1)	mA
I_{DVDD}	External load current (DVDD)	0	30(1)	mA
V_{VREF}	Current sense amplifier power supply input and reference (VREF)	3	5.5	V
I_{SO}	Current sense amplifier output current (SOx)	0	5	mA
V_{OD}	Open drain pin pullup voltage (nFAULT, SDO)	0	5.5	V
I_{OD}	Open drain pin output current (nFAULT, SDO)	0	5	mA
BUCK REGULATOR				
V_{VIN}	Power supply voltage (VIN)	4	60	V
V_{nSHDN}	Shutdown control input voltage (nSHDN)	0	60	V
DRV832x				
T_A	Operating ambient temperature	–40	125	°C

(1) Power dissipation and thermal limits must be observed

7.4 Thermal Information

THERMAL METRIC(1)		DRV832x				UNIT
		RTV (WQFN)	RHA (VQFN)	RTA (WQFN)	RGZ (VQFN)	
		32 PINS	40 PINS	40 PINS	48 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.9	30.1	32.1	26.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.8	16.7	11	13.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.8	9.9	7.1	9.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	0.5	0.1	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.8	9.9	7.1	9.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.1	2.2	2.1	2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

at T_A = –40°C to +125°C, V_{VM} = 6 to 60V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (DVDD, VCP, VM)						
I_{VM}	VM operating supply current	V_{VM} = 24V, ENABLE = 3.3V, INHx/INLx = 0		10.5	14	mA
I_{VMQ}	VM sleep mode supply current	ENABLE = 0V, V_{VM} = 24V, T_A = 25°C		12	20	µA
		ENABLE = 0V, V_{VM} = 24V, T_A = 125°C(1)			50	
t_{RST} (1)	Reset pulse time	ENABLE = low period to reset faults	8		40	µs
t_{WAKE}	Wake up time	V_{VM} > V_{UVLO}, ENABLE = 3.3V to outputs ready			1	ms
t_{SLEEP}	Sleep time	ENABLE = 0V to device sleep mode			1	ms
V_{DVDD}	DVDD regulator voltage	I_{DVDD} = 0 to 30mA	3	3.3	3.6	V
V_{VCP}	VCP operating voltage with respect to VM	V_{VM} = 13V, I_{VCP} = 0 to 25mA	8.4	11	12.5	V
		V_{VM} = 10V, I_{VCP} = 0 to 20mA	6.3	9	10	
		V_{VM} = 8V, I_{VCP} = 0 to 15mA	5.4	7	8	
		V_{VM} = 6V, I_{VCP} = 0 to 10mA	4	5	6	
LOGIC-LEVEL INPUTS (CAL, ENABLE, INHx, INLx, nSCS, SCLK, SDI)						
V_{IL}	Input logic low voltage		0		0.8	V
V_{IH}	Input logic high voltage		1.5		5.5	V
V_{HYS}	Input logic hysteresis			100		mV
I_{IL}	Input logic low current	V_{VIN} = 0V	–5		5	µA
I_{IH}	Input logic high current	V_{VIN} = 5V		50	70	µA
R_{PD}	Pulldown resistance	To AGND		100		kΩ
t_{PD}	Propagation delay	INHx/INLx transition to GHx/GLx transition		150		ns
FOUR-LEVEL H/W INPUTS (GAIN, MODE)						
V_{I1}	Input mode 1 voltage	Tied to AGND		0		V
V_{I2}	Input mode 2 voltage	45kΩ ± 5% tied to AGND		1.2		V
V_{I3}	Input mode 3 voltage	Hi-Z		2		V
V_{I4}	Input mode 4 voltage	Tied to DVDD		3.3		V
R_{PU}	Pullup resistance	Internal pullup to DVDD		50		kΩ
R_{PD}	Pulldown resistance	Internal pulldown to AGND		84		kΩ
SEVEN-LEVEL H/W INPUTS (IDRIVE, VDS)						
V_{I1}	Input mode 1 voltage	Tied to AGND		0		V
V_{I2}	Input mode 2 voltage	18kΩ ± 5% tied to AGND		0.5		V
V_{I3}	Input mode 3 voltage	75kΩ ± 5% tied to AGND		1.1		V
V_{I4}	Input mode 4 voltage	Hi-Z		1.65		V
V_{I5}	Input mode 5 voltage	75kΩ ± 5% tied to DVDD		2.2		V
V_{I6}	Input mode 6 voltage	18kΩ ± 5% tied to DVDD		2.8		V
V_{I7}	Input mode 7 voltage	Tied to DVDD		3.3		V
R_{PU}	Pullup resistance	Internal pullup to DVDD		73		kΩ
R_{PD}	Pulldown resistance	Internal pulldown to AGND		73		kΩ
OPEN DRAIN OUTPUTS (nFAULT, SDO)						
V_{OL}	Output logic low voltage	I_O = 5mA			0.1	V
I_{OZ}	Output high impedance leakage	V_O = 5V	–2		2	µA
GATE DRIVERS (GHx, GLx)						

7.5 Electrical Characteristics (continued)

at T_A = –40°C to +125°C, V_{VM} = 6 to 60V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{GSH} (1)	High-side gate drive voltage with respect to SHx		V_{VM} = 13V, I_{VCP} = 0 to 25mA	8.4	11	12.5	V
			V_{VM} = 10V, I_{VCP} = 0 to 20mA	6.3	9	10	
			V_{VM} = 8V, I_{VCP} = 0 to 15mA	5.4	7	8	
			V_{VM} = 6V, I_{VCP} = 0 to 10mA	4	5	6	
V_{GSL} (1)	Low-side gate drive voltage with respect to PGND		V_{VM} = 12V, I_{VGLS} = 0 to 25mA	9	11	12	V
			V_{VM} = 10V, I_{VGLS} = 0 to 20mA	7.5	9	10	
			V_{VM} = 8V, I_{VGLS} = 0 to 15mA	5.5	7	8	
			V_{VM} = 6V, I_{VGLS} = 0 to 10mA	4	5	6	
t_{DEAD}	Gate drive dead time	SPI Device	DEAD_TIME = 00b		50		ns
			DEAD_TIME = 01b		100		
			DEAD_TIME = 10b		200		
			DEAD_TIME = 11b		400		
		H/W Device			100		
t_{DRIVE}	Peak current gate drive time	SPI Device	TDRIVE = 00b		500		ns
			TDRIVE = 01b		1000		
			TDRIVE = 10b		2000		
			TDRIVE = 11b		4000		
		H/W Device			4000		
I_{DRIVEP}	Peak source gate current	SPI Device	IDRIVEP_HS or IDRIVEP_LS = 0000b		10		mA
			IDRIVEP_HS or IDRIVEP_LS = 0001b		30		
			IDRIVEP_HS or IDRIVEP_LS = 0010b		60		
			IDRIVEP_HS or IDRIVEP_LS = 0011b		80		
			IDRIVEP_HS or IDRIVEP_LS = 0100b		120		
			IDRIVEP_HS or IDRIVEP_LS = 0101b		140		
			IDRIVEP_HS or IDRIVEP_LS = 0110b		170		
			IDRIVEP_HS or IDRIVEP_LS = 0111b		190		
			IDRIVEP_HS or IDRIVEP_LS = 1000b		260		
			IDRIVEP_HS or IDRIVEP_LS = 1001b		330		
			IDRIVEP_HS or IDRIVEP_LS = 1010b		370		
			IDRIVEP_HS or IDRIVEP_LS = 1011b		440		
			IDRIVEP_HS or IDRIVEP_LS = 1100b		570		
			IDRIVEP_HS or IDRIVEP_LS = 1101b		680		
			IDRIVEP_HS or IDRIVEP_LS = 1110b		820		
			IDRIVEP_HS or IDRIVEP_LS = 1111b		1000		
		H/W Device	IDRIVE = Tied to AGND		10		
			IDRIVE = 18kΩ ± 5% tied to AGND		30		
			IDRIVE = 75kΩ ± 5% tied to AGND		60		
			IDRIVE = Hi-Z		120		
			IDRIVE = 75kΩ ± 5% tied to DVDD		260		
			IDRIVE = 18kΩ ± 5% tied to DVDD		570		
			IDRIVE = Tied to DVDD		1000		

7.5 Electrical Characteristics (continued)

at T_A = –40°C to +125°C, V_{VM} = 6 to 60V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DRIVEN}	Peak sink gate current	SPI Device	IDRIVEN_HS or IDRIVEN_LS = 0000b		20		mA
			IDRIVEN_HS or IDRIVEN_LS = 0001b		60		
			IDRIVEN_HS or IDRIVEN_LS = 0010b		120		
			IDRIVEN_HS or IDRIVEN_LS = 0011b		160		
			IDRIVEN_HS or IDRIVEN_LS = 0100b		240		
			IDRIVEN_HS or IDRIVEN_LS = 0101b		280		
			IDRIVEN_HS or IDRIVEN_LS = 0110b		340		
			IDRIVEN_HS or IDRIVEN_LS = 0111b		380		
			IDRIVEN_HS or IDRIVEN_LS = 1000b		520		
			IDRIVEN_HS or IDRIVEN_LS = 1001b		660		
			IDRIVEN_HS or IDRIVEN_LS = 1010b		740		
			IDRIVEN_HS or IDRIVEN_LS = 1011b		880		
			IDRIVEN_HS or IDRIVEN_LS = 1100b		1140		
			IDRIVEN_HS or IDRIVEN_LS = 1101b		1360		
			IDRIVEN_HS or IDRIVEN_LS = 1110b		1640		
			IDRIVEN_HS or IDRIVEN_LS = 1111b		2000		
		H/W Device	IDRIVE = Tied to AGND		20		
			IDRIVE = 18kΩ ± 5% tied to AGND		60		
			IDRIVE = 75kΩ ± 5% tied to AGND		120		
			IDRIVE = Hi-Z		240		
			IDRIVE = 75kΩ ± 5% tied to DVDD		520		
			IDRIVE = 18kΩ ± 5% tied to DVDD		1140		
			IDRIVE = Tied to DVDD		2000		
I_{HOLD}	Gate holding current		Source current after t_{DRIVE}		10		mA
			Sink current after t_{DRIVE}		50		
I_{STRONG}	Gate strong pulldown current		GHx to SHx and GLx to PGND		2		A
R_{OFF}	Gate hold off resistor		GHx to SHx		480		kΩ
			GLx to PGND		150		
CURRENT SENSE AMPLIFIER (SNx, SOx, SPx, VREF)							
G_{CSA}	Amplifier gain	SPI Device	CSA_GAIN = 00b	4.85	5	5.15	V/V
			CSA_GAIN = 01b	9.7	10	10.3	
			CSA_GAIN = 10b	19.4	20	20.6	
			CSA_GAIN = 11b	38.8	40	41.2	
		H/W Device	GAIN = Tied to AGND	4.85	5	5.15	
			GAIN = 47kΩ ± 5% tied to AGND	9.7	10	10.3	
			GAIN = Hi-Z	19.4	20	20.6	
			GAIN = Tied to DVDD	38.8	40	41.2	
t_{SET} (1)	Settling time to ±1%		V_{O_STEP} = 0.5V, G_{CSA} = 5V/V		150		ns
			V_{O_STEP} = 0.5V, G_{CSA} = 10V/V		300		
			V_{O_STEP} = 0.5V, G_{CSA} = 20V/V		600		
			V_{O_STEP} = 0.5V, G_{CSA} = 40V/V		1200		
V_{COM}	Common mode input range			–0.15		0.15	V
V_{DIFF}	Differential mode input range			–0.3		0.3	V

7.5 Electrical Characteristics (continued)

at T_A = –40°C to +125°C, V_{VM} = 6 to 60V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OFF}	Input offset error		V_{SP} = V_{SN} = 0V, CAL = 3.3 , VREF = 3.3V	–4		4	mV
V_{DRIFT} (1)	Drift offset		V_{SP} = V_{SN} = 0V		10		µV/°C
V_{LINEAR}	SOx output voltage linear range			0.25		V_{VREF} – 0.25	V
V_{BIAS}	SOx output voltage bias	SPI Device	V_{SP} = V_{SN} = 0V, CAL = 3.3V, VREF_DIV = 0b		V_{VREF} – 0.3		V
			V_{SP} = V_{SN} = 0V, CAL = 3.3 , VREF_DIV = 1b		V_{VREF} / 2		
		H/W Device	V_{SP} = V_{SN} = 0V, CAL = 3.3V		V_{VREF} / 2		
I_{BIAS}	SPx/SNx input bias current		VREF_DIV = 1b			100	µA
V_{SLEW} (1)	SOx output slew rate		60pF load		10		V/µs
I_{VREF}	VREF input current		V_{VREF} = 5V		2	3	mA
UGB(1)	Unity gain bandwidth		60pF load		10		MHz
PROTECTION CIRCUITS							
V_{UVLO}	VM undervoltage lockout		VM falling, UVLO report	5.4	5.6	5.8	V
			VM rising, UVLO recovery	5.6	5.8	6	
V_{UVLO_HYS}	VM undervoltage hysteresis		Rising to falling threshold		200		mV
t_{UVLO_DEG}	VM undervoltage deglitch time		VM falling, UVLO report		10		µs
V_{CPUV}	Charge pump undervoltage lockout		VCP falling, CPUV report		V_{VM} + 2.8		V
V_{GS_CLAMP}	High-side gate clamp		Positive clamping voltage	15	16.5	18	V
			Negative clamping voltage		–0.7		
V_{VDS_OCP}	V_{DS} overcurrent trip voltage	SPI Device	VDS_LVL = 0000b		0.06		V
			VDS_LVL = 0001b		0.13		
			VDS_LVL = 0010b		0.2		
			VDS_LVL = 0011b		0.26		
			VDS_LVL = 0100b		0.31		
			VDS_LVL = 0101b		0.45		
			VDS_LVL = 0110b		0.53		
			VDS_LVL = 0111b		0.6		
			VDS_LVL = 1000b		0.68		
			VDS_LVL = 1001b		0.75		
			VDS_LVL = 1010b		0.94		
			VDS_LVL = 1011b		1.13		
			VDS_LVL = 1100b		1.3		
			VDS_LVL = 1101b		1.5		
			VDS_LVL = 1110b		1.7		
			VDS_LVL = 1111b		1.88		
		H/W Device	VDS = Tied to AGND		0.06		
			VDS = 18kΩ ± 5% tied to AGND		0.13		
			VDS = 75kΩ ± 5% tied to AGND		0.26		
			VDS = Hi-Z		0.6		
			VDS = 75kΩ ± 5% tied to DVDD		1.13		
			VDS = 18kΩ ± 5% tied to DVDD		1.88		
			VDS = Tied to DVDD		Disabled		

7.5 Electrical Characteristics (continued)

at T_A = –40°C to +125°C, V_{VM} = 6 to 60V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OCP_DEG}	V_{DS} and V_{SENSE} overcurrent deglitch time	SPI Device	OCP_DEG = 00b		2		µs
			OCP_DEG = 01b		4		
			OCP_DEG = 10b		6		
			OCP_DEG = 11b		8		
		H/W Device			4		
V_{SEN_OCP}	V_{SENSE} overcurrent trip voltage	SPI Device	SEN_LVL = 00b		0.25		V
			SEN_LVL = 01b		0.5		
			SEN_LVL = 10b		0.75		
			SEN_LVL = 11b		1		
		H/W Device			1		
t_{RETRY}	Overcurrent retry time	SPI Device	TRETRY = 0b		4		ms
			TRETRY = 1b		50		µs
		H/W Device			4		ms
T_{OTW} (1)	Thermal warning temperature		Die temperature, T_J	130	150	165	°C
T_{OTSD} (1)	Thermal shutdown temperature		Die temperature, T_J	150	170	185	°C
T_{HYS} (1)	Thermal hysteresis		Die temperature, T_J		20		°C
BUCK REGULATOR SUPPLY (VIN)							
I_{nSHDN}	Shutdown supply current		V_{nSHDN} = 0V		1	3	µA
I_Q	Operating quiescent current		V_{VIN} = 12V, no load; not switching		28		µA
V_{VIN_UVLO}	VIN undervoltage lockout threshold		VIN Rising			4	V
			VIN Falling	3			
BUCK REGULATOR SHUTDOWN (nSHDN)							
V_{nSHDN_TH}	Rising nSHDN threshold			1.05	1.25	1.38	V
I_{nSHDN}	Input current		V_{nSHDN} = 2.3V		–4.2		µA
			V_{nSHDN} = 0.9V		–1		
I_{nSHDN_HYS}	Hysteresis current				–3		µA
BUCK REGULATOR HIGH-SIDE MOSFET							
R_{DS_ON}	MOSFET on resistance		V_{VIN} = 12V, V_{CB} to V_{SW} = 5.8V, T_A = 25°C		900		mΩ
BUCK REGULATOR VOLTAGE REFERENCE (FB)							
V_{FB}	Feedback voltage			0.747	0.765	0.782	V
BUCK REGULATOR CURRENT LIMIT							
I_{LIMIT}	Peak current limit		V_{VIN} = 12V, T_A = 25°C		1200		mA
						1700	
BUCK REGULATOR SWITCHING (SW)							
f_{SW}	Switching frequency			595	700	805	kHz
D_{MAX}	Maximum duty cycle				96%		
BUCK REGULATOR THERMAL SHUTDOWN							
T_{SHDN} (1)	Thermal shutdown threshold				170		°C
T_{HYS} (1)	Thermal shutdown hysteresis				10		°C

(1) Specified by design and characterization data

7.6 SPI Timing Requirements

at T_A = –40°C to +125°C, V_{VM} = 6 to 60V (unless otherwise noted) (1)

			MIN	NOM	MAX	UNIT
SPI (nSCS, SCLK, SDI, SDO)						
t_{READY}	SPI ready after enable	VM > UVLO, ENABLE = 3.3V			1	ms
t_{CLK}	SCLK minimum period		100			ns
t_{CLKH}	SCLK minimum high time		50			ns
t_{CLKL}	SCLK minimum low time		50			ns
t_{SU_SDI}	SDI input data setup time		20			ns
t_{H_SDI}	SDI input data hold time		30			ns
t_{D_SDO}	SDO output data delay time	SCLK high to SDO valid			30	ns
t_{SU_nSCS}	nSCS input setup time		50			ns
t_{H_nSCS}	nSCS input hold time		50			ns
t_{HI_nSCS}	nSCS minimum high time before active low		400			ns
t_{DIS_nSCS}	nSCS disable time	nSCS high to SDO high impedance		10		ns

(1) Specified by design and characterization data

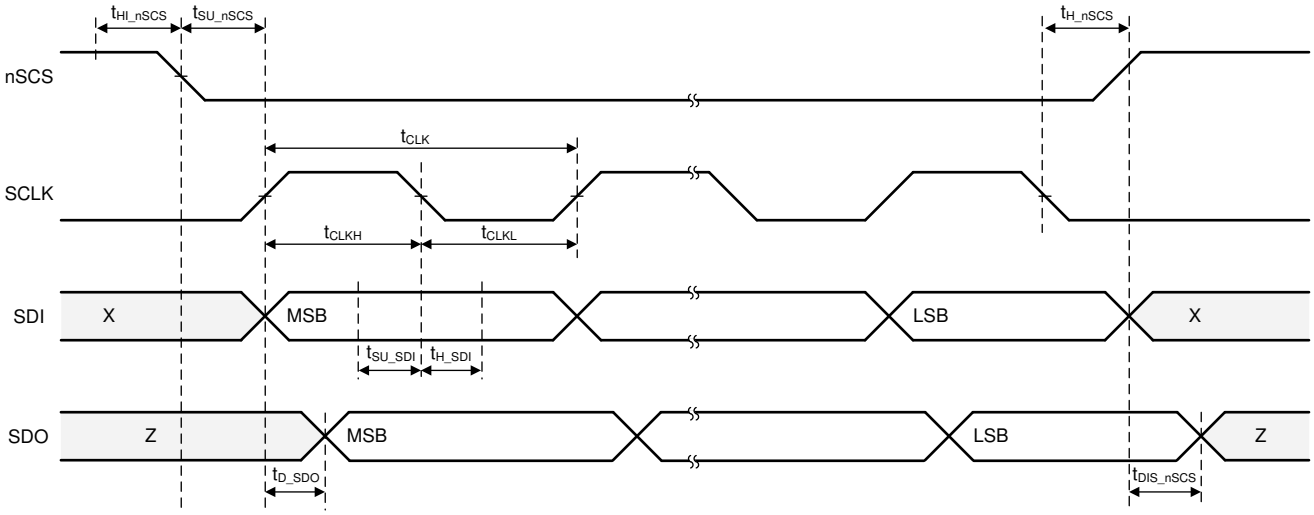


Figure 7-1. SPI Slave Mode Timing Diagram

7.7 Typical Characteristics

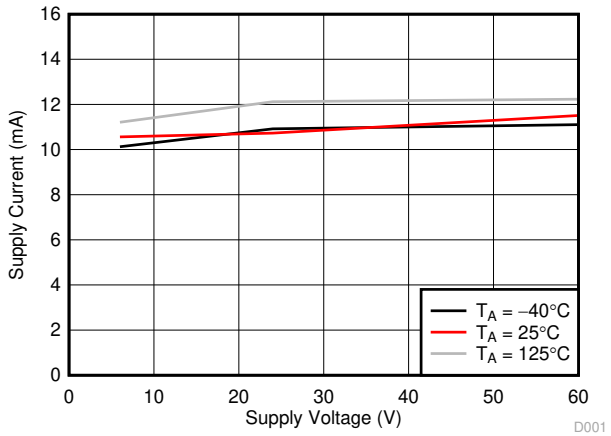


Figure 7-2. Supply Current Over VM

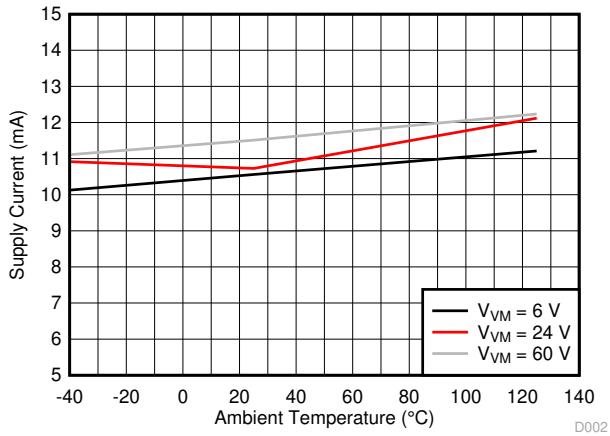


Figure 7-3. Supply Current Over Temperature

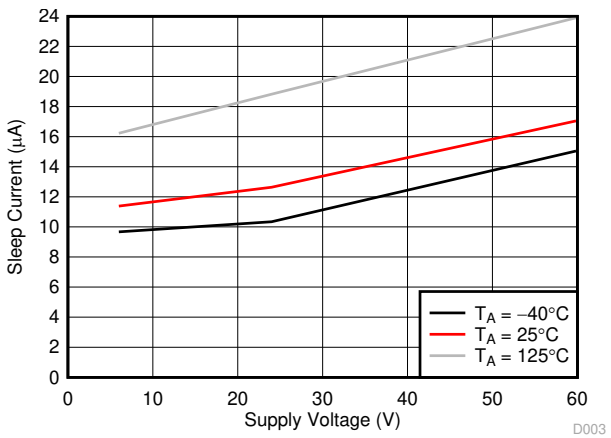


Figure 7-4. Sleep Current Over VM

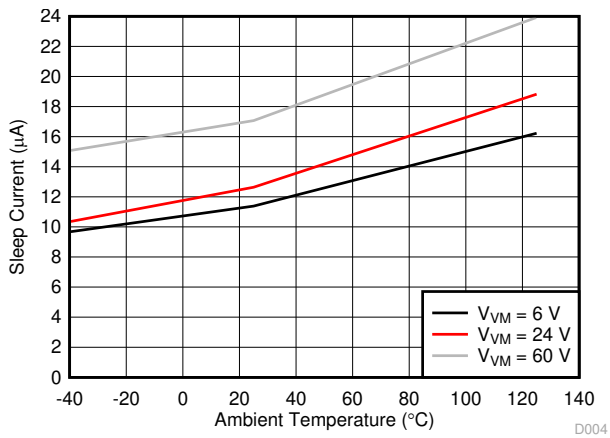


Figure 7-5. Sleep Current Over Temperature

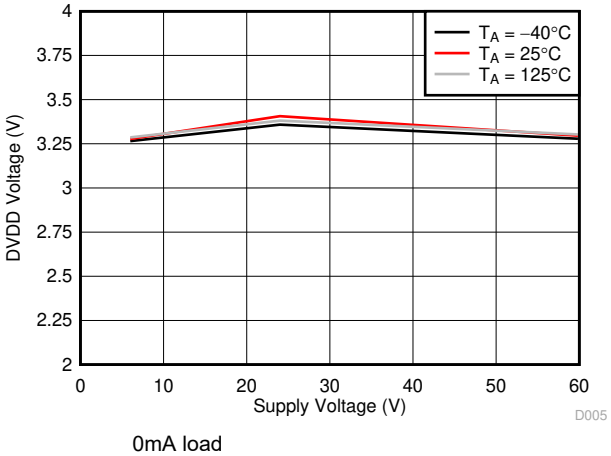


Figure 7-6. DVDD Voltage Over VM

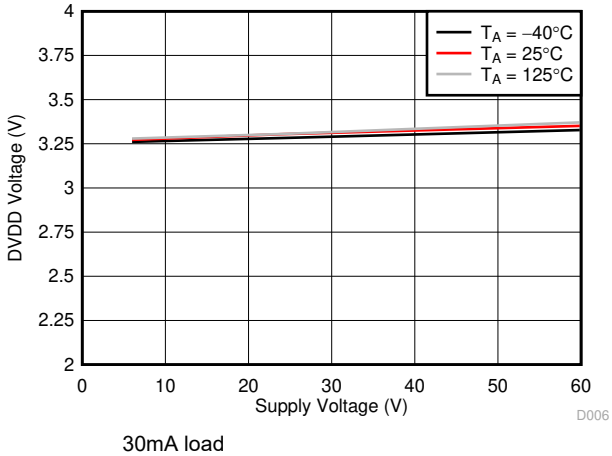


Figure 7-7. DVDD Voltage Over VM

7.7 Typical Characteristics (continued)

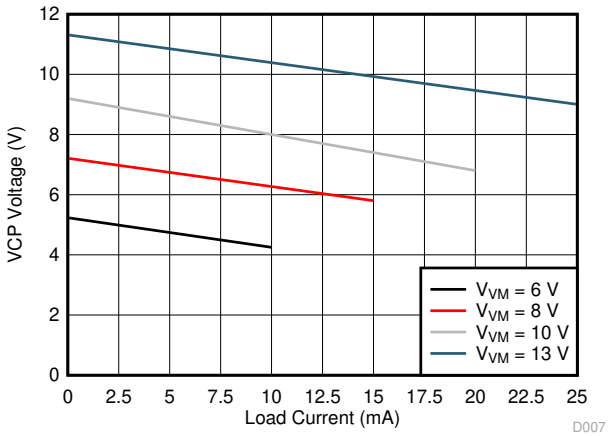
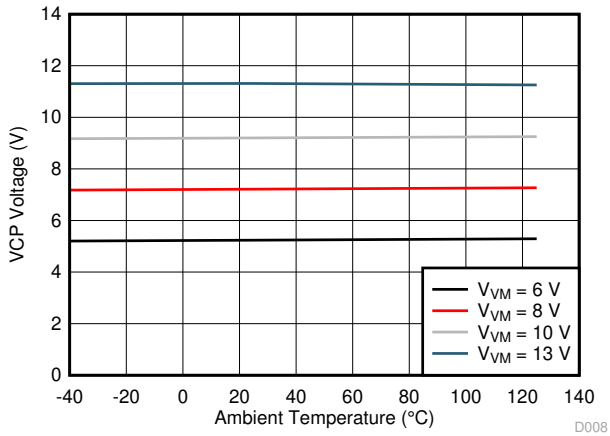


Figure 7-8. VCP Voltage Over Load



0mA load

Figure 7-9. VCP Voltage Over Temperature

8 Detailed Description

8.1 Overview

The DRV832x family of devices is an integrated 6 to 60-V gate driver for three-phase motor drive applications. These devices decrease system component count, cost, and complexity by integrating three independent halfbridge gate drivers, charge pump, and linear regulator for the supply voltages of the high-side and low-side gate drivers.The device also integrates optional triple current shunt (or current sense) amplifiers and an optional 600-mA buck regulator. A standard serial peripheral interface (SPI) provides a simple method for configuring the various device settings and reading fault diagnostic information through an external controller. Alternatively, a hardware interface (H/W) option allows for configuring the most common settings through fixed external resistors.

The gate drivers support external N-channel high-side and low-side power MOSFETs and can drive up to 1A source, 2A sink peak currents with a 25mA average output current. A doubler charge pump generates the supply voltage of the high-side gate drive. This charge pump architecture regulates the VCP output to V_{VM} + 11V. The supply voltage of the low-side gate driver is generated using a linear regulator from the VM power supply that regulates to 11V. A Smart Gate Drive architecture provides the ability to dynamically adjust the strength of the gate drive output current which lets the gate driver control the V_{DS} switching speed of the power MOSFET. This feature lets the user remove the external gate drive resistors and diodes, reducing the component count in the bill of materials (BOM), cost, and area of the printed circuit board (PCB). The architecture also uses an internal state machine to protect against short-circuit events in the gate driver, control the half-bridge dead time, and protect against dV/dt parasitic turnon of the external power MOSFET.

The DRV8323 and DRV8323R devices integrate three bidirectional current sense amplifiers for monitoring the current level through each of the external half-bridges using a low-side shunt resistor. The gain setting of the current sense amplifier can be adjusted through the SPI or hardware interface. The SPI method provides additional flexibility to adjust the output bias point.

The DRV8320R and DRV8323R devices integrate a 600mA buck regulator that can be used to power an external controller or other logic circuits. The buck regulator is implemented as a separate internal die that can use either the same or a different power supply than the gate driver.

In addition to the high level of device integration, the DRV832x family of devices provides a wide range of integrated protection features. These features include power supply undervoltage lockout (UVLO), charge pump undervoltage lockout (CPUV), V_{DS} overcurrent monitoring (OCP), gate driver short-circuit detection (GDF), and overtemperature shutdown (OTW and OTSD). Fault events are indicated by the nFAULT pin with detailed information available in the SPI registers on the SPI device version.

The DRV832x family of devices are available in 0.5mm pin pitch, QFN surface-mount packages. The QFN sizes are 5 × 5mm for the 32pin package, 6 × 6mm for the 40pin package, and 7 × 7mm for the 48pin package.

8.2 Functional Block Diagram

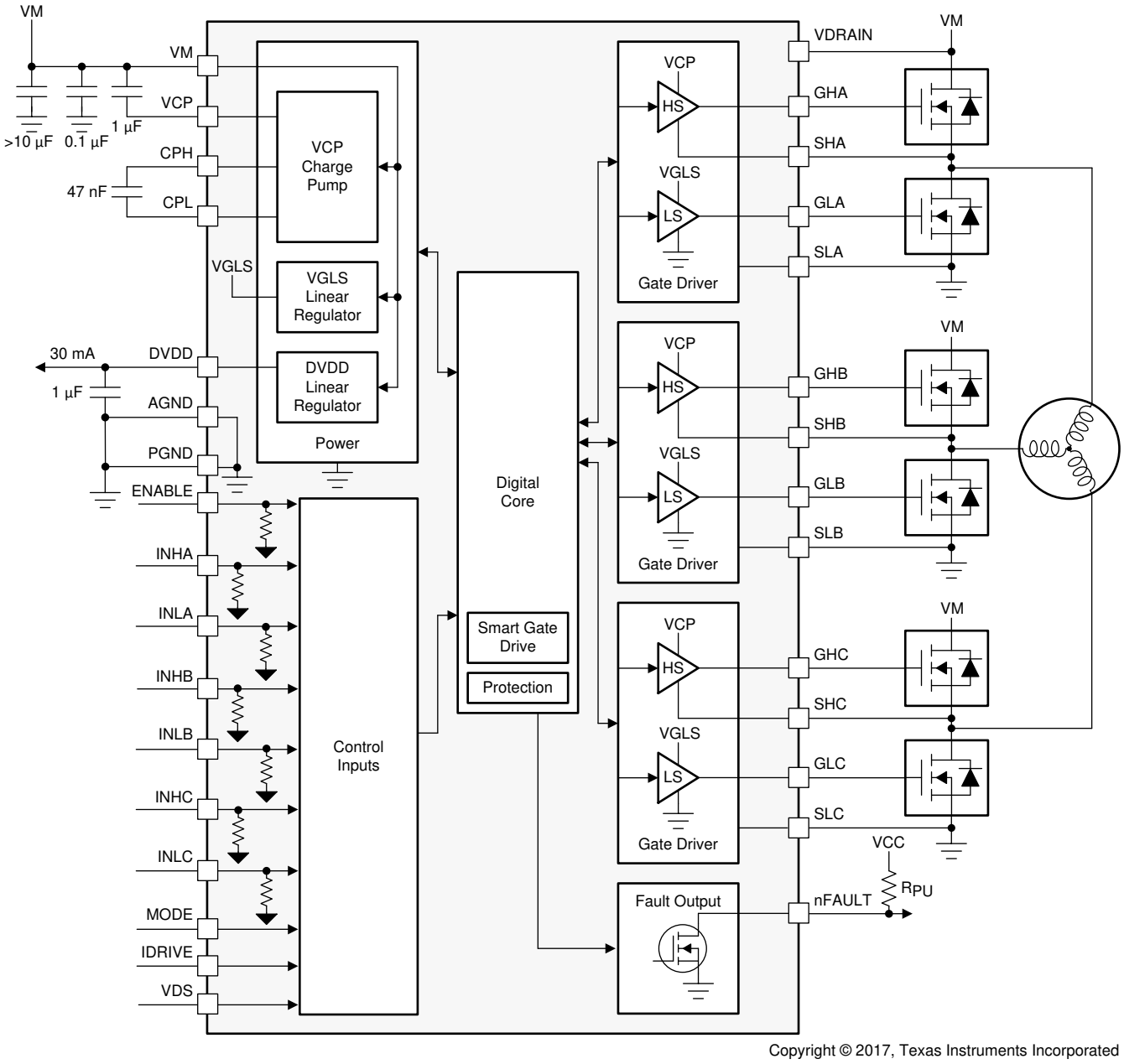


Figure 8-1. Block Diagram for DRV8320H

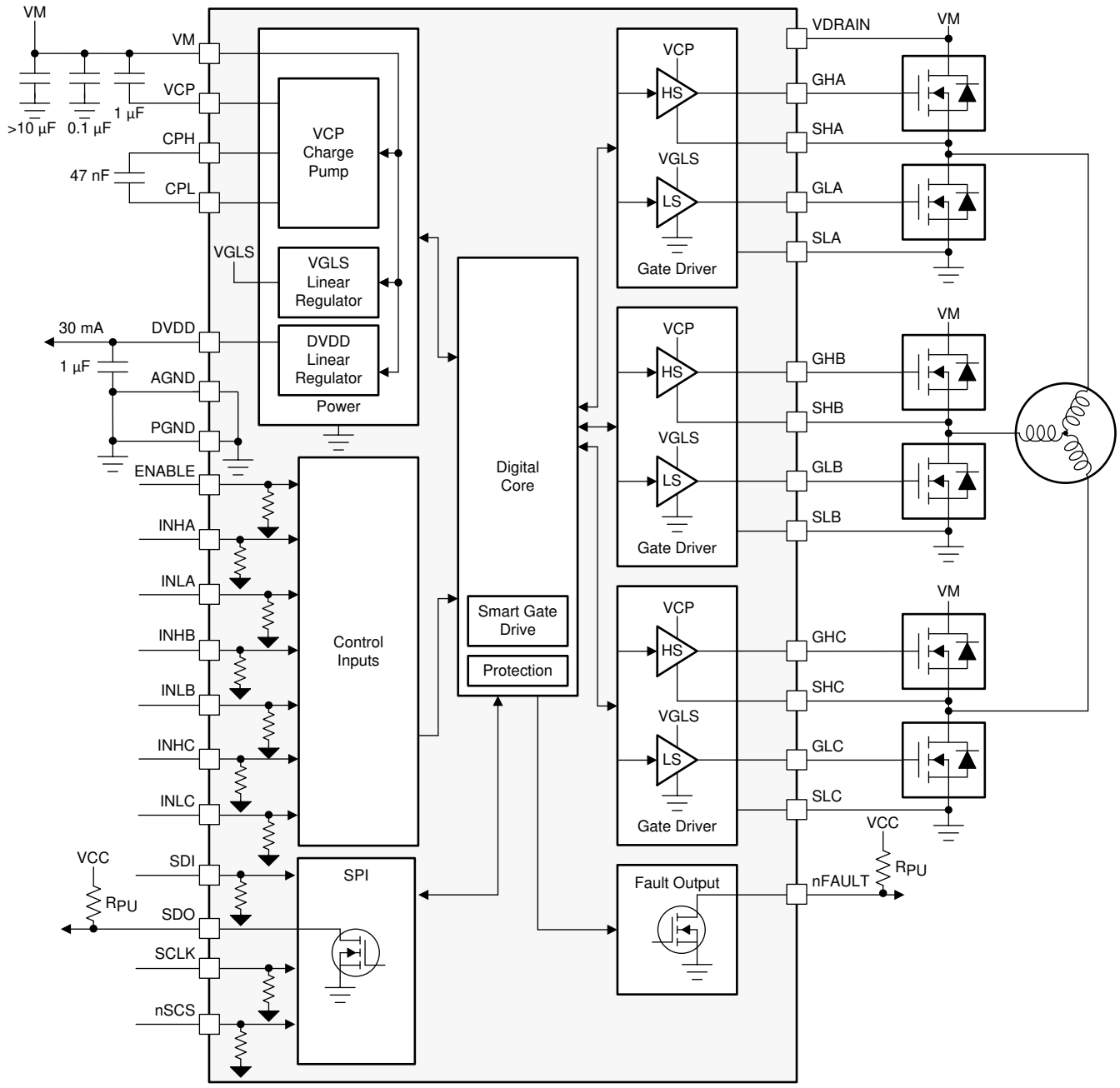


Figure 8-2. Block Diagram for DRV8320S

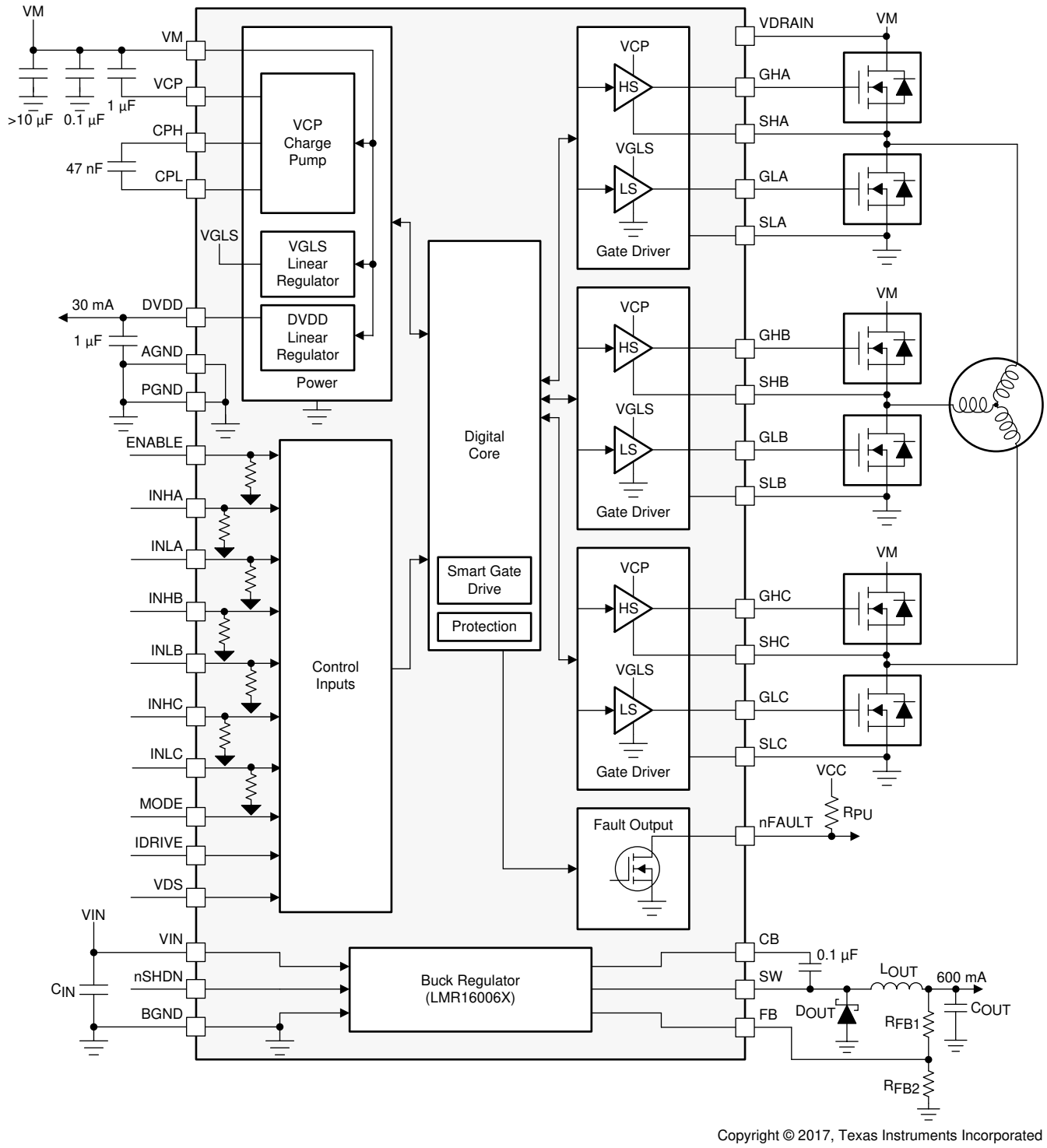


Figure 8-3. Block Diagram for DRV8320RH

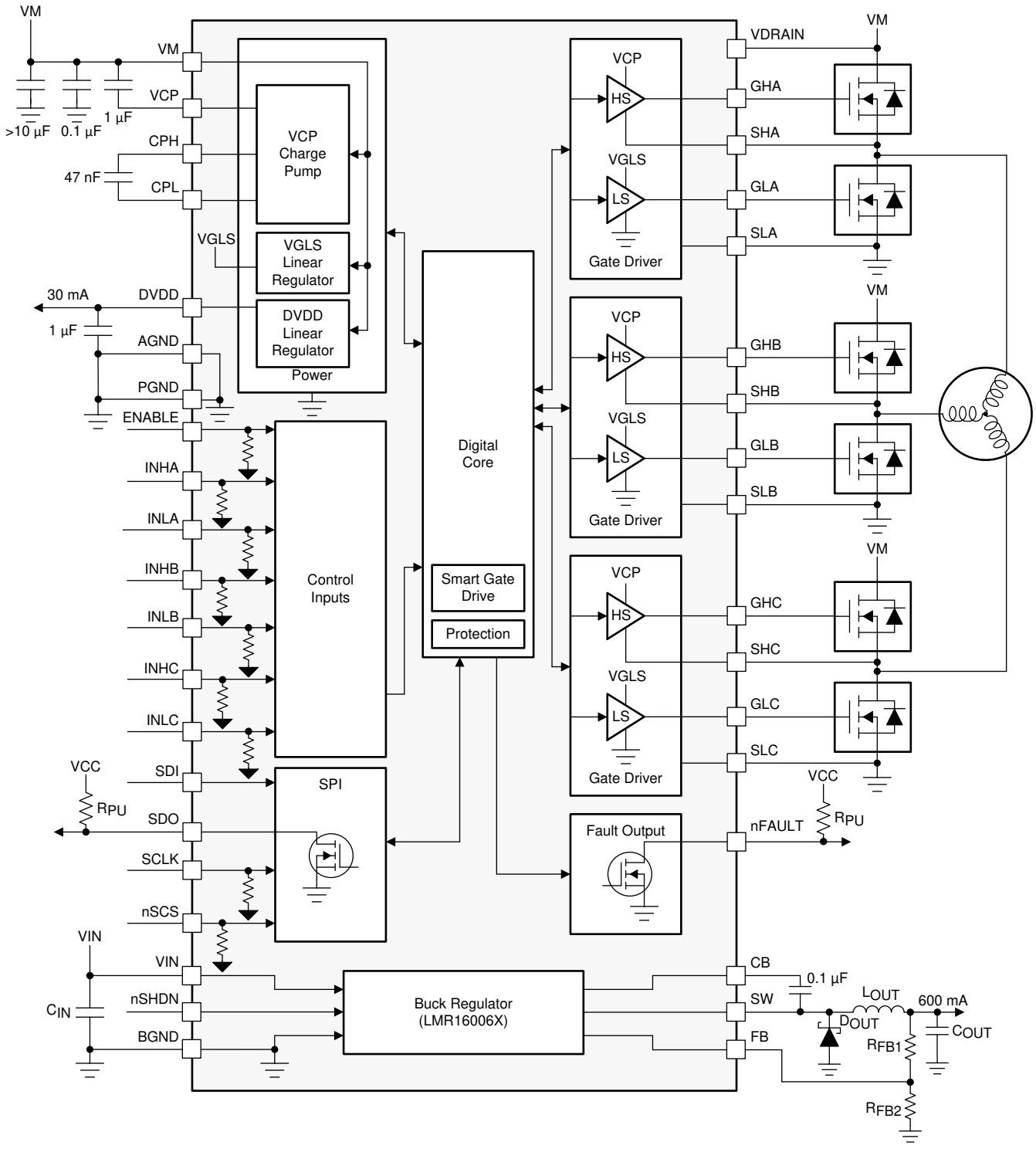


Figure 8-4. Block Diagram for DRV8320RS

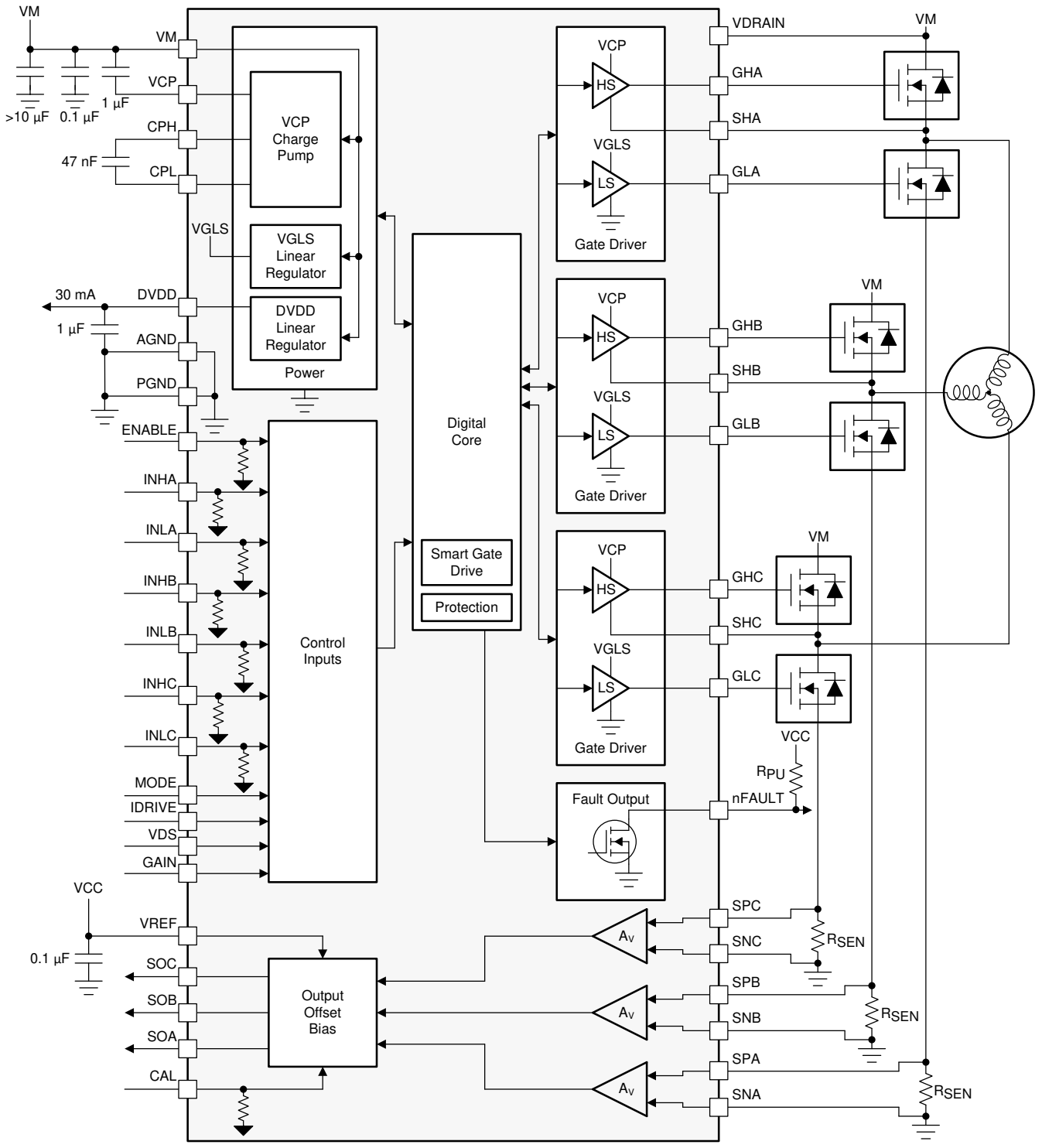


Figure 8-5. Block Diagram for DRV8323H

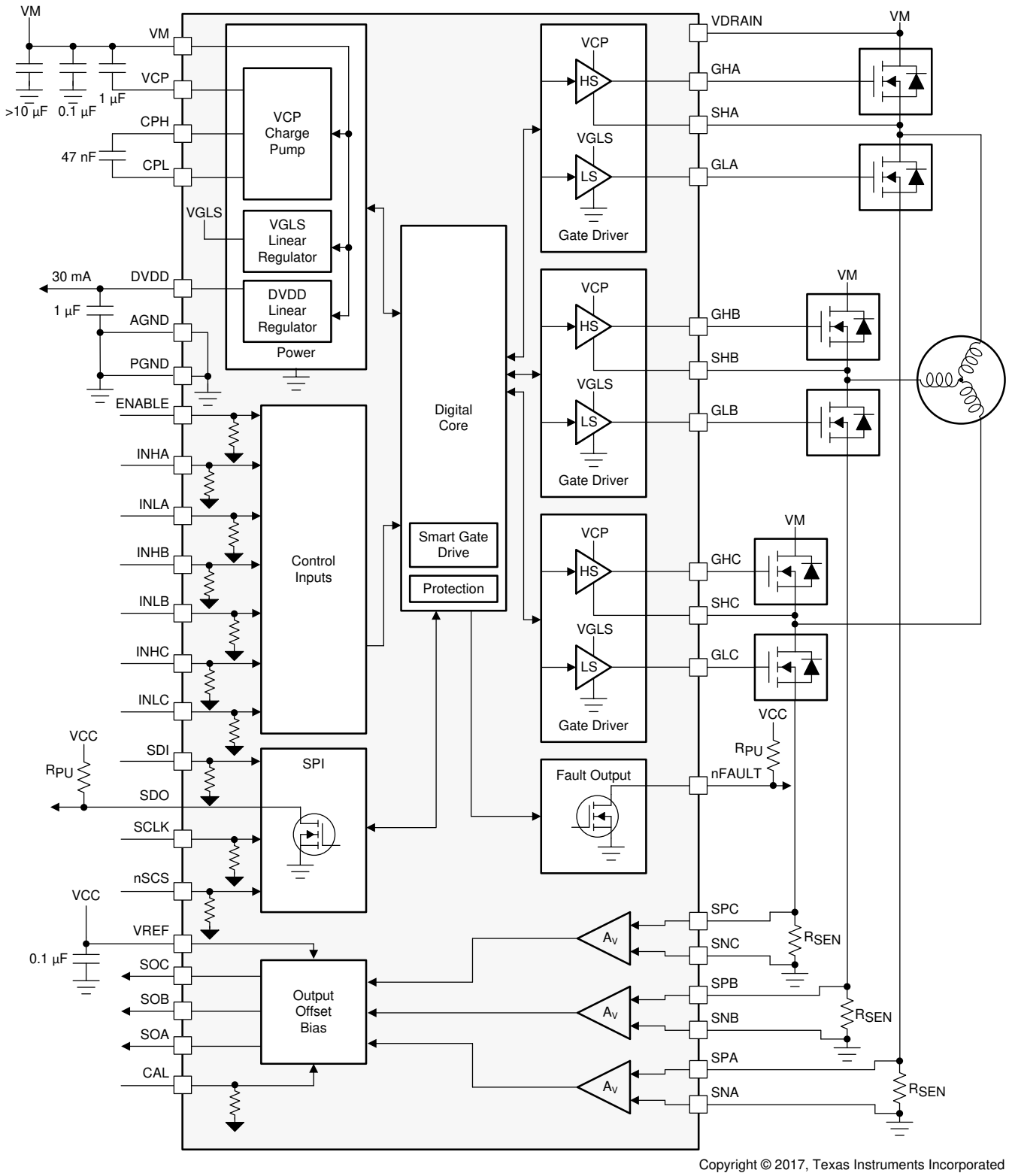


Figure 8-6. Block Diagram for DRV8323S

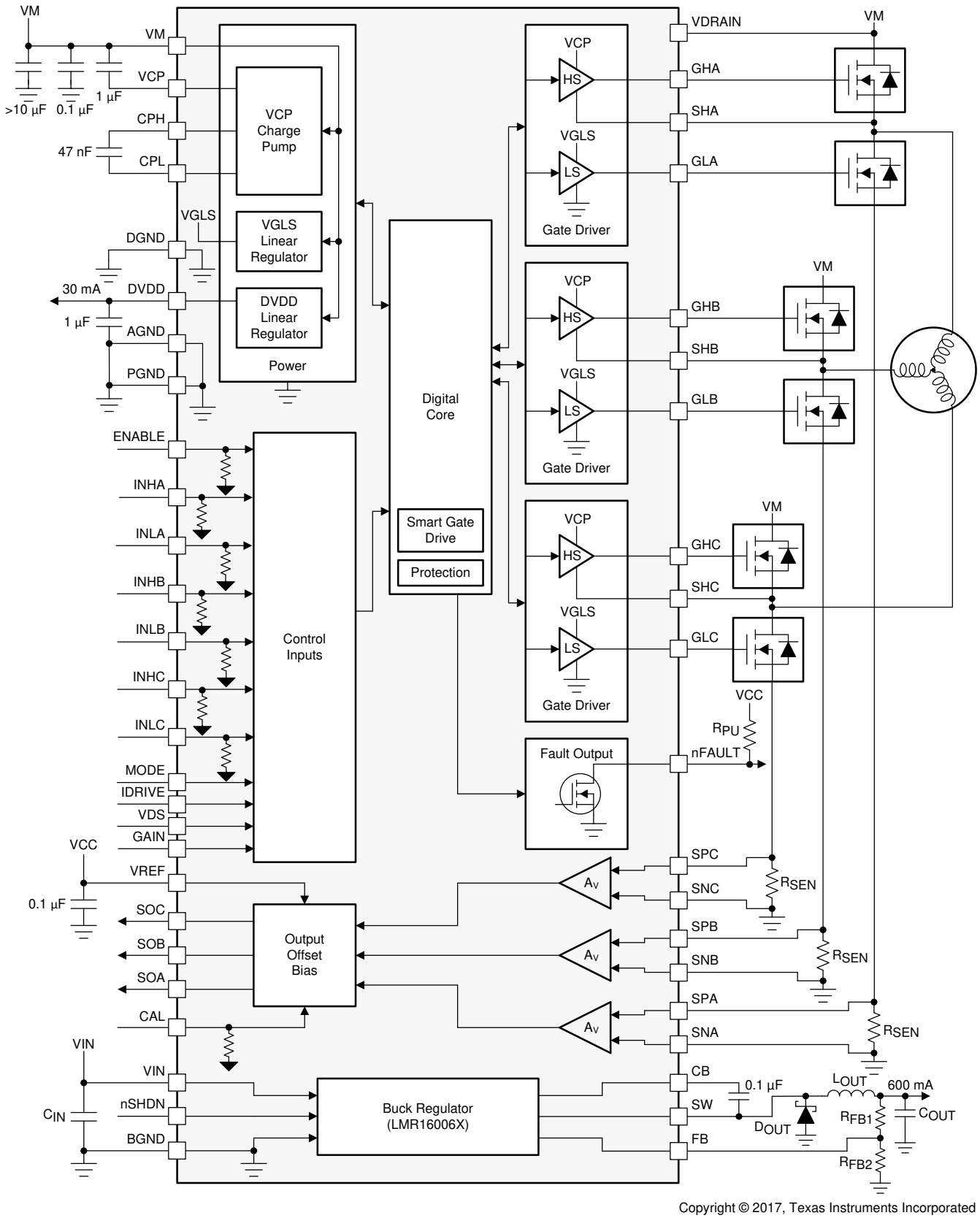


Figure 8-7. Block Diagram for DRV8323RH

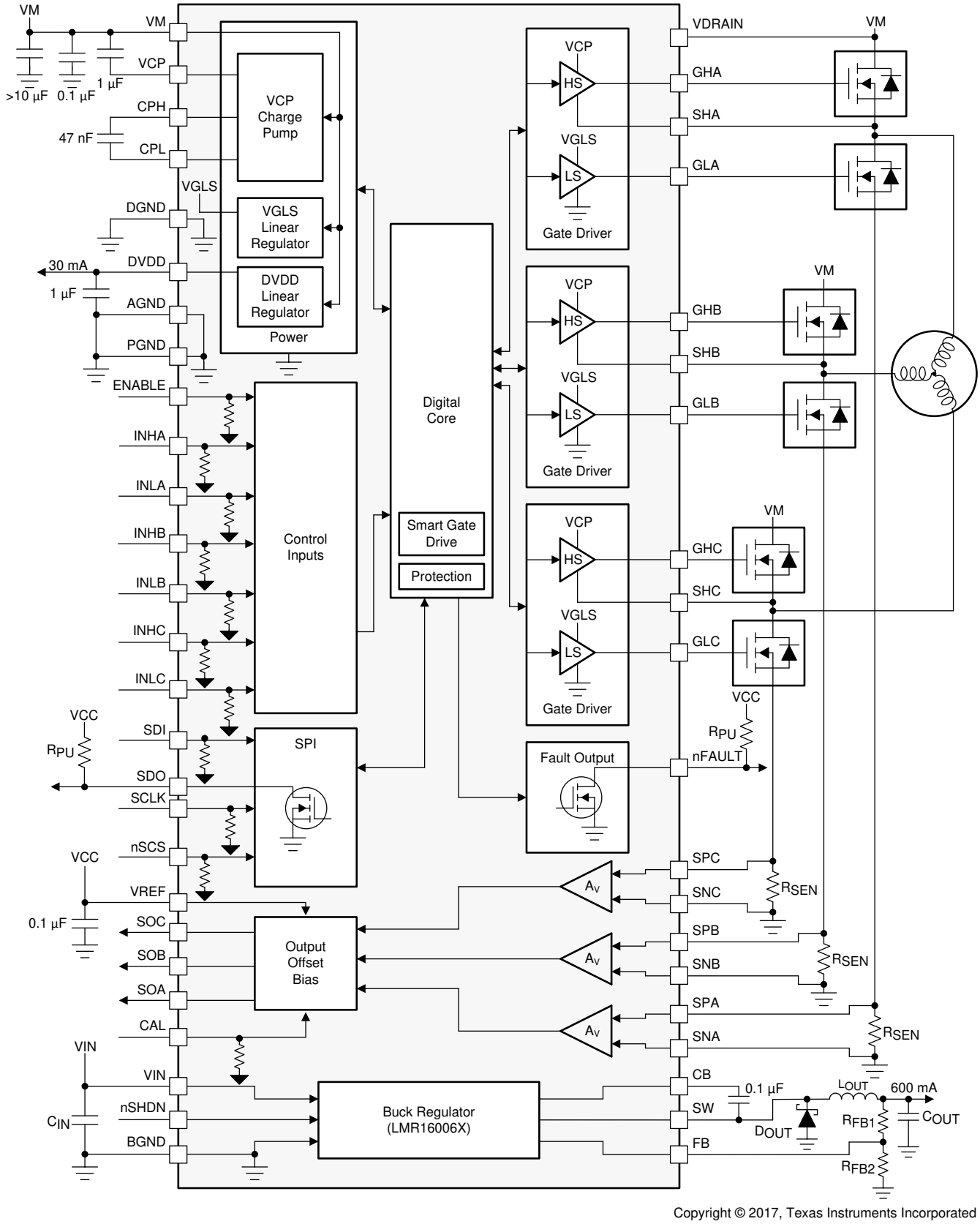


Figure 8-8. Block Diagram for DRV8323RS

8.3 Feature Description

Table 8-1 lists the recommended values of the external components for the gate driver and the buck regulator.

Table 8-1. DRV832x External Components

COMPONENTS	PIN 1	PIN 2	RECOMMENDED
GATE DRIVER AND SENSE AMPLIFIER			
C_{VM1}	VM	PGND	X5R or X7R, 0.1µF, VM-rated capacitor
C_{VM2}	VM	PGND	≥ 10µF, VM-rated capacitor
C_{VCP}	VCP	VM	X5R or X7R, 25V, 1µF capacitor
C_{SW}	CPH	CPL	X5R or X7R, 47nF, VM-rated capacitor
C_{DVDD}	DVDD	AGND	X5R or X7R, 1µF, 6.3V capacitor
R_{nFAULT}	VCC(1)	nFAULT	Pullup resistor
R_{SDO}	VCC(1)	SDO	Pullup resistor
R_{IDRIVE}	IDRIVE	AGND or DVDD	DRV832x hardware interface
R_{VDS}	VDS	AGND or DVDD	DRV832x hardware interface
R_{MODE}	MODE	AGND or DVDD	DRV832x hardware interface
R_{GAIN}	GAIN	AGND or DVDD	DRV832x hardware interface
C_{VREF}	VREF	AGND or DGND	X5R or X7R, 0.1µF, VREF-rated capacitor
R_{ASENSE}	SPA	SNA and PGND	Sense shunt resistor
R_{BSENSE}	SPB	SNB and PGND	Sense shunt resistor
R_{CSENSE}	SPC	SNC and PGND	Sense shunt resistor
BUCK REGULATOR			
C_{VIN}	VIN	BGND	X5R or X7R, 1 to 10µF, VM-rated capacitor
C_{BOOT}	SW	CB	X5R or X7R, 0.1µF, 16V capacitor
D_{SW}	SW	BGND	Schottky diode
L_{SW}	SW	OUT(2)	Output inductor
C_{OUT}	OUT(2)	BGND	X5R or X7R, OUT rated capacitor
R_{FB1}	OUT(2)	FB	Resistor divider to set buck output voltage
R_{FB2}	FB	BGND	

(1) The VCC pin is not a pin on the DRV832x family of devices, but a VCC supply voltage pullup is required for the open-drain outputs, nFAULT and SDO. These pins can also be pulled up to DVDD.
(2) The OUT pin is not a pin on the DRV8320R and DRV8323R devices, but is the regulated output voltage of the buck regulator after the output inductor.

8.3.1 Three Phase Smart Gate Drivers

The DRV832x family of devices integrates three, half-bridge gate drivers, each capable of driving high-side and low-side N-channel power MOSFETs. A doubler charge pump provides the correct gate bias voltage to the high-side MOSFETs across a wide operating voltage range in addition to providing 100% support of the duty cycle. An internal linear regulator provides the gate bias voltage for the low-side MOSFETs. The half-bridge gate drivers can be used in combination to drive a three-phase motor or separately to drive other types of loads.

The DRV832x family of devices implements a Smart Gate Drive architecture which allows the user to dynamically adjust the gate drive current without requiring external resistors to limit the gate current. Additionally, this architecture provides a variety of protection features for the external MOSFETs including automatic dead time insertion, prevention of parasitic dV/dt gate turnon, and gate fault detection.

8.3.1.1 PWM Control Modes

The DRV832x family of devices provides four different PWM control modes to support various commutation and control methods. Texas Instruments does not recommend changing the MODE pin or PWM_MODE register

during operation of the power MOSFETs. Instead, set all INHx and INLx pins to logic low before changing the MODE pin or PWM_MODE register.

8.3.1.1.1 6x PWM Mode (PWM_MODE = 00b or MODE Pin Tied to AGND)

In 6x PWM mode, each half-bridge supports three output states: low, high, or high-impedance (Hi-Z). The corresponding INHx and INLx signals control the output state as listed in Table 8-2.

Table 8-2. 6x PWM Mode Truth Table

INLx	INHx	GLx	GHx	SHx
0	0	L	L	Hi-Z
0	1	L	H	H
1	0	H	L	L
1	1	L	L	Hi-Z

8.3.1.1.2 3x PWM Mode (PWM_MODE = 01b or MODE Pin = 47kΩ to AGND)

In 3x PWM mode, the INHx pin controls each half-bridge and supports two output states: low or high. The INLx pin is used to put the half bridge in the Hi-Z state. If the Hi-Z state is not required, tie all INLx pins to logic high. The corresponding INHx and INLx signals control the output state as listed in Table 8-3.

Table 8-3. 3x PWM Mode Truth Table

INLx	INHx	GLx	GHx	SHx
0	X	L	L	Hi-Z
1	0	H	L	L
1	1	L	H	H

8.3.1.1.3 1x PWM Mode (PWM_MODE = 10b or MODE Pin = Hi-Z)

In 1x PWM mode, the DRV832x family of devices uses 6-step block commutation tables that are stored internally. This feature allows for a three-phase BLDC motor to be controlled using one PWM sourced from a simple controller. The PWM is applied on the INHA pin and determines the output frequency and duty cycle of the half-bridges.

The half-bridge output states are managed by the INLA, INHB, and INLB pins which are used as state logic inputs. The state inputs can be controlled by an external controller or connected directly to the digital outputs of the Hall effect sensor from the motor (INLA = HALL_A, INHB = HALL_B, INLB = HALL_C). The 1x PWM mode usually operates with synchronous rectification (low-side MOSFET recirculation); however, the mode can be configured to use asynchronous rectification (MOSFET body diode freewheeling) on SPI devices. This configuration is set using the 1PWM_COM bit in the SPI registers.

The INHC input controls the direction through the 6-step commutation table which is used to change the direction of the motor when Hall effect sensors are directly controlling the state of the INLA, INHB, and INLB inputs. Tie the INHC pin low if this feature is not required.

The INLC input brakes the motor by turning off all high-side MOSFETs and turning on all low-side MOSFETs when the INLC pin is pulled low. This brake is independent of the state of the other input pins. Tie the INLC pin high if this feature is not required.

Table 8-4. Synchronous 1x PWM Mode

LOGIC AND HALL INPUTS							GATE DRIVE OUTPUTS[1]						
STATE	INHC = 0			INHC = 1			PHASE A		PHASE B		PHASE C		DESCRIPTION
	INLA	INHB	INLB	INLA	INHB	INLB	GHA	GLA	GHB	GLB	GHC	GLC	
Stop	0	0	0	0	0	0	L	L	L	L	L	L	Stop
Align	1	1	1	1	1	1	PWM	!PWM	L	H	L	H	Align
1	1	1	0	0	0	1	L	L	PWM	!PWM	L	H	B → C
2	1	0	0	0	1	1	PWM	!PWM	L	L	L	H	A → C
3	1	0	1	0	1	0	PWM	!PWM	L	H	L	L	A → B

Table 8-4. Synchronous 1x PWM Mode (continued)

LOGIC AND HALL INPUTS							GATE DRIVE OUTPUTS[1]						
STATE	INHC = 0			INHC = 1			PHASE A		PHASE B		PHASE C		DESCRIPTION
	INLA	INHB	INLB	INLA	INHB	INLB	GHA	GLA	GHB	GLB	GHC	GLC	
4	0	0	1	1	1	0	L	L	L	H	PWM	!PWM	C → B
5	0	1	1	1	0	0	L	H	L	L	PWM	!PWM	C → A
6	0	1	0	1	0	1	L	H	PWM	!PWM	L	L	B → A

(1) *!PWM* is the inverse of the PWM signal.

Table 8-5. Asynchronous 1x PWM Mode 1PWM_COM = 1 (SPI Only)

LOGIC AND HALL INPUTS							GATE DRIVE OUTPUTS						
STATE	INHC = 0			INHC = 1			PHASE A		PHASE B		PHASE C		DESCRIPTION
	INLA	INHB	INLB	INLA	INHB	INLB	GHA	GLA	GHB	GLB	GHC	GLC	
Stop	0	0	0	0	0	0	L	L	L	L	L	L	Stop
Align	1	1	1	1	1	1	PWM	L	L	H	L	H	Align
1	1	1	0	0	0	1	L	L	PWM	L	L	H	B → C
2	1	0	0	0	1	1	PWM	L	L	L	L	H	A → C
3	1	0	1	0	1	0	PWM	L	L	H	L	L	A → B
4	0	0	1	1	1	0	L	L	L	H	PWM	L	C → B
5	0	1	1	1	0	0	L	H	L	L	PWM	L	C → A
6	0	1	0	1	0	1	L	H	PWM	L	L	L	B → A

Figure 8-9 and Figure 8-10 show the different possible configurations in 1x PWM mode.

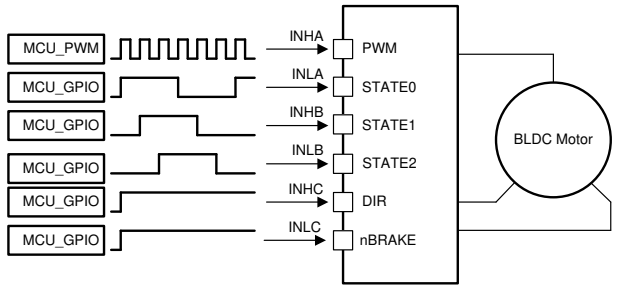


Figure 8-9. 1x PWM—Simple Controller

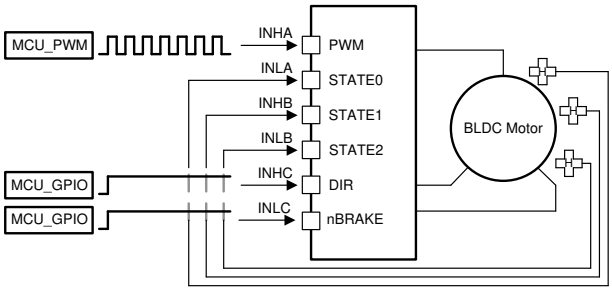


Figure 8-10. 1x PWM—Hall Effect Sensor

8.3.1.1.4 Independent PWM Mode (PWM_MODE = 11b or MODE Pin Tied to DVDD)

In independent PWM mode, the corresponding input pin independently controls each high-side and low-side gate driver. This control mode lets the DRV832x family of devices drive separate high-side and low-side loads with each half-bridge. These types of loads include unidirectional brushed DC motors, solenoids, and low-side and high-side switches. In this mode, if the system is configured in a half-bridge configuration, turning on both the high-side and low-side MOSFETs at the same time causes shoot-through.

Table 8-6. Independent PWM Mode Truth Table

INLx	INHx	GLx	GHx
0	0	L	L
0	1	L	H
1	0	H	L
1	1	H	H

Because the high-side and low-side V_{DS} overcurrent monitors share the SHx sense line, using the monitors when both the high-side and low-side gate drivers of one half-bridge are split and being used is not possible.

In this case, connect the SHx pin to the high-side driver and disable the V_{DS} overcurrent monitors as shown in Figure 8-11.

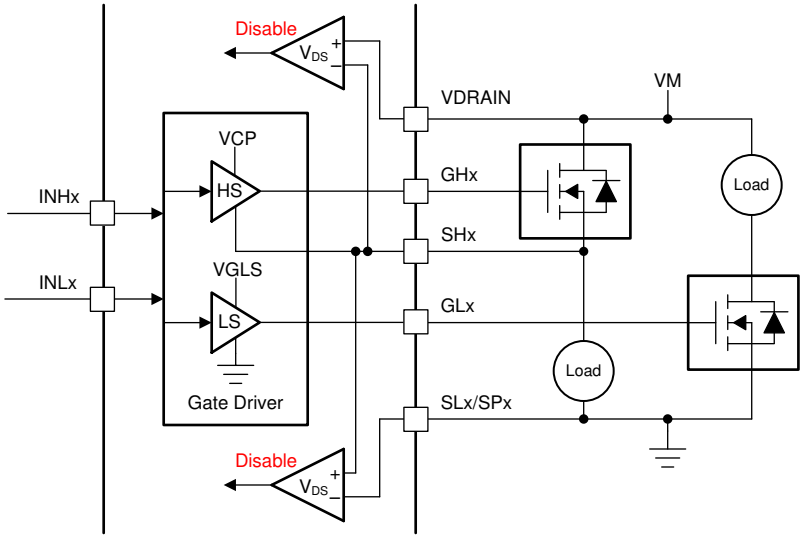


Figure 8-11. Independent PWM High-Side and Low-Side Drivers

If the half-bridge is used to implement only a high-side or low-side driver, using the V_{DS} overcurrent monitors is still possible. Connect the SHx pin as shown in Figure 8-12 or Figure 8-13. The unused gate driver and the corresponding input pin can stay disconnected.

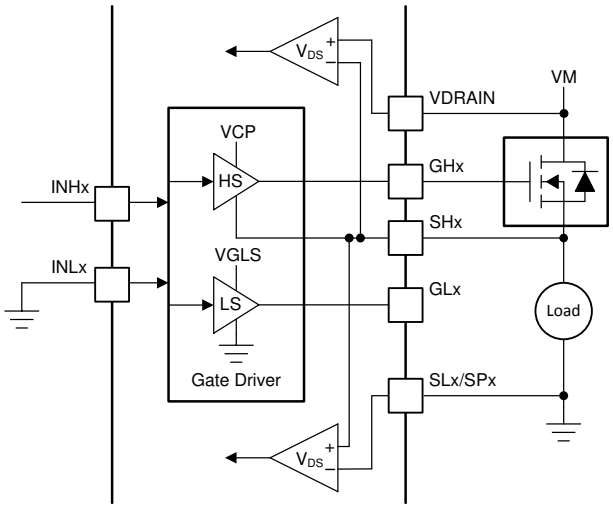


Figure 8-12. One High-Side Driver

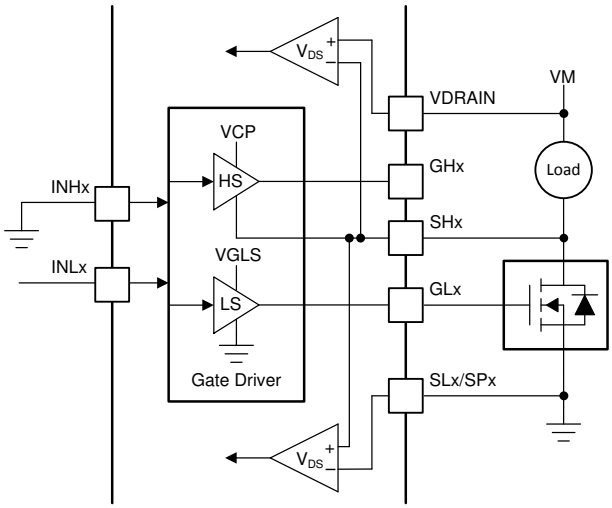


Figure 8-13. One Low-Side Driver

8.3.1.2 Device Interface Modes

The DRV832x family of devices supports two different interface modes (SPI and hardware) to let the end application design for either flexibility or simplicity. The two interface modes share the same four pins, allowing the different versions to be pin-to-pin compatible. This compatibility lets application designers evaluate with one interface version and potentially switch to another with minimal modifications to their design.

8.3.1.2.1 Serial Peripheral Interface (SPI)

The SPI devices support a serial communication bus that lets an external controller send and receive data with the DRV832x. This support lets the external controller configure device settings and read detailed fault

information. The interface is a four wire interface using the SCLK, SDI, SDO, and nSCS pins which are described as follows:

- The SCLK pin is an input that accepts a clock signal to determine when data is captured and propagated on the SDI and SDO pins.
- The SDI pin is the data input.
- The SDO pin is the data output. The SDO pin uses an open-drain structure and requires an external pullup resistor.
- The nSCS pin is the chip select input. A logic low signal on this pin enables SPI communication with the DRV832x.

For more information on the SPI, see *Section 8.5.1*.

8.3.1.2.2 Hardware Interface

Hardware interface devices convert the four SPI pins into four resistor-configurable inputs which are GAIN, IDRIVE, MODE, and VDS. This conversion lets the application designer configure the most common device settings by tying the pin logic high or logic low, or with a simple pullup or pulldown resistor. This removes the requirement for an SPI bus from the external controller. General fault information can still be obtained through the nFAULT pin.

- The GAIN pin configures the gain of the current sense amplifier.
- The IDRIVE pin configures the gate drive current strength.
- The MODE pin configures the PWM control mode.
- The VDS pin configures the voltage threshold of the V_{DS} overcurrent monitors.

For more information on the hardware interface, see *Section 8.3.3*.

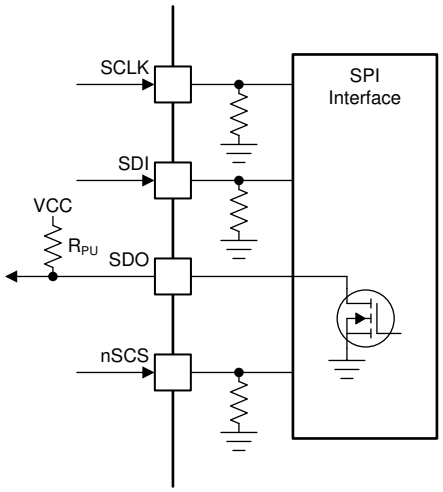


Figure 8-14. SPI

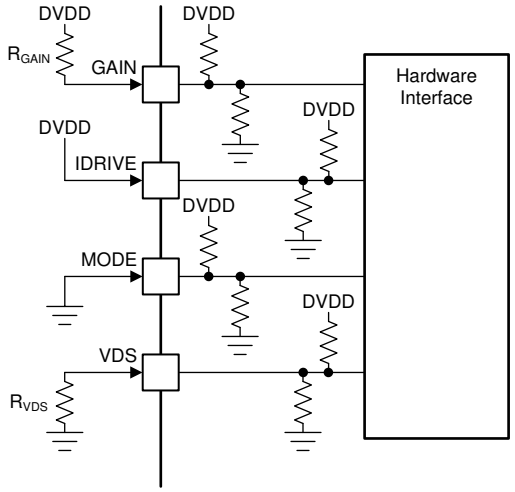


Figure 8-15. Hardware Interface

8.3.1.3 Gate Driver Voltage Supplies

The voltage supply for the high-side gate driver is created using a doubler charge pump that operates from the VM voltage supply input. The charge pump lets the gate driver correctly bias the high-side MOSFET gate with respect to the source across a wide input supply voltage range. The charge pump is regulated to keep a fixed output voltage of V_{VM} + 11V and supports an average output current of 25mA. When V_{VM} is less than 12V, the charge pump operates in full doubler mode and generates V_{VCP} = 2 × V_{VM} – 1.5V when unloaded. The charge pump is continuously monitored for undervoltage events to prevent under-driven MOSFET conditions. The charge pump requires an X5R or X7R, 1µF, 25V ceramic capacitor between the VM and VCP pins to act as the storage capacitor. Additionally, an X5R or X7R, 47nF, VM-rated ceramic capacitor is required between the CPH and CPL pins to act as the flying capacitor.

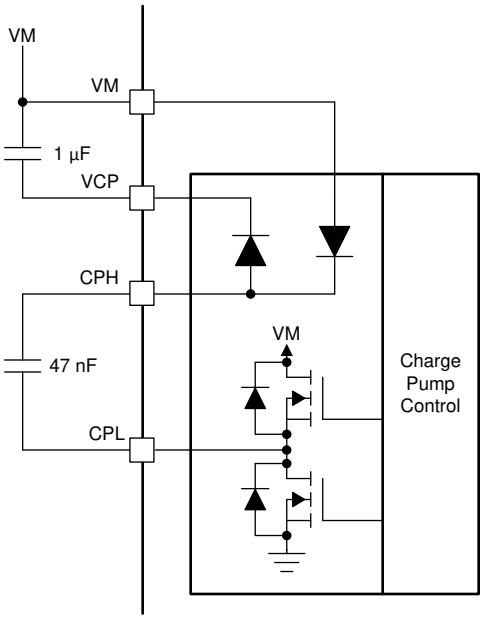


Figure 8-16. Charge Pump Architecture

The voltage supply of the low-side gate driver is created using a linear regulator that operates from the VM voltage supply input. The linear regulator lets the gate driver correctly bias the low-side MOSFET gate with respect to ground. The linear regulator output is fixed at 11V and supports an output current of 25mA.

8.3.1.4 Smart Gate Drive Architecture

The DRV832x gate drivers use an adjustable, complimentary, push-pull topology for both the high-side and low-side drivers. This topology allows for both a strong pullup and pulldown of the external MOSFET gates.

Additionally, the gate drivers use a Smart Gate Drive architecture to provide additional control of the external power MOSFETs, additional steps to protect the MOSFETs, and optimal tradeoffs between efficiency and robustness. This architecture is implemented through two components called IDRIVE and TDRIVE which are described in *Section 8.3.1.4.1* and *Section 8.3.1.4.2*. Figure 8-17 shows the high-level functional block diagram of the gate driver.

The IDRIVE gate drive current and TDRIVE gate drive time should be initially selected based on the parameters of the external power MOSFET used in the system and the desired rise and fall times (see *Section 9*).

The high-side gate driver also implements a Zener clamp diode to help protect the external MOSFET gate from overvoltage conditions in the case of external short-circuit events on the MOSFET.

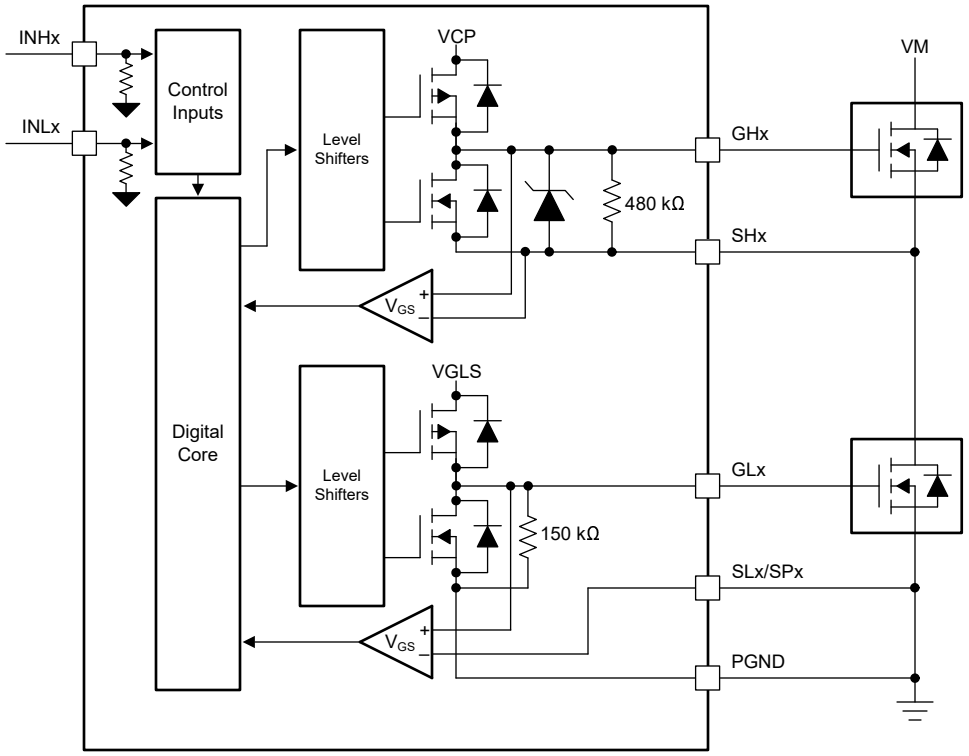


Figure 8-17. Gate Driver Block Diagram

8.3.1.4.1 IDRIVE: MOSFET Slew-Rate Control

The IDRIVE component implements adjustable gate drive current to control the MOSFET V_{DS} slew rates. The MOSFET V_{DS} slew rates are a critical factor for optimizing radiated emissions, energy, duration of diode recovery spikes, dV/dt gate turnon resulting in shoot-through, and switching voltage transients related to parasitics in the external half-bridge. The IDRIVE component operates on the principal that the MOSFET V_{DS} slew rates are predominately determined by the rate of gate charge (or gate current) delivered during the MOSFET Q_{GD} or Miller charging region. By letting the gate driver adjust the gate current, the gate driver can effectively control the slew rate of the external power MOSFETs.

The IDRIVE component lets the DRV832x family of devices dynamically switch between gate drive currents either through a register setting on SPI devices or the IDRIVE pin on hardware interface devices. The SPI devices provide 16 I_{DRIVE} settings ranging from 10mA to 1A source and 20mA to 2A sink. Hardware interface devices provide 7 I_{DRIVE} settings within the same ranges. The setting of the gate drive current is delivered to the gate during the turnon and turnoff of the external power MOSFET for the t_{DRIVE} duration. After the MOSFET turnon or turnoff, the gate driver switches to a smaller hold I_{HOLD} current to improve the gate driver efficiency. For additional details on the IDRIVE settings, see *Section 8.6* for the SPI devices and *Section 8.3.3* for the hardware interface devices.

8.3.1.4.2 TDRIVE: MOSFET Gate Drive Control

The TDRIVE component is an integrated gate drive state machine that provides automatic dead time insertion through handshaking between the high-side and low-side gate drivers, parasitic dV/dt gate turnon prevention, and MOSFET gate fault detection.

The first component of the TDRIVE state machine is automatic dead time insertion. Dead time is the period of time between the switching of the external high-side and low-side MOSFETs to make sure that they do not cross conduct and cause shoot-through. The DRV832x family of devices uses V_{GS} voltage monitors to measure the MOSFET gate-to-source voltage and determine the correct time to switch instead of relying on a fixed time value. This feature lets the dead time of the gate driver adjust for variation in the system such as temperature

drift and variation in the MOSFET parameters. An additional digital dead time (t_{DEAD}) can be inserted and is adjustable through the registers on SPI devices.

The second component of the TDRIVE state machine is parasitic dV/dt gate turnon prevention. To implement this component, the TDRIVE state machine enables a strong pulldown current (I_{STRONG}) on the opposite MOSFET gate whenever a MOSFET is switching. The strong pulldown occurs for the TDRIVE duration. This feature helps remove parasitic charge that couples into the MOSFET gate when the voltage half-bridge switch mode slews rapidly.

The third component of the TDRIVE state machine implements a scheme for gate fault detection to detect pin-to-pin solder defects, a MOSFET gate failure, or stuck-high or stuck-low voltage condition on a MOSFET gate. This implementation occurs with a pair of V_{GS} gate-to-source voltage monitors for each half-bridge gate driver. When the gate driver receives a command to change the state of the half-bridge, it starts to monitor the gate voltage of the external MOSFET. If the V_{GS} voltage has not reached the correct threshold at the end of the t_{DRIVE} period, the gate driver reports a fault. To make sure that a false fault is not detected, a t_{DRIVE} time should be selected that is longer than the time required to charge or discharge the MOSFET gate. The t_{DRIVE} time does not increase the PWM time and will terminate if another PWM command is received while active. For additional details on the TDRIVE settings, see the *Section 8.6* section for SPI devices. The hardware interface devices have a fixed t_{DRIVE} of 4µs.

Figure 8-18 shows an example of the TDRIVE state machine in operation.

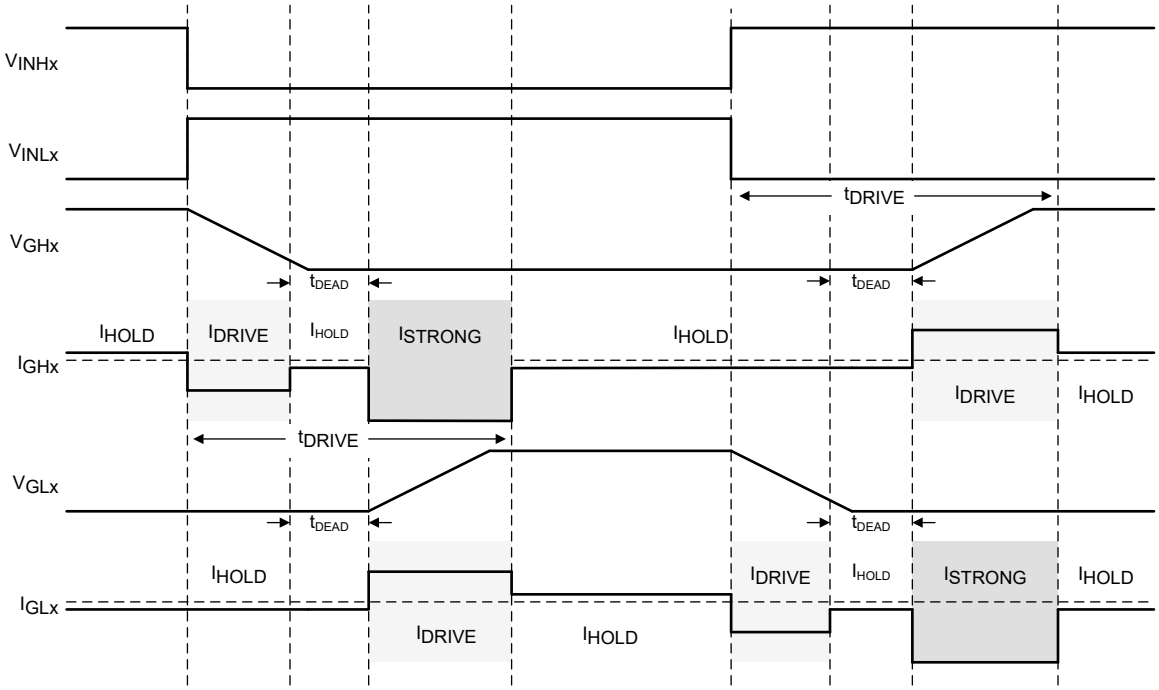


Figure 8-18. TDRIVE State Machine

8.3.1.4.3 Propagation Delay

The propagation delay time (t_{pd}) is measured as the time between an input logic edge to a detected output change. This time has three parts consisting of the digital input deglitcher delay, the digital propagation delay, and the delay through the analog gate drivers.

The input deglitcher prevents high-frequency noise on the input pins from affecting the output state of the gate drivers. To support multiple control modes and dead time insertion, a small digital delay is added as the input command propagates through the device. Lastly, the analog gate drivers have a small delay that contributes to the overall propagation delay of the device.

8.3.1.4.4 MOSFET V_{DS} Monitors

The gate drivers implement adjustable V_{DS} voltage monitors to detect overcurrent or short-circuit conditions on the external power MOSFETs. When the monitored voltage is greater than the V_{DS} trip point (V_{VDS_OCP}) for longer than the deglitch time (t_{OCP}), an overcurrent condition is detected and action is taken according to the device V_{DS} fault mode.

The high-side V_{DS} monitors measure the voltage between the VDRAIN and SHx pins. In devices with three current sense amplifiers (DRV8323 and DRV8323R), the low-side V_{DS} monitors measure the voltage between the SHx and SPx pins. If the current sense amplifier is unused, tie the SP pins to the common ground point of the external half-bridges. On device options without the current sense amplifiers (DRV8320 and DRV8320R) the low-side V_{DS} monitor measures between the SHx and SLx pins.

For the SPI devices, the reference point of the low-side V_{DS} monitor can be changed between the SPx and SNx pins if desired with the LS_REF register setting.

The V_{VDS_OCP} threshold is programmable from 0.06V to 1.88V. For additional information on the V_{DS} monitor levels, see *Section 8.6* for SPI devices and in *Section 8.3.3* for hardware interface devices.

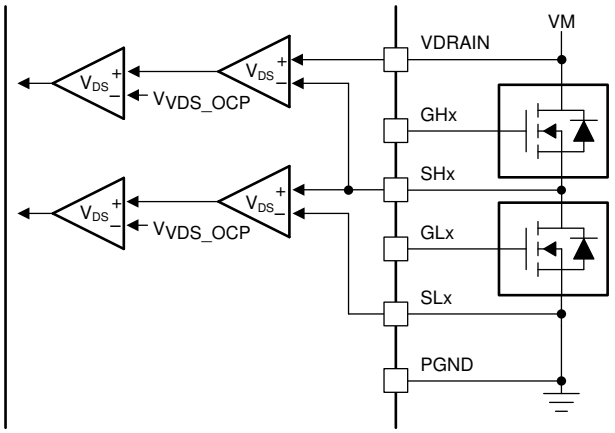


Figure 8-19. DRV8320 and DRV8320R V_{DS} Monitors

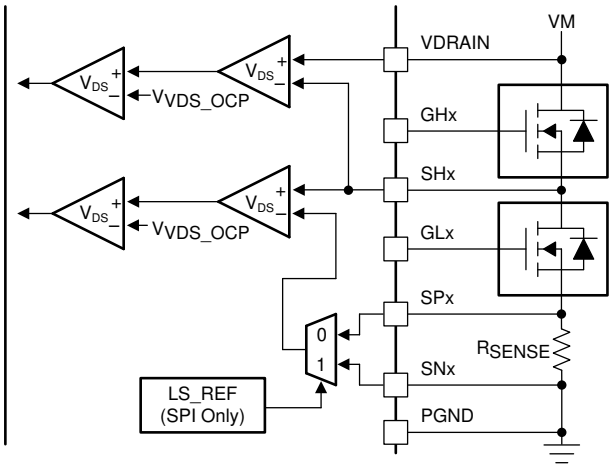


Figure 8-20. DRV8323 and DRV8323R V_{DS} Monitors

8.3.1.4.5 VDRAIN Sense Pin

The DRV832x family of devices provides a separate sense pin for the common point of the high-side MOSFET drain. This pin is called VDRAIN. This pin lets the sense line for the overcurrent monitors (VDRAIN) and the power supply (VM) stay separate and prevent noise on the VDRAIN sense line. This separation also lets implementation of a small filter on the gate driver supply (VM) or insertion of a boost converter to support lower voltage operation if desired. Care must still be used when designing the filter or separate supply because VM is still the reference point for the VCP charge pump that supplies the high-side gate drive voltage (V_{GSH}). The VM supply must not drift too far from the VDRAIN supply to avoid violating the V_{GS} voltage specification of the external power MOSFETs.

8.3.2 DVDD Linear Voltage Regulator

A 3.3V, 30mA linear regulator is integrated into the DRV832x family of devices and is available for use by external circuitry. This regulator can provide the supply voltage for a low-power MCU or other circuitry supporting low current. The output of the DVDD regulator should be bypassed near the DVDD pin with a X5R or X7R, 1µF, 6.3V ceramic capacitor routed directly back to the adjacent AGND ground pin.

The DVDD nominal, no-load output voltage is 3.3V. When the DVDD load current exceeds 30mA, the regulator functions like a constant-current source. The output voltage drops significantly with a current load greater than 30mA.

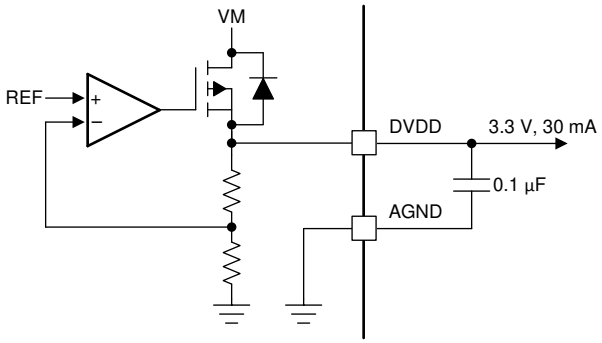


Figure 8-21. DVDD Linear Regulator Block Diagram

Use Equation 1 to calculate the power dissipated in the device by the DVDD linear regulator.

$$P = (V_{VM} - V_{DVDD}) \times I_{DVDD} \quad (1)$$

For example, at a V_{VM} of 24V, drawing 20mA out of DVDD results in a power dissipation as shown in Equation 2.

$$P = (24\ V - 3.3\ V) \times 20\ mA = 414\ mW \quad (2)$$

8.3.3 Pin Diagrams

Figure 8-22 shows the input structure for the logic level pins, INHx, INLx, CAL, ENABLE, nSCS, SCLK, and SDI. The input can be driven with a voltage or external resistor.

STATE	RESISTANCE
V_{IH}	Tied to DVDD
V_{IL}	Tied to AGND

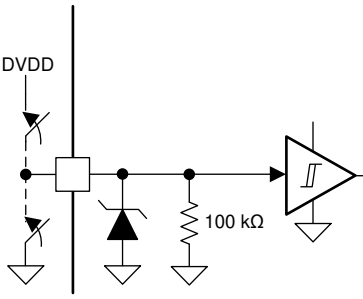
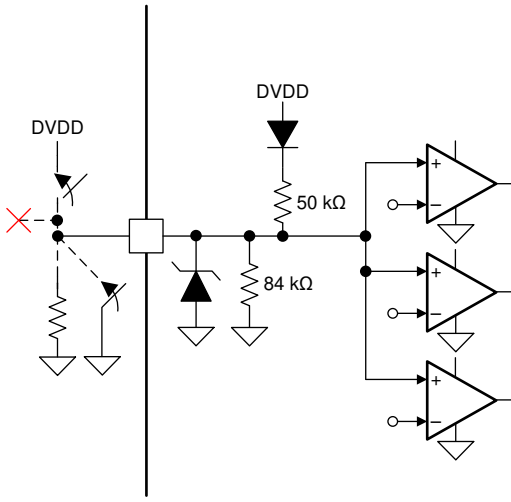


Figure 8-22. Logic-Level Input Pin Structure

Figure 8-23 shows the structure of the four level input pins, MODE and GAIN, on hardware interface devices. The input can be set with an external resistor.

STATE	RESISTANCE
V_{I4}	Tied to DVDD
V_{I3}	Hi-Z (>500 kΩ to AGND)
V_{I2}	47 kΩ ±5% to AGND
V_{I1}	Tied to AGND

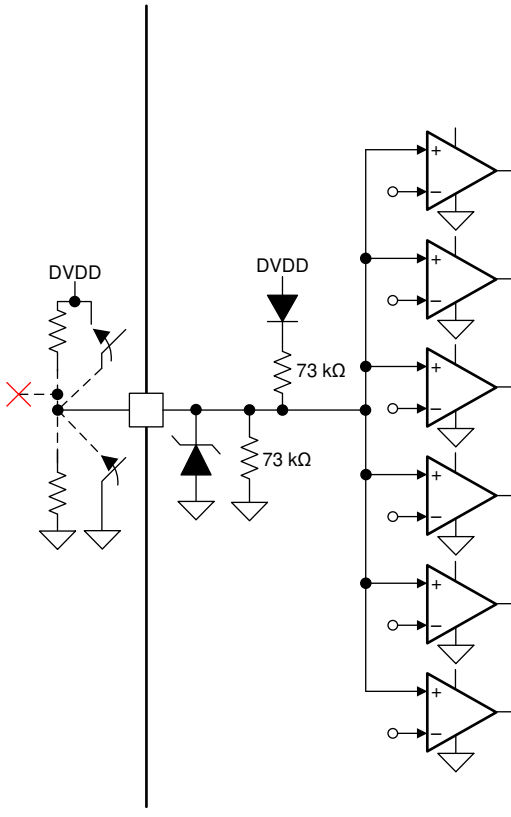


MODE	GAIN
Independent	40 V/V
1x PWM	20V/V
3x PWM	10 V/V
6x PWM	5 V/V

Figure 8-23. Four Level Input Pin Structure

Figure 8-24 shows the structure of the seven level input pins, IDRIVE and VDS, on hardware interface devices. The input can be set with an external resistor.

STATE	RESISTANCE
V_{I7}	Tied to DVDD
V_{I6}	18 kΩ ± 5% to DVDD
V_{I5}	75 kΩ ± 5% to DVDD
V_{I4}	Hi-Z (>500 kΩ to AGND)
V_{I3}	75 kΩ ± 5% to AGND
V_{I2}	18 kΩ ±5% to AGND
V_{I1}	Tied to AGND



IDRIVE	VDS
1/2 A	Disabled
570/1140 mA	1.88 V
260/520 mA	1.13 V
120/240 mA	0.60 V
60/120 mA	0.26 V
30/60 mA	0.13 V
10/20 mA	0.06 V

Figure 8-24. Seven Level Input Pin Structure

Figure 8-25 shows the structure of the open-drain output pins, nFAULT and SDO. The open-drain output requires an external pullup resistor to function correctly.

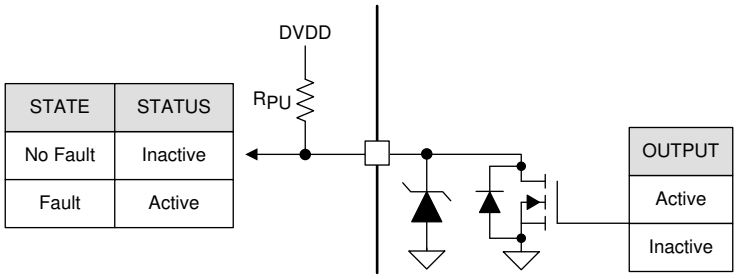


Figure 8-25. Open-Drain Output Pin Structure

8.3.4 Low-Side Current Sense Amplifiers (DRV8323 and DRV8323R Only)

The DRV8323 and DRV8323R integrate three, high-performance low-side current sense amplifiers for current measurements using low-side shunt resistors in the external half-bridges. Low-side current measurements are commonly used to implement overcurrent protection, external torque control, or brushless DC commutation with the external controller. All three amplifiers can be used to sense the current in each of the half-bridge legs or one amplifier can be used to sense the sum of the half-bridge legs. The current sense amplifiers include features such as programmable gain, offset calibration, unidirectional and bidirectional support, and a voltage reference pin (VREF). If any of the three current sense amplifiers are not being used, they can be tied off by shorting the o connect the SPx or SNx pin to the SNx pin to the SPx pin and leaving the SOx pin unconnected. Remember t low-side FET source, so that the overcurrent VDS monitor is still functional.

8.3.4.1 Bidirectional Current Sense Operation

The SOx pin on the DRV8323 and DRV8323R outputs an analog voltage equal to the voltage across the SPx and SNx pins multiplied by the gain setting (G_{CSA}). The gain setting is adjustable between four different levels (5V/V, 10V/V, 20V/V, and 40V/V). Use Equation 3 to calculate the current through the shunt resistor.

$$I = \frac{\frac{V_{VREF}}{2} - V_{SOx}}{G_{CSA} \times R_{SENSE}} \quad (3)$$

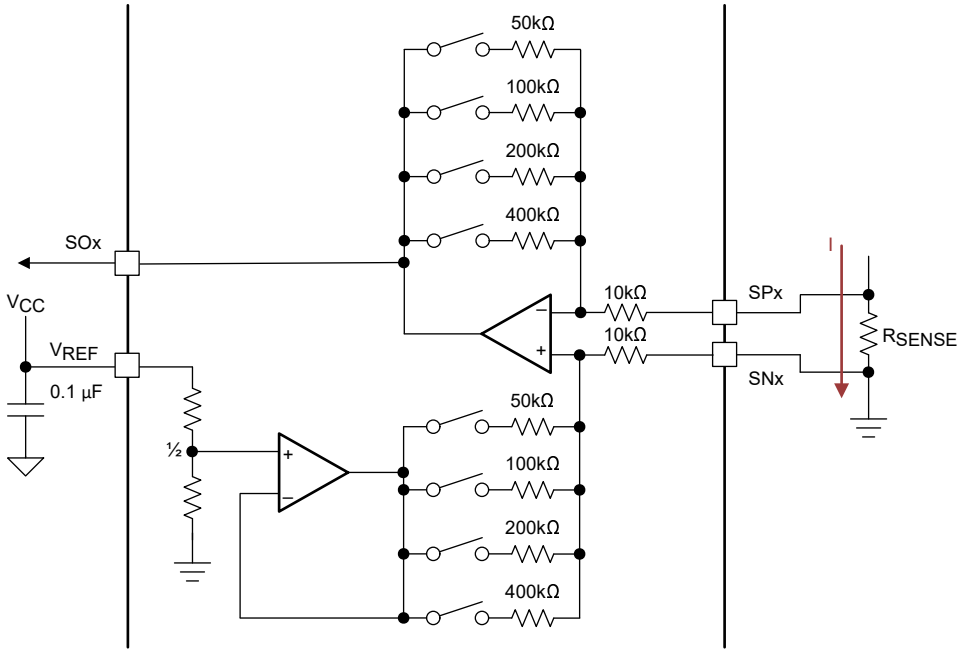


Figure 8-26. Bidirectional Current Sense Configuration

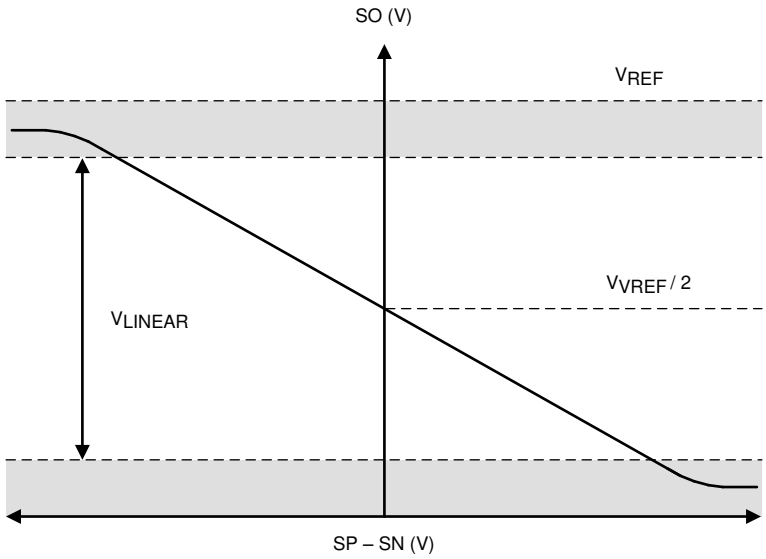


Figure 8-27. Bidirectional Current Sense Output

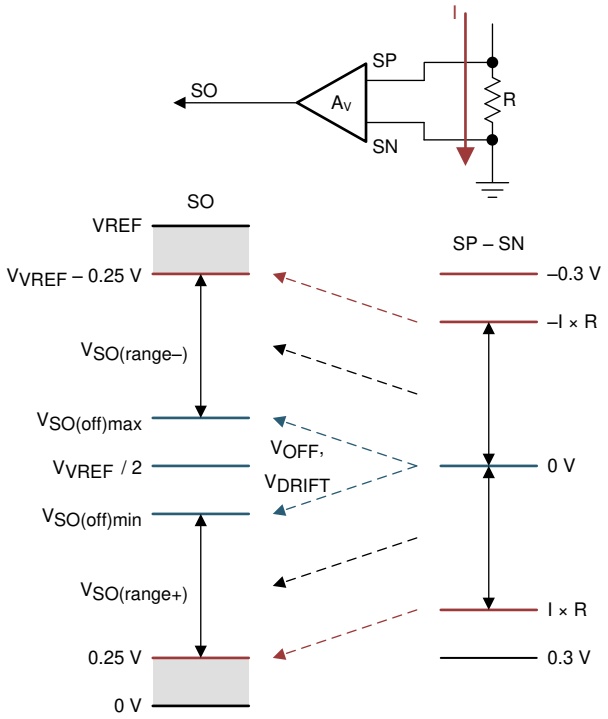


Figure 8-28. Bidirectional Current Sense Regions

8.3.4.2 Unidirectional Current Sense Operation (SPI only)

On the DRV8323 and DRV8323R SPI devices, use the VREF_DIV bit to remove the VREF divider. In this case the current sense amplifier operates unidirectionally and the SOx pin outputs an analog voltage equal to the voltage across the SPx and SNx pins multiplied by the gain setting (G_{CSA}). Use Equation 4 to calculate the current through the shunt resistor.

$$I = \frac{V_{VREF} - 0.3 - V_{SOx}}{G_{CSA} \times R_{SENSE}} \quad (4)$$

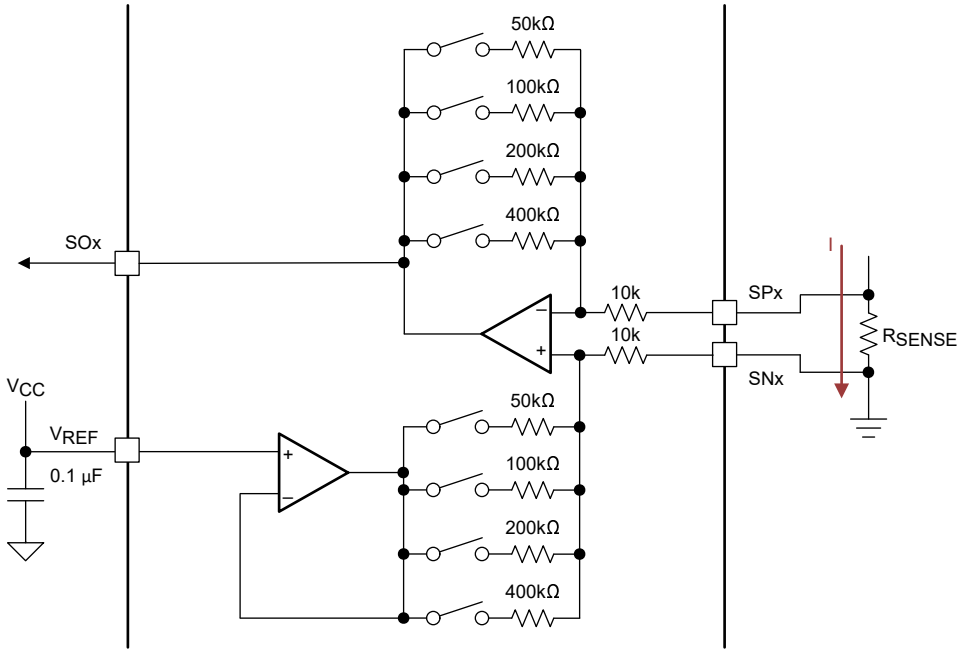


Figure 8-29. Unidirectional Current-Sense Configuration

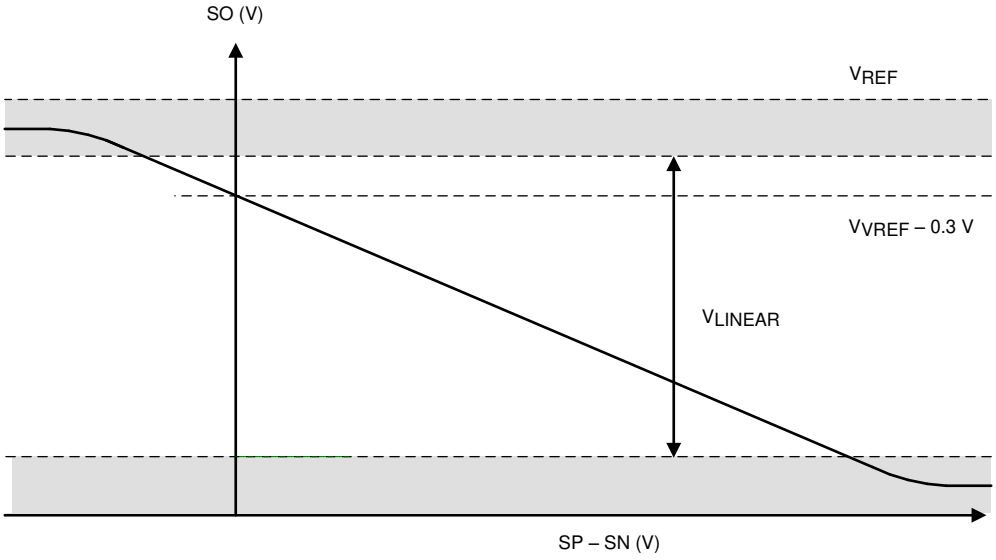


Figure 8-30. Unidirectional Current-Sense Output

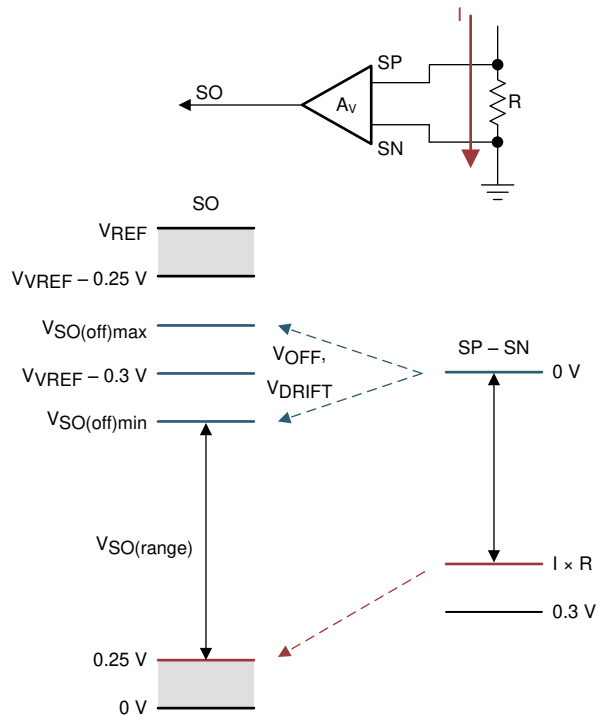


Figure 8-31. Unidirectional Current-Sense Regions

8.3.4.3 Auto Offset Calibration

To minimize DC offset, the DRV8323 and DRV8323R devices can perform an automatic offset calibration through the SPI registers (CSA_CAL_X) or CAL pin. When the calibration is enabled, the inputs to the amplifier are shorted, the load is disconnected, and the gain (G_{CSA}) of the amplifier is changed to the 40V/V setting. The amplifier then goes through an automatic trim routine to minimize the input offset. The automatic trim routine requires 100µs to complete after the calibration is enabled. After this time, the inputs of the amplifier stay shorted, the load stays disconnected, and the gain stays at 40V/V if further offset calibration is desired to be done by the external controller. To complete the offset calibration, the CSA_CAL_X registers or CAL pin should be taken back low. The gain is returned to the original gain setting after the device completes calibration. For the best results, perform offset calibration when the external MOSFETS are not switching to decrease the potential noise impact to the amplifier. When the current sense amplifiers go into a calibration mode, the VREF pin is set to bidirectional mode if the device is configured in unidirectional mode. The setting of the VREF pin affects the channels all three current sense amplifier, even if the CSA_CAL_X register is not set for the all channels.

8.3.4.4 MOSFET V_{DS} Sense Mode (SPI Only)

The current sense amplifiers on the DRV8323 and DRV8323R SPI devices can be configured to amplify the voltage across the external low-side MOSFET V_{DS}. This configuration lets the external controller measure the voltage drop across the MOSFET $R_{DS(on)}$ without the shunt resistor and then calculate the half-bridge current level.

To enable this mode set the CSA_FET bit to 1. The positive input of the amplifier is then internally connected to the SHx pin with an internal clamp to prevent high voltage on the SHx pin from damaging the sense amplifier inputs. During this mode of operation, the SPx pins should stay disconnected. When the CSA_FET bit is set to 1, the negative reference for the low-side V_{DS} monitor is automatically set to the SNx pin, regardless of the state of the LS_REF bit. This setting is implemented to prevent disabling of the low-side V_{DS} monitor.

If the system operates in MOSFET V_{DS} current sense mode, route the SHx and SNx pins with Kelvin connections across the drain and source of the external low-side MOSFETs.

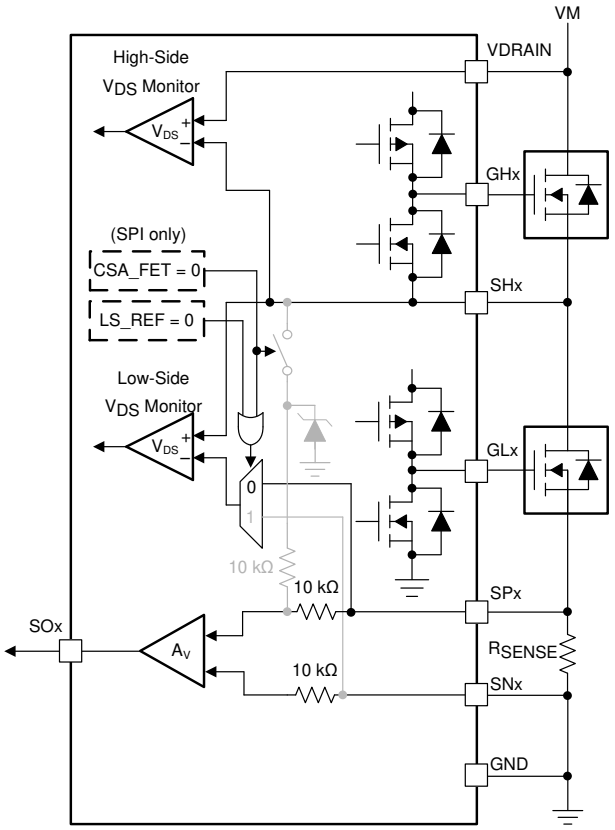


Figure 8-32. Resistor Sense Configuration

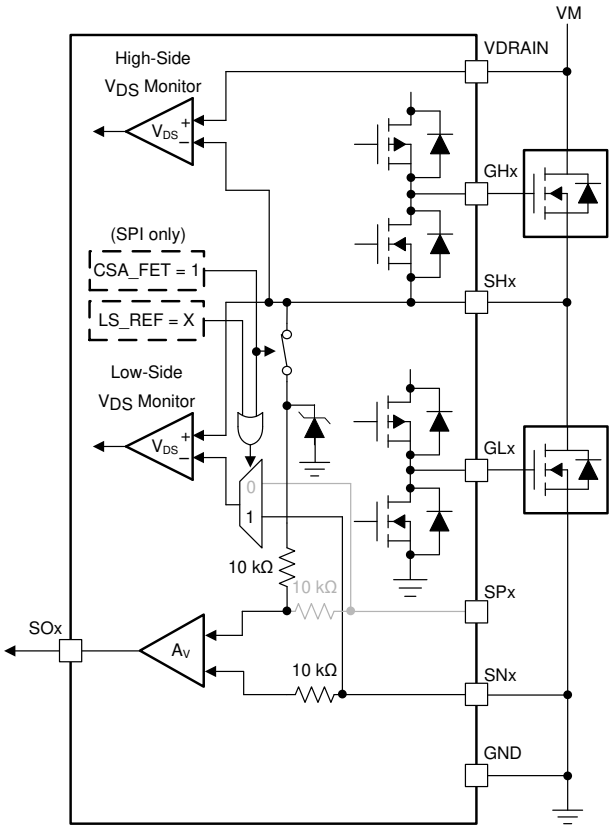


Figure 8-33. V_{DS} Current Sense Mode

When operating in MOSFET V_{DS} current sense mode, the amplifier is enabled at the end of the t_{DRIVE} time. At this time, the amplifier input is connected to the SHx pin, and the SOx output is valid. When the low-side MOSFET receives a signal to turn off the amplifier inputs, SPx and SNx, are shorted together internally.

8.3.5 Step-Down Buck Regulator

The DRV8320R and DRV8323R have an integrated buck regulator (LMR16006) to supply power for an external controller or system voltage rail. The LMR16006 device is a 60V, 600mA, buck (step-down) regulator.

The buck regulator has a very-low quiescent current during light loads to prolong battery life. The LMR16006 device improves performance during line and load transients by implementing a constant-frequency current-mode control scheme which requires less output capacitance and simplifies frequency compensation design. The LMR16006 is the LMR16006X device version that uses a 0.7MHz switching frequency.

The LMR16006 device decreases the external component count by integrating the bootstrap recharge diode. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor on the CB to SW pin. The bootstrap capacitor voltage is monitored by a UVLO circuit and turns off the high-side MOSFET when the boot voltage falls lower than a preset threshold.

The LMR16006 device can operate at high duty cycles because of the boot UVLO and then refreshes the wimp MOSFET. The output voltage can be stepped down to as low as the 0.8V reference. The internal soft-start feature minimizes inrush currents.

For additional details, a block diagram showing the wimp MOSFET, and design information refer to the *LMR16006 SIMPLE SWITCHER® 60 V 0.6 A Buck Regulators With High Efficiency Eco-mode* datasheet.

8.3.5.1 Fixed Frequency PWM Control

The LMR16006 device has a fixed switching frequency and implements peak current-mode control. The output voltage is compared through external resistors on the FB pin to an internal voltage reference by an error

amplifier which drives the internal COMP node. An internal oscillator initiates the turnon of the high-side power switch. The error amplifier output is compared to the high-side power switch current. When the power switch current reaches the level set by the internal COMP voltage, the power switch turns off. The internal COMP node voltage increases and decreases as the output current increases and decreases. The device implements a current limit by clamping the COMP node voltage to a maximum level.

8.3.5.2 Bootstrap Voltage (CB)

The LMR16006 device has an integrated bootstrap regulator, and requires a small ceramic capacitor between the CB and SW pins to provide the gate drive voltage for the high-side MOSFET. The CB capacitor is refreshed when the high-side MOSFET is off and the low-side diode conducts. To improve dropout, the LMR16006 device is designed to operate at 100% duty cycle as long as the CB to SW pin voltage is greater than 3V. When the voltage from the CB to SW pin drops to less than 3V, the high-side MOSFET turns off using a UVLO circuit which lets the low-side diode conduct and refresh the charge on the CB capacitor. Because the supply current sourced from the CB capacitor is low, the high-side MOSFET can stay on for more switching cycles than are required to refresh the capacitor. Therefore, the effective duty cycle of the switching regulator is high. Attention must be given in maximum duty-cycle applications with a light load. To make sure the SW pin can be pulled to ground to refresh the CB capacitor, an internal circuit charges the CB capacitor when the load is light or the device is working in dropout condition.

8.3.5.3 Output Voltage Setting

The output voltage is set using the feedback pin (FB) and a resistor divider connected to the output as shown in Figure 9-1. The voltage of the feedback pin is 0.765V, so the ratio of the feedback resistors sets the output voltage according to Equation 5.

$$V_O = 0.765\,V \times \left(1 + \left[\frac{R1}{R2}\right]\right) \tag{5}$$

Typically the starting value of R2 is from 1kΩ to 100kΩ. Use Equation 6 to calculate the value of R1.

$$R1 = R2 \times \left(\left[\frac{V_O}{0.765\,V}\right] - 1\right) \tag{6}$$

8.3.5.4 Enable nSHDN and VIN Undervoltage Lockout

The nSHDN pin of the LMR16006 device is an input that is tolerant of high voltages with an internal pullup circuit. The device can be enabled even if the nSHDN pin is floating. The regulator can also be turned on using 1.23V or higher logic signals. If the use of a higher voltage is desired because of system or other constraints, a 100kΩ or larger value resistor is recommended between the applied voltage and the nSHDN pin to help protect the device. When the nSHDN pin is pulled down to 0V, the device turns off and goes to the lowest shutdown current mode. In shutdown mode the supply current decreases to approximately 1μA. If the shutdown function is unused, the nSHDN pin can be tied to the VIN pin with a 100kΩ resistor. The maximum voltage to the nSHDN pin should not exceed 60V. The LMR16006 device has an internal UVLO circuit to shut down the output if the input voltage falls lower than a UVLO threshold level that is internally fixed. Shutting down the output in this way makes sure the regulator is not latched into an unknown state during low input voltage conditions. The regulator powers up when the input voltage exceeds the voltage level. If the UVLO voltage must be higher, use the nSHDN pin to adjust the system UVLO by using external resistors.

8.3.5.5 Current Limit

The LMR16006 device implements current-mode control which uses the internal COMP voltage to turn off the high-side MOSFET on a cycle-by-cycle basis. Each cycle, the switch current and internal COMP voltage are compared. When the peak switch current intersects the COMP voltage, the high-side switch turns off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP node high, increasing the switch current. The error amplifier output is clamped internally causing it to function as a switch current limit.

8.3.5.6 Overvoltage Transient Protection

The LMR16006 device incorporates an overvoltage transient protection (OVTP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unloaded transients on power supply designs with low-value output capacitance. For example, when the power supply output is overloaded, the error amplifier compares the actual output voltage to the internal reference voltage. If the voltage of the FB pin is lower than the internal reference voltage for a considerable time, the output of the error amplifier responds by clamping the error amplifier output to a high voltage, therefore requesting the maximum output current. When the condition clears, the regulator output rises and the error amplifier output transitions to the steady-state duty cycle. In some applications, the output voltage of the power supply can respond faster than the error amplifier output can respond which can result in output overshoot. The OVTP feature minimizes the output overshoot when using a low-value output capacitor by implementing a circuit to compare the FB pin voltage to the OVTP threshold which is 108% of the internal voltage reference. If the FB pin voltage is greater than the OVTP threshold, the high-side MOSFET is disabled preventing current from flowing to the output and minimizing output overshoot. When the FB voltage drops lower than the OVTP threshold, the high-side MOSFET can turn on at the next clock cycle.

8.3.5.7 Thermal Shutdown

The device implements an internal thermal shutdown to help protect the device if the junction temperature exceeds 170°C (typical). The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. When the junction temperature decreases to less than 160°C (typical), the device reinitiates the power-up sequence.

8.3.6 Gate Driver Protective Circuits

The DRV832x family of devices is protected against VM undervoltage, charge pump undervoltage, MOSFET V_{DS} overcurrent, gate driver shorts, and overtemperature events.

Table 8-7. Fault Action and Response (SPI Devices)

FAULT	CONDITION	CONFIGURATION	REPORT	GATE DRIVER	LOGIC	RECOVERY
VM undervoltage (UVLO)	$V_{VM} < V_{UVLO}$	—	nFAULT	Hi-Z	Disabled	Automatic: $V_{VM} > V_{UVLO}$
Charge pump undervoltage (CPUV)	$V_{VCP} < V_{CPUV}$	DIS_CPUV = 0b	nFAULT	Hi-Z	Active	Automatic: $V_{VCP} > V_{CPUV}$
		DIS_CPUV = 1b	None	Active	Active	
V_{DS} overcurrent (VDS_OCP)	$V_{DS} > V_{VDS\_OCP}$	OCP_MODE = 00b	nFAULT	Hi-Z	Active	Latched: CLR_FLT, ENABLE Pulse
		OCP_MODE = 01b	nFAULT	Hi-Z	Active	Retry: t_{RETRY}
		OCP_MODE = 10b	nFAULT	Active	Active	No action
		OCP_MODE = 11b	None	Active	Active	No action
V_{SENSE} overcurrent (SEN_OCP)	$V_{SP} > V_{SEN\_OCP}$	OCP_MODE = 00b	nFAULT	Hi-Z	Active	Latched: CLR_FLT, ENABLE Pulse
		OCP_MODE = 01b	nFAULT	Hi-Z	Active	Retry: t_{RETRY}
		OCP_MODE = 10b	nFAULT	Active	Active	No action
		OCP_MODE = 11b or DIS_SEN = 1b	None	Active	Active	No action
Gate driver fault (GDF)	Gate voltage stuck after t_{DRIVE}	DIS_GDF = 0b	nFAULT	Hi-Z	Active	Latched: CLR_FLT, ENABLE Pulse
		DIS_GDF = 1b	None	Active	Active	No action
Thermal warning (OTW)	$T_J > T_{OTW}$	OTW_REP = 0b	None	Active	Active	No action
		OTW_REP = 1b	nFAULT	Active	Active	Automatic: $T_J < T_{OTW} - T_{HYS}$
Thermal shutdown (OTSD)	$T_J > T_{OTSD}$	—	nFAULT	Hi-Z	Active	Automatic: $T_J < T_{OTSD} - T_{HYS}$

8.3.6.1 VM Supply Undervoltage Lockout (UVLO)

If at any time the input supply voltage on the VM pin falls lower than the V_{UVLO} threshold, all of the external MOSFETs are disabled, the charge pump is disabled, and the nFAULT pin is driven low. The FAULT and VM_UVLO bits are also latched high in the registers on SPI devices. Normal operation starts again (gate driver

operation and the nFAULT pin is released) when the VM undervoltage condition clears. The VM_UVLO bit stays set until cleared through the CLR_FLT bit or an ENABLE pin reset pulse (t_{RST}).

8.3.6.2 VCP Charge Pump Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin (charge pump) falls lower than the V_{CPUV} threshold voltage of the charge pump, all of the external MOSFETs are disabled and the nFAULT pin is driven low. The FAULT and CPUV bits are also latched high in the registers on SPI devices. Normal operation starts again (gate driver operation and the nFAULT pin is released) when the VCP undervoltage condition clears. The CPUV bit stays set until cleared through the CLR_FLT bit or an ENABLE pin reset pulse (t_{RST}). Setting the DIS_CPUV bit high on the SPI devices disables this protection feature. On hardware interface devices, the CPUV protection is always enabled.

8.3.6.3 MOSFET V_{DS} Overcurrent Protection (VDS_OCP)

A MOSFET overcurrent event is sensed by monitoring the V_{DS} voltage drop across the external MOSFET $R_{DS(on)}$. If the voltage across an enabled MOSFET exceeds the V_{VDS_OCP} threshold for longer than the t_{OCP_DEG} deglitch time, a VDS_OCP event is recognized and action is done according to the OCP_MODE bit. On hardware interface devices, the V_{VDS_OCP} threshold is set with the VDS pin, the t_{OCP_DEG} is fixed at 4µs, and the OCP_MODE bit is configured for 4ms automatic retry but can be disabled by tying the VDS pin to DVDD. On SPI devices, the V_{VDS_OCP} threshold is set through the VDS_LVL SPI register, the t_{OCP_DEG} is set through the OCP_DEG SPI register, and the OCP_MODE bit can operate in four different modes: V_{DS} latched shutdown, V_{DS} automatic retry, V_{DS} report only, and V_{DS} disabled.

8.3.6.3.1 V_{DS} Latched Shutdown (OCP_MODE = 00b)

After a VDS_OCP event in this mode, all external MOSFETs are disabled and the nFAULT pin is driven low. When the external MOSFETs are disabled in this way, the driver automatically uses a lower setting for the gate drive current instead of the programmed IDRIVE setting. This setting lets any large current that may be present to be switched off slowly to minimize any inductive kickback caused by parasitic inductance in the system. The FAULT, VDS_OCP, and corresponding MOSFET OCP bits are latched high in the SPI registers. Normal operation starts again (gate driver operation and the nFAULT pin is released) when the VDS_OCP condition clears and a clear faults command is issued either through the CLR_FLT bit or an ENABLE reset pulse (t_{RST}).

8.3.6.3.2 V_{DS} Automatic Retry (OCP_MODE = 01b)

After a VDS_OCP event in this mode, all the external MOSFETs are disabled and the nFAULT pin is driven low. When the external MOSFETs are disabled in this way, the driver automatically uses a lower setting for the gate drive current instead of the programmed IDRIVE setting. This setting lets any large current that may be present to be switched off slowly to minimize any inductive kickback caused by parasitic inductance in the system. The FAULT, VDS_OCP, and corresponding MOSFET OCP bits are latched high in the SPI registers. Normal operation starts again automatically (gate driver operation and the nFAULT pin is released) after the t_{RETRY} time elapses. The FAULT, VDS_OCP, and MOSFET OCP bits stay latched until the t_{RETRY} period expires.

8.3.6.3.3 V_{DS} Report Only (OCP_MODE = 10b)

No protective action occurs after a VDS_OCP event in this mode. The overcurrent event is reported by driving the nFAULT pin low and latching the FAULT, VDS_OCP, and corresponding MOSFET OCP bits high in the SPI registers. The gate drivers continue to operate as usual. The external controller must manage the overcurrent condition by acting appropriately. The reporting clears (nFAULT pin is released) when the VDS_OCP condition clears and a clear faults command is issued either through the CLR_FLT bit or an ENABLE reset pulse (t_{RST}).

8.3.6.3.4 V_{DS} Disabled (OCP_MODE = 11b)

No action or reporting occurs after a VDS_OCP event in this mode.

8.3.6.4 V_{SENSE} Overcurrent Protection (SEN_OCP)

Half-bridge overcurrent is also monitored by sensing the voltage drop across the external current sense resistor with the SP pin. If at any time the voltage on the SP input of the CSA exceeds the V_{SEN_OCP} threshold for longer than the t_{OCP_DEG} deglitch time, a SEN_OCP event is recognized and action is done according to the

OCP_MODE bit. On hardware interface devices, the V_{SENSE} threshold is fixed at 1V, t_{OCP_DEG} is fixed at 4µs, and the OCP_MODE for V_{SENSE} is fixed for 4ms automatic retry. On SPI devices, the V_{SENSE} threshold is set through the SEN_LVL SPI register, the t_{OCP_DEG} is set through the OCP_DEG SPI register, and the OCP_MODE bit can operate in four different modes: V_{SENSE} latched shutdown, V_{SENSE} automatic retry, V_{SENSE} report only, and V_{SENSE} disabled.

8.3.6.4.1 V_{SENSE} Latched Shutdown (OCP_MODE = 00b)

After a SEN_OCP event in this mode, all the external MOSFETs are disabled and the nFAULT pin is driven low. The FAULT and SEN_OCP bits are latched high in the SPI registers. Normal operation starts again (gate driver operation and the nFAULT pin is released) when the SEN_OCP condition clears and a clear faults command is issued either through the CLR_FLT bit or an ENABLE reset pulse (t_{RST}).

8.3.6.4.2 V_{SENSE} Automatic Retry (OCP_MODE = 01b)

After a SEN_OCP event in this mode, all the external MOSFETs are disabled and the nFAULT pin is driven low. The FAULT, SEN_OCP, and corresponding sense OCP bits are latched high in the SPI registers. Normal operation starts again automatically (gate driver operation and the nFAULT pin is released) after the t_{RETRY} time elapses. The FAULT, SEN_OCP, and sense OCP bits stay latched until the t_{RETRY} period expires.

8.3.6.4.3 V_{SENSE} Report Only (OCP_MODE = 10b)

No protective action occurs after a SEN_OCP event in this mode. The overcurrent event is reported by driving the nFAULT pin low and latching the FAULT and SEN_OCP bits high in the SPI registers. The gate drivers continue to operate. The external controller manages the overcurrent condition by acting appropriately. The reporting clears (nFAULT released) when the SEN_OCP condition clears and a clear faults command is issued either through the CLR_FLT bit or an ENABLE reset pulse (t_{RST}).

8.3.6.4.4 V_{SENSE} Disabled (OCP_MODE = 11b or DIS_SEN = 1b)

No action occurs after a SEN_OCP event in this mode. The SEN_OCP bit can be disabled independently of the VDS_OCP bit by using the DIS_SEN SPI register.

8.3.6.5 Gate Driver Fault (GDF)

The GHx and GLx pins are monitored such that if the voltage on the external MOSFET gate does not increase or decrease after the t_{DRIVE} time, a gate driver fault is detected. This fault may be encountered if the GHx or GLx pins are shorted to the PGND, SHx, or VM pins. Additionally, a gate driver fault may be encountered if the selected I_{DRIVE} setting is not sufficient to turn on the external MOSFET within the t_{DRIVE} period. After a gate drive fault is detected, all external MOSFETs are disabled and the nFAULT pin driven low. In addition, the FAULT, GDF, and corresponding VGS bits are latched high in the SPI registers. Normal operation starts again (gate driver operation and the nFAULT pin is released) when the gate driver fault condition clears and a clear faults command is issued either through the CLR_FLT bit or an ENABLE reset pulse (t_{RST}). On SPI devices, setting the DIS_GDF bit high disables this protection feature.

Gate driver faults can indicate that the selected I_{DRIVE} or t_{DRIVE} settings are too low to slew the external MOSFET in the desired time. Increasing either the I_{DRIVE} or t_{DRIVE} setting can resolve gate driver faults in these cases. Alternatively, if a gate-to-source short occurs on the external MOSFET, a gate driver fault is reported because of the MOSFET gate not turning on.

8.3.6.6 Thermal Warning (OTP) (SPI only)

If the die temperature exceeds the trip point of the thermal warning (T_{OTW}), the OTW bit is set in the registers of SPI devices. The device performs no additional action and continues to function. When the die temperature falls lower than the hysteresis point of the thermal warning, the OTW bit clears automatically. The OTW bit can also be configured to report on the nFAULT pin by setting the OTW_REP bit to 1 through the SPI registers.

8.3.6.7 Thermal Shutdown (OTSD)

If the die temperature exceeds the trip point of the thermal shutdown limit (T_{OTSD}), all the external MOSFETs are disabled, the charge pump is shut down, and the nFAULT pin is driven low. In addition, the FAULT and TSD bits are latched high. Normal operation starts again (gate driver operation and the nFAULT pin is released) when the

overtemperature condition clears. The TSD bit stays latched high indicating that a thermal event occurred until a clear fault command is issued either through the CLR_FLT bit or an ENABLE reset pulse (t_{RST}). This protection feature cannot be disabled.

8.4 Device Functional Modes

8.4.1 Gate Driver Functional Modes

8.4.1.1 Sleep Mode

The ENABLE pin manages the state of the DRV832x family of devices. When the ENABLE pin is low, the device goes to a low-power sleep mode. In sleep mode, all gate drivers are disabled, sense amplifiers (if present) are disabled, all external MOSFETs are disabled, the charge pump is disabled, the DVDD regulator is disabled, and the SPI bus is disabled. The LMR16006X buck regulator (if present) is not controlled by the ENABLE pin and can be operated independently of the gate driver. The t_{SLEEP} time must elapse after a falling edge on the ENABLE pin before the device goes to sleep mode.

Note

The INHx and INLx pins should be low before t_{RST} (max 40µs) after ENABLE goes low to prevent the GHx and GLx outputs from entering into Hi-Z state while any of the gates are high.

Figure 8-34 shows the behavior of the device after ENABLE goes low when the INHx and INLx pins are low prior to the time when the driver outputs ignore the inputs 50µs after ENABLE goes low. The GHx and GLx pins will remain low as the device begins the process to enter sleep mode. Figure 8-35 shows the behavior of the device if the input PWMs are not pulled low prior to the driver outputs ignoring the inputs. The GHx and GLx pins will follow the inputs for 50µs after ENABLE goes low, then will become Hi-Z until nFAULT goes low up to 400µs after ENABLE is low. To avoid this behavior, the INHx and INLx pins should be low before tRST (max 40µs) after ENABLE goes low as shown in Figure 8-34 to avoid the GHx and GLx outputs going into Hi-Z state while any of the gate outputs are high.

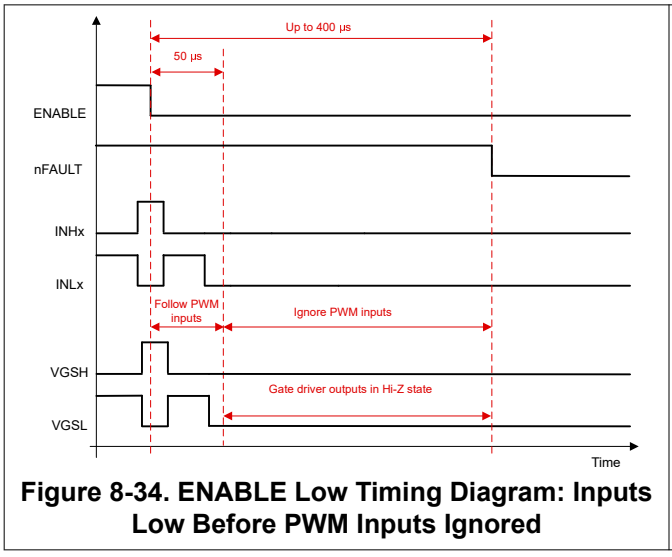


Figure 8-34. ENABLE Low Timing Diagram: Inputs Low Before PWM Inputs Ignored

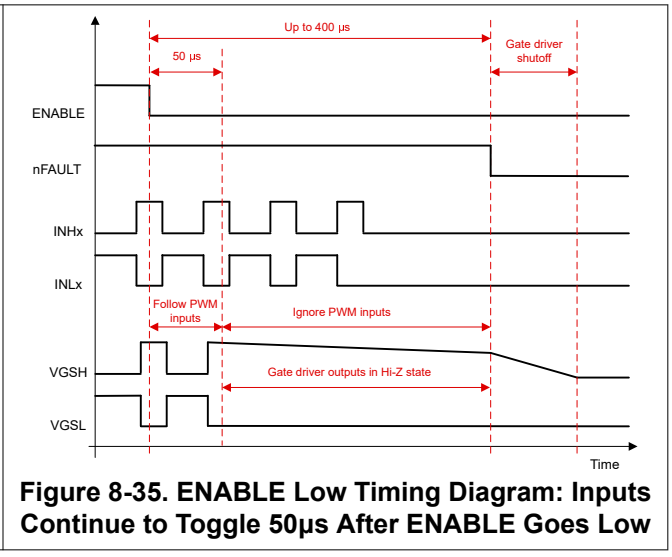


Figure 8-35. ENABLE Low Timing Diagram: Inputs Continue to Toggle 50µs After ENABLE Goes Low

The device comes out of sleep mode automatically if the ENABLE pin is pulled high. The t_{WAKE} time must elapse before the device is ready for inputs.

In sleep mode and when $V_{VM} < V_{UVLO}$, all external MOSFETs are disabled. The high-side gate pins, GHx, are pulled to the SHx pin by an internal pulldown resistor and the low-side gate pins, GLx, are pulled to the PGND pin by an internal pulldown resistor.

Note

During power up and power down of the device through the ENABLE pin, the nFAULT pin is held low as the internal regulators enable or disable. After the regulators have enabled or disabled, the nFAULT pin is automatically released. The duration that the nFAULT pin is low does not exceed the t_{SLEEP} or t_{WAKE} time.

8.4.1.2 Operating Mode

When the ENABLE pin is high and the V_{VM} voltage is greater than the V_{UVLO} voltage, the device goes to operating mode. The t_{WAKE} time must elapse before the device is ready for inputs. In this mode the charge pump, low-side gate regulator, DVDD regulator, and SPI bus are active.

8.4.1.3 Fault Reset (CLR_FLT or ENABLE Reset Pulse)

In the case of device latched faults, the DRV832x family of devices goes to a partial shutdown state to help protect the external power MOSFETs and system.

When the fault condition clears, the device can go to the operating state again by either setting the CLR_FLT SPI bit on SPI devices or issuing a reset pulse to the ENABLE pin on either interface variant. The ENABLE reset pulse (t_{RST}) consists of a high-to-low-to-high transition on the ENABLE pin. The low period of the sequence should fall with the t_{RST} time window or else the device will start the complete shutdown sequence. The reset pulse has no effect on any of the regulators, device settings, or other functional blocks.

8.4.2 Buck Regulator Functional Modes

8.4.2.1 Continuous Conduction Mode (CCM)

The LMR16006 integrated buck regulator steps the input voltage down to a lower output voltage. In continuous conduction mode (when the inductor current never reaches zero at CCM), the buck regulator operates in two cycles. The power switch is connected between the VIN and SW pins. During the first cycle of operation, the transistor is closed and the diode is reverse biased. Energy is collected in the inductor and the load current is supplied by the C_{OUT} capacitor and the rising current through the inductor. During the second cycle of operation, the transistor is open and the diode is forward biased because the inductor current cannot instantaneously change direction. The energy stored in the inductor is transferred to the load and output capacitor. The ratio of these two cycles determines the output voltage. Equation 7 and Equation 8 define the approximate output voltage.

$$D = \frac{V_O}{V_{VIN}} \tag{7}$$

where

- D is the duty cycle of the switch

$$D' = (1 - D) \tag{8}$$

The value of D and D' is required for design calculations.

8.4.2.2 Eco-mode™ Control Scheme

The LMR16006 device operates with the Eco-mode control scheme at light-load currents to improve efficiency by reducing switching and gate drive losses. The LMR16006 device is designed so that if the output voltage is within regulation and the peak switch current at the end of any switching cycle is less than the sleep-current threshold, $I_{INDUCTOR}$ ≤ 80mA, the device goes into Eco-mode. For Eco-mode operation, the LMR16006 device senses peak current, not average or load current, so the load current when the device goes into Eco-mode is dependent on the input voltage, the output voltage, and the value of the output inductor. When the load current is low and the output voltage is within regulation, the device goes into Eco-mode and draws only 28µA input quiescent current.

8.5 Programming

This section applies only to the DRV832x SPI devices.

8.5.1 SPI Communication

8.5.1.1 SPI

On DRV832x SPI devices, a SPI bus is used to set device configurations, operating parameters, and read out diagnostic information. The SPI operates in secondary mode and connects to a primary controller. The SPI input data (SDI) word consists of a 16bit word, with a 5bit command and 11bits of data. The SPI output data (SDO) word consists of 11bit register data. The first 5bits are don't care bits.

A valid frame must meet the following conditions:

- The SCLK pin should be low when the nSCS pin transitions from high to low and from low to high.
- The nSCS pin should be pulled high for at least 400ns between words.
- When the nSCS pin is pulled high, any signals at the SCLK and SDI pins are ignored and the SDO pin is placed in the Hi-Z state.
- Data is captured on the falling edge of the SCLK pin and data is propagated on the rising edge of the SCLK pin.
- The most significant bit (MSB) is shifted in and out first.
- A full 16 SCLK cycles must occur for transaction to be valid.
- If the data word sent to the SDI pin is less than or more than 16 bits, a frame error occurs and the data word is ignored.
- For a write command, the existing data in the register being written to is shifted out on the SDO pin following the 5-bit command data.

The SPI registers are reset to the default settings on power up, when the device enters sleep mode, and when a UVLO fault occurs.

8.5.1.1.1 SPI Format

The SDI input data word is 16 bits long and consists of the following format:

- 1 read or write bit, W (bit B15)
- 4 address bits, A (bits B14 through B11)
- 11 data bits, D (bits B10 through B0)

The SDO output data word is 16 bits long and the first 5 bits are don't care bits. The data word is the content of the register being accessed.

For a write command (W0 = 0), the response word on the SDO pin is the data currently in the register being written to.

For a read command (W0 = 1), the response word is the data currently in the register being read.

Table 8-8. SDI Input Data Word Format

R/W	ADDRESS				DATA										
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
W0	A3	A2	A1	A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 8-9. SDO Output Data Word Format

DON'T CARE BITS					DATA										
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
X	X	X	X	X	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

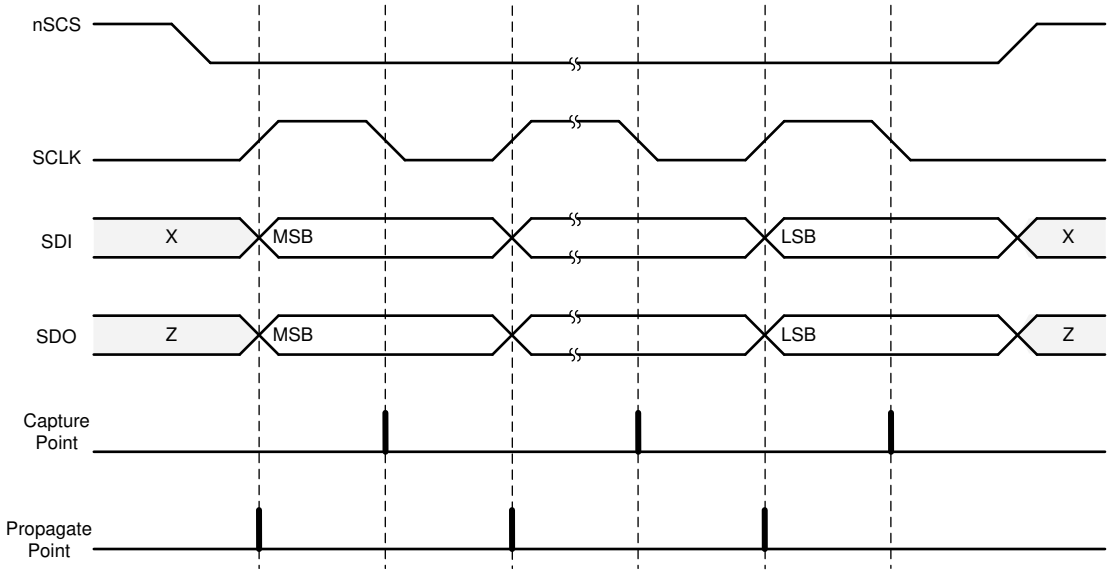


Figure 8-36. SPI Secondary Timing Diagram

8.6 Register Maps

This section applies only to the DRV832x SPI devices.

Note

Do not modify reserved registers or addresses not listed in the register map (Table 8-10). Writing to these registers may have unintended effects. For all reserved bits, the default value is 0. To help prevent erroneous SPI writes from the primary controller, set the LOCK bits to lock the SPI registers.

Table 8-10. DRV832xS and DRV832xRS Register Map

Name	10	9	8	7	6	5	4	3	2	1	0	Type	Address
DRV8320S and DRV8320RS													
Fault Status 1	FAULT	VDS_OCP	GDF	UVLO	OTSD	VDS_HA	VDS_LA	VDS_HB	VDS_LB	VDS_HC	VDS_LC	R	0h
VGS Status 2	SA_OC	SB_OC	SC_OC	OTW	CPUV	VGS_HA	VGS_LA	VGS_HB	VGS_LB	VGS_HC	VGS_LC	R	1h
Driver Control	Reserved	DIS_CPUV	DIS_GDF	OTW_REP	PWM_MODE		1PWM_COM	1PWM_DIR	COAST	BRAKE	CLR_FLT	RW	2h
Gate Drive HS	LOCK			IDRIVEP_HS				IDRIVEN_HS				RW	3h
Gate Drive LS	CBC	TDRIVE		IDRIVEP_LS				IDRIVEN_LS				RW	4h
OCP Control	TRETRY	DEAD_TIME		OCP_MODE		OCP_DEG		VDS_LVL				RW	5h
Reserved	Reserved											RW	6h
Reserved	Reserved											RW	7h
DRV8323S and DRV8323RS													
Fault Status 1	FAULT	VDS_OCP	GDF	UVLO	OTSD	VDS_HA	VDS_LA	VDS_HB	VDS_LB	VDS_HC	VDS_LC	R	0h
VGS Status 2	SA_OC	SB_OC	SC_OC	OTW	CPUV	VGS_HA	VGS_LA	VGS_HB	VGS_LB	VGS_HC	VGS_LC	R	1h
Driver Control	Reserved	DIS_CPUV	DIS_GDF	OTW_REP	PWM_MODE		1PWM_COM	1PWM_DIR	COAST	BRAKE	CLR_FLT	RW	2h
Gate Drive HS	LOCK			IDRIVEP_HS				IDRIVEN_HS				RW	3h
Gate Drive LS	CBC	TDRIVE		IDRIVEP_LS				IDRIVEN_LS				RW	4h
OCP Control	TRETRY	DEAD_TIME		OCP_MODE		OCP_DEG		VDS_LVL				RW	5h
CSA Control	CSA_FET	VREF_DIV	LS_REF	CSA_GAIN		DIS_SEN	CSA_CAL_A	CSA_CAL_B	CSA_CAL_C	SEN_LVL		RW	6h
Reserved	Reserved											RW	7h

8.6.1 Status Registers

The status registers are used for reporting warning and fault conditions. The status registers are read-only registers

Complex bit access types are encoded to fit into small table cells. Table 8-11 shows the codes that are used for access types in this section.

Table 8-11. Status Registers Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

8.6.1.1 Fault Status Register 1 (address = 0x00)

The fault status register 1 is shown in Figure 8-37 and described in Table 8-12.

Register access type: Read only

Figure 8-37. Fault Status Register 1

10	9	8	7	6	5	4	3	2	1	0
FAULT	VDS_OCP	GDF	UVLO	OTSD	VDS_HA	VDS_LA	VDS_HB	VDS_LB	VDS_HC	VDS_LC
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 8-12. Fault Status Register 1 Field Descriptions

Bit	Field	Type	Default	Description
10	FAULT	R	0b	Logic OR of FAULT status registers. Mirrors nFAULT pin.
9	VDS_OCP	R	0b	Indicates VDS monitor overcurrent fault condition
8	GDF	R	0b	Indicates gate drive fault condition
7	UVLO	R	0b	Indicates undervoltage lockout fault condition
6	OTSD	R	0b	Indicates overtemperature shutdown
5	VDS_HA	R	0b	Indicates VDS overcurrent fault on the A high-side MOSFET
4	VDS_LA	R	0b	Indicates VDS overcurrent fault on the A low-side MOSFET
3	VDS_HB	R	0b	Indicates VDS overcurrent fault on the B high-side MOSFET
2	VDS_LB	R	0b	Indicates VDS overcurrent fault on the B low-side MOSFET
1	VDS_HC	R	0b	Indicates VDS overcurrent fault on the C high-side MOSFET
0	VDS_LC	R	0b	Indicates VDS overcurrent fault on the C low-side MOSFET

8.6.1.2 Fault Status Register 2 (address = 0x01)

The fault status register 2 is shown in Figure 8-38 and described in Table 8-13.

Register access type: Read only

Figure 8-38. Fault Status Register 2

10	9	8	7	6	5	4	3	2	1	0
SA_OC	SB_OC	SC_OC	OTW	CPUV	VGS_HA	VGS_LA	VGS_HB	VGS_LB	VGS_HC	VGS_LC
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 8-13. Fault Status Register 2 Field Descriptions

Bit	Field	Type	Default	Description
10	SA_OC	R	0b	Indicates overcurrent on phase A sense amplifier (DRV8323xS)
9	SB_OC	R	0b	Indicates overcurrent on phase B sense amplifier (DRV8323xS)
8	SC_OC	R	0b	Indicates overcurrent on phase C sense amplifier (DRV8323xS)
7	OTW	R	0b	Indicates overtemperature warning
6	CPUV	R	0b	Indicates charge pump undervoltage fault condition
5	VGS_HA	R	0b	Indicates gate drive fault on the A high-side MOSFET
4	VGS_LA	R	0b	Indicates gate drive fault on the A low-side MOSFET
3	VGS_HB	R	0b	Indicates gate drive fault on the B high-side MOSFET
2	VGS_LB	R	0b	Indicates gate drive fault on the B low-side MOSFET
1	VGS_HC	R	0b	Indicates gate drive fault on the C high-side MOSFET
0	VGS_LC	R	0b	Indicates gate drive fault on the C low-side MOSFET

8.6.2 Control Registers

The control registers are used to configure the device. The control registers are read and write capable.

Complex bit access types are encoded to fit into small table cells. Table 8-14 shows the codes that are used for access types in this section.

Table 8-14. Control Registers Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.2.1 Driver Control Register (address = 0x02)

The driver control register is shown in Figure 8-39 and described in Table 8-15.

Register access type: Read/Write

Figure 8-39. Driver Control Register

10	9	8	7	6	5	4	3	2	1	0
Reserved	DIS _CPUV	DIS _GDF	OTW _REP	PWM_MODE		1PWM _COM	1PWM _DIR	COAST	BRAKE	CLR _FLT
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-00b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-15. Driver Control Field Descriptions

Bit	Field	Type	Default	Description
10	Reserved	R/W	0b	Reserved
9	DIS_CPUV	R/W	0b	**0b = Charge pump UVLO fault is enabled** 1b = Charge pump UVLO fault is disabled
8	DIS_GDF	R/W	0b	**0b = Gate drive fault is enabled** 1b = Gate drive fault is disabled
7	OTW_REP	R/W	0b	**0b = OTW is not reported on nFAULT or the FAULT bit** 1b = OTW is reported on nFAULT and the FAULT bit
6-5	PWM_MODE	R/W	00b	**00b = 6x PWM Mode** 01b = 3x PWM mode 10b = 1x PWM mode 11b = Independent PWM mode
4	1PWM_COM	R/W	0b	**0b = 1x PWM mode uses synchronous rectification** 1b = 1x PWM mode uses asynchronous rectification (diode freewheeling)
3	1PWM_DIR	R/W	0b	In 1x PWM mode this bit is ORed with the INHC (DIR) input
2	COAST	R/W	0b	Write a 1 to this bit to put all MOSFETs in the Hi-Z state
1	BRAKE	R/W	0b	Write a 1 to this bit to turn on all three low-side MOSFETs in 1x PWM mode. This bit is ORed with the INLC (BRAKE) input.
0	CLR_FLT	R/W	0b	Write a 1 to this bit to clear latched fault bits. This bit automatically resets after being written.

8.6.2.2 Gate Drive HS Register (address = 0x03)

The gate drive HS register is shown in Figure 8-40 and described in Table 8-16.

Register access type: Read/Write

Figure 8-40. Gate Drive HS Register

10	9	8	7	6	5	4	3	2	1	0
LOCK			IDRIVEP_HS				IDRIVEN_HS			
R/W-011b			R/W-1111b				R/W-1111b			

Table 8-16. Gate Drive HS Field Descriptions

Bit	Field	Type	Default	Description
10-8	LOCK	R/W	011b	Write 110b to lock the settings by ignoring further register writes except to these bits and address 0x02 bits 0-2. Writing any sequence other than 110b has no effect when unlocked. Write 011b to this register to unlock all registers. Writing any sequence other than 011b has no effect when locked.
7-4	IDRIVEP_HS	R/W	1111b	0000b = 10mA 0001b = 30mA 0010b = 60mA 0011b = 80mA 0100b = 120mA 0101b = 140mA 0110b = 170mA 0111b = 190mA 1000b = 260mA 1001b = 330mA 1010b = 370mA 1011b = 440mA 1100b = 570mA 1101b = 680mA 1110b = 820mA **1111b = 1000mA**
3-0	IDRIVEN_HS	R/W	1111b	0000b = 20mA 0001b = 60mA 0010b = 120mA 0011b = 160mA 0100b = 240mA 0101b = 280mA 0110b = 340mA 0111b = 380mA 1000b = 520mA 1001b = 660mA 1010b = 740mA 1011b = 880mA 1100b = 1140mA 1101b = 1360mA 1110b = 1640mA **1111b = 2000mA**

8.6.2.3 Gate Drive LS Register (address = 0x04)

The gate drive LS register is shown in Figure 8-41 and described in Table 8-17.

Register access type: Read/Write

Figure 8-41. Gate Drive LS Register

10	9	8	7	6	5	4	3	2	1	0
CBC	TDRIVE		IDRIVEP_LS				IDRIVEN_LS			
R/W-1b	R/W-11b		R/W-1111b				R/W-1111b			

Table 8-17. Gate Drive LS Register Field Descriptions

Bit	Field	Type	Default	Description
10	CBC	R/W	1b	Cycle-by-cycle operation. In retry OCP_MODE, for both VDS_OCP and SEN_OCP, the fault is automatically cleared when a PWM input is given
9-8	TDRIVE	R/W	11b	00b = 500ns peak gate-current drive time 01b = 1000ns peak gate-current drive time 10b = 2000ns peak gate-current drive time **11b = 4000ns peak gate-current drive time**
7-4	IDRIVEP_LS	R/W	1111b	0000b = 10mA 0001b = 30mA 0010b = 60mA 0011b = 80mA 0100b = 120mA 0101b = 140mA 0110b = 170mA 0111b = 190mA 1000b = 260mA 1001b = 330mA 1010b = 370mA 1011b = 440mA 1100b = 570mA 1101b = 680mA 1110b = 820mA **1111b = 1000mA**
3-0	IDRIVEN_LS	R/W	1111b	0000b = 20mA 0001b = 60mA 0010b = 120mA 0011b = 160mA 0100b = 240mA 0101b = 280mA 0110b = 340mA 0111b = 380mA 1000b = 520mA 1001b = 660mA 1010b = 740mA 1011b = 880mA 1100b = 1140mA 1101b = 1360mA 1110b = 1640mA **1111b = 2000mA**

8.6.2.4 OCP Control Register (address = 0x05)

The OCP control register is shown in Figure 8-42 and described in Table 8-18.

Register access type: Read/Write

Figure 8-42. OCP Control Register

10	9	8	7	6	5	4	3	2	1	0
TRETRY	DEAD_TIME		OCP_MODE		OCP_DEG		VDS_LVL			
R/W-0b	R/W-01b		R/W-01b		R/W-01b		R/W-1001b			

Table 8-18. OCP Control Field Descriptions

Bit	Field	Type	Default	Description
10	TRETRY	R/W	0b	**0b = VDS_OCP and SEN_OCP retry time is 4ms** 1b = VDS_OCP and SEN_OCP retry time is 50µs
9-8	DEAD_TIME	R/W	01b	00b = 50ns dead time **01b = 100ns dead time** 10b = 200ns dead time 11b = 400ns dead time
7-6	OCP_MODE	R/W	01b	00b = Overcurrent causes a latched fault **01b = Overcurrent causes an automatic retrying fault** 10b = Overcurrent is report only but no action is taken 11b = Overcurrent is not reported and no action is taken
5-4	OCP_DEG	R/W	01b	00b = Overcurrent deglitch time of 2µs **01b = Overcurrent deglitch time of 4µs** 10b = Overcurrent deglitch time of 6µs 11b = Overcurrent deglitch time of 8µs
3-0	VDS_LVL	R/W	1001b	0000b = 0.06V 0001b = 0.13V 0010b = 0.2V 0011b = 0.26V 0100b = 0.31V 0101b = 0.45V 0110b = 0.53V 0111b = 0.6V 1000b = 0.68V **1001b = 0.75V** 1010b = 0.94V 1011b = 1.13V 1100b = 1.3V 1101b = 1.5V 1110b = 1.7V 1111b = 1.88V

8.6.2.5 CSA Control Register (DRV8323x Only) (address = 0x06)

The CSA control register is shown in Figure 8-43 and described in Table 8-19.

Register access type: Read/Write
This register is only available with the DRV8323x family of devices.

Figure 8-43. CSA Control Register

10	9	8	7	6	5	4	3	2	1	0
CSA_FET	VREF_DIV	LS_REF	CSA_GAIN		DIS_SEN	CSA_CAL_A	CSA_CAL_B	CSA_CAL_C	SEN_LVL	
R/W-0b	R/W-1b	R/W-0b	R/W-10b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-11b	

Table 8-19. CSA Control Field Descriptions

Bit	Field	Type	Default	Description
10	CSA_FET	R/W	0b	**0b = Current sense amplifier positive input is SPx** 1b = Current sense amplifier positive input is SHx (also automatically sets the LS_REF bit to 1)
9	VREF_DIV	R/W	1b	0b = Current sense amplifier reference voltage is VREF (unidirectional mode) **1b = Current sense amplifier reference voltage is VREF divided by 2**
8	LS_REF	R/W	0b	**0b = VDS_OCP for the low-side MOSFET is measured across SHx to SPx** 1b = VDS_OCP for the low-side MOSFET is measured across SHx to SNx
7-6	CSA_GAIN	R/W	10b	00b = 5V/V current sense amplifier gain 01b = 10V/V current sense amplifier gain **10b = 20V/V current sense amplifier gain** 11b = 40V/V current sense amplifier gain
5	DIS_SEN	R/W	0b	**0b = Sense overcurrent fault is enabled** 1b = Sense overcurrent fault is disabled
4	CSA_CAL_A	R/W	0b	**0b = Normal current sense amplifier A operation** 1b = Short inputs to current sense amplifier A for offset calibration
3	CSA_CAL_B	R/W	0b	**0b = Normal current sense amplifier B operation** 1b = Short inputs to current sense amplifier B for offset calibration
2	CSA_CAL_C	R/W	0b	**0b = Normal current sense amplifier C operation** 1b = Short inputs to current sense amplifier C for offset calibration
1-0	SEN_LVL	R/W	11b	00b = Sense OCP 0.25V 01b = Sense OCP 0.5V 10b = Sense OCP 0.75V **11b = Sense OCP 1V**

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The DRV832x family of devices is primarily used in applications for three-phase brushless DC motor control. The design procedures in *Section 9.2* highlight how to use and configure the DRV832x family of devices.

9.2 Typical Application

9.2.1 Primary Application

The DRV8323R SPI device is used in this application example.

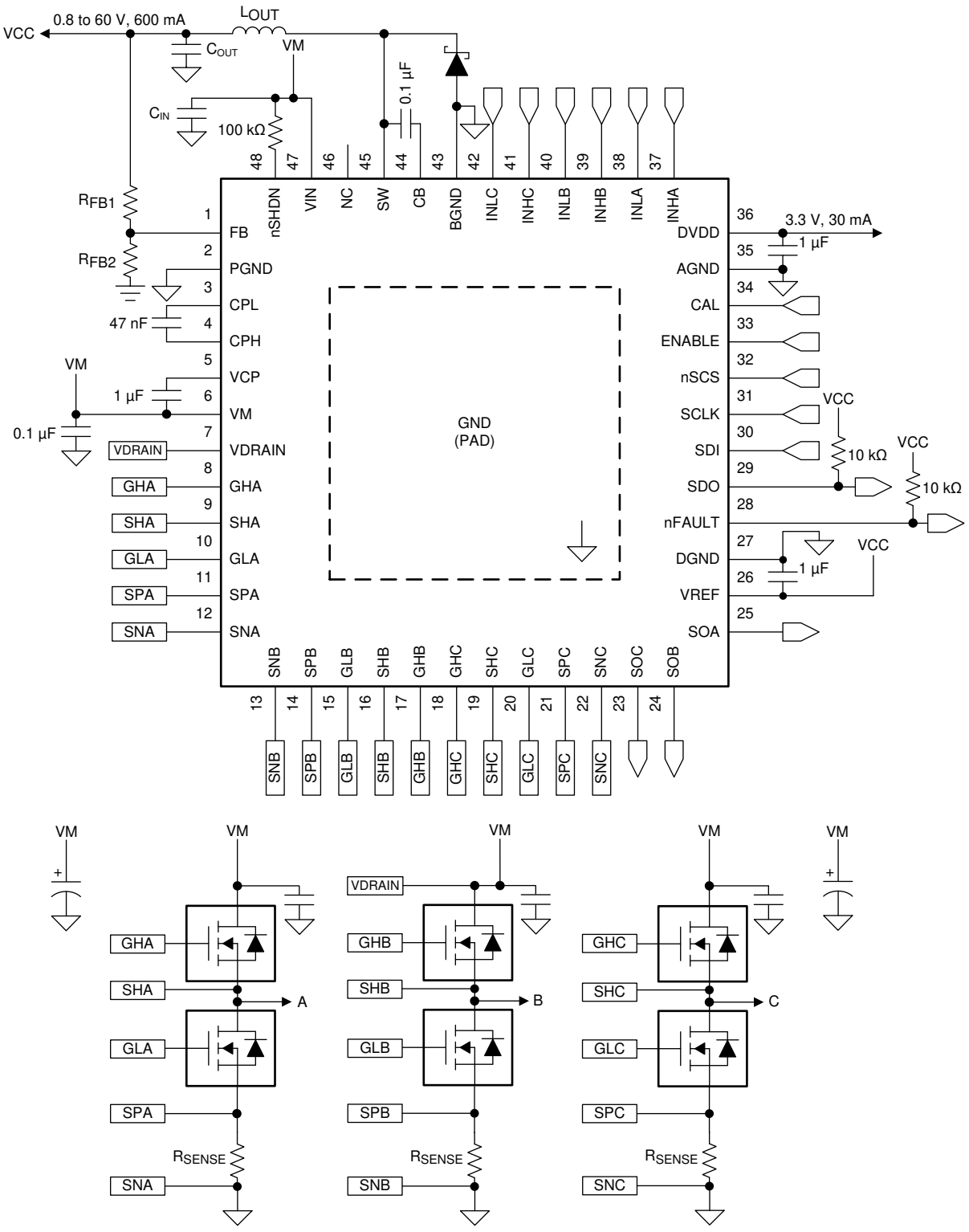


Figure 9-1. Primary Application Schematic

9.2.1.1 Design Requirements

Table 9-1 lists the example input parameters for the system design.

Table 9-1. Design Parameters

EXAMPLE DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Nominal supply voltage	V_{VM}	24V
Supply voltage range		8V to 45V
MOSFET part number		CSD18536KCS
MOSFET total gate charge	Q_g	83nC (typical) at V_{VGS} = 10V
MOSFET gate to drain charge	Q_{gd}	14nC (typical)
Target output rise time	t_r	100 to 300ns
Target output fall time	t_f	50 to 150ns
PWM Frequency	f_{PWM}	45kHz
Buck regulator output voltage	V_{VCC}	3.3V
Maximum motor current	I_{max}	100A
ADC reference voltage	V_{VREF}	3.3V
Winding sense current range	I_{SENSE}	–40A to +40A
Motor RMS current	I_{RMS}	28.3A
Sense resistor power rating	P_{SENSE}	2W
System ambient temperature	T_A	–20°C to +105°C

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 External MOSFET Support

The DRV832x MOSFET support is based on the capacity of the charge pump and PWM switching frequency of the output. For a quick calculation of MOSFET driving capacity, use Equation 9 and Equation 10 for three phase BLDC motor applications.

Trapezoidal 120° Commutation: $$I_{VCP} > Q_g \times f_{PWM} \quad (9)$$

where

- f_{PWM} is the maximum desired PWM switching frequency.
- I_{VCP} is the charge pump capacity, which depends on the VM pin voltage.
- The multiplier based on the commutation control method, may vary based on implementation.

Sinusoidal 180° Commutation: $$I_{VCP} > 3 \times Q_g \times f_{PWM} \quad (10)$$

9.2.1.2.1.1 Example

If a system with a V_{VM} voltage of 8V (I_{VCP} = 15mA) uses a maximum PWM switching frequency of 45kHz, then the charge pump can support MOSFETs using trapezoidal commutation with a Q_g less than 333nC, and MOSFETs using sinusoidal commutation with a Q_g less than 111nC.

9.2.1.2.2 IDRIVE Configuration

The strength of the gate drive current, I_{DRIVE}, is selected based on the gate-to-drain charge of the external MOSFETs and the target rise and fall times at the outputs. If the I_{DRIVE} selected is too low for a given MOSFET, then the MOSFET may not turn on completely within the t_{DRIVE} time and a gate drive fault may be asserted. Additionally, slow rise and fall times result in higher switching power losses. If the I_{DRIVE} selected is too high for a given MOSFET/layout, the gate-to-source voltage may overshoot, undershoot, or ring excessively which could violate the ABS MAX of the device and damage the driver or FET. TI recommends adjusting these values in the system with the required external MOSFETs and motor to determine the best possible setting for any application.

The I_{DRIVEP} and I_{DRIVEN} current for both the low-side and high-side MOSFETs are independently adjustable on SPI devices through the SPI registers. On hardware interface devices, both source and sink settings are selected at the same time on the IDRIVE pin.

For MOSFETs with a known gate-to-drain charge Q_{gd}, desired rise time (t_r), and a desired fall time (t_f), use Equation 11 and Equation 12 to calculate the value of I_{DRIVEP} and I_{DRIVEN} (respectively).

$$I_{DRIVEP} > \frac{Q_{gd}}{t_r} \tag{11}$$

$$I_{DRIVEN} > \frac{Q_{gd}}{t_f} \tag{12}$$

9.2.1.2.2.1 Example

Use Equation 13 and Equation 14 to calculate the value of $I_{DRIVEP1}$ and $I_{DRIVEP2}$ (respectively) for a gate-to-drain charge of 14 nC and a rise time from 100 to 300ns.

$$I_{DRIVEP1} = \frac{14\ nC}{100\ ns} = 140\ mA \tag{13}$$

$$I_{DRIVEP2} = \frac{14\ nC}{300\ ns} = 47\ mA \tag{14}$$

Select a value for I_{DRIVEP} that is between 47mA and 140mA. For this example, the value of I_{DRIVEP} was selected as 120mA source.

Use Equation 15 and Equation 16 to calculate the value of $I_{DRIVEN1}$ and $I_{DRIVEN2}$ (respectively) for a gate-to-drain charge of 14nC and a fall time from 50 to 150ns.

$$I_{DRIVEN1} = \frac{14\ nC}{50\ ns} = 280\ mA \tag{15}$$

$$I_{DRIVEN2} = \frac{14\ nC}{150\ ns} = 93\ mA \tag{16}$$

Select a value for I_{DRIVEN} that is between 93mA and 280mA. For this example, the value of I_{DRIVEN} was selected as 240mA sink.

9.2.1.2.3 V_{DS} Overcurrent Monitor Configuration

The V_{DS} monitors are configured based on the worst-case motor current and the $R_{DS(on)}$ of the external MOSFETs as shown in Equation 17.

$$V_{DS\_OCP} > I_{max} \times R_{DS(on)max} \tag{17}$$

9.2.1.2.3.1 Example

The goal of this example is to set the V_{DS} monitor to trip at a current greater than 100A. According to the *CSD18536KCS 60 V N-Channel NexFET™ Power MOSFET* data sheet, the $R_{DS(on)}$ value is 1.8 times higher at 175°C, and the maximum $R_{DS(on)}$ value at a V_{GS} of 10V is 1.6mΩ. From these values, the approximate worst-case value of $R_{DS(on)}$ is 1.8 × 1.6mΩ = 2.88mΩ.

Using Equation 17 with a value of 2.88mΩ for $R_{DS(on)}$ and a worst-case motor current of 100A, Equation 18 shows the calculated value of the V_{DS} monitors.

$$V_{DS\_OCP} > 100\ A \times 2.88\ m\Omega \rightarrow V_{DS\_OCP} > 0.288\ V \tag{18}$$

For this example, the value of V_{DS_OCP} was selected as 0.31V.

The SPI devices allow for adjustment of the deglitch time for the V_{DS} overcurrent monitor. The deglitch time can be set to 2µs, 4µs, 6µs, or 8µs.

9.2.1.2.4 Sense Amplifier Bidirectional Configuration (DRV8323 and DRV8323R)

The sense amplifier gain on the DRV8323, DRV8323R devices and sense resistor value are selected based on the target current range, VREF voltage supply, power rating of the sense resistor, and operating temperature range. For bidirectional operation of the sense amplifier, the dynamic range at the output is approximately calculated as shown in Equation 19.

$$V_O = (V_{VREF} - 0.25\,V) - \frac{V_{VREF}}{2} \tag{19}$$

Use Equation 20 to calculate the approximate value of the selected sense resistor with V_O calculated using Equation 19.

$$R = \frac{V_O}{A_V \times I} \quad P_{SENSE} > {I_{RMS}}^2 \times R \tag{20}$$

From Equation 19 and Equation 20, select a target gain setting based on the power rating of the target sense resistor.

9.2.1.2.4.1 Example

In this system example, the value of the VREF voltage is 3.3V with a sense current from –40 to +40A. The linear range of the SOx output is 0.25V to V_{VREF} – 0.25V (from the V_{LINEAR} specification). The differential range of the sense amplifier input is –0.3 to +0.3V (V_{DIFF}).

$$V_O = (3.3\,V - 0.25\,V) - \frac{3.3\,V}{2} = 1.4\,V \tag{21}$$

$$\mathrm{R} = \frac{1.4\ \mathrm{V}}{\mathrm{A_V} \times 40\ \mathrm{A}} \quad 2\ \mathrm{W} > {28.3}^2 \times \mathrm{R} \rightarrow \mathrm{R} < 2.5\ \mathrm{m\Omega} \tag{22}$$

$$2.5\ \mathrm{m\Omega} > \frac{1.4\ \mathrm{V}}{\mathrm{A_V} \times 40\ \mathrm{A}} \rightarrow \mathrm{A}_V > 14 \tag{23}$$

Therefore, the gain setting must be selected as 20V/V or 40V/V and the value of the sense resistor must be less than 2.5mΩ to meet the power rating for the sense resistor. For this example, the gain setting was selected as 20V/V. The value of the resistor and worst case current can be verified that R < 2.5mΩ and I_{max} = 40A does not violate the differential range specification of the current sense amplifier input (V_{SPxD}).

9.2.1.2.5 Buck Regulator Configuration (DRV8320R and DRV8323R)

For a detailed design procedure and information on selecting the correct buck regulator external components, refer to the *LMR16006 SIMPLE SWITCHER® 60 V 0.6 A Buck Regulators With High Efficiency Eco-mode* data sheet.

9.2.1.3 Application Curves

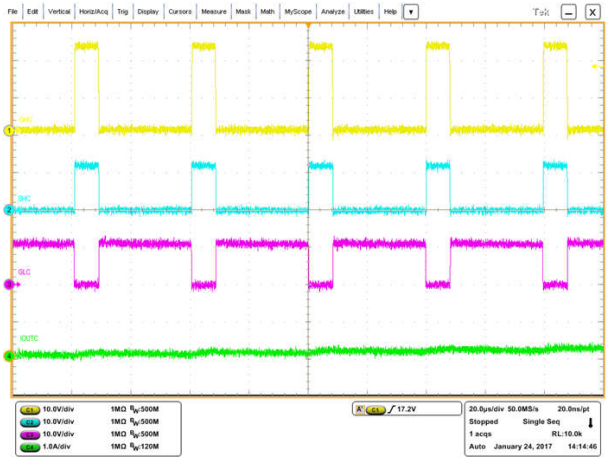


Figure 9-2. Gate Drive at 20% Duty Cycle

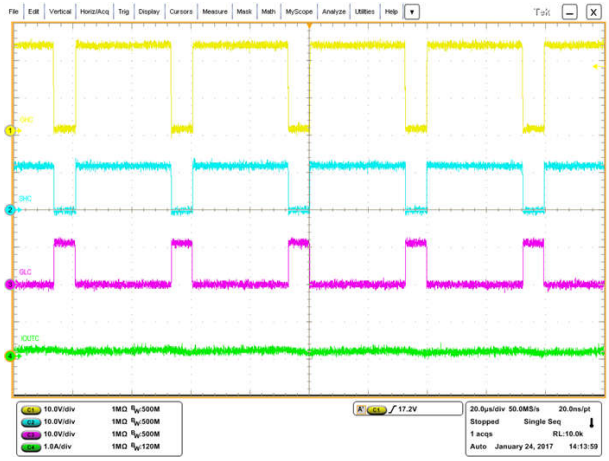


Figure 9-3. Gate Drive at 80% Duty Cycle

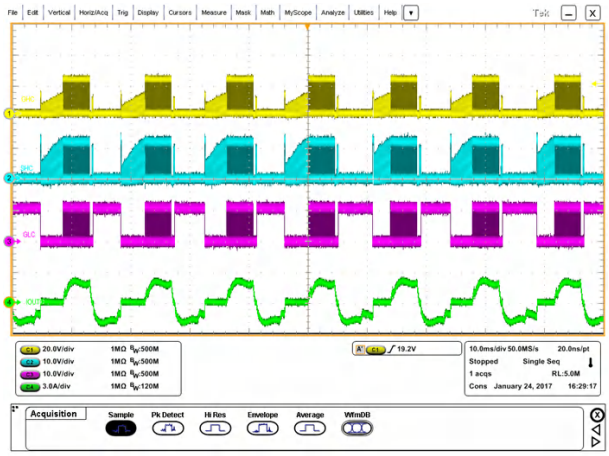


Figure 9-4. BLDC Motor Commutation 1000 RPM

Figure 9-5. BLDC Motor Commutation 2000 RPM

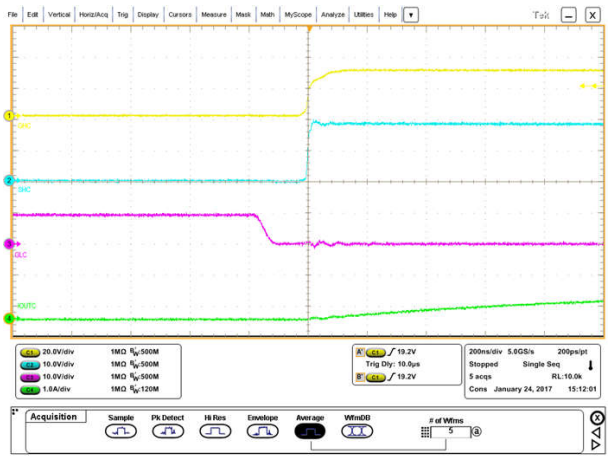


Figure 9-6. IDRIVE Maximum Setting Positive Current

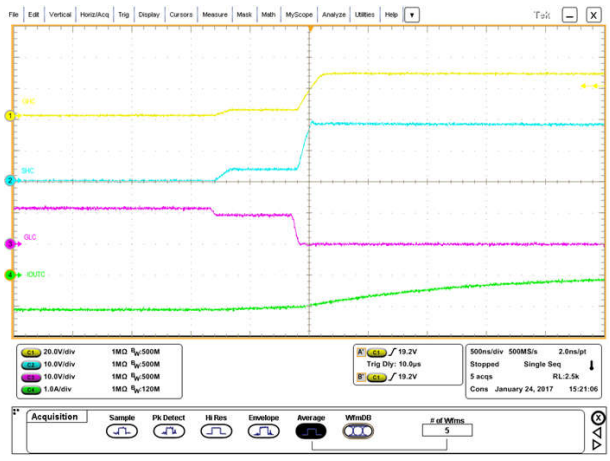


Figure 9-7. IDRIVE Maximum Setting Negative Current

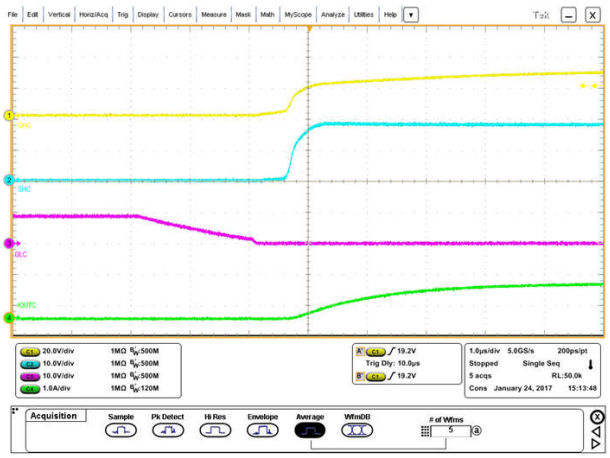


Figure 9-8. IDRIVE Minimum Setting Positive Current

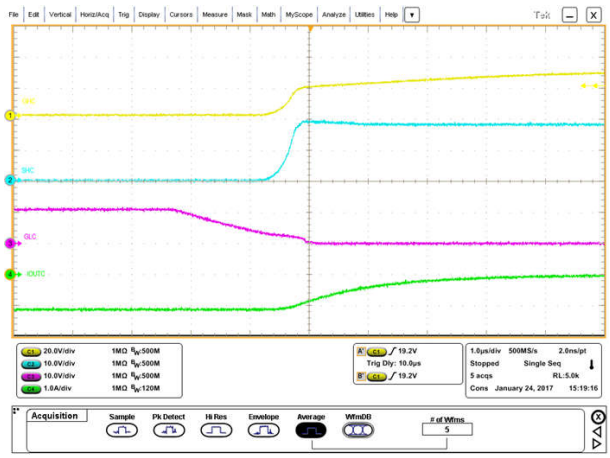


Figure 9-9. IDRIVE Minimum Setting Negative Current

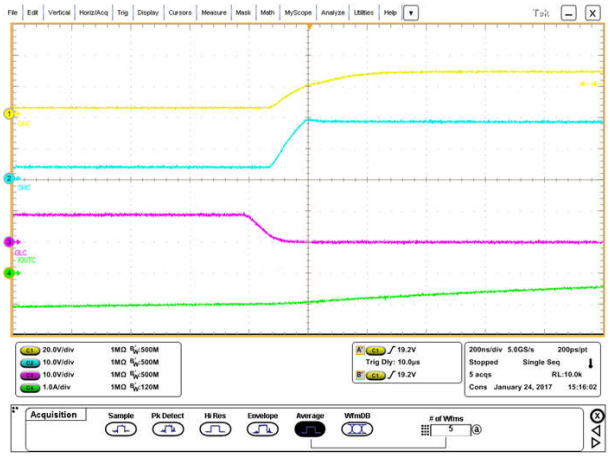


Figure 9-10. Current going out of SHx, IDRIVE_P = 260mA and IDRIVE_N =520-mA

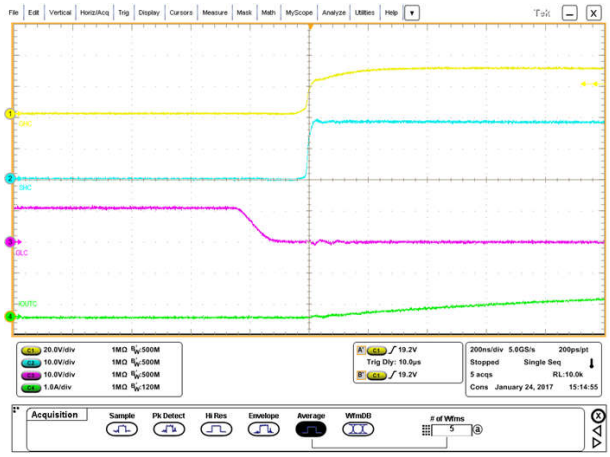


Figure 9-11. Current going into of SHx, IDRIVE_P = 260mA and IDRIVE_N =520-mA

9.2.2 Alternative Application

In this application, one sense amplifier is used in unidirectional mode for a summing current sense scheme often used in trapezoidal or hall-based BLDC commutation control.

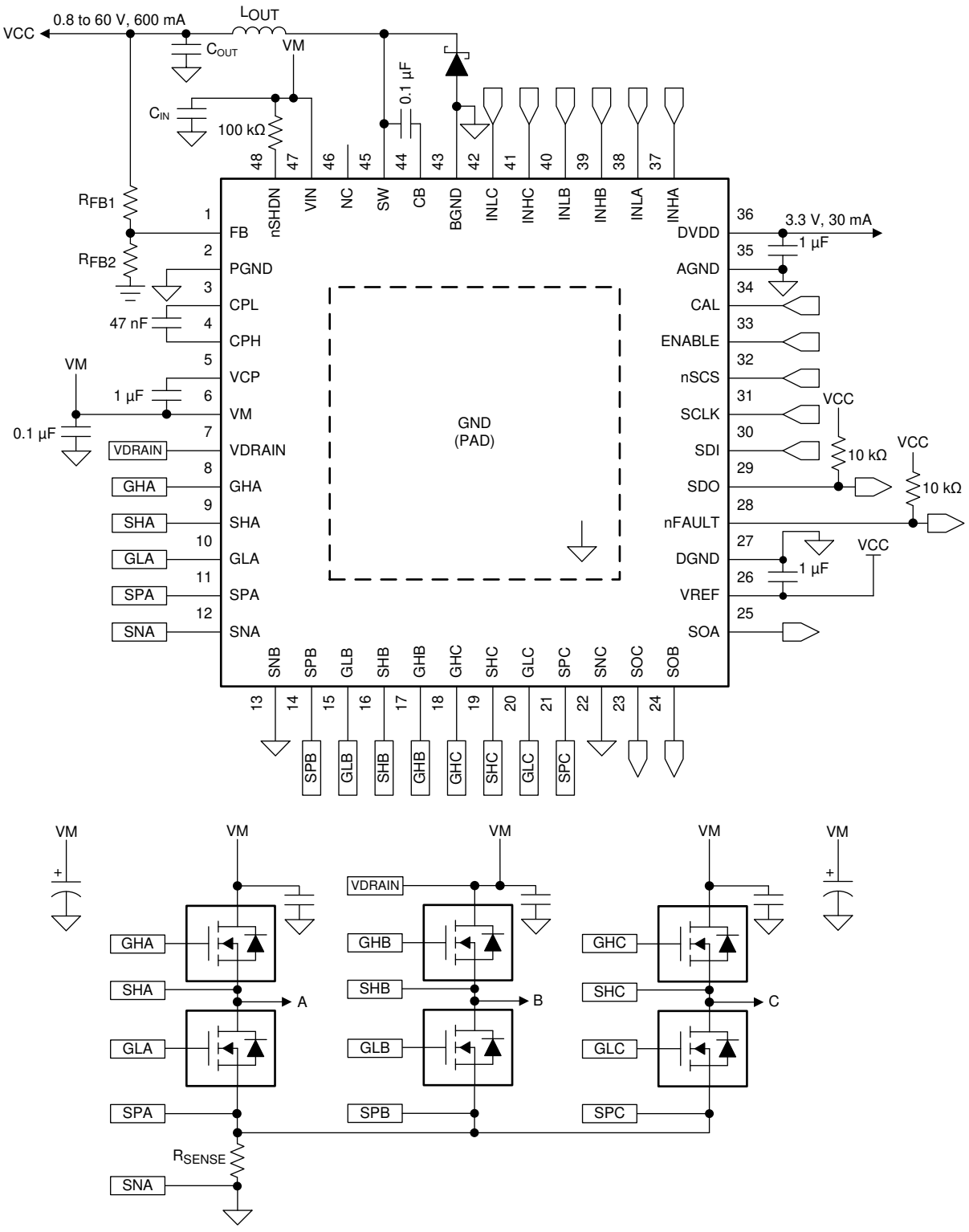


Figure 9-12. Alternative Application Schematic

9.2.2.1 Design Requirements

Table 9-2 lists the example design input parameters for system design.

Table 9-2. Design Parameters

EXAMPLE DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
ADC reference voltage	V_{VREF}	3.3V
Sensed current	I_{SENSE}	0 to 40A
Motor RMS current	I_{RMS}	28.3A
Sense-resistor power rating	P_{SENSE}	3W
System ambient temperature	T_A	–20°C to +105°C

9.2.2.2 Detailed Design Procedure

9.2.2.2.1 Sense Amplifier Unidirectional Configuration

The sense amplifiers are configured to be unidirectional through the registers on SPI devices by writing a 0 to the VREF_DIV bit.

The sense amplifier gain and sense resistor values are selected based on the target current range, VREF, power rating of the sense resistor, and operating temperature range. In unidirectional operation of the sense amplifier, use Equation 24 to calculate the approximate value of the dynamic range at the output.

$$V_O = (V_{VREF} - 0.25\,V) - 0.25\,V = V_{VREF} - 0.5\,V \tag{24}$$

Use Equation 25 to calculate the approximate value of the selected sense resistor.

$$R = \frac{V_O}{A_V \times I} \quad P_{SENSE} > {I_{RMS}}^2 \times R \tag{25}$$

where

- $V_O = V_{VREF} - 0.5\,V$

From Equation 24 and Equation 25, select a target gain setting based on the power rating of a target sense resistor.

9.2.2.2.1.1 Example

In this system example, the value of the VREF voltage is 3.3 V with a sense current from 0 to 40 A. The linear range of the SOx output for the DRV8323x device is 0.25 V to V_{VREF} – 0.25 V (from the V_{LINEAR} specification). The differential range of the sense-amplifier input is –0.3 to +0.3 V (V_{DIFF}).

$$V_O = 3.3\,V - 0.5\,V = 2.8\,V \tag{26}$$

$$R = \frac{2.8\,V}{A_V \times 40\,A} \quad 3\,W > {28.3}^2 \times R \rightarrow R < 3.75\,m\Omega \tag{27}$$

$$3.75\ \text{m}\Omega > \frac{2.8\ \text{V}}{\text{A}_\text{V} \times 40\ \text{A}} \rightarrow \text{A}_V > 18.7 \tag{28}$$

Therefore, the gain setting must be selected as 20 V/V or 40 V/V and the value of the sense resistor must be less than 3.75 mΩ to meet the power rating for the sense resistor. For this example, the gain setting was selected as 20 V/V. The value of the resistor and worst-case current can be verified that R < 3.75 mΩ and I_{max} = 40 A does not violate the differential range specification of the sense amplifier input (V_{SPxD}).

9.2.3 Unused Pins and Features

This section details the appropriate handling of unused pins and blocks of the device. If a feature such as the CSA or Buck will not be used, check this section for guidance.

Table 9-3. Unused Pins and Features

Unused Feature	Associated Pin(s)	Recommendation
Unused Half-Bridge	GHx and GLx	Float
	PWM Inputs	Tie to GND or float
	SHx	Float
Unused HS or LS (Individually)	SHx/INHx/INLx/GHx/GLx	See *Independent PWM Mode*
Unused CSA	SPx and SNx	Tie to GND
	SOx	Float
	VREF	Tie to DVDD
Unused Buck	All Pins	Tie to GND, remove all external components
Unused SPI	SDI/SDO/nSCS/SCLK	Float

10 Power Supply Recommendations

The DRV832x family of devices is designed to operate from an input voltage supply (VM) range from 6V to 60V. A 0.1µF ceramic capacitor rated for VM must be placed as close to the device as possible. In addition, a bulk capacitor must be included on the VM pin but can be shared with the bulk bypass capacitance for the external power MOSFETs. Additional bulk capacitance is required to bypass the external half-bridge MOSFETs and should be sized according to the application requirements.

10.1 Power Supply Consideration in Generator Mode

When the motor shaft of BLDC or PMSM motor is turned by an external force, the motor windings will generate a voltage on the motor inputs. This condition is known as generator mode or motor back-drive. In the generator mode, a positive voltage can be observed on SHx pins of the device. If there is a switch between VDRAIN and VM (SW_{VDRAIN} in Figure 10-1) and the following conditions exist in the system, the absolute max voltage of VCP with respect to VM needs to be reviewed;

- Generator mode
- SW_{VDRAIN} is off
- VM and VCP are low voltage (e.g. VM = 0V)

If SHx voltage (V_{SHx}) exceeds VCP voltage, the VCP voltage starts following V_{SHx} because of the device internal diodes D1 and D2 (or D3). If VCP - VM voltage exceeds the absolute max voltage of DRV832x, the ESD diode D4 starts conducting and results in a big current from SHx to VM through the diodes D2, D1 and D4. To avoid this condition, it is recommended to add an external diode D_{VDRAIN_VM} between VDRAIN and VM.

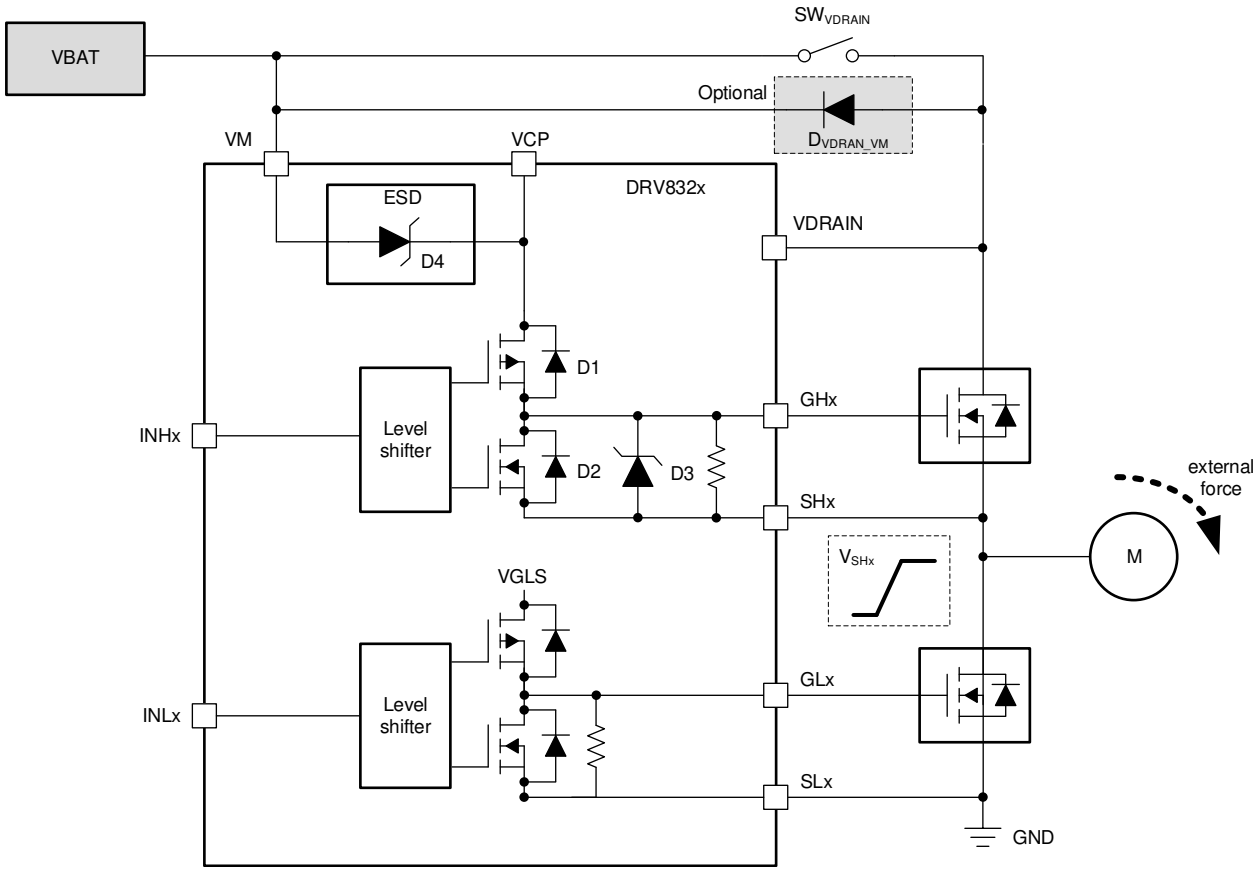


Figure 10-1. Power Supply Consideration in Generator mode

10.2 Bulk Capacitance Sizing

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size. The amount of local capacitance depends on a variety of factors including:

- The highest current required by the motor system
- The power supply's type, capacitance, and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable supply voltage ripple
- Type of motor (brushed DC, brushless DC, stepper)
- The motor startup and braking methods

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet provides a recommended minimum value, but system level testing is required to determine the appropriate sized bulk capacitor.

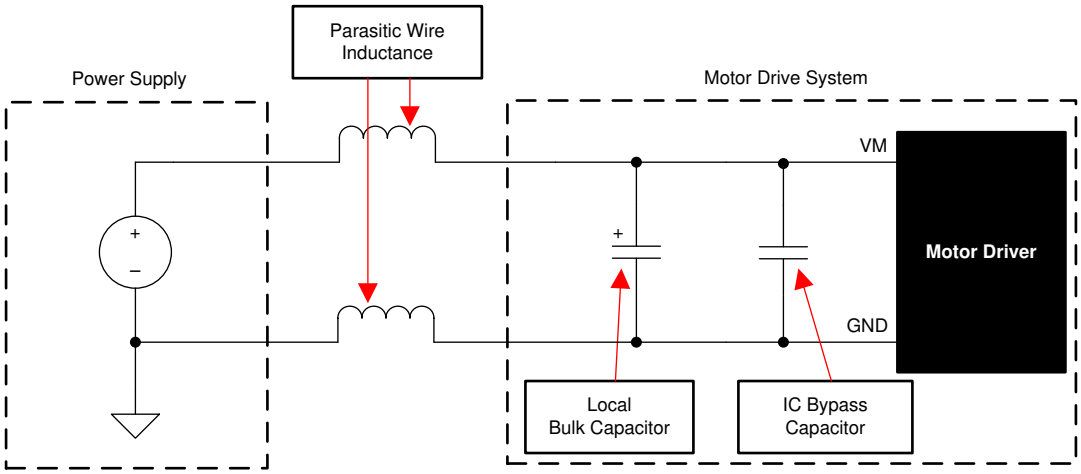


Figure 10-2. Motor Drive Supply Parasitics Example

11 Layout

11.1 Layout Guidelines

Bypass the VM pin to the PGND pin using a low-ESR ceramic bypass capacitor with a recommended value of 0.1µF. Place this capacitor as close to the VM pin as possible with a thick trace or ground plane connected to the PGND pin. Additionally, bypass the VM pin using a bulk capacitor rated for VM. This component can be electrolytic. This capacitance must be at least 10µF.

Additional bulk capacitance is required to bypass the high current path on the external MOSFETs. This bulk capacitance should be placed such that it minimizes the length of any high current paths through the external MOSFETs. The connecting metal traces should be as wide as possible, with numerous vias connecting PCB layers. These practices minimize inductance and let the bulk capacitor deliver high current.

Place a low-ESR ceramic capacitor between the CPL and CPH pins. This capacitor should be 47nF, rated for VM, and be of type X5R or X7R. Additionally, place a low-ESR ceramic capacitor between the VCP and VM pins. This capacitor should be 1µF, rated for 25V, and be of type X5R or X7R.

Bypass the DVDD pin to the AGND pin with a 1µF low-ESR ceramic capacitor rated for 6.3V and of type X5R or X7R. Place this capacitor as close to the pin as possible and minimize the path from the capacitor to the AGND pin.

The VDRAIN pin can be shorted directly to the VM pin. However, if a significant distance is between the device and the external MOSFETs, use a dedicated trace to connect to the common point of the drains of the high-side external MOSFETs. Do not connect the SLx pins directly to PGND. Instead, use dedicated traces to connect these pins to the sources of the low-side external MOSFETs. These recommendations offer more accurate V_{DS} sensing of the external MOSFETs for overcurrent detection.

Minimize the loop length for the high-side and low-side gate drivers. The high-side loop is from the GHx pin of the device to the high-side power MOSFET gate, then follows the high-side MOSFET source back to the SHx pin. The low-side loop is from the GLx pin of the device to the low-side power MOSFET gate, then follows the low-side MOSFET source back to the PGND pin. Gate and source traces should be sufficiently sized to carry the full I_{DRIVE} current, and layer changes and vias should be avoided. These techniques should reduce inductance in the gate and source nodes which will help ensure best performance and efficiency. Extra care should be taken in the low side path as excessive inductance can cause the VGLS regulator to overshoot which could overstress the FET V_{GS}.

For additional layout guidelines and examples see the *Layout Guide for the DRV832x Family of Three-Phase Smart Gate Drivers* application report and the *Best Practices for Board Layout of Motor Drivers* application report.

11.1.1 Buck-Regulator Layout Guidelines

Layout is a critical portion of good power supply design. The following guidelines help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted electromagnetic interference (EMI):

- Place the feedback network resistors close to the FB pin and away from the inductor to minimize coupling noise into the feedback pin.
- Place the input bypass capacitor close to the VIN pin to decrease copper trace resistance which effects the input voltage ripple of the device.
- Place the inductor close to the SW pin to decrease magnetic and electrostatic noise.
- Place the output capacitor close to the junction of the inductor and the diode. The inductor, diode, and C_{OUT} trace should be as short as possible to decrease conducted and radiated noise and increase overall efficiency.
- Make the ground connection for the diode, C_{VIN}, and C_{OUT} as small as possible and tie it to the system ground plane in only one spot (preferably at the C_{OUT} ground point) to minimize conducted noise in the system ground plane.

For more detail on switching power supply layout considerations refer to the *AN-1149 Layout Guidelines for Switching Power Supplies* application report.

11.2 Layout Example

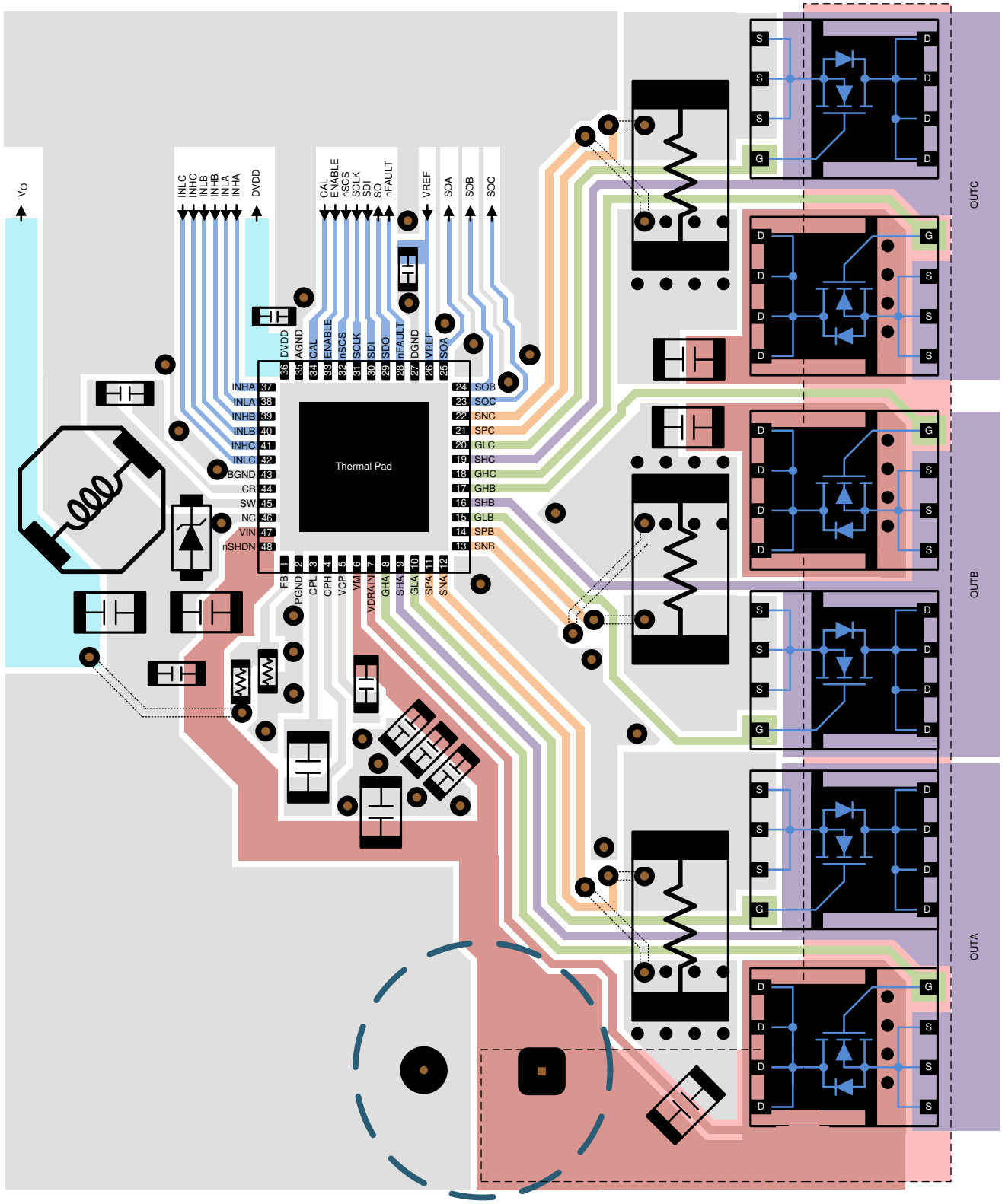


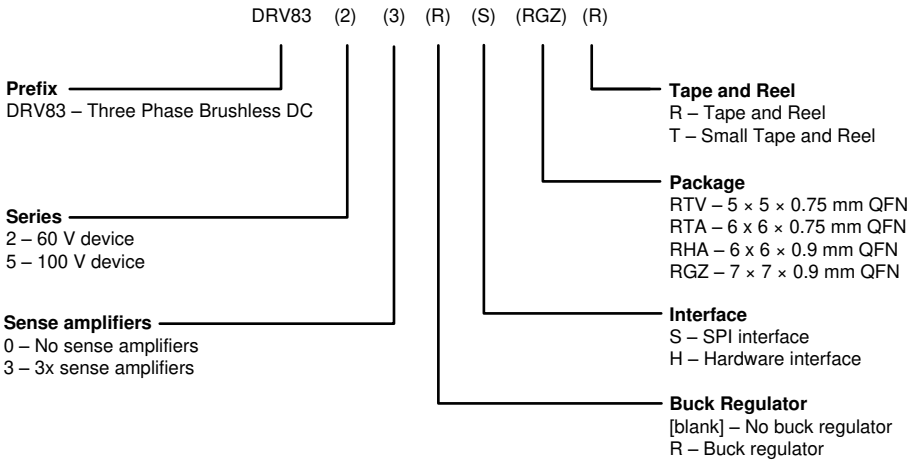
Figure 11-1. Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

The following figure shows a legend for interpreting the complete device name:



12.2 Documentation Support

12.2.1 Related Documentation

- Texas Instruments, *Architecture for Brushless-DC Gate Drive Systems* application report
- Texas Instruments, *LMR16006 SIMPLE SWITCHER® 60 V 0.6 A Buck Regulators With High Efficiency Eco-mode* data sheet
- Texas Instruments, *Layout Guide for the DRV832x Family of Three-Phase Smart Gate Drivers* application report
- Texas Instruments, *AN-1149 Layout Guidelines for Switching Power Supplies* application report
- Texas Instruments, *Understanding IDRIVE and TDRIVE In TI Motor Gate Drivers* application report
- Texas Instruments, *Reduce Motor Drive BOM and PCB Area with TI Smart Gate Drive* TI TechNote
- Texas Instruments, *Reducing EMI Radiated Emissions with TI Smart Gate Drive* TI TechNote
- Texas Instruments, *Motor Drive Protection With TI Smart Gate Drive* TI TechNote
- Texas Instruments, *QFN/SON PCB Attachment* application report
- Texas Instruments, *Cut-Off Switch in High-Current Motor-Drive Applications* application report
- Texas Instruments, *Hardware Design Considerations for an Efficient Vacuum Cleaner using BLDC Motor* application report
- Texas Instruments, *Hardware Design Considerations for an Electric Bicycle using BLDC Motor* application report
- Texas Instruments, *Sensored 3-Phase BLDC Motor Control Using MSP430™* application report

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.5 Trademarks

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SIMPLE SWITCHER® is a registered trademark of Texas Instruments.
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12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8320HRTVR	Active	Production	WQFN (RTV) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV8320H
DRV8320HRTVR.A	Active	Production	WQFN (RTV) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV8320H
DRV8320HRTVT	Active	Production	WQFN (RTV) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV8320H
DRV8320HRTVT.A	Active	Production	WQFN (RTV) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV8320H
DRV8320HRTVTG4	Active	Production	WQFN (RTV) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV8320H
DRV8320HRTVTG4.A	Active	Production	WQFN (RTV) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV8320H
DRV8320RHRHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV 8320RH
DRV8320RHRHAR.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV 8320RH
DRV8320RHRHAT	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV 8320RH
DRV8320RHRHAT.A	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV 8320RH
DRV8320RSRHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV 8320RS
DRV8320RSRHAR.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV 8320RS
DRV8320RSRHAT	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV 8320RS
DRV8320RSRHAT.A	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV 8320RS
DRV8320SRTVR	Active	Production	WQFN (RTV) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV8320S
DRV8320SRTVR.A	Active	Production	WQFN (RTV) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV8320S
DRV8320SRTVT	Active	Production	WQFN (RTV) | 32	250 | SMALL T&R	Yes	Call TI | Nipdau	Level-2-260C-1 YEAR	-40 to 125	DRV8320S
DRV8320SRTVT.A	Active	Production	WQFN (RTV) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8320S
DRV8323HRTAR	Active	Production	WQFN (RTA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV8323H
DRV8323HRTAR.A	Active	Production	WQFN (RTA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV8323H
DRV8323HRTAT	Active	Production	WQFN (RTA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV8323H
DRV8323HRTAT.A	Active	Production	WQFN (RTA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV8323H
DRV8323RHRGZR	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8323RH

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8323RHRGZR.A	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8323RH
DRV8323RHRGZT	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8323RH
DRV8323RHRGZT.A	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8323RH
DRV8323RSRGZR	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8323RS
DRV8323RSRGZR.A	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8323RS
DRV8323RSRGZRG4	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8323RS
DRV8323RSRGZRG4.A	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8323RS
DRV8323RSRGZT	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8323RS
DRV8323RSRGZT.A	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DRV8323RS
DRV8323SRTAR	Active	Production	WQFN (RTA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV8323S
DRV8323SRTAR.A	Active	Production	WQFN (RTA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV8323S
DRV8323SRTARG4	Active	Production	WQFN (RTA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV8323S
DRV8323SRTARG4.A	Active	Production	WQFN (RTA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV8323S
DRV8323SRTAT	Active	Production	WQFN (RTA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV8323S
DRV8323SRTAT.A	Active	Production	WQFN (RTA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV8323S

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

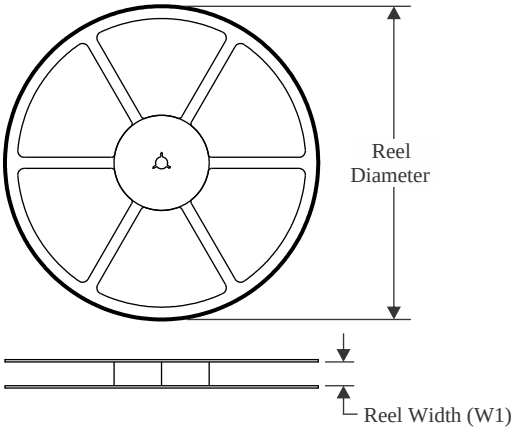
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

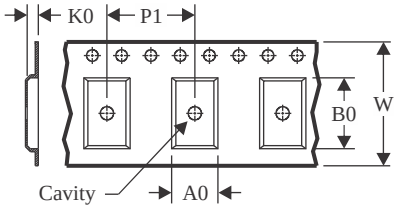
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

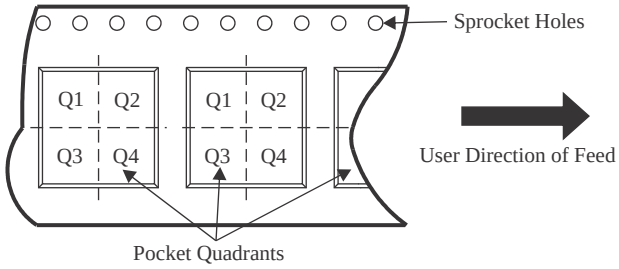


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

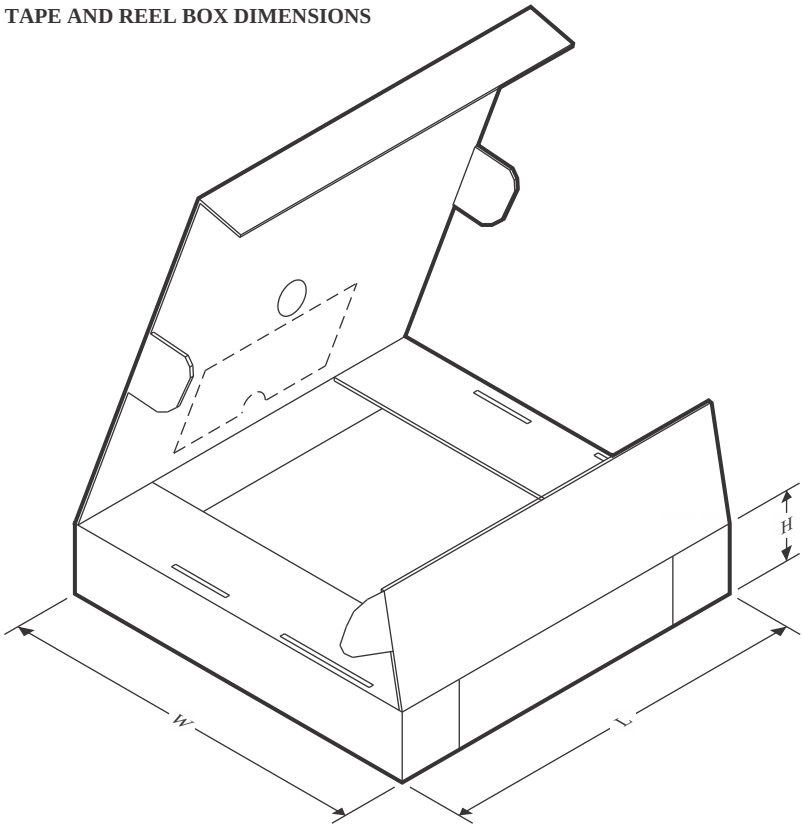


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8320HRTVR	WQFN	RTV	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
DRV8320HRTVT	WQFN	RTV	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
DRV8320HRTVTG4	WQFN	RTV	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
DRV8320RHRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DRV8320RHRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DRV8320RSRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DRV8320RSRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DRV8320SRTVR	WQFN	RTV	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
DRV8320SRTVT	WQFN	RTV	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
DRV8323HRTAR	WQFN	RTA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DRV8323HRTAT	WQFN	RTA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DRV8323RHRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
DRV8323RHRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
DRV8323RSRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
DRV8323RSRGZRG4	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
DRV8323RSRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8323SRTAR	WQFN	RTA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DRV8323SRTARG4	WQFN	RTA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DRV8323SRTAT	WQFN	RTA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8320HRTVR	WQFN	RTV	32	3000	346.0	346.0	33.0
DRV8320HRTVT	WQFN	RTV	32	250	182.0	182.0	20.0
DRV8320HRTVTG4	WQFN	RTV	32	250	182.0	182.0	20.0
DRV8320RHRHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
DRV8320RHRHAT	VQFN	RHA	40	250	182.0	182.0	20.0
DRV8320RSRHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
DRV8320RSRHAT	VQFN	RHA	40	250	182.0	182.0	20.0
DRV8320SRTVR	WQFN	RTV	32	3000	346.0	346.0	33.0
DRV8320SRTVT	WQFN	RTV	32	250	210.0	185.0	35.0
DRV8323HRTAR	WQFN	RTA	40	2500	367.0	367.0	38.0
DRV8323HRTAT	WQFN	RTA	40	250	182.0	182.0	20.0
DRV8323RHRGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
DRV8323RHRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
DRV8323RSRGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
DRV8323RSRGZRG4	VQFN	RGZ	48	2500	367.0	367.0	38.0
DRV8323RSRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
DRV8323SRTAR	WQFN	RTA	40	2500	367.0	367.0	38.0
DRV8323SRTARG4	WQFN	RTA	40	2500	367.0	367.0	38.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8323SRTAT	WQFN	RTA	40	250	182.0	182.0	20.0

GENERIC PACKAGE VIEW

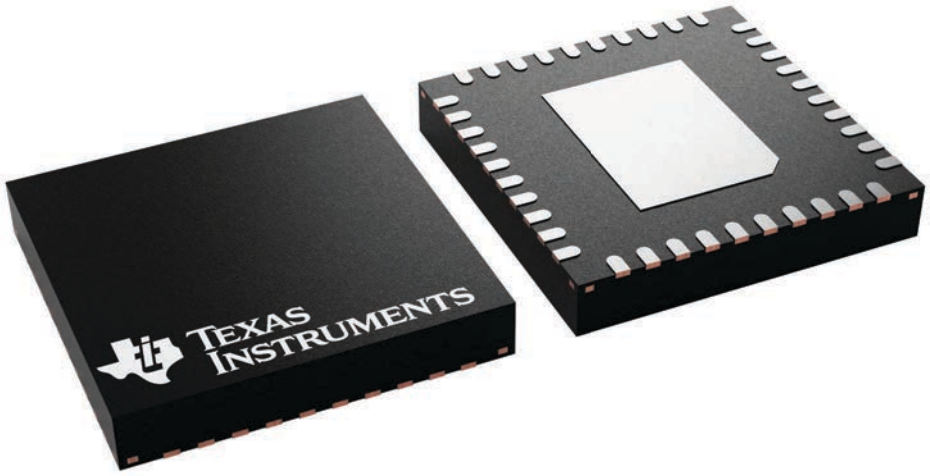
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

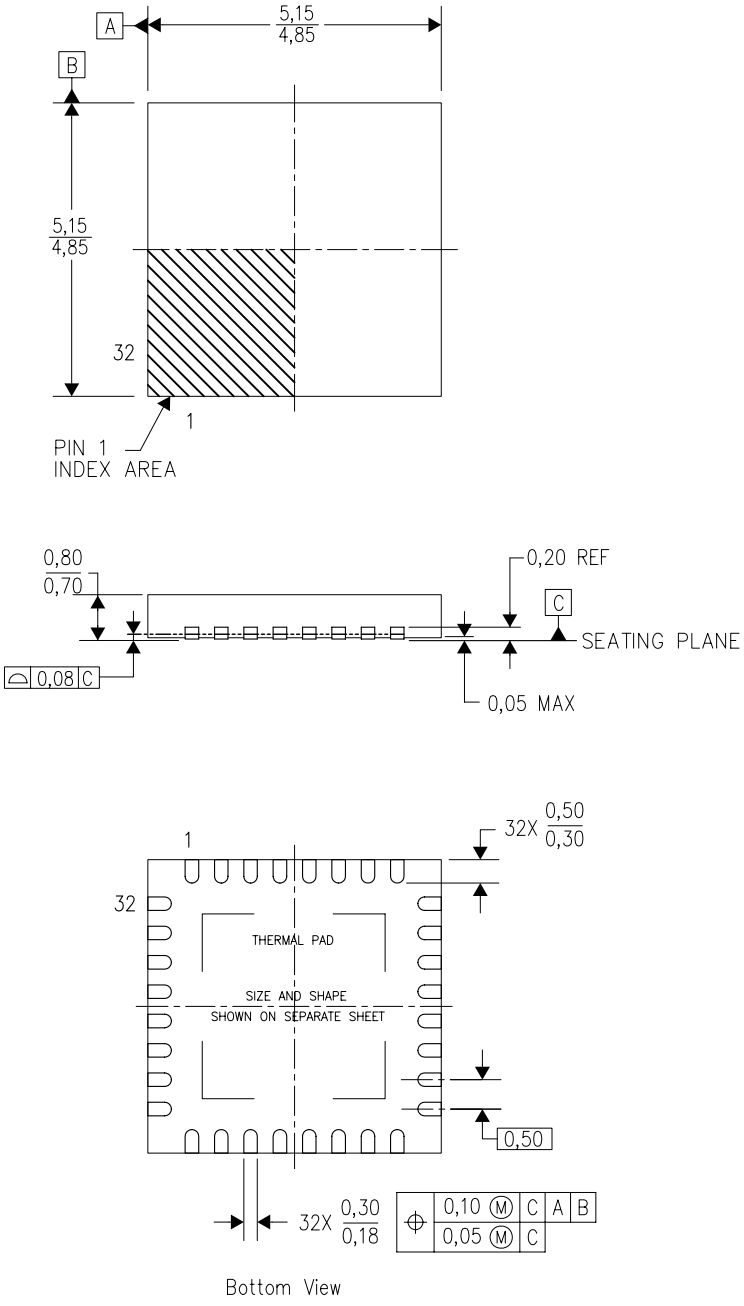
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225870/A

RTV (S–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



4206245/C 10/11

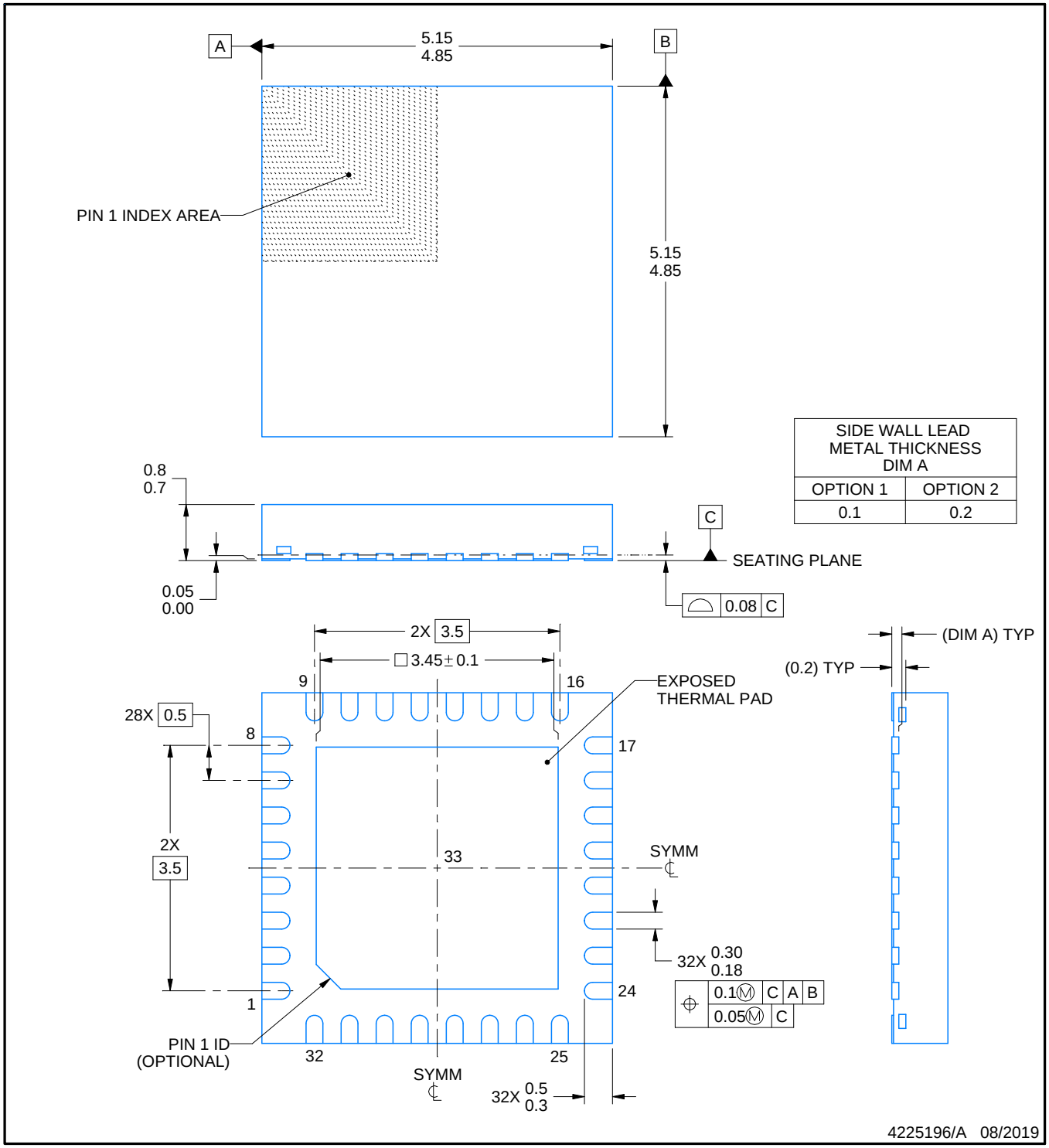
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

RTV0032E

PACKAGE OUTLINE

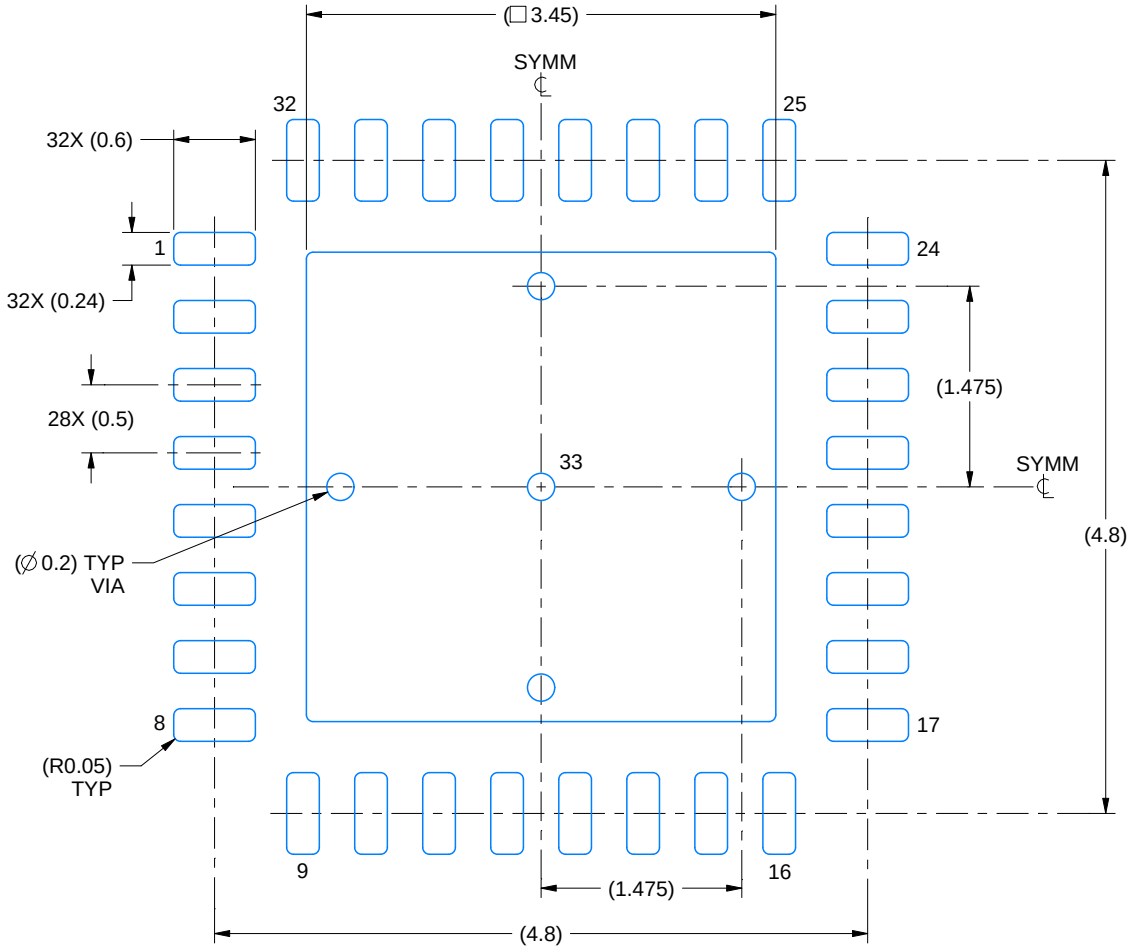
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

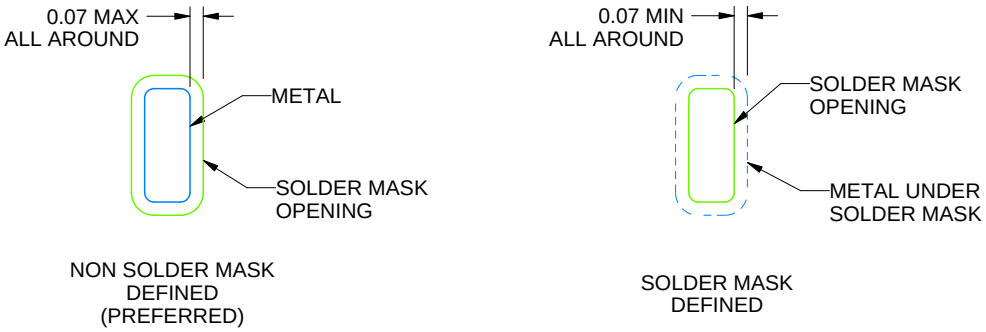


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X

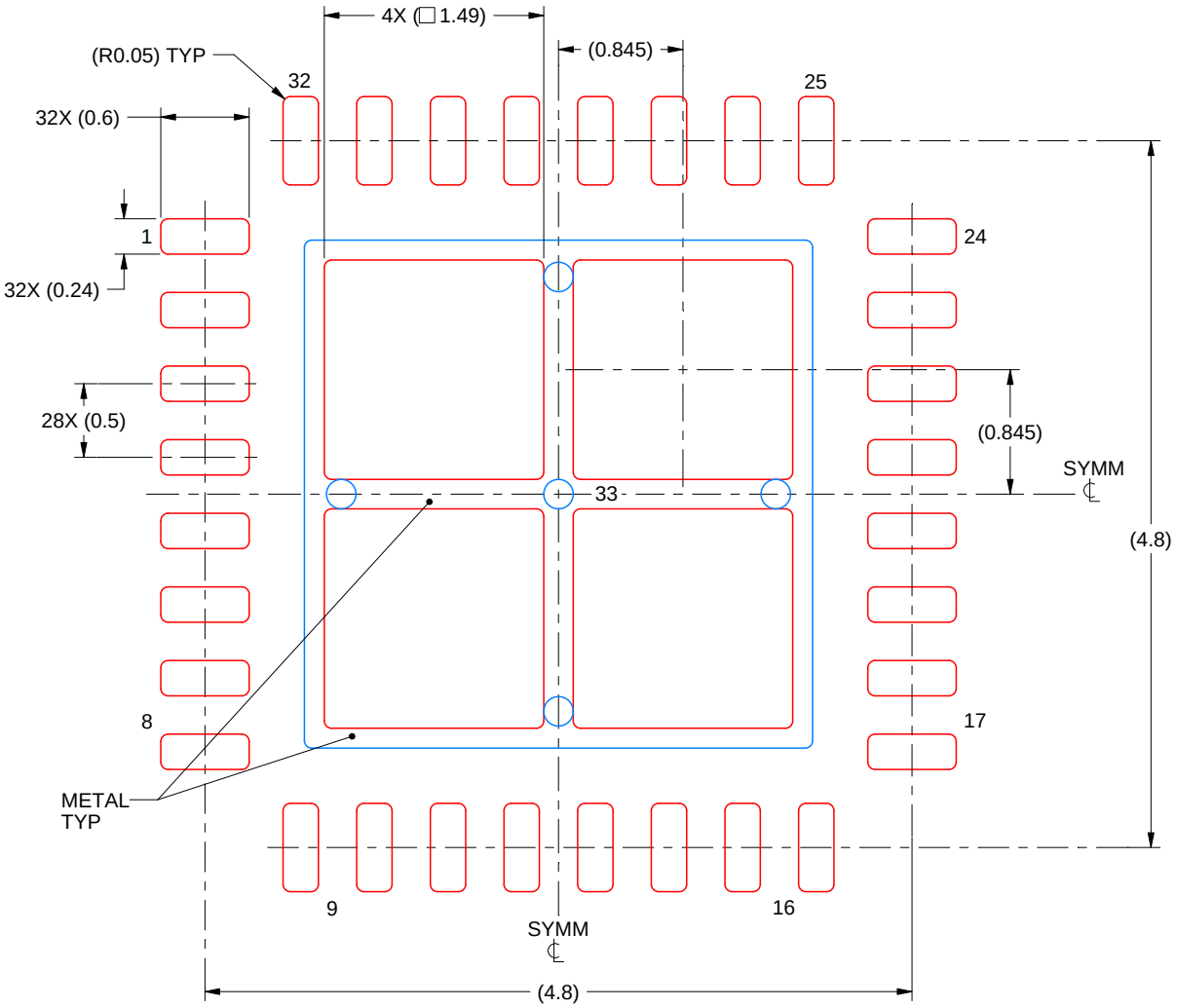


SOLDER MASK DETAILS

4225196/A 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4225196/A 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

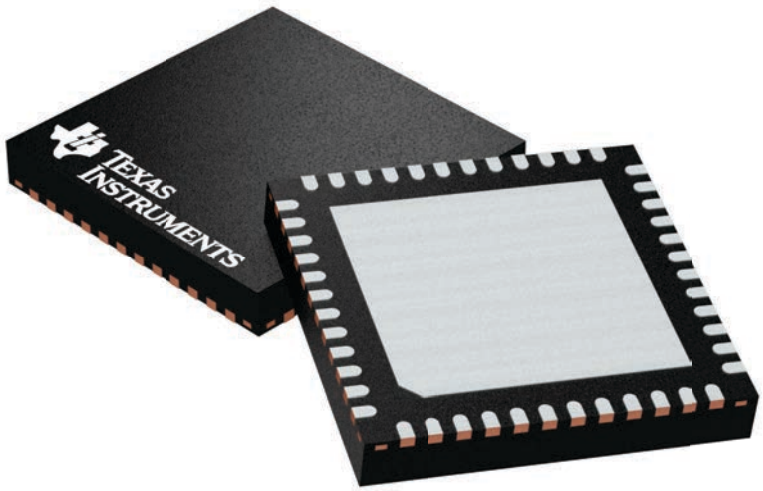
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

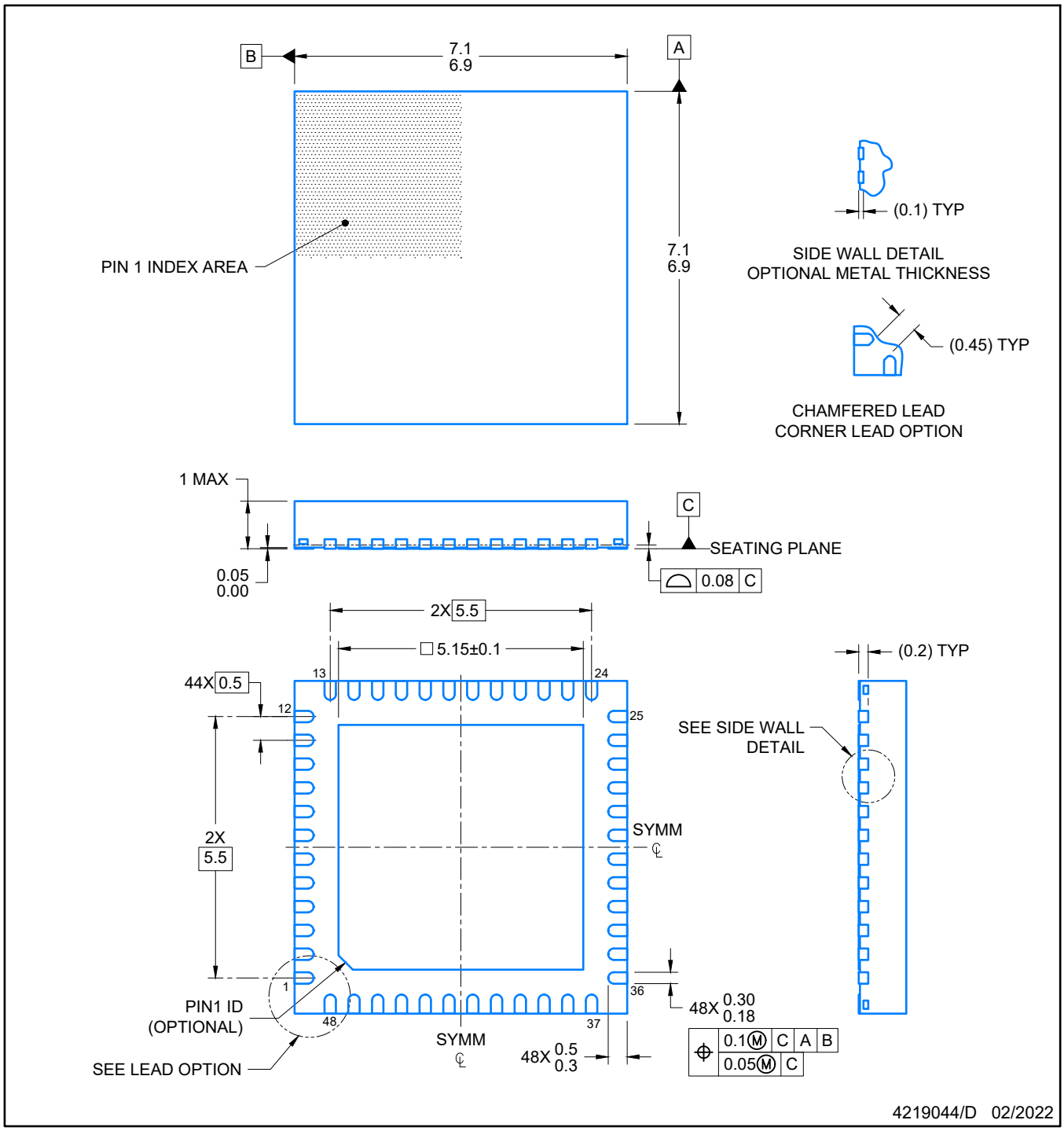
PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

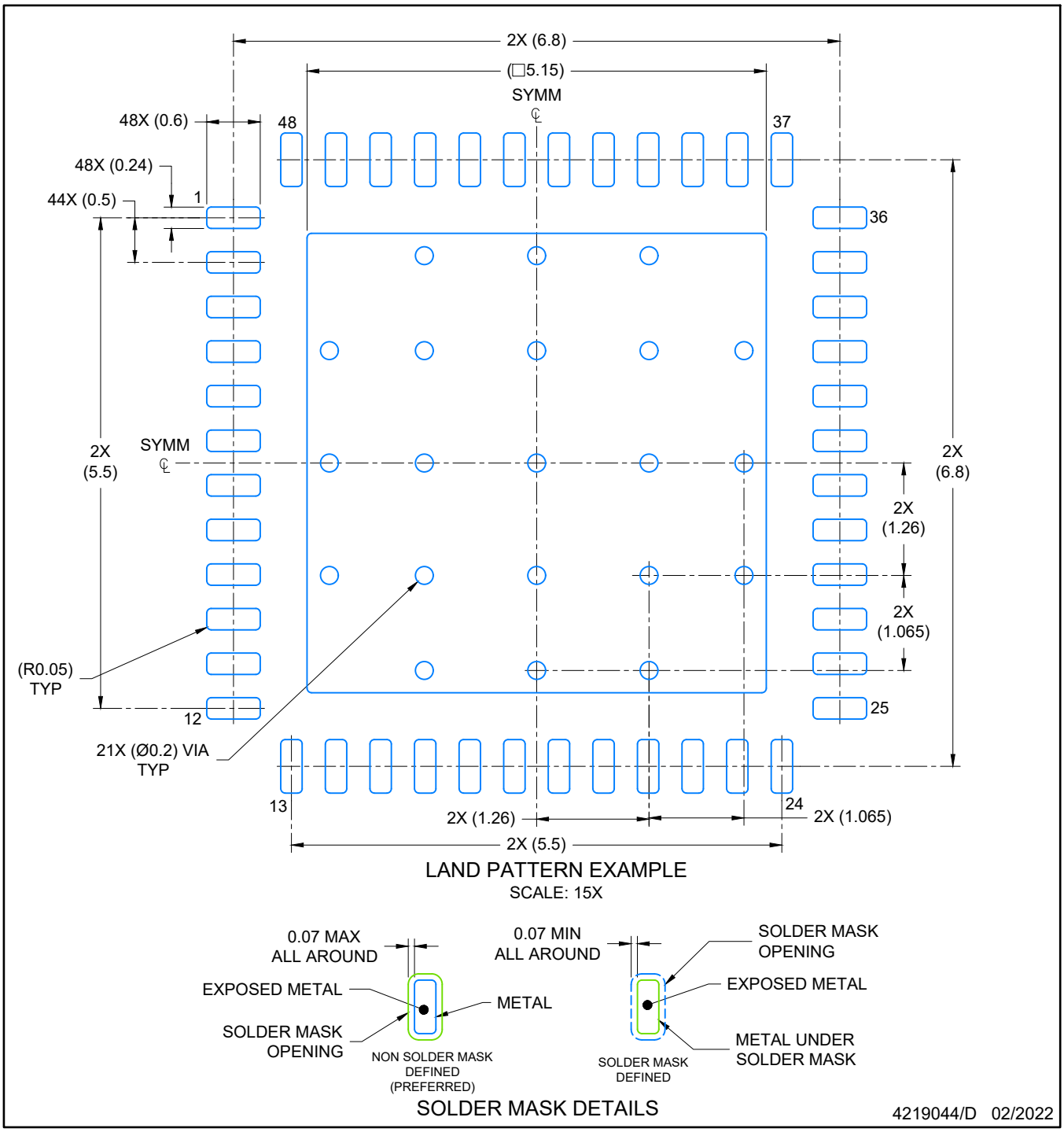
4224671/A

PLASTIC QUADFLAT PACK- NO LEAD



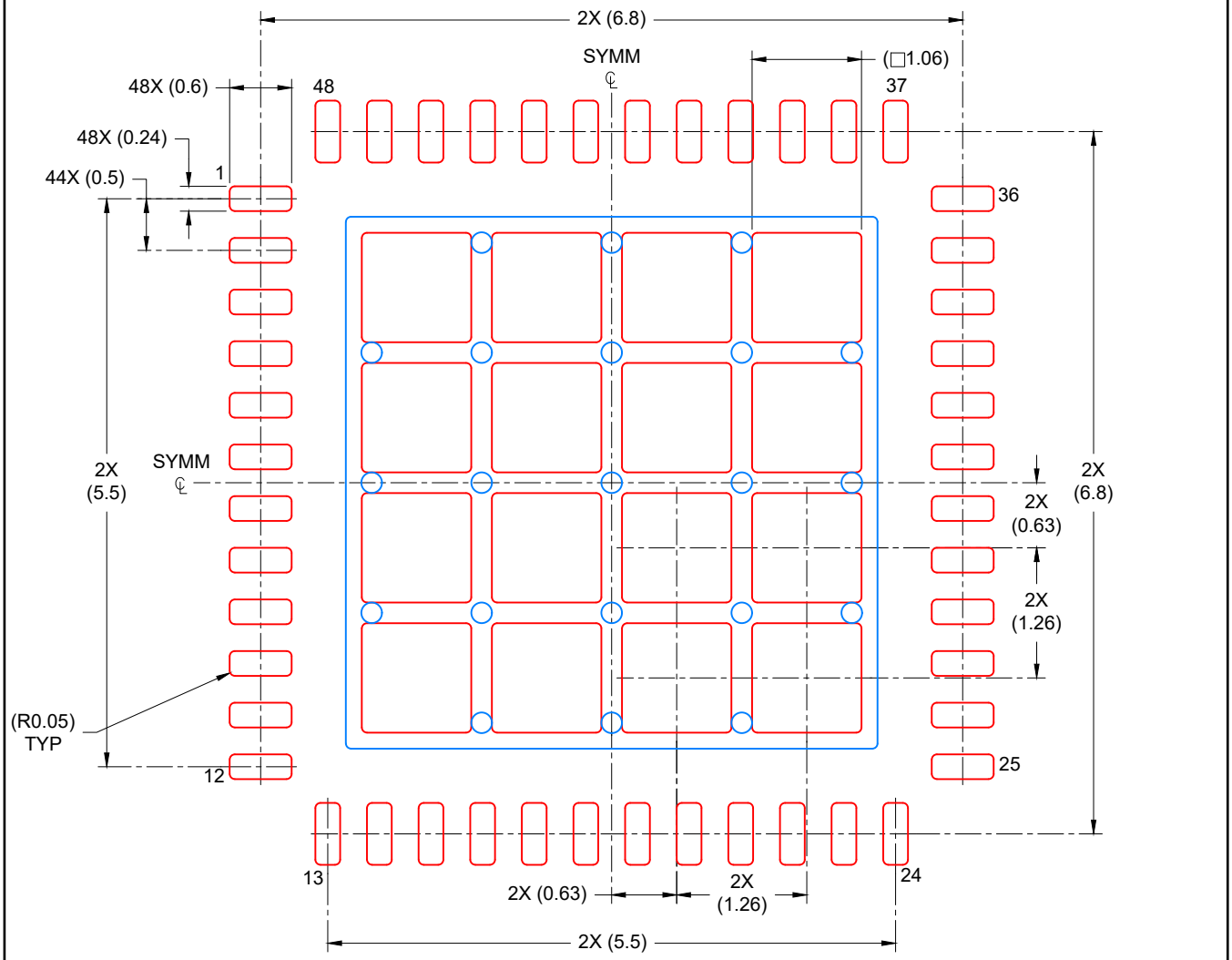
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

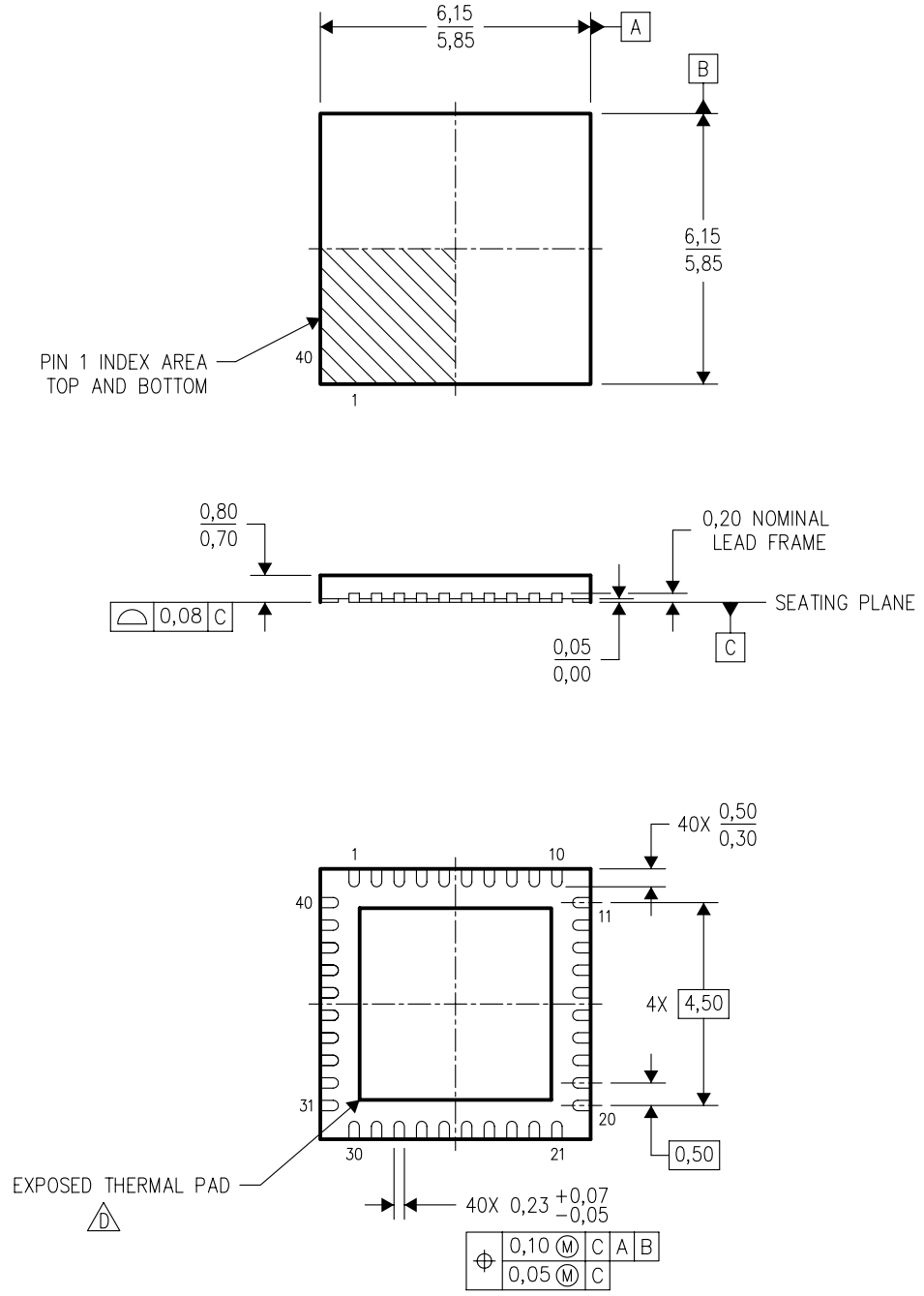
EXPOSED PAD
67% PRINTED COVERAGE BY AREA
SCALE: 15X

4219044/D 02/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

RTA (S–PQFP–N40) PLASTIC QUAD FLATPACK



4204422/B 11/04

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

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Last updated 10/2025