FAN31790 6-Channel PWM/RPM Fan Controller

1 Features

- **Fan Control and Monitoring**
  - Control up to 6 fans with 9-bit PWM Drive, Customizable PWM Dutycycle Rate-of-change, and PWM Frequencies from 25Hz to 25kHz
  - Up to 12, 11-bit Tachometer Inputs for speed and failure detection
  - Automatic Fan Speed Control Loops, RPM control on fans with digital tachometer outputs
- **High System Reliability**
  - Fan failure/fault detection with automatic safe state responses.
  - Power-up defaults are hardware selectable. Default PWM frequency, duty cycle, and start-up speed can be set by external pin connections.
  - Integrated Watchdog Timer
- **I2C Communication interface**
  - Fast-mode I^2C controller up to 400kbps
  - Open-drain pins
  - 16 possible hardware-selectable addresses
- **Operating characteristics**
  - Wide supply voltage range: 1.62V to 3.6V
  - Extended temperature: –40°C up to 125°C
- **Clock system**
  - Internal 32kHz oscillator with ±5% accuracy
  - External 32kHz crystal oscillator (LFXT)
  - 32.768kHz Digital clock output
- **Package**
  - Bom-to-BOM and Pin-to-pin with common fan controllers
  - 28 pin LGA 4x4mm (Identical footprint to WQFN 4x4mm)
  - RoHS Compliant

2 Applications

- Desktop PC/Motherboard
- Rack Server Motherboard
- GPU card & Hardware Accelerator
- Automotive Seat Fan
- Air Purifier

3 Description

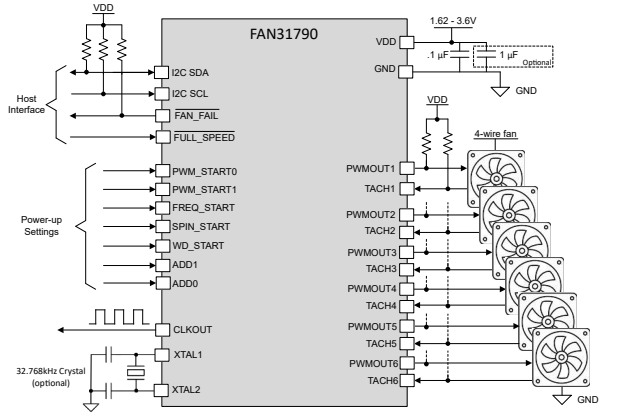
The FAN31790 is an intelligent fan controller that can control the speed of six fans using independent PWM outputs and dedicated TACH inputs. The device is designed for 4-wire fans but can still be used to modulate the speed of 3-wire and 2-wire fans via external power transistors. The device can monitor the speed of up to 12 fans with six dedicated tachometer inputs and any of the PWM output channels can be reconfigured as additional tachometers. Using a tachometer allows the device to automatically adjust the PWM duty cycles to maintain desired fan speeds. Target fan speeds and update rates can be configured via an I2C interface.

This device's default power-up states are hardware configurable with external connections. The fan spin-up behavior, PWM frequency, PWM duty cycle, and the integrated watchdog timer can all be configured via pin configurations. This allows customization of fan behavior before custom settings are loaded via the I2C bus.

The FAN31790 supports a 1.62-3.6V supply voltage for PWM/TACH pins and the I2C interface. The FAN31790 is designed to be pin-to-pin and BOM-to-BOM compatible with common fan controllers and it offers a matching I2C interface and register map to leverage any pre-existing software drivers.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)	Pin-to-pin
FAN31790SZFPR	28 LGA	4.0mm × 4.0mm	Common Fan Controllers



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4 Pin Configuration and Functions

28-pin ZFP (LGA) Package

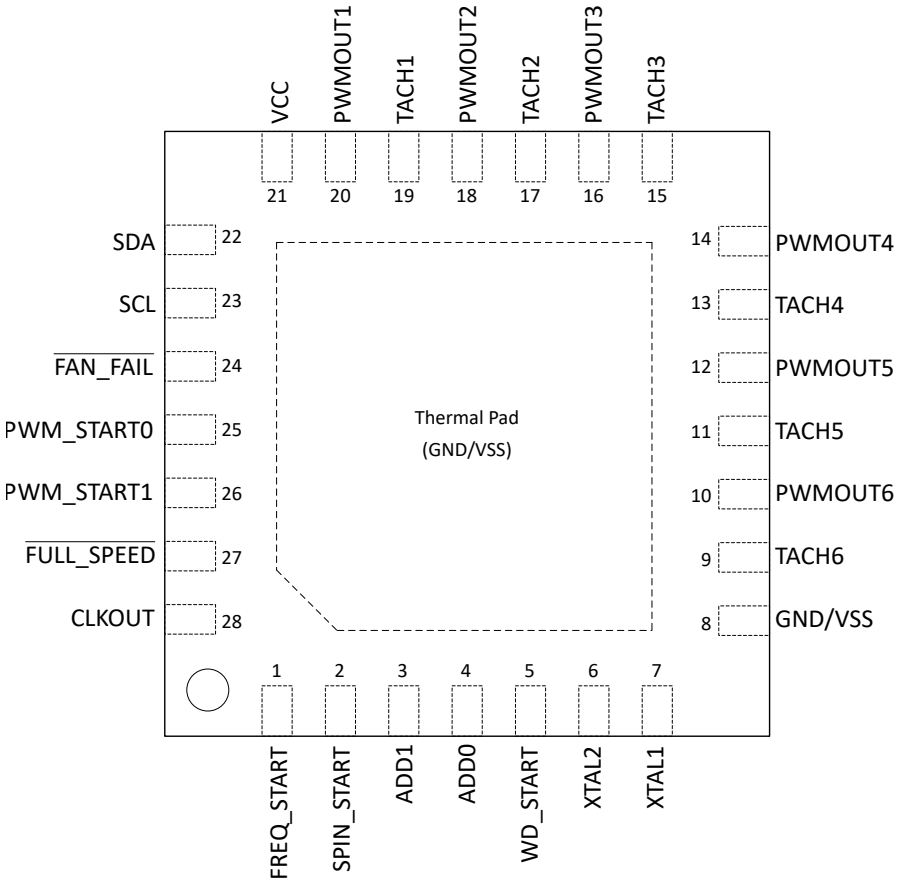


Figure 4-1. 28-pin ZFP (LGA) Package

Table 4-1. Pin Function

PIN		I/O	DESCRIPTION
No.	NAME		
1	FREQ_START	I	This input is sampled at power-up and sets the power-up value for the PWM output frequency.
2	SPIN_START	I	This input is sampled at power-up and sets the initial spin-up behavior.
3	ADD1	I	I2C Address select inputs. Can be connected to VCC, GND, SCL, or SDA for 16 possible addresses. Address inputs sampled at the start of every I2C transmission.
4	ADD0	I	
5	WD_START	I	Input sampled at power up and sets initial Watchdog Behavior.
6	XTAL2	I	Pins to connect optional 32.768kHz Crystal oscillator. A crystal can be used when additional timing precision is required. The device also has an integrated 32.768kHz internal oscillator that can be used and will be defaulted to until the crystal stabilizes.
7	XTAL1	I	
8	GND	--	Ground
9	TACH6	I	Inputs for tachometer signals. Can be configured for digital or analog signals. If fan has digital tachometer output, these pins can be used for RPM control. In 2-pin fans, analog signal can be used to detect fan failure.
11	TACH5	I	
13	TACH4	I	
15	TACH3	I	
17	TACH2	I	
19	TACH1	I	
10	PWMOUT6 (TACH12)	I/O	Open-drain output for 4-wire fan PWM inputs or for 2-pin and 3-pin fans, modulating the power transistor. Can also be configured to act as additional tachometer inputs. Can be pulled high to 3.3V.
12	PWMOUT5 (TACH11)	I/O	
14	PWMOUT4 (TACH10)	I/O	
16	PWMOUT3 (TACH9)	I/O	
18	PWMOUT2 (TACH8)	I/O	
20	PWMOUT1 (TACH7)	I/O	
21	VCC	I	Power Supply. 1.62-3.6V. Need a minimum of a .1 uF bypass cap to GND.
22	SDA	I/O	I2C Serial Data Line. Open Drain.
23	SCL	I	I2C Serial Clock Line. Open Drain.
24	$\overline{\text{FAN\_FAIL}}$	O	Active-low open drain fan-failure Output. Goes low when fault condition is met.
25	PWM_START0	I	Input sampled at power-up. Sets the default value for all PWMOUT duty cycles.
26	PWM_START1	I	
27	$\overline{\text{FULL\_SPEED}}$	I	When driven low, this input forces all PWMs to 100% duty cycle. Only exception is if a fan has failed and "Duty cycle = 0 on failure" mode has been selected.
28	CLKOUT	O	32.768kHz Clock Output. Clock is sourced from either the external crystal or the internal oscillator when the crystal is not used. Clock output is always active.
--	Thermal Pad	--	Connect to GND.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
VDD	Supply voltage	At VDD pin	–0.3	4.1	V
V_I	Input voltage	Applied to any input pins	–0.3	V_{DD} + 0.3 (4.1 MAX)	V
I_{VDD}	Current of VDD pin	Current into VDD pin (source), VDD >= 2.7V, -40 ℃ ≤ T_a ≤ 125 ℃		48	mA
I_{VSS}	Current of VSS pin	Current out of VSS pin (sink), VDD >= 2.7V, -40 ℃ ≤ T_a ≤ 125 ℃		48	mA
I_{IO}	Current for standard IO pin	Current sunk or sourced by each IO pin, VDD >= 2.7V		6	mA
T_{stg}		Storage temperature	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins(1)	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Supply voltage	1.62		3.6	V
C_{VDD}	Capacitor placed between VDD and VSS (1)	0.1	1		uF
T_A	Ambient temperature	–40		125	°C
T_J	Max junction temperature			130	°C

(1) Connect C_{VDD} between VDD/VSS, as close to the device pins as possible. A low-ESR capacitor with at least the min specified value and tolerance of ±20% or better is required for C_{VDD}.

5.4 Thermal Information

THERMAL METRIC(1)		PACKAGE	VALUE	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	LGA-28 (ZFP)	82.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		49.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		61.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		3.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		61.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		48.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Power Supply

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
IDD	Current	VDD = 3.3V		2.9	5	mA
	Power dissipation	VDD = 3.3V		9.6		mW
V_{POR}	POR Threshold		1.50	1.58	1.65	V

5.6 Fan Controller Characteristics

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
r_{PWM}	PWM Resolution		9		9	bits
f_{PWM}	PWM Frequency Accuracy		-4		4	%
r_{TACH}	TACH Count Resolution		11		11	bits
f_{TOSC}	TACH Count Oscillator and CLKOUT clock			32.768		kHz
$f_{ERR:TOSC}$	TACH Count Oscillator and CLKOUT accuracry	-40 °C ≤ Ta ≤ 85 °C, 1.62V ≤ VDD ≤ 3.6V	-3		3	%
		-40 °C ≤ Ta ≤ 125 °C, 1.62V ≤ VDD ≤ 3.6V	-5		5	%
		Using External Crystal	-0.1		0.1	%
$t_{TACHMIN}$	TACH Minimum Pulse		25		75	µS

5.7 External Crystal Parameters

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
F_{EXT}	External Crystal Frequency		32.768		kHz
	Crystal Startup time		1		s
ESR	Series Resistance			50	kΩ
C_L	Load Capacitance		12		pF

5.8 Digital IO

5.8.1 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High level input voltage	All I/O	VDD≥1.62V	0.7*VDD		VDD+0.3	V
V_{IL}	Low level input voltage	All I/O	VDD≥1.62V	-0.3		0.3*VDD	V
V_{HYS}	Hysteresis	All I/O		0.1*VDD			V
I_{lkg}	High-Z leakage current	All IO (1) (2)	VDD = 3V			50	nA
C_I	Input capacitance		VDD = 3.3V		5		pF
V_{OH}	High level output voltage	CLK_OUT	VDD≥2.7V, $\|I_{IO}\|_{,max}$=6mA	VDD-0.5			V
V_{OH}	High level output voltage	CLK_OUT	VDD ≥ 1.71V, $\|I_{IO}\|_{,max}$=2mA	VDD-0.4			V

5.8.1 Electrical Characteristics (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OL}	Low level output voltage	CLK_OUT	VDD≥2.7V, $\|I_{IO}\|_{,max}$=6mA VDD≥1.71V, $\|I_{IO}\|_{,max}$=2mA			0.4	V

(1) The leakage current is measured with VSS or VDD applied to the corresponding pin(s), unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

5.8.2 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_r,t_f	Output rise/fall time	All I/O	VDD ≥ 1.71V			12.5	ns

5.9 I2C Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	Fast mode		UNIT
			MIN	MAX	
f_{SCL}	SCL clock frequency			400	kHz
$t_{HD,STA}$	Hold time (repeated) START		0.6		us
t_{LOW}	LOW period of the SCL clock		1.3		us
t_{HIGH}	High period of the SCL clock		0.6		us
$t_{SU,STA}$	Setup time for a repeated START		0.6		us
$t_{HD,DAT}$	Data hold time		0		ns
$t_{SU,DAT}$	Data setup time		100		ns
$t_{SU,STO}$	Setup time for STOP		0.6		us
t_{BUF}	bus free time between a STOP and START condition		1.3		us
t_{BUF_ADDx}	bus free time between a STOP and START condition for new I2C address.	Changing ADDx pins inbetween transactions	250		us
$t_{VD;DAT}$	data valid time			0.9	us
$t_{VD;ACK}$	data valid acknowledge time			0.9	us

5.9.1 I2C Filter

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SP}	Pulse duration of spikes suppressed by input filter			11	35	ns

5.9.2 I²C Timing Diagram

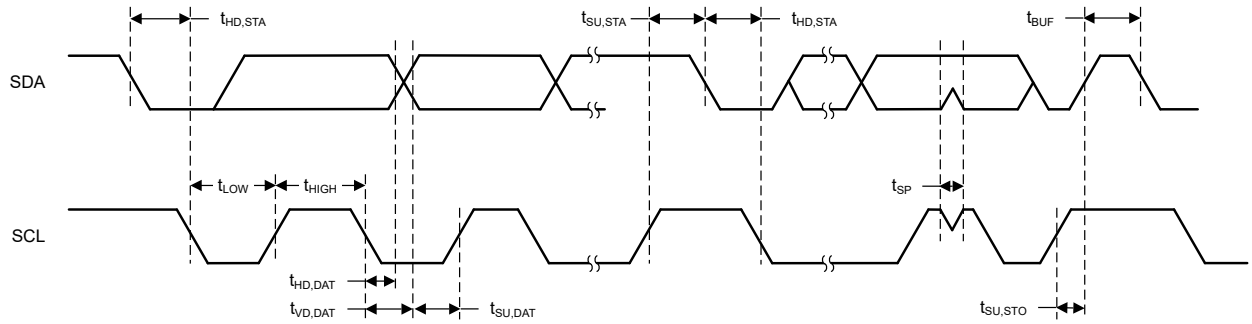


Figure 5-1. I2C Timing Diagram

6 Detailed Description

The FAN31790 is a PWM fan controller IC that manages the speed and health of up to 12 independent cooling fans in a system. It communicates with a host via an I2C, allowing software to dynamically adjust fan speeds based on temperature, load, or other system conditions.

The core function of the FAN31790 is generating independent PWM signals to provide speed control for up to 6 fans. It supports two control modes: PWM mode where the duty cycle is directly specified (0-100%), and RPM mode where the device actively monitors fan tachometer feedback and automatically adjusts the PWM duty cycle to maintain a target RPM. This closed-loop control ensures fans spin at the desired speed regardless of load variations.

Beyond speed control, the FAN31790 provides comprehensive fan monitoring and diagnostics. It can read up to 12 tachometer signals (six dedicated inputs plus six configurable from the PWM outputs), allowing it to detect fan failure conditions and report faults to the host system. Additional features include acoustic optimization through controlled duty cycle rate-of-change, fan spin-up assistance for reliable starting, sequential activation of multiple fans to reduce inrush current, and an I2C watchdog timer that forces fans to full speed if the host system becomes unresponsive.

6.1 Fan Control

FAN31790 Fan control is initially configured by hardware configuration of several POR configuration pins. From there, fan control is adjusted by the host via I2C and in one of the two operation modes: PWM mode and RPM mode.

6.1.1 PWM Mode

The key advantage of PWM mode is simplicity: the host directly commands the FAN31790 to output a desired speed without requiring feedback. The duty cycle for the PWMOUTx pins are configured by writing the PWM target duty cycle registers (0-511, representing 0-100%.) Each PWMOUTx channel can be individually controller. The fan's speed is proportional to the duty cycle output.

The PWM duty cycle changes gradually at a programmable rate set in the Fan Dynamics registers to minimize acoustic noise from sudden speed changes. Therefore, the actual current PWM duty cycle being output can be read anytime from the PWMOUT Duty Cycle registers.

6.1.2 RPM Mode

In RPM mode, the FAN31790 implements closed-loop speed control by continuously monitoring fan tachometer pulses and automatically adjusting the PWM duty cycle to maintain a target speed. RPM mode provides superior control compared to PWM mode since it compensates for fan aging, load variations, and manufacturing tolerances by maintaining precise speed regardless of conditions.

The host system writes a desired tachometer count to the TACH Target Count registers (50h-5Bh) for each fan, representing the desired RPM. The device then measures the actual tachometer frequency by counting internal 8192Hz clock cycles during a selectable number of tachometer periods (set in the Fan Dynamics registers 08h-0Dh), storing the result in the TACH Count registers (18h-2Fh). If the actual count is below the target, the device increases the PWM duty cycle; if above target, it decreases the duty cycle. It is continuously closing the loop until the fan reaches the commanded speed.

For fine-tuned control, the Window registers (60h-65h) allow the control loop to slow the duty cycle rate-of-change to 1 LSB per second when the TACH count is within a specified window of the target, improving stability near steady-state.

6.1.3 Rate-of-Change Control

Sudden changes in fan speed produce audible noise that users can hear. The FAN31790 provides a programmable rate-of-change mechanism to smooth PWM duty cycle transitions and minimize acoustic impact.

The PWM Rate-of-Change bits (4:2 in the Fan Dynamics registers 08h-0Dh) control the time interval between each 1 LSB increment or decrement of the 9-bit duty cycle, ranging from 0ms (immediate) to 125ms per step.

This allows the fan speed to ramp smoothly over time. Additionally, the Asymmetric Rate of Change bit (1 in the Fan Dynamics registers) enables a slower rates for duty cycle decrease compared to increase, further refining acoustic behavior.

Note

This Rate-of-change will also be applied when the $\overline{\text{FULL\_SPEED}}$ pin is activated or if the internal fault detection has been triggered and configured to drive any fan to 100%.

6.1.4 Spin-Up

When a fan is stationary and a low PWM duty cycle is applied, the fan may lack sufficient torque to overcome its rotational inertia and fail to start. The FAN31790 provides an automatic spin-up feature that applies 100% duty cycle for a short period to accelerate the fan, then transitions to the target duty cycle.

The Spin-Up bits (6:5 in the Fan Configuration registers) allow selection of no spin-up, or spin-up until 2 tachometer pulses are detected (indicating the fan is rotating.) Maximum durations waiting for the TACH signals is configurable to 0.5 seconds, 1 second, or 2 seconds. The SPIN_START pin sets the POR spin-up configuration.

6.1.5 Sequential Fan Start

When multiple high-current fans are powered on simultaneously, the startup current surge can stress the system power supply. The FAN31790 provides sequential fan activation to minimize this inrush current by inserting programmable delays between fan activations. The fans are started one at a time. The Sequential Start Delay bits (7:5 in the Failed Fan Options/Sequential Start register 14h) select the delay interval: 0s, 250ms, 500ms, 1s, 2s, or 4s between fan starts.

Sequential activation applies when fans are forced to full speed during POR, when responding to a fan failure, or when the $\overline{\text{FULL\_SPEED}}$ input is asserted. Each PWM is started and will follow it's spin-up and rate-of-change settings. After the delay interval, the next PWM will start.

Note

Delay Interval will apply even to unused or disabled PWM channels.

6.1.6 $\overline{\text{FULL\_SPEED}}$ Input

The $\overline{\text{FULL\_SPEED}}$ input provides a hardware-driven safety mechanism for fail-safe overtemperature protection. Driving this input low forces all PWM outputs to 100% duty cycle, except failed fans that have "Duty Cycle = 0% on Failure" is selected. This allows an external monitors to immediately drive fans to maximum speed if the system overheats. In systems with multiple FAN31790s, all $\overline{\text{FAN\_FAIL}}$ outputs can be wired together and connected to all $\overline{\text{FULL\_SPEED}}$ inputs, ensuring that if any fan fails on any controller, all fans on all controllers run at full speed. The $\overline{\text{FULL\_SPEED}}$ input remains active even when the device is in standby mode.

6.1.7 I2C Watchdog Timer

The I2C watchdog timer monitors communication with the host system and forces fans to full speed if the host becomes unresponsive. This is a safety feature for data centers and mission-critical equipment. When enabled, the device tracks the time between I2C transactions and forces all fans to 100% duty cycle if no valid I2C transactions occur within a selected timeout period. The I2C Watchdog bits (2:1 in the Global Configuration register 00h) set the timeout to 5 seconds, 10 seconds, or 30 seconds, or watchdog disabled. The WD_START pin sets the power-up watchdog configuration. Once the watchdog times out it forces fans to full speed. Normal operation resumes if valid I2C transactions resume and the FAN31790 returns to its previous PWM values. The host must periodically communicate with each FAN31790 device to keep the watchdog satisfied. For example, by reading a status register.

6.1.8 Power-on Reset Configuration Pins

The FAN31790 has five pins that are sampled at power-up to configure initial device behavior and default value for certain configuration registers. This allows the device to start controlling fans immediately without waiting for I2C interaction from the host.

Table 6-1. POR Configuration Pins

Name	Pin	Function	Registers	Pin State at POR		
				GND	Unconnected/Floating	VCC
FREQ_START	1	Initial PWM Output Frequency	PWM Freq Register (01h)	30 Hz	1.47 kHz	25 kHz
SPIN_START	2	Initial spin-up behavior	Fan Config Registers (02-07h)	Disabled	0.5s or 2 TACH counts	1s or 2 TACH counts
WD_START	5	Initial Watchdog behavior	Global Config Register (00h)	Disabled	N/A	Enabled 30s timeout
PWM_START0	25	Initial duty cycle	PWM Target Duty Cycle Registers (40-4Bh)	See Table below.		
PWM_START1	26					

Note

FREQ_Start, Spin_start, PWM_Start0/1 pins all have an internal ~40k pull-down resistor on them used as part of the intial pin state logic. It's perfectly fine to connect these POR pins to VCC via an external pull-up resistor, even if the voltage on the actual pin ends up being a middling voltage due to this internal pull-down. The internal logic still handles this case at power-up.

Table 6-2. PWM_START0/1 Configuration Pins

PWM_START0	PWM_START1	PWM Duty Cycle (%)
GND	GND	0
GND	Unconnected	30
GND	VCC	40
Unconnected	GND	50
Unconnected	VCC	60
VCC	GND	75
VCC	VCC	100

6.2 Fan Monitoring

6.2.1 Tachometer Signals

The FAN31790 measures fan speed by monitoring a fan's tachometer pulse output. FAN31790 counts the number of internal 8192Hz (fTOSC/4) clock cycles that occur during a selectable number of tachometer periods (1, 2, 4, 8, 16, or 32 periods), with measurements updated once per second. The Speed Range bits (7:5 in the Fan Dynamics registers 08h-0Dh) select how many tachometer periods to count, allowing optimization for different fan speed ranges. The resulting TACH Count (stored in registers 18h-2Fh) is an 11-bit value that directly correlates to RPM using the formula: RPM = (60 × NP × SR × 8192) / TACH Count, where NP is the number of tachometer pulses per revolution and SR is the Speed Range which selects the number of periods to measure. Tachometer pulses shorter than $t_{TACHMIN}$ are automatically rejected to minimize noise susceptibility on the tachometer lines.

6.2.2 PWM Outputs as Tachometer Inputs

The FAN31790 provides flexibility by allowing any of the six PWM outputs to be reconfigured as additional tachometer inputs. The PWM/TACH bit (0 in the Fan Configuration registers 02h-07h) selects whether a channel operates as a PWM output (0) or TACH input (1). When configured as a TACH input, the PWM output becomes a tachometer channel numbered as the original PWM channel plus six (e.g., PWMOUT1 becomes TACH7). All tachometer settings for the original channel, including speed range, locked rotor configuration, and TACH input enable, apply to the reconfigured PWM/TACH pin. This allows up to 12 total tachometer inputs: six dedicated TACH pins plus up to six PWM outputs converted to TACH, enabling monitoring of up to 12 fans.

6.3 Fan Faults and Failures

When enabled, the FAN31790 continuously monitors tachometer signals to detect when a fan has stopped spinning or is running abnormally. The device can detect fan failures in three distinct ways depending on the control mode (PWM mode, RPM mode, or locked rotor mode). Once a fault condition is detected, it is counted in a fault queue and the host can configure whether 1, 2, 4, or 6 consecutive fault detections are required before the fan is declared failed. After the selected number of consecutive faults occur, the $\overline{\text{FAN\_FAIL}}$ output asserts (unless masked) and the fault bit is set in the Fan Fault Status registers (10h, 11h). The failed condition persists until the host clears it by writing a new value to either the PWM Target Duty Cycle or TACH Target Count register for that fan.

6.3.1 PWM Mode Failure Detection

In PWM mode, the host sets a maximum allowable tachometer count in the TACH Target Count register. If the actual TACH Count exceeds this limit (indicating the fan is running too slowly), a fault is detected. The comparison occurs once per second; if the subsequent measurement also exceeds the limit, and the Fan Fault Queue is set to 1, the fan is marked failed. When a PWM output is used as a TACH input, the same PWM-mode failure mode applies. Failure detection is masked when the PWM target duty cycle is set to 0%.

6.3.2 RPM Mode Failure Detection

In RPM mode, the device will detect three fault conditions:

1. TACH count exceeds the TACH Target Count while PWM duty cycle is 100% (fan not reaching commanded speed at full drive)
2. TACH count exceeds twice the TACH Target Count while duty cycle is less than 100% (fan running dangerously slow)
3. TACH count reaches maximum value 7FFh (indicates sensor failure or absence).

IN RPM mode, Failure detection is masked when TACH Target Count is set to full scale.

6.3.3 Locked Rotor Mode Failure Detection

Some fans include a dedicated locked rotor output signal. By setting the TACH/Locked Rotor bit (2 in the Fan Configuration registers) and selecting polarity (Locked Rotor Polarity bit 1), the device monitors this signal and declares a fan failed if the locked rotor condition persists for 1 second.

6.3.4 Failure Indication

Fan failure status is reported through two mechanisms. First, individual fault bits are set in the Fan Fault Status registers. These bits latch once a fault is detected and remain set until the host clears them by writing a new PWM or TACH target value to the affected channel. Writing new values will cause the fault to be checked again and updated after a second. Secondly, the $\overline{\text{FAN\_FAIL}}$ open-drain pin is pulled low when any unmasked fan fault occurs.

Specific faults can be masked using the Fan Fault Mask registers, preventing certain fans from triggering the $\overline{\text{FAN\_FAIL}}$ output while still logging fault status. Additionally, the Failed Fan Options bits (3:2 in the Failed Fan Options/Sequential Start register 14h) control what happens to the PWM output when a failure is detected: the duty cycle can be forced to 0%, remain at current value, forced to 100%, or all fans can be forced to 100% on any unmasked failure.

6.4 I²C Interface

6.4.1 I2C Addresses and ADDRx Pins

The FAN31790's I2C address is determined by the state of the ADD0 and ADD1 address pins at the start of every I2C transaction on the I2C bus. The ADD0 and ADD1 pins can be connected to GND, VCC, SDA, or SCL. These pins allow up to 16 FAN31790 to reside on the same I2C bus. See the table bellow for a complete list of all 16 I2C address possibilities and the corresponding ADD0 and ADD1 pin connections. For example, FAN31790's address is 20h when ADD0 and ADD1 pins are grounded at power up.

The I2C addresses are also written down below as an "Address Byte" which is just the 7-bit address left shift one bit to leave a bit for the R/W bit.

Table 6-3. FAN31790 Address Table

ADD1 Connection	AAD0 Connection	FAN31790 I2C Address	FAN31790 "Address Byte"
GND	GND	0x20	0x40
GND	SCL	0x21	0x42
GND	SDA	0x22	0x44
GND	VCC	0x23	0x46
SCL	GND	0x24	0x48
SCL	SCL	0x25	0x4A
SCL	SDA	0x26	0x4C
SCL	VCC	0x27	0x4E
SDA	GND	0x28	0x50
SDA	SCL	0x29	0x52
SDA	SDA	0x2A	0x54
SDA	VCC	0x2B	0x56
VCC	GND	0x2C	0x58
VCC	SCL	0x2D	0x5A
VCC	SDA	0x2E	0x5C
VCC	VCC	0x2F	0x5E

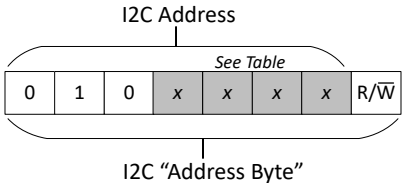


Figure 6-1. FAN31790 I2C Target Address

6.4.2 I2C Command Structure

Device Memory Address

During an I2C write operation to the FAN31790, the controller must transmit a memory address to identify the memory location where the FAN31790 is to store the data. The memory address is always the second byte transmitted during a write operation following the FAN31790 address byte.

Writing To and Reading From the Registers and Memory

To write a single byte to the FAN31790, the controller must generate a START condition, write the address byte (R/W = 0), write the memory address, write the byte of data, and generate a STOP condition. The controller must read theFAN31790's acknowledgment during all byte write operations. This method can be used to write in the register/memory of the FAN31790.

Unlike the write operation that uses the specified memory address byte to define where the data is to be written, the read operation occurs at the present value of the memory address counter. To read a single byte from the FAN31790, the controller generates a START condition, writes the address byte with R/W =1, reads the data byte with a NACK to indicate the end of the transfer, and generates a STOP condition. However, since requiring the controller to keep track of the memory address counter is impractical, the following method should be used to perform reads from a specified memory location. From here, the controller can manipulate the Address Counter for Reads by forcing the address counter to a particular value. To do this, the controller generates a START condition, writes the address byte (R/W = 0), writes the memory address where it desires to read, generates a repeated START condition, writes the address byte (R/W = 1), reads data with ACK or NACK as applicable, and generates a STOP condition. Recall that the controller must NACK the last byte to inform the FAN31790 that no additional bytes are to be read.

Finally, if the controller wants to read multiple bytes from the FAN31790, the controller simply ACKs the data byte if it desires to read another byte before terminating the transaction. After the FAN31790 reads the last byte, it must NACK to indicate the end of the transfer and generate a STOP condition.

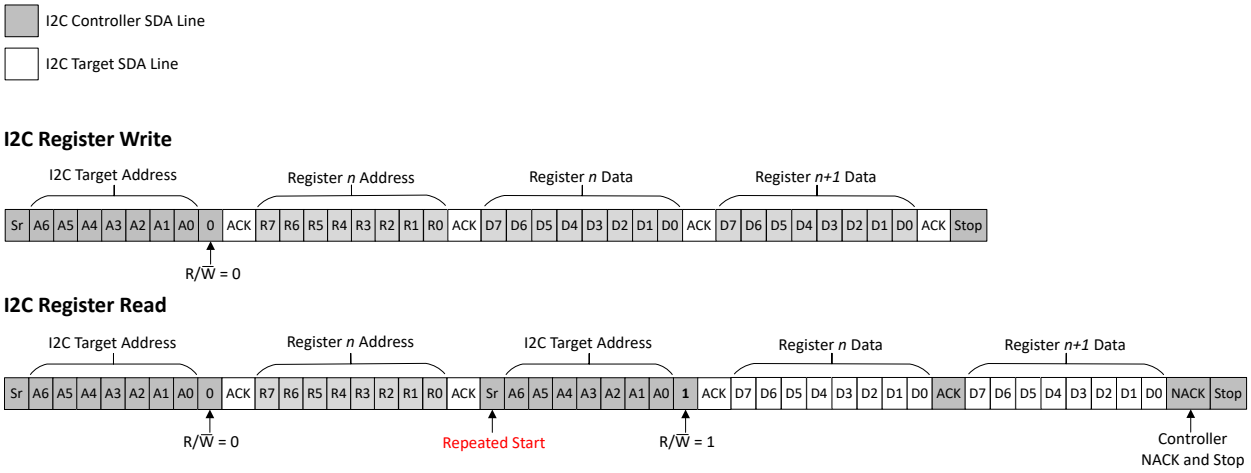


Figure 6-2. FAN31790 I2C Register Interface

7 Register Map

All registers are 8 bits (1 byte) each but they are also grouped into pages of 8 registers per page. The I2C controller can read or write single bytes or consecutive bytes. When writing consecutive register bytes, they must all be on the same page. If the final register on a page is reached and another byte is written, then the register address pointer will loop back to the start of the page and the byte will be written to the first register on that page.

Consecutive reads are not limited to a single page. A continuous read can will continue all the way until the end of the register map. After the last register in the register map, a continuous read will return 0xFF until the address reaches FFh. It will then loop back up to 0x00 at the top of the register map.

Some registers default reset states are configured by hardware input pins at power up. These register reset values are marked with an X. All User Byte registers are just general-purpose volatile memory.

Table 7-1. Register Map

ADDR	NAME	R/W	RESET	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
GLOBAL CONFIGURATION REGISTERS											
Memory Page 0											
00h	Global Configuration	R/W	0010 0XX0b	Run/ Standby 0 = Run 1 = Standby	Reset: 0 = Normal 1 = Reset	Bus Timeout 0 = Enabled	RESERVED	OSC: 0 = Internal oscillator 1 = External crystal	I2C Watchdog: 00b = Disabled 01b = 5s 10b = 10s 11b = 30s		I2C Watchdog Status 1 = Watchdog fault detected
01h	PWM Frequency	R/W	FREQ_START	PWM4-PWM6 Frequency: 0000b = 25Hz 0001b = 30Hz (FREQ_START = GND) 0010b = 35Hz 0011b = 100Hz 0100b = 125Hz 0101b = 149.7Hz 0110b = 1.25kHz 0111b = 1.47kHz (FREQ_START = Floating) 1000b = 3.57kHz 1001b = 5kHz 1010b = 12.5kHz 1011b = 25kHz (FREQ_START = VCC)				PWM1-PWM3 Frequency: 0000b = 25Hz 0001b = 30Hz (FREQ_START = GND) 0010b = 35Hz 0011b = 100Hz 0100b = 125Hz 0101b = 149.7Hz 0110b = 1.25kHz 0111b = 1.47kHz (FREQ_START = Floating) 1000b = 3.57kHz 1001b = 5kHz 1010b = 12.5kHz 1011b = 25kHz (FREQ_START = VCC)		
02h	Fan 1 Configuration	R/W	0XX0 0000b	Mode: 0 = PWM 1 = RPM	Spin-Up 00b = No Spin-up 01b = 2 TACH counts or 0.5s 10b = 2 TACH counts or 1s 11b = 2 TACH counts or 2s		Control/ Monitor 0 = Control 1 = Monitor only	TACH Input Enable 1 = Enabled	TACH/ Locked Rotor 0 = TACH 1 = Locked Rotor	Locked Rotor Polarity 0 = Low 1 = High	PWM/ TACH 0 = PWM 1 = TACH
03h	Fan 2 Configuration	R/W	0XX0 0000b	Same as Fan 1 Configuration							
04h	Fan 3 Configuration	R/W	0XX0 0000b	Same as Fan 1 Configuration							
05h	Fan 4 Configuration	R/W	0XX0 0000b	Same as Fan 1 Configuration							
06h	Fan 5 Configuration	R/W	0XX0 0000b	Same as Fan 1 Configuration							
07h	Fan 6 Configuration	R/W	0XX0 0000b	Same as Fan 1 Configuration							
Memory Page 1											
08h	Fan 1 Dynamics	R/W	0100 1100b	Speed Range (TACH Periods Counted) 000b = 1 001b = 2 010b = 4 (default) 011b = 8 100b = 16 101b = 32 110b = 32 111b = 32			PWM Rate-of-Change: 000b = 0ms per LSB (PWM) 000b = 0.9765ms per LSB (RPM) 001b = 1.953125ms per LSB 010b = 3.90625ms per LSB 011b = 7.8125ms per LSB (default) 100b = 15.625ms per LSB 101b = 31.25ms per LSB 110b = 62.5ms per LSB 111b = 125ms per LSB		Asymmetric Rate of Change 1 = Enabled	RESERVED

Table 7-1. Register Map (continued)

ADDR	NAME	R/W	RESET	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
09h	Fan 2 Dynamics	R/W	0100 1100b	Same as Fan 1 Dynamics							
0Ah	Fan 3 Dynamics	R/W	0100 1100b	Same as Fan 1 Dynamics							
0Bh	Fan 4 Dynamics	R/W	0100 1100b	Same as Fan 1 Dynamics							
0Ch	Fan 5 Dynamics	R/W	0100 1100b	Same as Fan 1 Dynamics							
0Dh	Fan 6 Dynamics	R/W	0100 1100b	Same as Fan 1 Dynamics							
0Eh	User Byte	R/W	0000 0000b								
0Fh	User Byte	R/W	0000 0000b								
FAN FAULT REGISTERS				**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
Memory Page 2											
10h	Fan Fault Status 2	R	0000 0000b	RESERVED	RESERVED	Fan 12 Fault 1 = Fault	Fan 11 Fault 1 = Fault	Fan 10 Fault 1 = Fault	Fan 9 Fault 1 = Fault	Fan 8 Fault 1 = Fault	Fan 7 Fault 1 = Fault
11h	Fan Fault Status 1	R	0000 0000b	RESERVED	RESERVED	Fan 6 Fault 1 = Fault	Fan 5 Fault 1 = Fault	Fan 4 Fault 1 = Fault	Fan 3 Fault 1 = Fault	Fan 2 Fault 1 = Fault	Fan 1 Fault 1 = Fault
12h	Fan Fault Mask 2	R/W	0011 1111b	RESERVED	RESERVED	Fan 12 Mask 1 = Masked	Fan 11 Mask 1 = Masked	Fan 10 Mask 1 = Masked	Fan 9 Mask 1 = Masked	Fan 8 Mask 1 = Masked	Fan 7 Mask 1 = Masked
13h	Fan Fault Mask 1	R/W	0011 1111b	RESERVED	RESERVED	Fan 6 Mask 1 = Masked	Fan 5 Mask 1 = Masked	Fan 4 Mask 1 = Masked	Fan 3 Mask 1 = Masked	Fan 2 Mask 1 = Masked	Fan 1 Mask 1 = Masked
14h	Failed Fan Options/ Sequential Start	R/W	0100 0101b	Sequential Start Delay 000b = 0s 001b = 250ms 010b = 500ms 011b = 1s 100b = 2s 101b, 110b, 111b = 4s			RESERVED	Failed Fan Options 00b = duty cycle = 0% on fail 01b = Continue PWM or RPM mode operation on fail. 10b = duty cycle = 100% on fail 11b = All fans to 100% on any unmasked fan failure.		Fan Faut Queue 00b = 1 fault 01b = 2 faults 10b = 4 faults 11b = 6 faults	
15h	User Byte	R/W	0000 0000b								
16h	User Byte	R/W	0000 0000b								
17h	User Byte	R/W	0000 0000b								

Table 7-2. Register Map Continued

ADDR	NAME		R/W	RESET	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TACH AND PWM STATUS REGISTERS												
Memory Page 3												
18h	TACH 1 Count	MSB	R	1111 1111b	DATA							
19h		LSB	R	1110 0000b	DATA			R-0h				
1Ah	TACH 2 Count	MSB	R	1111 1111b	Same as TACH 1 Count							
1Bh		LSB	R	1110 0000b								
1Ch	TACH 3 Count	MSB	R	1111 1111b	Same as TACH 1 Count							
1Dh		LSB	R	1110 0000b								

Table 7-2. Register Map Continued (continued)

ADDR	NAME		R/W	RESET	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
1Eh	TACH 4 Count	MSB	R	1111 1111b	Same as TACH 1 Count							
1Fh		LSB	R	1110 0000b								
Memory Page 4												
20h	TACH 5 Count	MSB	R	1111 1111b	Same as TACH 1 Count							
21h		LSB	R	1110 0000b								
22h	TACH 6 Count	MSB	R	1111 1111b	Same as TACH 1 Count							
23h		LSB	R	1110 0000b								
24h	TACH 7 Count	MSB	R	1111 1111b	Same as TACH 1 Count							
25h		LSB	R	1110 0000b								
26h	TACH 8 Count	MSB	R	1111 1111b	Same as TACH 1 Count							
27h		LSB	R	1110 0000b								
Memory Page 5												
28h	TACH 9 Count	MSB	R	1111 1111b	Same as TACH 1 Count							
29h		LSB	R	1110 0000b								
2Ah	TACH 10 Count	MSB	R	1111 1111b	Same as TACH 1 Count							
2Bh		LSB	R	1110 0000b								
2Ch	TACH 11 Count	MSB	R	1111 1111b	Same as TACH 1 Count							
2Dh		LSB	R	1110 0000b								
2Eh	TACH 12 Count	MSB	R	1111 1111b	Same as TACH 1 Count							
2Fh		LSB	R	1110 0000b								
Memory Page 6												
30h	PWMOUT 1 Duty Cycle Status	MSB	R	0000 0000b	DATA							
31h		LSB	R	0000 0000b	DATA	R-0h						
32h	PWMOUT 2 Duty Cycle Status	MSB	R	0000 0000b	Same as PWMOUT 1 Duty Cycle							
33h		LSB	R	0000 0000b								
34h	PWMOUT 3 Duty Cycle Status	MSB	R	0000 0000b	Same as PWMOUT 1 Duty Cycle							
35h		LSB	R	0000 0000b								
36h	PWMOUT 4 Duty Cycle Status	MSB	R	0000 0000b	Same as PWMOUT 1 Duty Cycle							
37h		LSB	R	0000 0000b								
Memory Page 7												
38h	PWMOUT 5 Duty Cycle Status	MSB	R	0000 0000b	Same as PWMOUT 1 Duty Cycle							
39h		LSB	R	0000 0000b								
3Ah	PWMOUT 6 Duty Cycle Status	MSB	R	0000 0000b	Same as PWMOUT 1 Duty Cycle							
3Bh		LSB	R	0000 0000b								
3Ch	RESERVED		R	0000 0000b	R-0h							
3Dh	RESERVED		R	0000 0000b	R-0h							
3Eh	RESERVED		R	0000 0000b	R-0h							
3Fh	RESERVED		R	0000 0000b	R-0h							
PWM DUTY CYCLE CONTROL REGISTERS					**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
Memory Page 8												
40h	PWMOUT1 Target Duty Cycle	MSB	R/W	PWM_START	DATA							
41h		LSB	R/W	PWM_START	DATA	RESERVED						

Table 7-2. Register Map Continued (continued)

ADDR	NAME		R/W	RESET	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
42h	PWMOUT2 Target Duty Cycle	MSB	R/W	PWM_START	Same as PWMOUT 1 Target Duty Cycle							
43h		LSB	R/W	PWM_START								
44h	PWMOUT3 Target Duty Cycle	MSB	R/W	PWM_START	Same as PWMOUT 1 Target Duty Cycle							
45h		LSB	R/W	PWM_START								
46h	PWMOUT4 Target Duty Cycle	MSB	R/W	PWM_START	Same as PWMOUT 1 Target Duty Cycle							
47h		LSB	R/W	PWM_START								
Memory Page 9												
48h	PWMOUT5 Target Duty Cycle	MSB	R/W	PWM_START	Same as PWMOUT 1 Target Duty Cycle							
49h		LSB	R/W	PWM_START								
4Ah	PWMOUT6 Target Duty Cycle	MSB	R/W	PWM_START	Same as PWMOUT 1 Target Duty Cycle							
4Bh		LSB	R/W	PWM_START								
4Ch	User Byte		R/W	0000 0000b								
4Dh	User Byte		R/W	0000 0000b								
4Eh	User Byte		R/W	0000 0000b								
4Fh	User Byte		R/W	0000 0000b								
TACH TARGET COUNT REGISTERS					**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
Memory Page 10												
50h	TACH 1 Target Count	MSB	R/W	0011 1100b	DATA							
51h		LSB	R/W	0000 0000b	DATA			RESERVED				
52h	TACH 2 Target Count	MSB	R/W	0011 1100b	Same as TACH 1 Target Count							
53h		LSB	R/W	0000 0000b								
54h	TACH 3 Target Count	MSB	R/W	0011 1100b	Same as TACH 1 Target Count							
55h		LSB	R/W	0000 0000b								
56h	TACH 4 Target Count	MSB	R/W	0011 1100b	Same as TACH 1 Target Count							
57h		LSB	R/W	0000 0000b								
Memory Page 11												
58h	TACH 5 Target Count	MSB	R/W	0011 1100b	Same as TACH 1 Target Count							
59h		LSB	R/W	0000 0000b								
5Ah	TACH 6 Target Count	MSB	R/W	0011 1100b	Same as TACH 1 Target Count							
5Bh		LSB	R/W	0000 0000b								
5Ch	User Byte		R/W	0000 0000b								
5Dh	User Byte		R/W	0000 0000b								
5Eh	User Byte		R/W	0000 0000b								
5Fh	User Byte		R/W	0000 0000b								
WINDOW REGISTERS					**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
Memory Page 12												
60h	Window 1		R/W	0000 0000b	DATA							
61h	Window 2		R/W	0000 0000b	Same as Window 1							
62h	Window 3		R/W	0000 0000b	Same as Window 1							
63h	Window 4		R/W	0000 0000b	Same as Window 1							
64h	Window 5		R/W	0000 0000b	Same as Window 1							
65h	Window 6		R/W	0000 0000b	Same as Window 1							
66h	User Byte		R/W	0000 0000b								

Table 7-2. Register Map Continued (continued)

ADDR	NAME	R/W	RESET	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
67h	User Byte	R/W	0000 0000b								
DEVICE REVISION REGISTERS				**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
Memory Page 13											
68h	Device Major Revision	R	0000 0001b	Initial Major Revision = 0x01							
69h	Device Minor Revision	R	0000 0000b	Initial Minor Revision = 0x00							
6Ah	Device ID	R	0000 0000b	Device Identifiers. 0x00 = FAN31790							

8 Register Descriptions

Register Map lists the memory-mapped registers for the FAN31790.

Complex bit access types are encoded to fit into small table cells. Table 8-1 shows the codes that are used for access types in this section.

Table 8-1. Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.1 Global Configuration Registers

8.1.1 Global Configuration Register (Address = 00h) [Reset = 0010 0xx0b]

Global Configuration Register is shown in Figure 8-1 and described in Table 8-2.

Return to the Register Map.

Register to control register actions

Figure 8-1. Global Configuration Register

7	6	5	4	3	2	1	0
$\overline{\text{RUN}}$ / Standby	Reset	Bus Timeout	RESERVED	OSC	I2C Watchdog		I2C Watchdog Status
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h

Table 8-2. Global Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
7	$\overline{\text{RUN}}$/Standby	R/W	0b	Places device in standby mode. Entering standby mode sets all PWM duty cycles to 0 and stops fan failure detection. However, driving the $\overline{\text{FULL\_SPEED}}$ input low forces all enabled PWMOUT outputs high (100% duty cycle) regardless of the state of the Run bit. 0h = Run 0h = Standby
6	Reset	R/W	0b	Resets fan controller. This bit automatically resets itself and always returns a 0 when read. 0h = Normal operation 1h = Reset all registers to POR value
5	Bus Timeout	R/W	0b	I2C bus timeout. The I2C interface resets if SDA is low for more than 35ms 0h = Enabled 1h = Disabled
4	RESERVED	R/W	0b	
3	OSC	R/W	0b	Selects oscillator Source between the built in oscillator or external 32.768kHz crystal/ ceramic resonator. Used for TACH count and sourcing the CLKOUT pin. Use crystal or ceramic resonator if higher accuracy is required. When switching from the internal oscillator to an external crystal, the device operates from the internal oscillator until the crystal oscillator has started up. If the crystal is damaged or the oscillator fails to start, the device continues to operate from the internal oscillator. 0h = Internal oscillator (default at power-on) 1h = External 32.768kHz crystal

Table 8-2. Global Configuration Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-1	I2C Watchdog	R/W	WD_START pin	Watchdog configuratation. When enabled, WDT is restarted by valid I2C Transactions. If there are not valid transactions between the host and the fan controller withing the watchdog period, all fan PWMs outputs will go to 100%. If a valid I2C transaction happens after a WDT timeout, the fan controller returns to it's previous configuration. Make sure the host communicates with the fan controller periodically to avoid WDT intervention. Watchdog behavor at power up is controlled by the WD_START pin. 00h = Disabled (default if WD_START = GND) 01h = 5s timeout period 10h = 10s timeout period 11h = 30s timeout period (default if WD_START = VCC)
0	I2C Watchdog Status	R/W	0b	Current status of the Watchdog Timer. Clear this bit by writing a 0 to it. 0h = Watchdog not active / I2C transactions have occurred within the watchdog period. 1h = Watchdog triggered. Time between I2C transactions has been exceeded.

8.1.2 PWM Frequency Register (Address = 01h) [Reset = 08h]

PWM Frequency Register is shown in Figure 8-2 and described in Table 8-3.

Return to the Register Map.

Register to control the bridge

Figure 8-2. PWM Frequency Register

7	6	5	4	3	2	1	0
PWM4-PWM6 Frequency				PWM1-PWM3 Frequency			
R/W - xxxx b				R/W - xxxx b			

Table 8-3. PWM Frequency Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	PWM4-PWM6 Frequency	R/W	FREQ_START	PWM4-PWM6 Frequency: 0000b = 25Hz 0001b = 30Hz (FREQ_START = GND) 0010b = 35Hz 0011b = 100Hz 0100b = 125Hz 0101b = 149.7Hz 0110b = 1.25kHz 0111b = 1.47kHz (FREQ_START = Floating) 1000b = 3.57kHz 1001b = 5kHz 1010b = 12.5kHz 1011b = 25kHz (FREQ_START = VCC)

Table 8-3. PWM Frequency Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	PWM1-PWM3 Frequency	R/W	FREQ_START	PWM1-PWM3 Frequency: 0000b = 25Hz 0001b = 30Hz (FREQ_START = GND) 0010b = 35Hz 0011b = 100Hz 0100b = 125Hz 0101b = 149.7Hz 0110b = 1.25kHz 0111b = 1.47kHz (FREQ_START = Floating) 1000b = 3.57kHz 1001b = 5kHz 1010b = 12.5kHz 1011b = 25kHz (FREQ_START = VCC)

8.1.3 Fan X Configuration Register (Address = 02h-07h) [Reset = 0xx0 0000b]

Fan X Configuration Register is shown in Figure 8-3 and described in Table 8-4.

Return to the Register Map.

Register duplicated to configure each of the 1-6 Fans

Figure 8-3. Fan X Configuration Register

7	6	5	4	3	2	1	0
Mode	Spin-up		$\overline{\text{Control}}$/Monitor	TACH Input Enable	TACH/Locked Rotor Polarity	Locked Rotor Polarity	PWM/TACH
R/W-0b	R/W-xxb		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-4. Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Mode	R/W	0b	Selects either PWM or RPM Mode. PWM Duty cycle is set by the value in the associated PWMOUT Target Duty Cycle register. In RPM mode, the PWM Duty cycle is adjusted to produce the TACH count value in the associated TACH Target Count Register. When changing from PWM to RPM mode, if the current RPM value is different from the value selected in the TACH Target Count register, the PWM duty cycle starts from the current value and increment/decrements toward the desired value at the selected duty cycle rate-of-change. 0 = PWM Mode 1 = RPM Mode
6-5	Spin-up	R/W	SPIN_START pin	Spin-up is when a fan is first started, it's PWM duty cycle goes to 100% for a selectable period or time or until 2 TACH pulses have been detected. This is to help the fan get through it's initial start-up phase. After Spin-up, the duty cycle goes to the value in the PWMOUT Target Duty Cycle register. The Reset state for Spin-up is set at power-up by the state of the SPIN_START pin. 00b = No Spin-up (SPIN_START = GND) 01b = 2 TACH counts or 0.5s (SPIN_START = Unconnected) 10b = 2 TACH counts or 1s (SPIN_START = VCC) 11b = 2 TACH counts or 2s
4	Control/Monitor	R/W	0b	0 = Control fan speed 1 = Monitor only. Associated duty cycle = 0% regardless of other settings; monitor associated TACH or locked rotor if enabled by bit 3.
3	TACH Input Enable	R/W	0b	Enables associated TACH input function and fan fault detection (automatically enabled in RPM mode). When disabled and TACH input is not used, bits 1 and 2 are ignored. 0 = Disabled 1 = Enabled

Table 8-4. Configuration Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	TACH/Locked Rotor Polarity	R/W	0b	Selects TACH input function as TACH count or locked rotor. In locked rotor mode, assertion of the associated TACH input indicates that the fan has stopped. 0 = TACH 1 = Locked Rotor
1	Locked Rotor Polarity	R/W	0b	Associated TACH input either low or high in locked rotor mode indicates fan is stopped. 0 = Low 1 = High
0	PWM/TACH Mode	R/W	0b	Chooses between PWM and TACH modes. In PWM mode, associated PWMOUT produces a PWM waveform for control of fan speeds. In TACH mode, associated PWMOUT becomes a TACH input whose channel number is equal to the number of the PWMOUT channel plus six. 0 = PWM 1 = TACH

8.1.4 Fan X Dynamics Register (Address = 08h - 0Dh) [Reset = 0100 1100b]

Fan X Dynamics Register is shown in Figure 8-4 and described in Table 8-5.

Return to the Register Map.

Register to configure the fan speed control, such as PWM rate of change and time period for TACH measurements. The tables bellow describe in detail the functionality of the Table 8-6 and Table 8-7 bits:

Figure 8-4. Fan X Dynamics Register

7	6	5	4	3	2	1	0
Speed Range			PWM Rate-of-change			Asymmetric Rate of Change	Reserved
R-010b			R/W-011b			R/W-0b	R/W-0b

Table 8-5. Fan X Dynamics Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Speed Range	R/W	010b	The device determines fan speed by counting the number of internal 8192Hz (fTOSC/4) clock cycles (using an 11-bit counter) during one or more fan tachometer periods. Three bits set the nominal RPM range for the fan, as shown in the table below. For example, a setting of 010b causes the device to count the number of 8192Hz (fTOSC/4) clock cycles that occur during four complete tachometer periods. If the fan has a nominal speed of 2000 RPM and two tachometer pulses per revolution, one tachometer period is nominally 15ms, and four tachometer periods are 60ms. With an 8192Hz (fTOSC/4) clock, the TACH count is therefore equal to 491. With a fan speed of 1/3 the nominal value, the count is 1474. If the fan's nominal speed is 1000 RPM, the fullspeed TACH count is 983. At 1/3 the nominal speed, there are 2948 clock cycles in four tachometer periods. This is greater than the maximum 11-bit count of 2047, so four tachometer periods is too many for this fan; a setting of 001 (two clock cycles) is recommended instead. The table below shows the full-speed tachometer counts for several combinations of nominal fan speeds and bits 7:5 settings. The shaded combinations provide the best results. Nonshaded combinations should generally be avoided. When setting bits 7:5, the goal is to obtain the highest tachometer count without exceeding the maximum count of 2047 when the fan is at the minimum speed of interest. For example, if the minimum speed of interest is 1/3 of full speed, the maximum tachometer count is three times the value shown in the table.

Table 8-5. Fan X Dynamics Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-2	PWM Rate-of-Change	R/W	011b	Sets the PWM Duty cycle rate of change. The PWM duty cycle at the associated PWMOUT outputs varies from 0 to full scale in 512 increments. The rate-of-change bits determine the time interval between duty cycle output increments/decrements. Regardless of the settings, there are a few cases for which the rate-of-change is always 0: In RPM mode, when a TACH target count of 2047 (7FFh) is selected, the duty cycle immediately goes to 0%. A full-scale target count is assumed to mean that the intent is to shut down the fan, and going directly to 0% avoids the possibility of loss of control-loop feedback at high TACH counts. If a slow-speed decrease toward 0% is desired, select a TACH target count at the slowest practical value for the fan. Once that count has been reached, selecting a count of 2047 (7FF) then takes the drive immediately to 0%. In PWM mode, when a target duty cycle of 0% is selected, the duty cycle goes to 0%. Again, it is assumed that the intent is to shut down the fan. If a slow-speed decrease toward 0% is desired, a target duty cycle of the slowest practical value for the fan in question should be chosen. Once that duty cycle has been reached, selecting a target value of 0% then takes the drive immediately to 0%. When the current duty cycle is 0% in PWM mode, selecting a new target duty cycle immediately takes the duty cycle to that value. The fan spins up first if spin-up is enabled. When the current duty cycle is 0% in RPM mode, selecting a new TACH target count that is less than 2047 (7FFh) immediately takes the duty cycle to the value in the PWMOUT Target Duty Cycle register. From this value, the duty cycle increments as needed to achieve the desired TACH target count. The fan spins up first if spin-up is enabled.
1	Asymmetric Rate of Change	R/W	0h	0 = Same rate of change whether duty cycle is increasing or decreasing. 1 = Rate of change when duty cycle is decreasing is half the rate when increasing.
0	Reserved	R/W	0h	RESERVED

Table 8-6. Speed Range

BITS 7:5	NUMBER OF TACH PERIODS COUNTED	RPM					
		500	1000	2000	4000	8000	16000
000b	1	**491 (60ms)**	245 (30ms)	122 (15ms)	61 (7.5ms)	30 (3.75ms)	15 (1.87ms)
001b	2	**983 (120ms)**	**491 (60ms)**	245 (30ms)	122 (15ms)	61 (7.5ms)	30 (3.75ms)
010b (default)	4	**1966 (240ms)**	**983 (120ms)**	**491 (60ms)**	245 (30ms)	122 (15ms)	61 (7.5ms)
011b	8	2047 (480ms)	**1966 (240ms)**	**983 (120ms)**	**491 (60ms)**	245 (30ms)	122 (15ms)
100b	16	2047 (960ms)	2047 (480ms)	**1966 (240ms)**	**983 (120ms)**	**491 (60ms)**	245 (30ms)
101b, 110b, 111b	32	2047 (1920ms)	2047 (960ms)	2047 (480ms)	**1966 (240ms)**	**983 (120ms)**	**491 (60ms)**

Table 8-7. PWM Rate-of-Change Settings

BITS 4:2	TIME BETWEEN DUTY CYCLE INCREMENTS (ms) RPM		TIME FROM 33% TO 100% (s)	
	PWM	RPM	PWM	RPM
000b	0	0.9765	0	0.33
001b	1.95		0.67	
010b	3.91		1.34	

Table 8-7. PWM Rate-of-Change Settings (continued)

BITS 4:2	TIME BETWEEN DUTY CYCLE INCREMENTS (ms) RPM		TIME FROM 33% TO 100% (s)	
	PWM	RPM	PWM	RPM
011b (default)	7.81		2.7	
100b	15.63		5.3	
101b	31.25		10.7	
110b	62.50		21.4	
111b	125.00		42.8	

8.1.5 User Byte Register (Addresses = 0Eh–0Fh, 15h–17h, 4Ch–4Fh, 5Ch–5Fh, 66h–67h) [Reset = 0000 0000b]

User Byte Register is shown in Figure 8-5 and described in Table 8-8.

Return to the Register Map.

User can use this register for their own purposes.

Figure 8-5. User Byte Register

7	6	5	4	3	2	1	0
General-purpose bits							
R/W-0000 0000b							

Table 8-8. User Byte Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	General-purpose bits	R/W	00000000b	Volatile. These bits have no effect on the device operation

8.2 Fan Fault Registers

8.2.1 Fan Fault Status 2 Register (Address = 10h) [Reset = 0000 0000b]

Fan Fault Status 2 Register is shown in Figure 8-6 and described in Table 8-9.

Return to the Register Map.

This register applies only to PWMOUTs that are being used as TACH inputs. The associated fan experienced faults as defined in the Fan Failure section.

Figure 8-6. Fan Fault Status 2 Register

7	6	5	4	3	2	1	0
RESERVED		FAN [12-7] Fault					
R/W-00b		R/W-000000b					

Table 8-9. Fan Fault Status 2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W	00b	RESERVED
5-0	FAN [12-7] Fault	R/W	000000b	The associated fan experienced faults as defined in the Fan Failure section. When a fan fault is detected, the associated fault bit is set to 1. The fault bits latch until they are cleared by writing a PWM target duty cycle or TACH target count to the associate fan's control register, thus allowing short-term faults to be identified.

8.2.2 Fan Fault Status 1 Register (Address = 11h) [Reset =0000 0000b]

Fan Fault Status 1 Register is shown in Figure 8-7 and described in Table 8-10.

Return to the Register Map.

This register applies only to PWMOUTs that are being used as TACH inputs. The associated fan experienced faults as defined in the Fan Failure section.

Figure 8-7. Fan Fault Status 1 Register

7	6	5	4	3	2	1	0
RESERVED		FAN [6-1] Fault					
R/W-00b		R/W-000000b					

Table 8-10. Fan Fault Status 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W	00b	RESERVED
5-0	FAN [6-1] Fault	R/W	000000b	The associated fan experienced faults as defined in the Fan Failure section. When a fan fault is detected, the associated fault bit is set to 1. The fault bits latch until they are cleared by writing a PWM target duty cycle or TACH target count to the fan's control register, thus allowing short-term faults to be identified.

Fan Fault Mask 2 Register (Address = 12h) [Reset = 0011 1111b]

Fan Fault Mask 2 Register is shown in Figure 8-8 and described in Table 8-11 .

Return to the Register Map.

This register applies only to PWMOUTs that are being used as TACH inputs.

Figure 8-8. Fan Fault Mask 2 Register

7	6	5	4	3	2	1	0
RESERVED		FAN [12-7] Mask					
R/W-00b		R/W-111111b					

Table 8-11. Fan Fault Mask 2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W	00b	RESERVED
5-0	FAN [12-7] Mask	R/W	111111b	These bits mask faults on selected fans from asserting the $\overline{\text{FAN\_FAIL}}$ output. Faults are still indicated by the fault status bits. 0 : Not masked. 1 : Masked. (default) When a fan fails, the PWM behavior is controlled by the Failed Fan Options register.

Fan Fault Mask 1 Register (Address = 13h) [Reset = 0011 1111b]

Fan Fault Mask 1 Register is shown in Figure 8-9 and described in Table 8-12.

Return to the Register Map.

Figure 8-9. Fan Fault Mask 1 Register

7	6	5	4	3	2	1	0
RESERVED		FAN [6-1] Mask					
R/W-00b		R/W-111111b					

Table 8-12. Fan Fault Mask 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R/W	00b	RESERVED
5-0	FAN [6-1] Fault		111111b	These bits mask faults on selected fans from asserting the $\overline{\text{FAN\_FAIL}}$ output. Faults are still indicated by the fault status bits. 0 : Not masked. 1 : Masked. (default) When a fan fails, the PWM behavior is controlled by the Failed Fan Options register.

Failed Fan Options/Sequential Start Register (Address = 14h) [Reset =0100 0101b]

Failed Fan Options/Sequential Start Register is shown in Figure 8-10 and described in Table 8-13.

Return to the Register Map.

Figure 8-10. Failed Fan Options/Sequential Start Register

7	6	5	4	3	2	1	0
Sequential Start Delay			Reserved	Failed Fan Options		Fan Fault Queue	
R/W-010b			R/W-0b	R/W-01b		**R/W-01b**	

Table 8-13. Failed Fan Options/Sequential Start Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Sequential Start Delay	R/W	010h	Note that faults are not monitored until the channel is activated after its associated start delay. These bits select the time delay between sequential fan start-ups. 000h : 0s 001h : 250ms 010h : 500ms 011h : 1s 100h : 2s 101b : 4s 110b : 4s 111b : 4s
4	RESERVED		0h	
3-2	Failed Fan Options	R/W	01h	These bits select the duty cycle behavior following a fan failure. 00h : 0% on failed fan 01h : Continue current PWM or RPM mode operation. 10h : 100% on failed fan. 11h : All fans to 100% on any unmasked fan failure
1-0	Fan Fault Queue	R/W	01h	These bits select the number of consecutive fault detections that are required to decide that the fan has failed. When the selected number of fault detections has occurred, the $\overline{\text{FAN\_FAIL}}$ output asserts (if fault detection is not masked for the fan). Note: Fan fault queue bit have no effect on the locked rotor fan failure detection. 00h :1 01h : 2 10h : 4 11h : 6

8.3 TACH and PWM Status Registers

8.3.1 TACH X Count Registers (Addresses = 18h-2Fh) [Reset MSB = FFh & LSB= E0h]

TACH x Count is an 11bit count value that stretches over two registers at a time. They are shown in Figure 8-11 and Figure 8-12 with bits described in Table 8-14.

Return to the Register Map.

TACH 1 Count Registers (18h–19h)	**TACH 5** Count Registers (20h–21h)	**TACH 9** Count Registers (28h–29h)
TACH 2 Count Registers (1Ah–1Bh)	**TACH 6** Count Registers (22h–23h)	**TACH 10** Count Registers (2Ah–2Bh)
TACH 3 Count Registers (1Ch–1Dh)	**TACH 7** Count Registers (24h–25h)	**TACH 11** Count Registers (2Ch–2Dh)
TACH 4 Count Registers (1Eh–1Fh)	**TACH 8** Count Registers (26h–27h)	**TACH 12** Count Registers (2Eh–2Fh)

The TACH Count register consists of 11 bits, left-justified, contained in 2 bytes. Indicates the associated number of 8192Hz clock pulses counted during the counting period.

Figure 8-11. TACH X Count MSB Register

7	6	5	4	3	2	1	0
TACH Count bits 10-3							
R-1111 1111b							

Figure 8-12. TACH X Count LSB Register

7	6	5	4	3	2	1	0
TACH Count bits 2-0			Reserved				
R-111b			R-0 0000b				

Table 8-14. TACH X Count Field Descriptions

Bit	Field	Type	Reset	Description
MSB Register:				Indicates the associated number of 8192Hz (fTOSC/4) clock pulses counted during the counting period. The TACH Count register consists of 11 bits, left-justified, contained in 2 bytes. The lower 5 bits always return zeros. To minimize noise from spurious tachometer transitions, pulses less that tTACHMIN are ignored. The TACH 7 Count to TACH 12 Count registers apply only to PWMOUTs that are being used as TACH inputs.
7-0	TACH Count bits 10-3	R	11111111b	
LSB Register:				
7-5	TACH Count bits 2-0	R	111b	
4-0	Reserved	R	0b	RESERVED

8.3.2 PWMOUT X Duty Cycle Status Registers (Addresses = 30h-3Bh) [Reset MSB = 00h & LSB = 00h]

PWMOUT X Duty Cycle Status Register is shown in Figure 8-13 and Figure 8-14 with bits described in Table 8-15.

Return to the Register Map.

PWMOUT 1 Duty Cycle Status Registers (30h–31h)	**PWMOUT 4** Duty Cycle Status Registers (36h–37h)
PWMOUT 2 Duty Cycle Status Registers (32h–33h)	**PWMOUT 5** Duty Cycle Status Registers (38h–39h)
PWMOUT 3 Duty Cycle Status Registers (34h–35h)	**PWMOUT 6** Duty Cycle Status Registers (3Ah–3Bh)

This is a status only register that shows the the actual current PWM duty cycle for the associate PWM output. This is a 9-bit left-justified value that ranges from 0 to 511 and is contained in 2 bytes.

Figure 8-13. PWMOUT X Duty Cycle Status MSB Register

7	6	5	4	3	2	1	0
PWMOUT Duty Cycle bits 8-1							
R-0000 0000b							

Figure 8-14. PWMOUT X Duty Cycle Status LSB Register

7	6	5	4	3	2	1	0
PWMOUT Duty Cycle bit 0	0	0	0	0	0	0	0
R-0b	R- 000 0000b						

Table 8-15. PWMOUT X Duty Cycle Status Register Field Descriptions

Bit	Field	Type	Reset	Description
MSB Register:				This is a 9-bit left-justified value that ranges from 0 to 511 and is contained in 2 bytes. This register shows the actual PWM duty cycle for the associate PWM output. When the value is 511 (decimal), the duty cycle is 100%. The 6:1 bits always return zeros. Register does not apply when associated PWMOUTs are being used as TACH inputs. The register value is converted to the duty cycle at the fan.
7-0	PWMOUT Duty Cycle bits 8-1	R	00000000b	
LSB Register:				
7	PWMOUT Duty Cycle bit 0	R	0b	
6-0	RESERVED	R	0000 000b	Always return 0

8.4 PWM Duty Cycle Control Registers

8.4.1 PWMOUT x Target Duty Cycle (Register Addresses = 40h-4Bh) [Reset MSB = XXXX XXXXb & LSB= X000 0000b]

PWMOUT X Target Duty Cycle Register is shown in Figure 8-15 and described in Table 8-16.

Return to the Register Map.

PWMOUT 1 Target Duty Cycle Registers (40h–41h)	**PWMOUT 4** Target Duty Cycle Registers (46h–47h)
PWMOUT 2 Target Duty Cycle Registers (42h–43h)	**PWMOUT 5** Target Duty Cycle Registers (48h–49h)
PWMOUT 3 Target Duty Cycle Registers (44h–45h)	**PWMOUT 6** Target Duty Cycle Registers (4Ah–4Bh)

This is a 9-bit left-justified value that ranges from 0 to 511 and is contained in 2 bytes.

Figure 8-15. PWMOUT x Target Duty Cycle Register

7	6	5	4	3	2	1	0
PWMOUT Target Duty Cycle bits 8-1							
R/W-xxxx xxxxb							

Figure 8-16. PWMOUT x Target Duty Cycle Register

7	6	5	4	3	2	1	0
PWMOUT Target Duty Cycle bit 0	Reserved						
R/W-xb	R/W- 000 0000b						

Table 8-16. PWMOUT x Target Duty Cycle Field Descriptions

Bit	Field	Type	Reset	Description
MSB Register:				This is a 9-bit left-justified value that ranges from 0 to 511 and is contained in 2 bytes. In PWM mode, write the desired PWM duty cycle to these two registers. The device then increments the duty cycle to this value at a rate determined by the PWM duty cycle rate-of-change bits. In RPM mode, the value contained in this register is the duty cycle at PWMOUT immediately after spin-up or after changing the TACH target count from 2047 (7FF) to any value lower than 2047 (7FF). For example, if the fan is currently stopped with spin-up disabled, and a new TACH target count corresponding to 60% of the full-scale fan speed is to be selected, the duty cycle can be programmed to immediately go to 60% when the new TACH target count is selected, and then close the RPM control loop starting from that duty cycle. The register value is converted to the duty cycle at the fan.
7-0	PWMOUT Target Duty Cycle bits 8-1	R/W	PWM_START1 and PWM_START0	
LSB Register:				
7	PWMOUT Target Duty Cycle bit 0	R/W	PWM_START1 and PWM_START0	
6-0	RESERVED	R/W	0000000b	Always return 0

Target duty cycle at POR depends on the state of the PWM_START0 and PWM_START1 inputs as follows:

Table 8-17. PWMOUT Target Duty Cycle PWM_STARTx Pin Settings

POR CONDITION		PWM Duty Cycle (%)
PWM_START0	PWM_START1	
GND	GND	0
GND	Unconnected	30
GND	VCC	40
Unconnected	GND	50
Unconnected	VCC	60
VCC	GND	75
VCC	VCC	100

8.5 TACH Target Count Registers

8.5.1 TACH x Target Count Registers (Register Addresses = 50h-5Bh) [Reset MSB = 3Ch & LSB= 00h]

TACH X Target Count Register is shown in Figure 8-17 and Figure 8-18 with bits described in Table 8-18.

Return to the Register Map.

TACH 1 Target Count Registers (50h–51h)	**TACH 4** Target Count Registers (56h–57h)
TACH 2 Target Count Registers (52h–53h)	**TACH 5** Target Count Registers (58h–59h)
TACH 3 Target Count Registers (54h–55h)	**TACH 6** Target Count Registers (5Ah–5Bh)

This is an 11-bit left-justified value that is contained in 2 bytes. It indicates the desired number of 8192Hz clock pulses counted during the counting period.

Figure 8-17. TACH x Target Count MSB Register

7	6	5	4	3	2	1	0
TACH Target Count bits 10-3							
R/W-0011 1100b							

Figure 8-18. TACH x Target Count LSB Register

7	6	5	4	3	2	1	0
TACH Target Count bits 2-0			Reserved				

Figure 8-18. TACH x Target Count LSB Register (continued)

7	6	5	4	3	2	1	0
R/W-000b				R/W-00 0000b			

Table 8-18. TACH x Target Count Field Descriptions

Bit	Field	Type	Reset	Description
MSB Register:				This is an 11-bit left-justified value that is contained in 2 bytes. It indicates the desired number of 8192Hz clock pulses counted during the counting period. In RPM mode, write the desired tachometer count to this register. The device then adjusts the associated PWM duty cycle to achieve this tachometer count. In PWM mode, this register is not used as part of the fan control algorithm. In both PWM and RPM modes, this register is used to determine fan faults. See the Fan Faults register description for details. When changing from PWM mode to RPM mode, best results are obtained by loading this register with the current TACH count before changing to RPM mode. The TACH target count for a given RPM is obtained by the following equation: TACH Count = (60 / NP x RPM) x SR x 8192 where: NP = number of TACH pulse per revolution SR = 1, 2, 4, 8, 16, 32 (see the Speed Range bit information in the associated Fan Dynamics register)
7-0	TACH Target Count bits 10-3	R/W	00111100b	
LSB Register:				
7-5	TACH Target Count bits 2-0	R/W	000b	
4-0	RESERVED	R/W	00000b	Always return 0

8.6 Window Registers

8.6.1 Window X Register (Addresses = 60h-65h) [Reset = 00h]

Window X Register is shown in Figure 8-19 and described in Table 8-19.

Return to the Register Map.

Window 1 Register Address = 60h	**Window 4** Register Address = 63h
Window 2 Register Address = 61h	**Window 5** Register Address = 64h
Window 3 Register Address = 62h	**Window 6** Register Address = 65h

Used in RPM mode only. These registers set the size of the window around the target TACH count value when the PWM rate of change is slowed to 1 LSB from it's current step size.

Figure 8-19. Window X Register

7	6	5	4	3	2	1	0
Window size in TACH counts							
R/W-0000 0000b							

s

Table 8-19. Window X Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Window size in TACH counts	R/W	00000000b	When the fan's speed is near the target speed in RPM mode—that is, when the TACH count is near the corresponding TACH target count—the control loop dynamics can often be improved by slowing the rate of change of the PWM duty cycle. This operates as follows: First, set a value for the count "window" and store it in the appropriate window register. In RPM mode, calculate the difference between the current TACH count and the target TACH count. If the absolute value of this difference is less than the value in the window register, then the update rate of the PWM duty cycle is slowed to 1 LSB per second. When the current TACH count falls outside of the window, the duty cycle rate of change reverts to the selected value. Note: When operating in PWM mode, the window value is typically set to 0.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Typical Application

9.1.1 Schematic

TI recommends connecting C_{VDD} between VDD/VSS as close to the device pins as possible. It should be a low-ESR capacitor with a tolerance of±20% or better is required. A single 0.1uF cap is all that is required, but larger caps or more caps may also be used.

$\overline{\text{FAN\_FAIL}}$ is an open drain output pin and requires a 3.3V pull-up resistor and it can be connected to other open drain fault indication pins.

A 32.768kHz low frequency crstal is not required, but can be use for tighter accuracy for PWMs and TACH counts. If used, external 12pF load caps are required. Use typical crystal layout standards. CLKOUT is always an 32.768kHz output clock that will output from the internal oscillator of the low frequency crystal if populated and enabled. If CLKOUT is unused, just leave it floating.

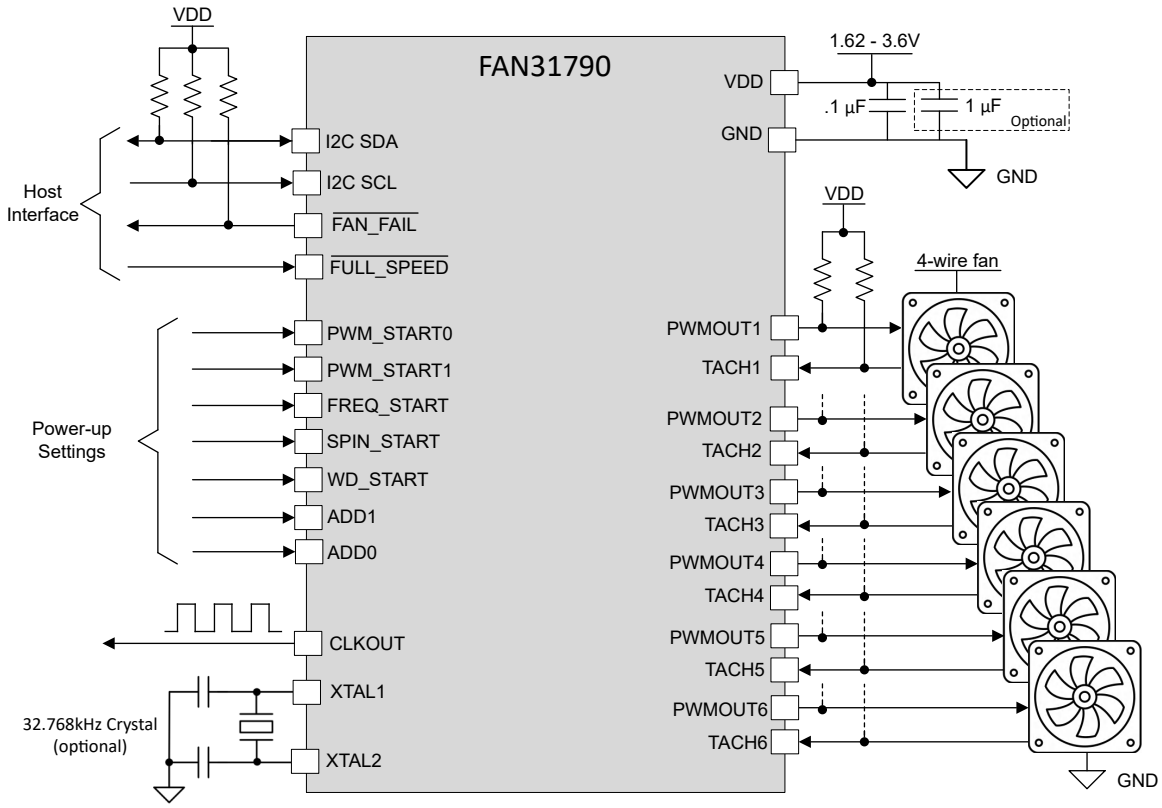
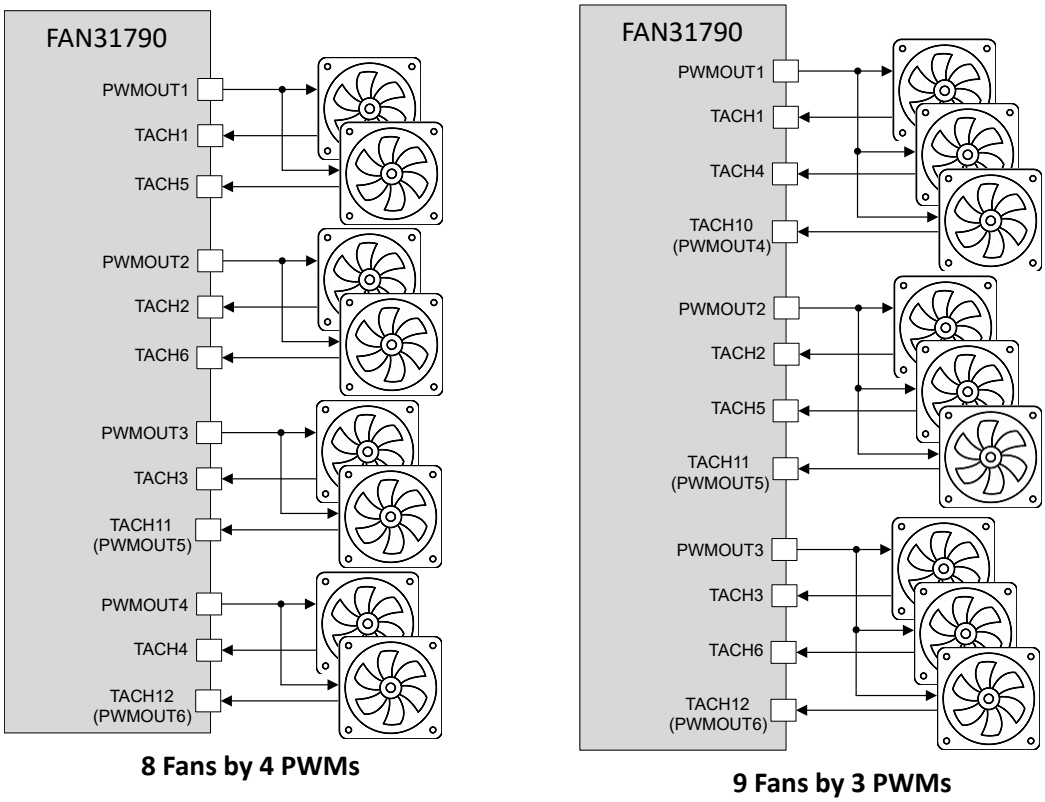


Figure 9-1. Application Schematic

9.1.2 Configuration Examples

The typical example above controls and monitors 6 fans independently but FAN31790 is very flexible in it's configurations. It is possible to monitor more fans but with less overall control by switching the PWMOUTx pins

to additional TACH inputs. The extreme is monitoring 12 fans with no PWM outputs remaining. Here are a few common example configurations.



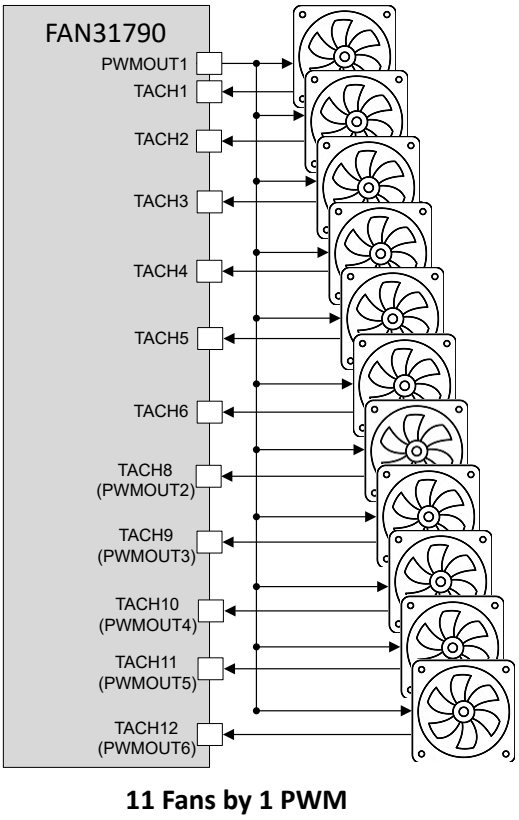


Figure 9-2. FAN31790 Configuration Examples

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

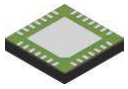
DATE	REVISION	NOTES
April 2026	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

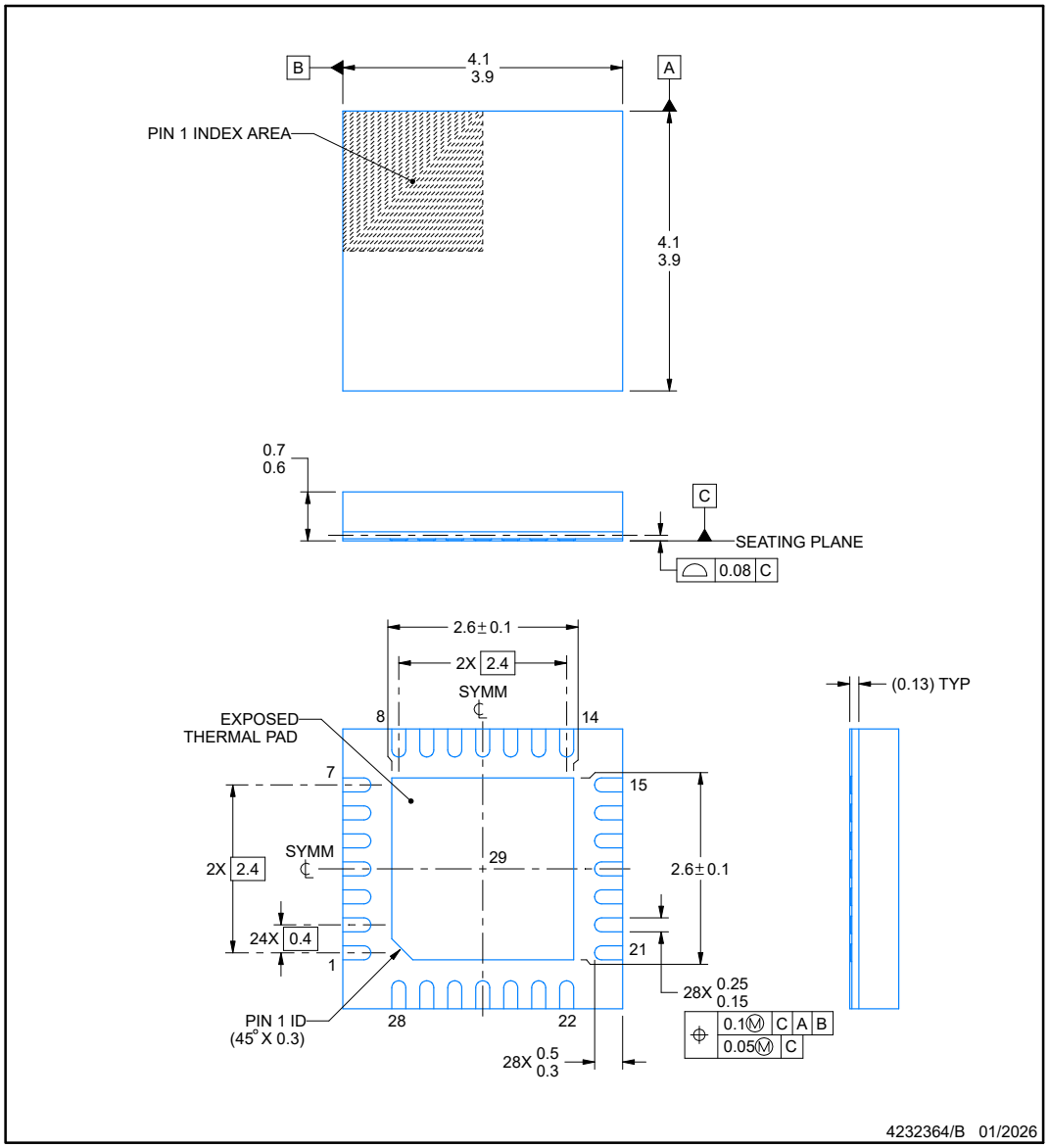
PACKAGE OUTLINE

ZFP0028B



LGA - 0.7 mm max height

LAND GRID ARRAY



NOTES:

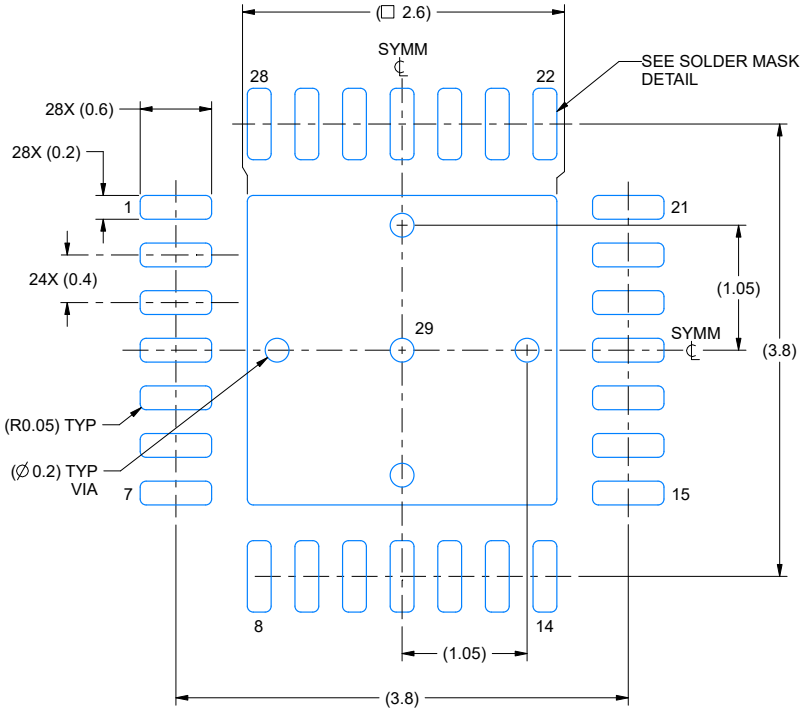
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

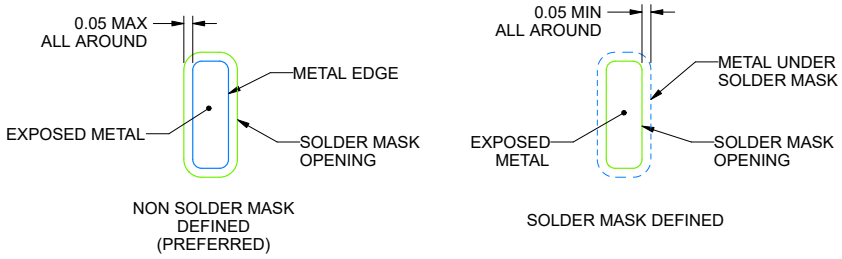
ZFP0028B

LGA - 0.7 mm max height

LAND GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4232364/B 01/2026

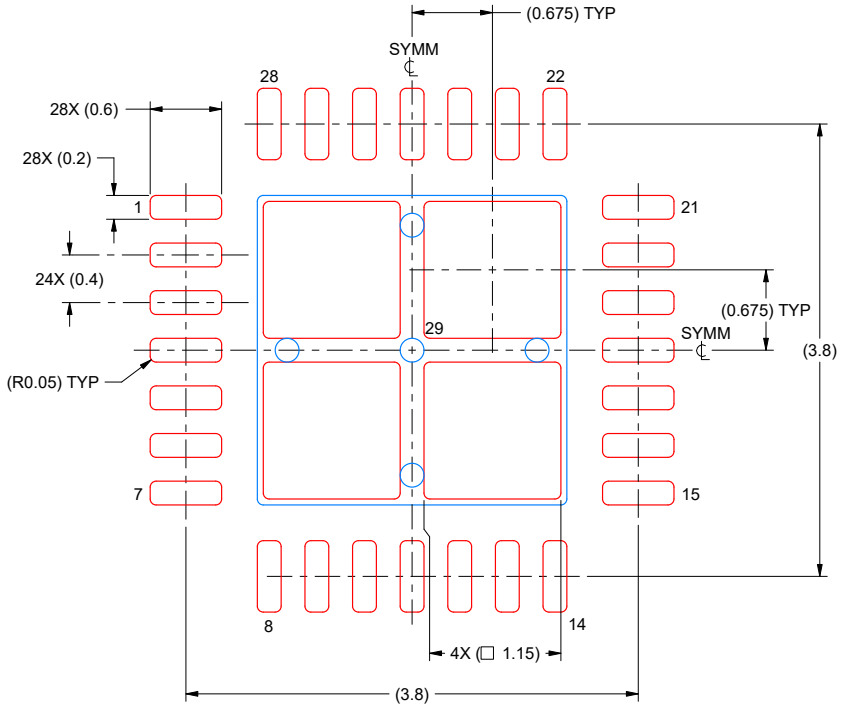
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

ZFP0028B — **LGA - 0.7 mm max height**

LAND GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 29
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

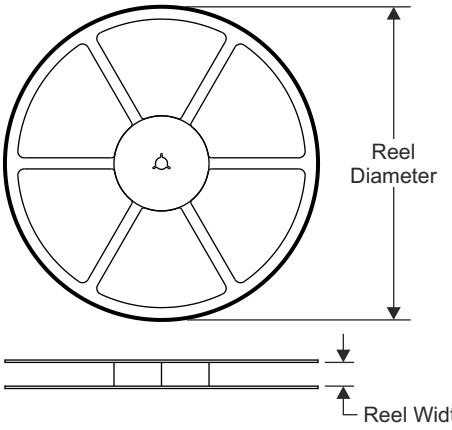
4232364/B 01/2026

NOTES: (continued)

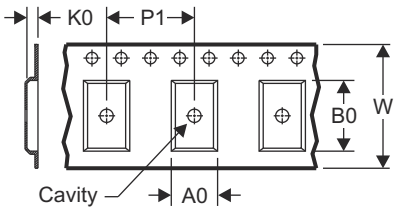
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

12.1 Tape and Reel Information

REEL DIMENSIONS

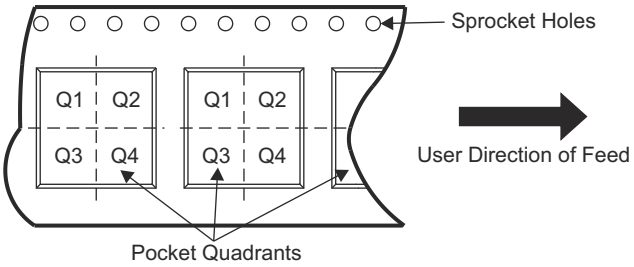


TAPE DIMENSIONS



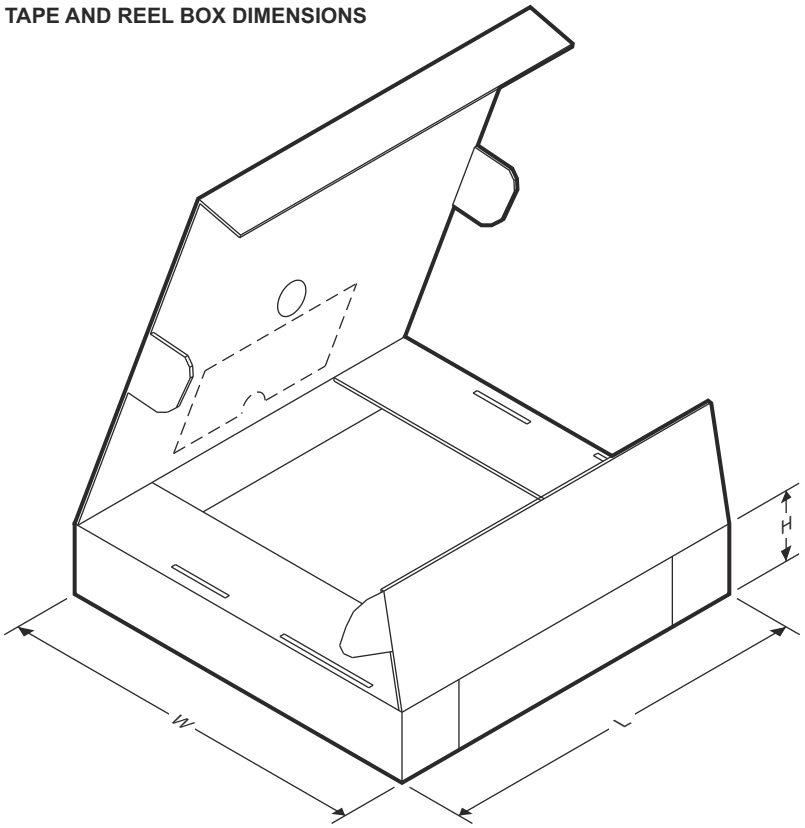
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
FAN31790SZFPR	LGA	ZFP	28	2500	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



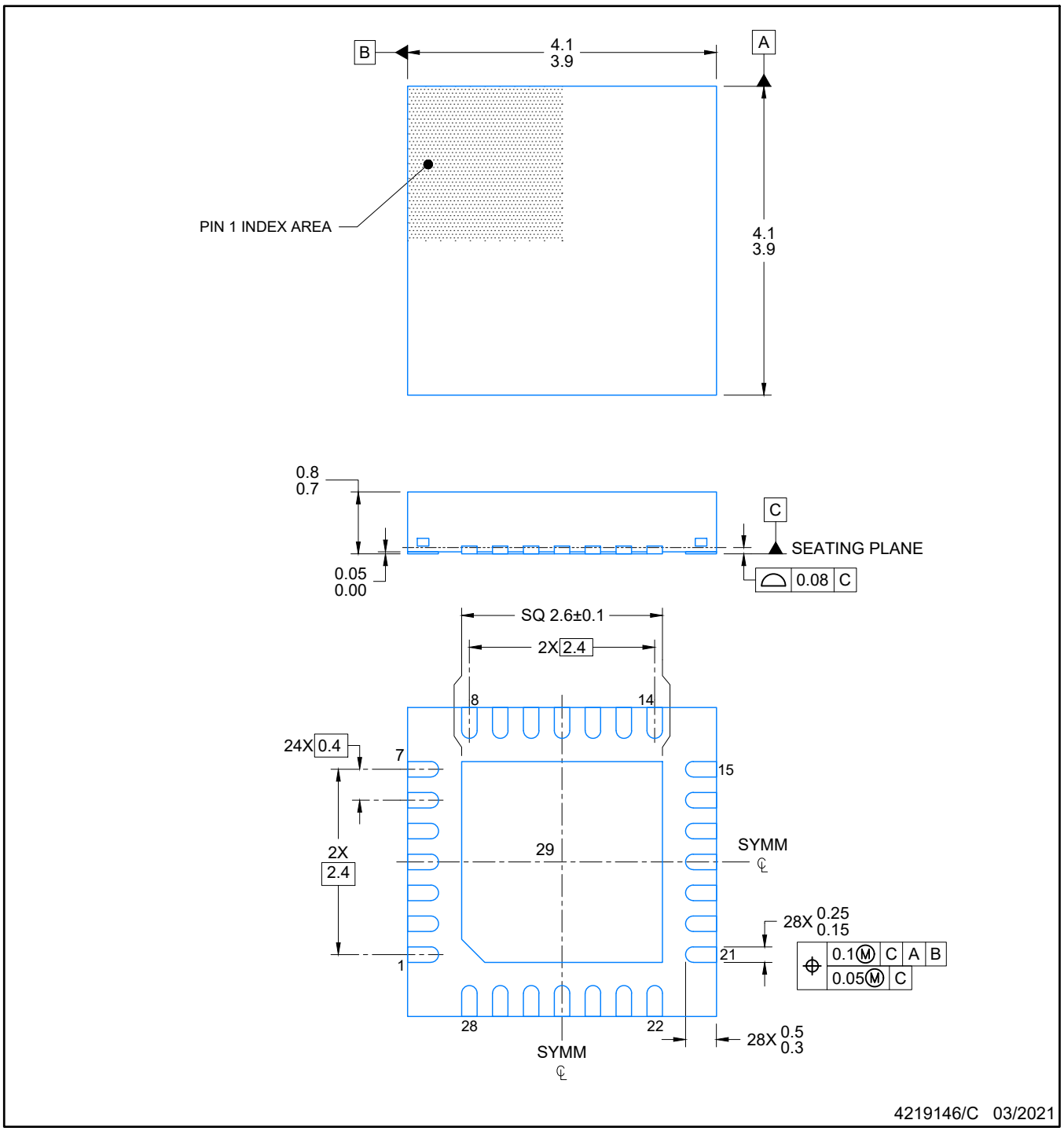
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
FAN31790SZFPR	LGA	ZFP	28	2500	336.6	336.6	31.8

PACKAGE OUTLINE

RUY0028A

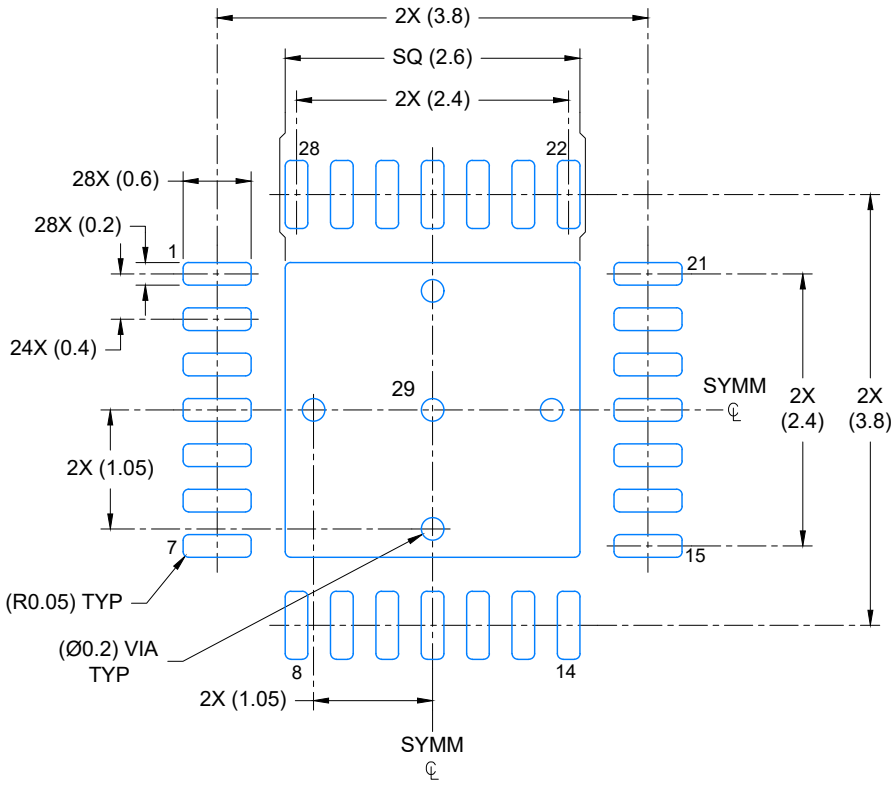
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK-NO LEAD

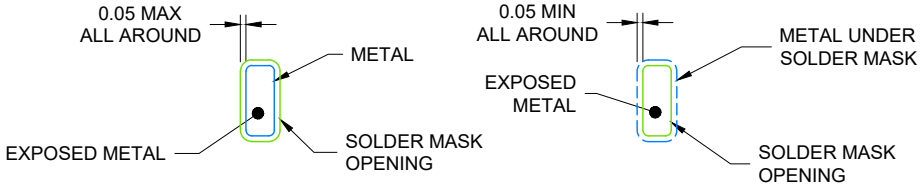


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON SOLDER MASK DEFINED (PREFERRED)

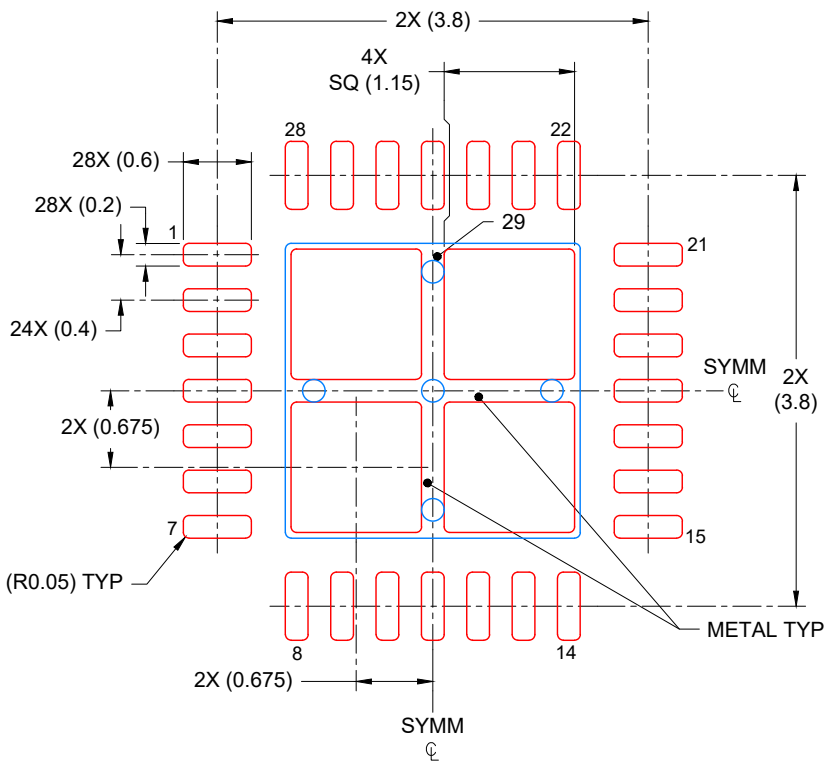
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4219146/C 03/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 15X

4219146/C 03/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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