INA141 Precision, Low-Power, G = 10V/V or 100V/V Instrumentation Amplifier

1 Features

- Low offset voltage:
  - 50µV maximum at G = 100V/V
- Low drift:
  - 0.5µV/°C maximum at G = 100V/V
- Accurate gain:
  - ±0.05% at G = 10V/V
- Low input bias current:
  - 5nA, maximum
- High CMR:
  - 117dB, minimum
- Inputs protected to ±40V
- Wide supply range: ±2.25V to ±18 V
- Low quiescent current: 750µA

2 Applications

- Temperature transmitter
- Medical instrumentation
- Data acquisition (DAQ)
- Process analytics (pH, gas, concentration, force and humidity)

3 Description

The INA141 is a low power, general-purpose instrumentation amplifier offering excellent accuracy. The versatile three-op-amp design and small size make this device an excellent choice for a wide range of applications. Current-feedback input circuitry provides wide bandwidth even at high gain (200 kHz at G = 100 V/V).

Simple pin connections set an accurate gain of 10 V/V or 100 V/V without external resistors. Internal input protection can withstand up to ±40 V without damage.

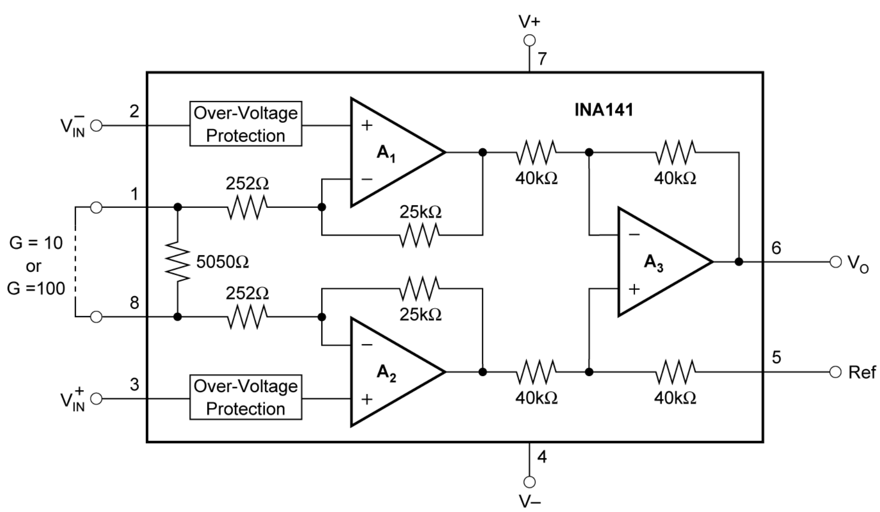
The INA141 is laser trimmed for very low offset voltage (50 µV), drift (0.5 µV/°C) and high common-mode rejection (117 dB at G = 100 V/V). The device operates with power supplies as low as ±2.25 V, and quiescent current is only 750 µA.

The INA141 is available in an 8-pin SOIC package, and is specified for the −40°C to +85°C temperature range.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
INA141	D (SOIC, 8)	4.9mm × 6mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Basic Connections

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4 Pin Configuration and Functions

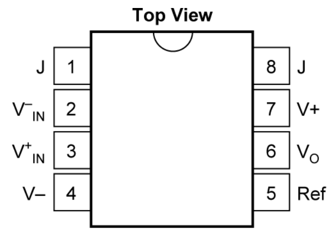


Figure 4-1. D Package, 8-Pin SOIC (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
J	1, 8	Input	Gain selection. G = 10V/V if not shorted G = 100V/V if shorted A resistance of 0.5Ω decreases gain by 0.1%.
Ref	5	Input	Reference input. This pin must be driven by low impedance
V–	4	—	Negative supply
V+	7	—	Positive supply
V^{-}_{IN}	2	Input	Negative (inverting) input
V^{+}_{IN}	3	Input	Positive (noninverting) input
V_O	6	Output	Output

5 Specifications

Note

TI has qualified multiple fabrication flows for this device. Differences in performance are labeled by chip site origin (CSO). For system robustness, designing for all flows is highly recommended. For more information, please see Section 8.1.

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_S	Supply voltage	Dual supply, V_S = (V+) – (V–)		±18	V
		Single supply, V_S = (V+) – 0 V		36	
	Input voltage			±40	V
	Output short-circuit (to ground)[2]		Continuous		
T_A	Operating temperature		–40	125	°C
T_{stg}	Storage temperature		–40	125	°C
T_J	Junction temperature			150	°C
	Lead temperature (soldering, 10 s)			300	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to V_S / 2.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_S	Supply voltage	Single-supply	4.5	30	36	V
		Dual-supply	±2.25	±15	±18	
T_A	Specified temperature		–40		85	°C

5.4 Thermal Information

THERMAL METRIC[1]		INA141 D (SOIC) 8 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	150	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	11	°C/W

THERMAL METRIC[(1)]		INA141 D (SOIC) 8 PINS	UNIT
Ψ_{JB}	Junction-to-board characterization parameter	53	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, V_{CM} = V_S / 2, and G = 10 V/V, all chips site origins (CSO) (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
INPUT								
V_{OS}	Offset voltage (RTI)	G = 10 V/V	CSO: SHE	INA141P, INA141U		±50	±100	µV
				INA141PA, INA141UA		±50	±250	
			CSO: TID	INA141U		±9.2	±80	
				INA141UA		±9.2	±200	
		G = 100 V/V	CSO: SHE	INA141P, INA141U		±20	±50	
				INA141PA, INA141UA		±20	±125	
			CSO: TID	INA141U		±3.8	±50	
				INA141UA		±3.8	±125	
	Offset voltage drift (RTI)	G = 10 V/V, T_A = –40°C to +85°C	CSO: SHE	INA141P, INA141U		±0.5	±2	µV/°C
				INA141PA, INA141UA		±0.5	±2.5	
			CSO: TID	INA141U		±0.2	±2	
				INA141UA		±0.2	±2.5	
		G = 100 V/V, T_A = –40°C to +85°C	CSO: SHE	INA141P, INA141U		±0.2	±0.5	
				INA141PA, INA141UA		±0.2	±1.5	
			CSO: TID	INA141U		±0.04	±0.5	
				INA141UA		±0.04	±1.5	
PSRR	Power-supply rejection ratio (RTI)	V_S = ±2.25 V to ±18 V	INA141P, INA141U	G = 10 V/V		±2	±10	µV/V
				G = 100 V/V		±0.4	±1	
			INA141PA, INA141UA	G = 10 V/V		±2	±20	
				G = 100 V/V		±0.4	±3	
	Long-term stability	G = 10 V/V				0.5		µV/mo
		G = 100 V/V				0.2		
	Input impedance	Differential				100 || 2		GΩ || pF
		Common-mode				100 || 9		
V_{CM}	Common-mode voltage[(1)]	V_O = 0 V			(V–) +2		(V+) – 2	V
CMRR	Common-mode rejection	V_{CM} = ±13 V, ΔR_S = 1 kΩ	INA141P, INA141U	G = 10 V/V	100	106		dB
				G = 100 V/V	117	125		
			INA141PA, INA141UA	G = 10 V/V	93	100		
				G = 100 V/V	110	120		
INPUT BIAS CURRENT								
I_B	Input bias current	INA141P, INA141U				±2	±5	nA
		INA141PA, INA141UA				±2	±10	
	Input bias current drift	T_A = –40°C to +85°C				±30		pA/°C
I_{OS}	Input offset current	INA141P, INA141U				±1	±5	nA
		INA141PA, INA141UA				±1	±10	
	Input offset current drift	T_A = –40°C to +85°C				±30		pA/°C

5.5 Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, V_{CM} = V_S / 2, and G = 10 V/V, all chips site origins (CSO) (unless otherwise noted)

	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
NOISE								
e_N	Voltage noise (RTI)	G = 10 V/V, R_S = 0 Ω	f = 10 Hz	CSO: SHE		22		nV/√Hz
				CSO: TID		15.2		nV/√Hz
			f = 100 Hz	CSO: SHE		13		nV/√Hz
				CSO: TID		14.6		nV/√Hz
			f = 1 kHz	CSO: SHE		12		nV/√Hz
				CSO: TID		15.1		nV/√Hz
			f_B = 0.1 Hz to 10 Hz	CSO: SHE		0.6		$μV_{PP}$
				CSO: TID		0.37		$μV_{PP}$
		G = 100 V/V, R_S = 0 Ω	f = 10 Hz	CSO: SHE		10		nV/√Hz
				CSO: TID		7.5		nV/√Hz
			f = 100 Hz	CSO: SHE		8		nV/√Hz
				CSO: TID		7.5		nV/√Hz
			f = 1 kHz	CSO: SHE		8		nV/√Hz
				CSO: TID		7.4		nV/√Hz
			f_B = 0.1 Hz to 10 Hz	CSO: SHE		0.2		$μV_{PP}$
				CSO: TID		0.17		$μV_{PP}$
I_n	Current noise	f = 10 Hz	CSO: SHE			0.9		pA/√Hz
			CSO: TID			0.2		pA/√Hz
		f = 1 kHz	CSO: SHE			0.3		pA/√Hz
			CSO: TID			0.19		pA/√Hz
		f_B = 0.1 Hz to 10 Hz				30		pA_{PP}
GAIN								
G	Gain				10		100	V/V
GE	Gain error	V_O = ±13.6 V	INA141P, INA141U	G = 10 V/V		±0.01	±0.05	%
				G = 100 V/V		±0.03	±0.075	%
			INA141PA, INA141UA	G = 10 V/V		±0.01	±0.15	%
				G = 100 V/V		±0.03	±0.15	%
	Gain drift[2]	G = 10 V/V or 100 V/V, T_A = –40°C to +85°C				±2	±10	ppm/°C
	Gain nonlinearity	INA141P, INA141U	G = 10 V/V			±0.0003	±0.001	% of FSR
			G = 100 V/V			±0.0005	±0.002	% of FSR
		INA141PA, INA141UA	G = 10 V/V			±0.0003	±0.002	% of FSR
			G = 100 V/V			±0.0005	±0.004	% of FSR
OUTPUT								
	Output voltage	CSO: SHE			(V–) + 1.4	(V±) ∓ 0.9	(V+) – 1.4	V
		CSO: TID			(V–) + 0.15		(V+) – 0.15	V
C_L	Load capacitance	Stable operation				1000		pF
I_{SC}	Short-circuit current	Continuous to V_S / 2				±20		mA

5.5 Electrical Characteristics (continued)

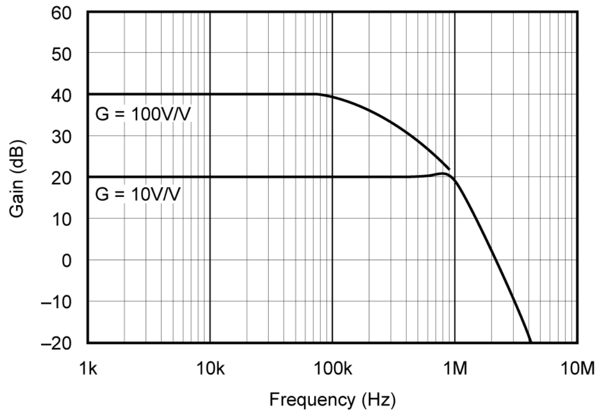
at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, V_{CM} = V_S / 2, and G = 10 V/V, all chips site origins (CSO) (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
BW	Bandwidth, –3 dB	G = 10 V/V	CSO: SHE		994		kHz
			CSO: TID		610		
		G = 100 V/V			200		
SR	Slew rate	G = 10 V/V, V_O = ±10 V	CSO: SHE		4		V/µs
			CSO: TID		2		
t_S	Settling time	To 0.01%, V_O = ±5 V	G = 10 V/V		7		µs
			G = 100 V/V		9		
	Overload recovery	50% input overload			4		µs
POWER SUPPLY							
I_Q	Quiescent current	V_{IN} = 0 V	CSO: SHE		±750	±800	µA
			CSO: TID		±590	±800	

(1) Input common-mode voltage varies with output voltage; see *Typical Characteristics*.
(2) Specified by wafer test.

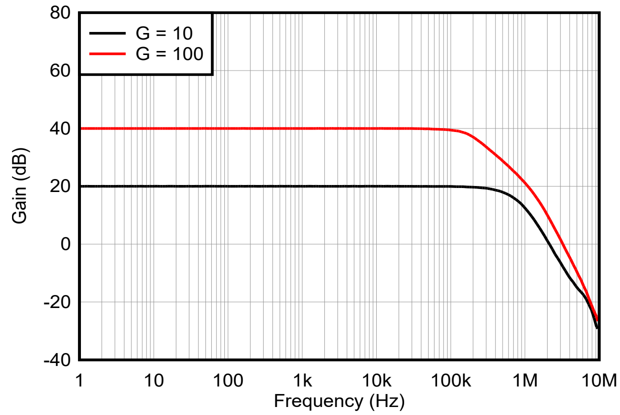
5.6 Typical Characteristics

at T_A = 25°C, V_S = ±15 V, V_{REF} = 0 V, G = 10 V/V, VCM = V_S / 2, and R_L = 10 kΩ, all chips site origins (CSO) (unless otherwise noted)



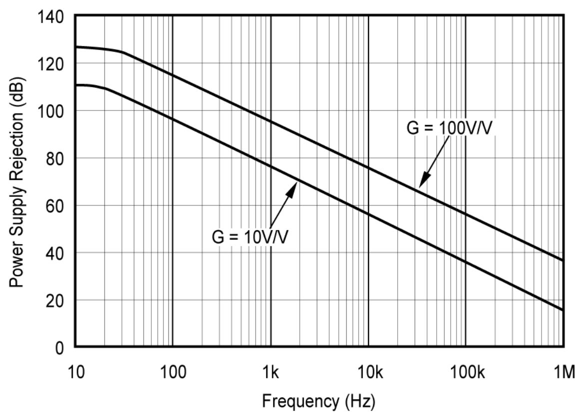
CSO: SHE

Figure 5-1. Gain vs Frequency



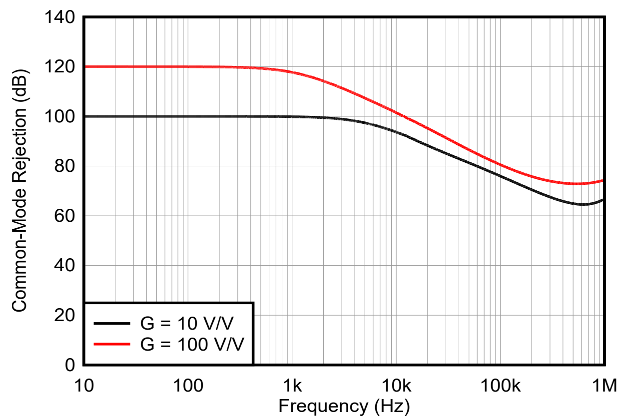
CSO: TID

Figure 5-2. Gain vs Frequency



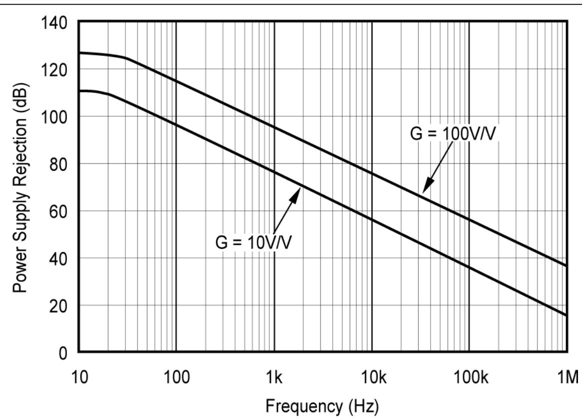
CSO: SHE

Figure 5-3. Common-Mode Rejection vs Frequency



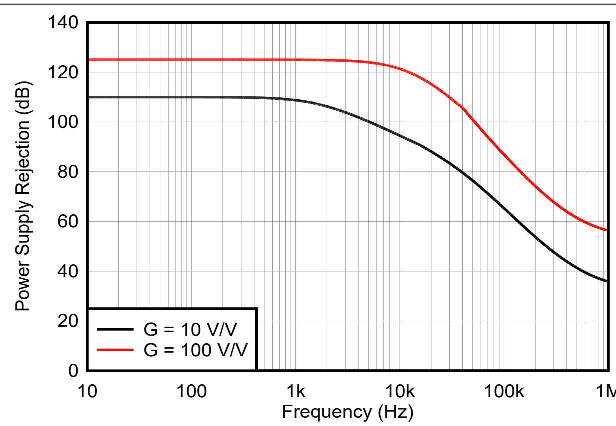
CSO: TID

Figure 5-4. Common-Mode Rejection vs Frequency



CSO: SHE

Figure 5-5. Positive Power Supply Rejection vs Frequency



CSO: TID

Figure 5-6. Positive Power Supply Rejection vs Frequency

5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{REF} = 0 V, G = 10 V/V, VCM = V_S / 2, and R_L = 10 kΩ, all chips site origins (CSO) (unless otherwise noted)

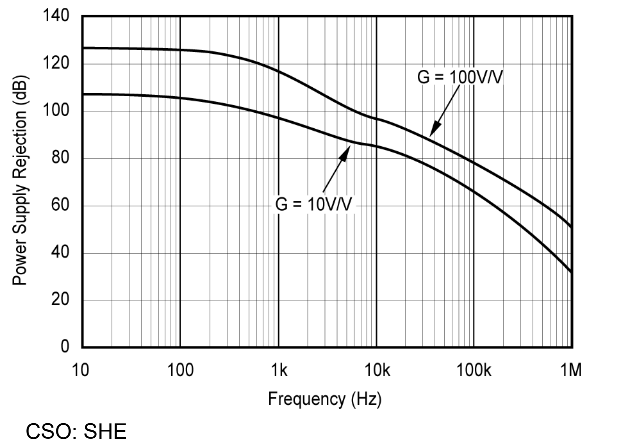


Figure 5-7. Negative Power Supply Rejection vs Frequency

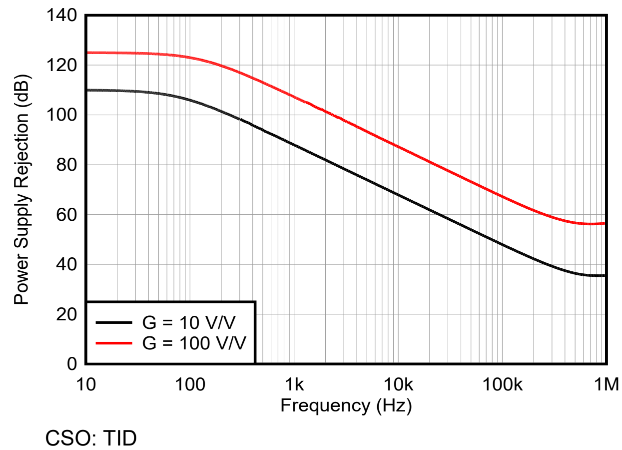


Figure 5-8. Negative Power Supply Rejection vs Frequency

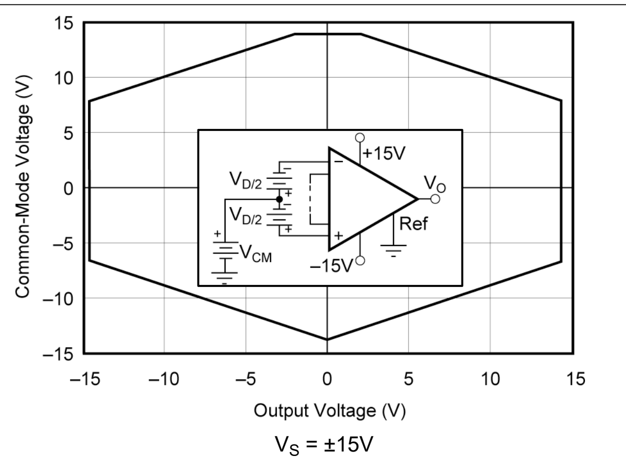


Figure 5-9. Input Common-Mode Range vs Output Voltage

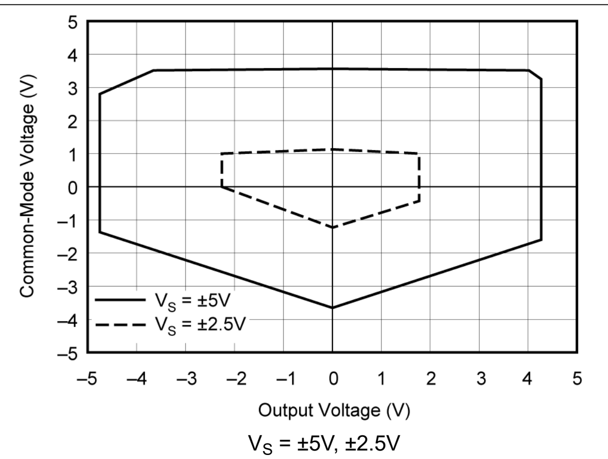


Figure 5-10. Input Common-Mode Range vs Output Voltage

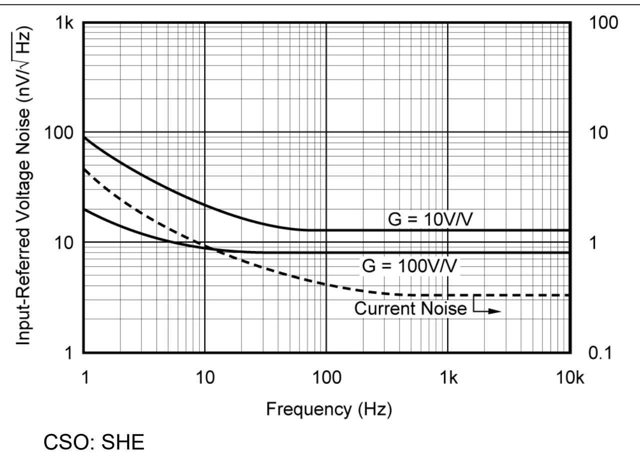


Figure 5-11. Input-Referred Noise vs Frequency

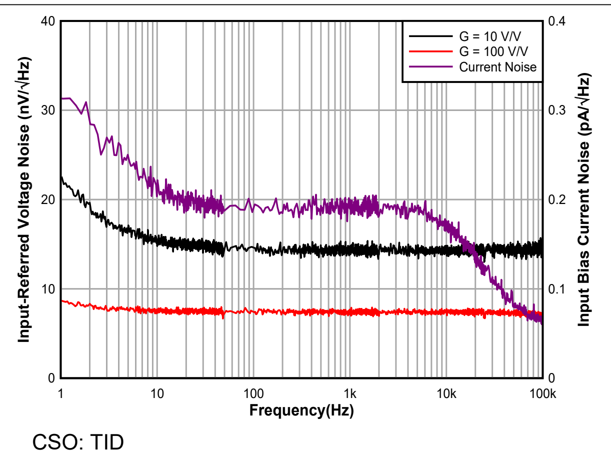


Figure 5-12. Input-Referred Noise vs Frequency

5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{REF} = 0 V, G = 10 V/V, VCM = V_S / 2, and R_L = 10 kΩ, all chips site origins (CSO) (unless otherwise noted)

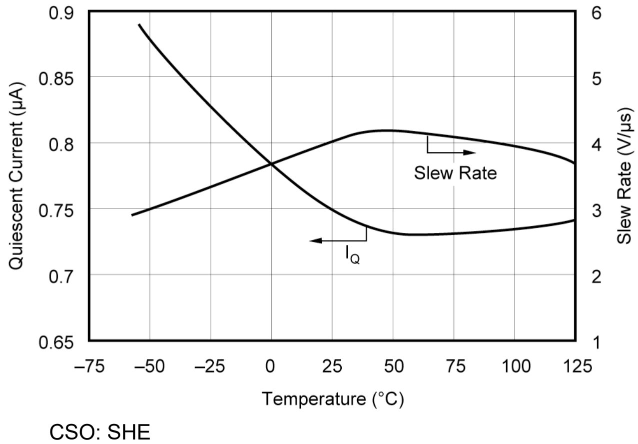


Figure 5-13. Quiescent Current and Slew Rate vs Temperature

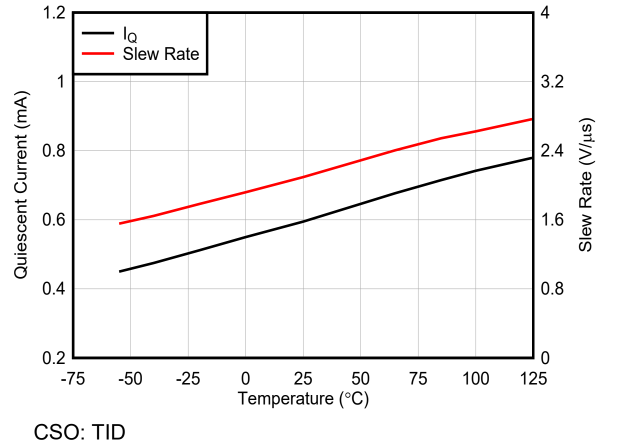


Figure 5-14. Quiescent Current and Slew Rate vs Temperature

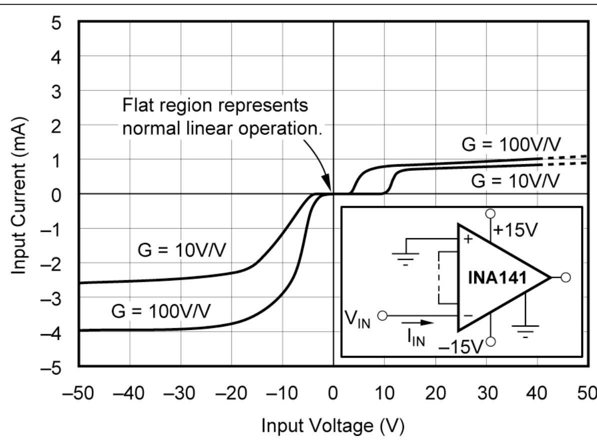


Figure 5-15. Input Overvoltage V/I Characteristics

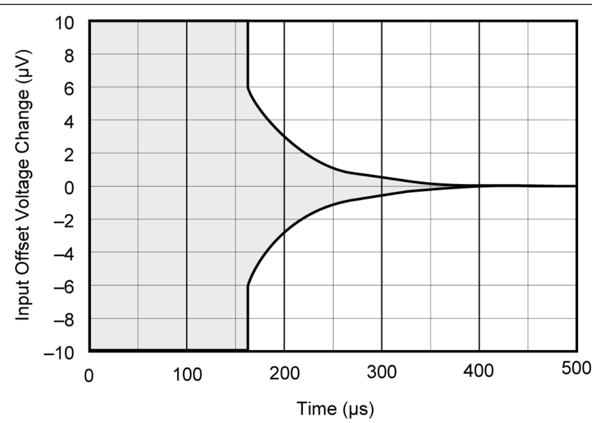


Figure 5-16. Input Offset Voltage Warmup

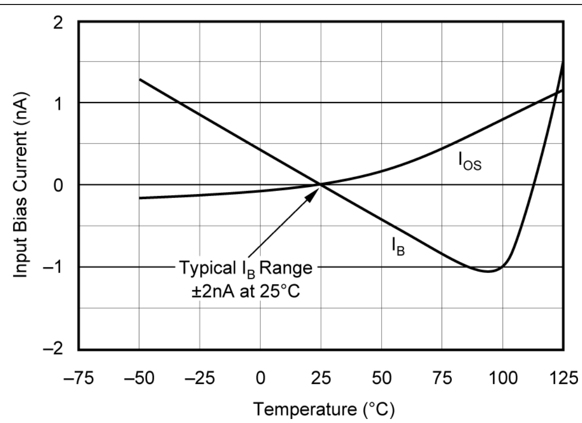


Figure 5-17. Input Bias Current vs Temperature

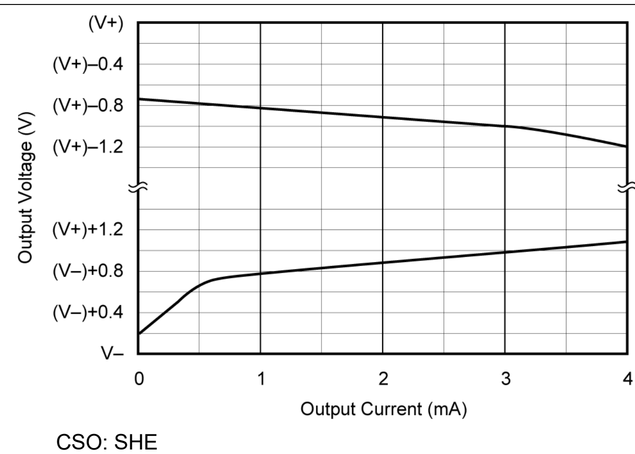


Figure 5-18. Output Voltage Swing vs Output Current

5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{REF} = 0 V, G = 10 V/V, VCM = V_S / 2, and R_L = 10 kΩ, all chips site origins (CSO) (unless otherwise noted)

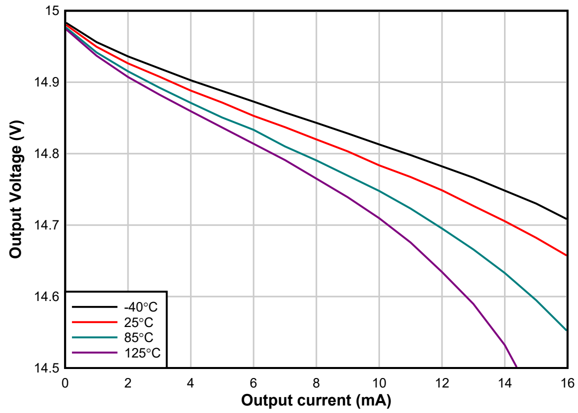


Figure 5-19. Positive Output Voltage Swing vs Output Current

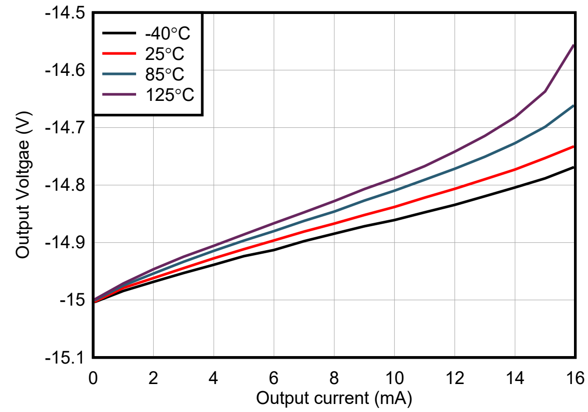


Figure 5-20. Negative Output Voltage Swing vs Output Current

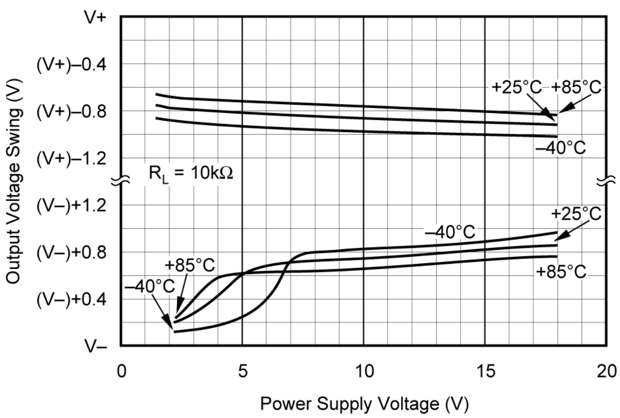


Figure 5-21. Output Voltage Swing vs Power Supply Voltage

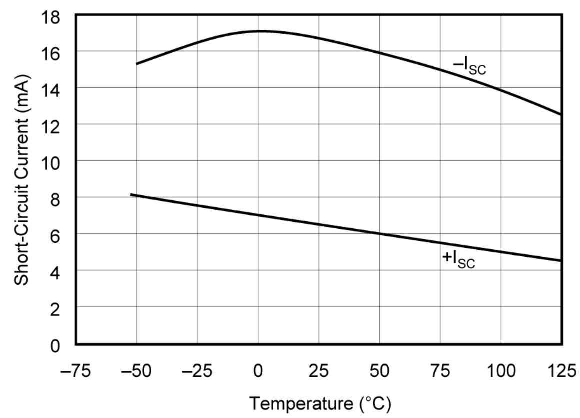


Figure 5-22. Short-circuit Output Current vs Temperature

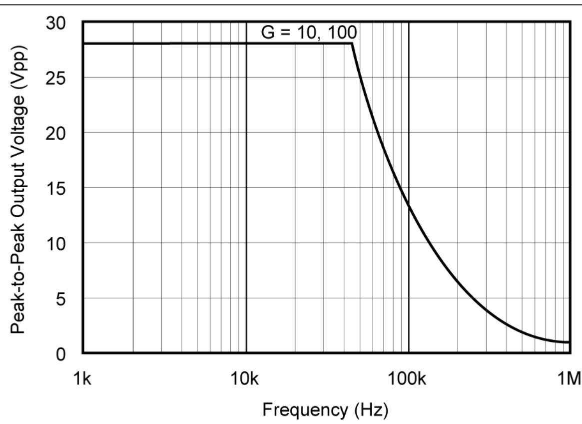


Figure 5-23. Maximum Output Voltage vs Frequency

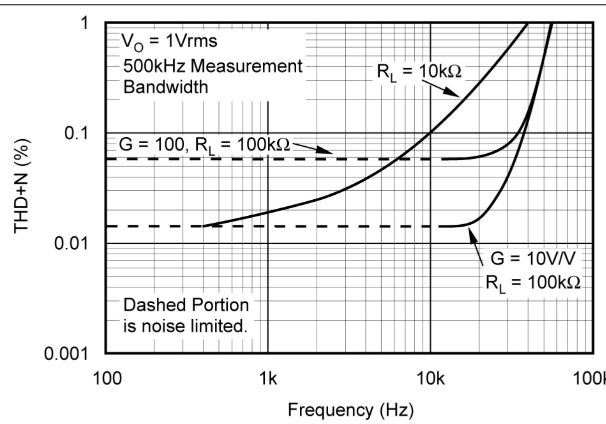
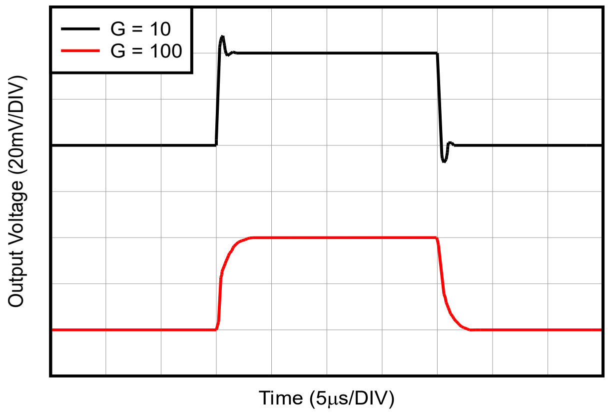


Figure 5-24. Total Harmonic Distortion + Noise vs Frequency

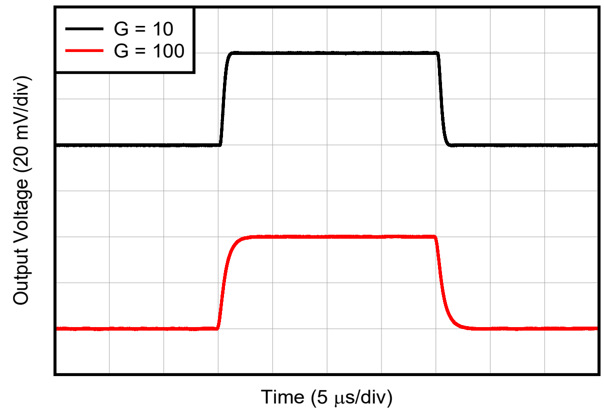
5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, V_{REF} = 0 V, G = 10 V/V, VCM = V_S / 2, and R_L = 10 kΩ, all chips site origins (CSO) (unless otherwise noted)



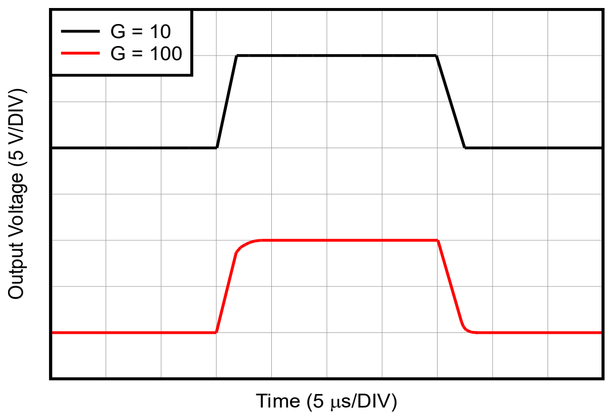
CSO: SHE

Figure 5-25. Small-Signal Step Response



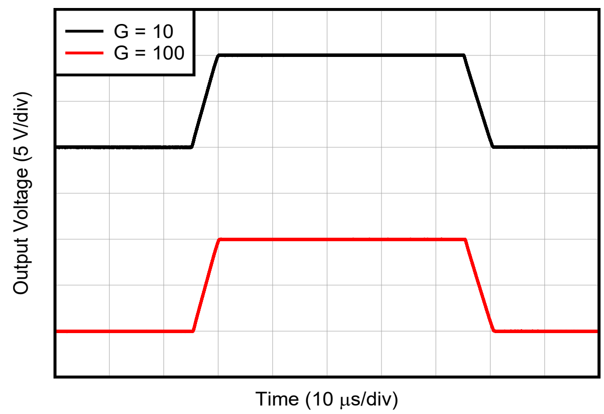
CSO: TID

Figure 5-26. Small-Signal Step Response



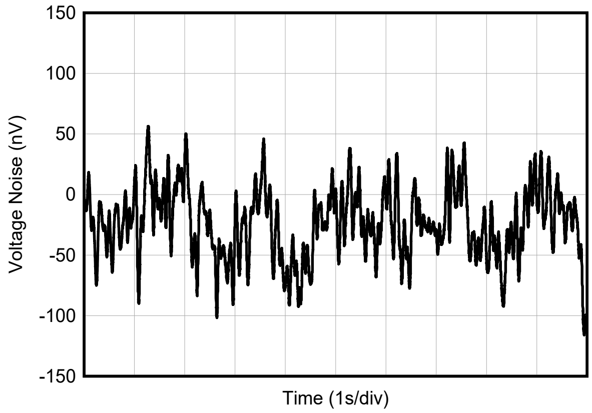
CSO: SHE

Figure 5-27. Large-Signal Step Response



CSO: TID

Figure 5-28. Large-Signal Step Response



G = 100

Figure 5-29. 0.1Hz to 10Hz Input-Referred Voltage Noise

6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

Figure 6-1 shows the basic connections required for operation of the INA141. Applications with noisy or high impedance power supplies can require decoupling capacitors close to the device pins as shown.

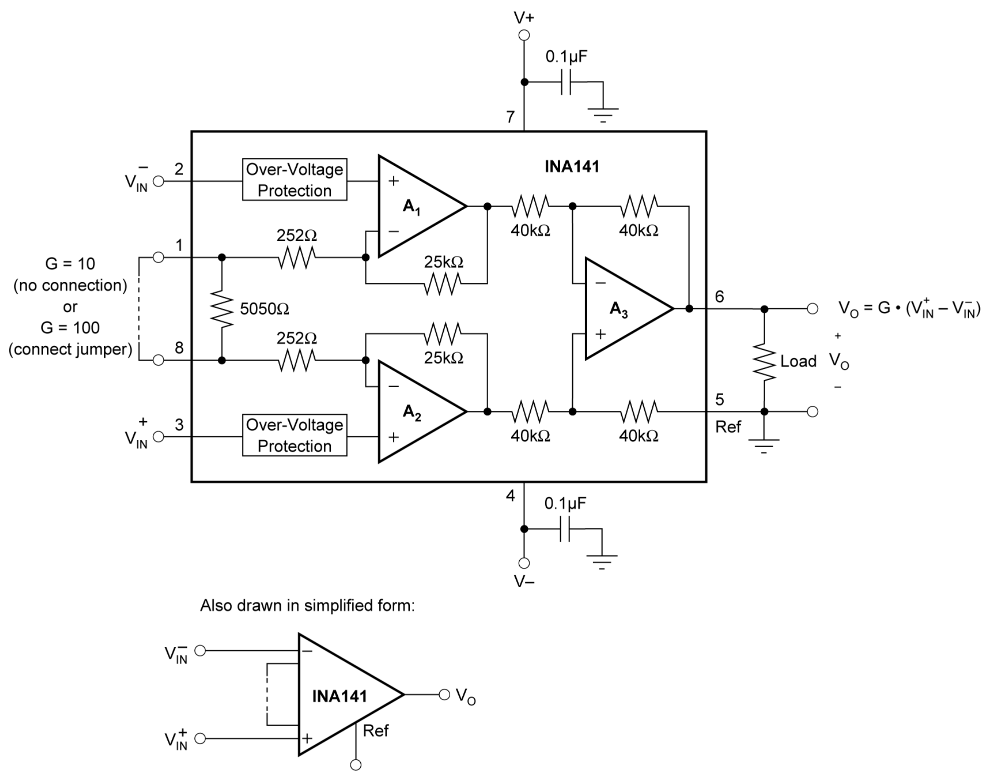


Figure 6-1. Basic Connections.

The output is referred to the output reference (Ref) pin, which is normally grounded. This connection must be low-impedance to maintain good common-mode rejection. A resistance of 8 Ω in series with the Ref pin causes a typical device to degrade to approximately 80 dB CMR (G = 10 V/V).

6.1.1 Setting the Gain

Gain is selected with a jumper connection (see Figure 6-1). With no jumper installed, G = 10 V/V. With a jumper installed, G = 100 V/V. To preserve good gain accuracy, this jumper must have low series resistance. A resistance of 0.5 Ω in series with the jumper decreases the gain by 0.1%.

Internal resistor ratios are laser trimmed to provide excellent gain accuracy. Actual resistor values can vary by approximately ±25% from the nominal values shown.

Gains between 10 V/V and 100 V/V are achieved by connecting an external resistor to the jumper pins. However, this configuration is not recommended because the ±25% variation of internal resistor values makes the required external resistor value uncertain. A companion model, the INA128, features accurately trimmed internal resistors so that gains from 1V/V to 10,000V/V can be set with an external resistor.

6.1.2 Dynamic Performance

Typical performance curve *Gain vs Frequency* (Figure 5-1) shows that, despite the low quiescent current, the INA141 achieves wide bandwidth, even at G = 100 V/V. This wide bandwidth is a result of the current-feedback topology of the INA141. Settling time also remains excellent at G = 100 V/V.

6.1.3 Noise Performance

The INA141 provides very low noise in most applications. Low-frequency noise is approximately 0.2 μV_{PP} measured from 0.1 Hz to 10 Hz (G = 100 V/V). The INA141 provides dramatically improved noise when compared to state-of-the-art, chopper-stabilized amplifiers.

6.1.4 Offset Trimming

The INA141 is laser trimmed for low offset voltage and offset voltage drift. Most applications require no external offset adjustment. Figure 6-2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref pin is summed with the output. The op-amp buffer provides low impedance at the Ref pin to preserve good common-mode rejection.

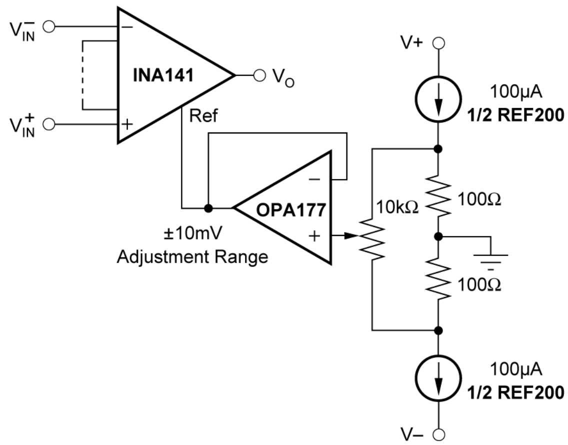


Figure 6-2. Optional Trimming of Output Offset Voltage.

6.1.5 Input Bias Current Return Path

The input impedance of the INA141 is extremely high—approximately 10^{10} Ω. However, a path must be provided for the input bias current of both inputs. This input bias current is approximately ±2 nA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 6-3 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the INA141 and the input amplifiers saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 6-3). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

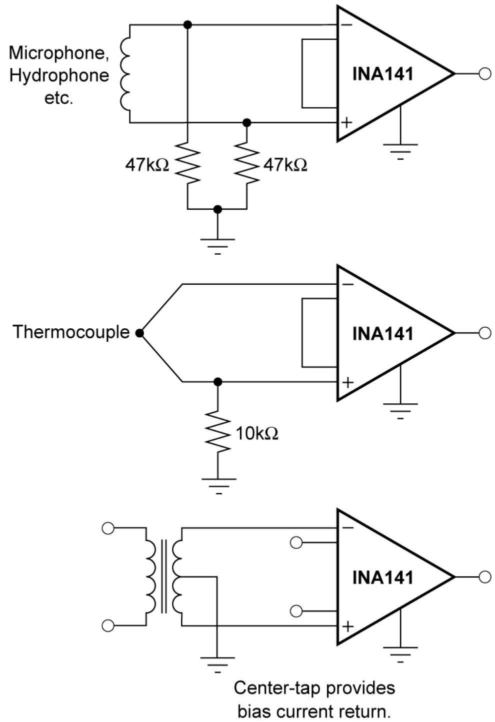


Figure 6-3. Providing an Input Common-Mode Current Path.

6.1.6 Input Common-Mode Range

The linear input voltage range of the input circuitry of the INA141 is from approximately 1.4 V less than the positive supply voltage to 1.7 V greater than the negative supply. As a differential input voltage causes the output voltage to increase, however, the linear input range is limited by the output voltage swing of amplifiers A_1 and A_2. Therefore, the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage (see the *Input Common-Mode Range vs Output Voltage* plots, Figure 5-9 and Figure 5-10.

Input overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to the positive output swing limit, the difference voltage measured by the output amplifier is near zero. The output of the INA141 is near 0V even though both inputs are overloaded.

6.1.7 Low-Voltage Operation

The INA141 operates on power supplies as low as ±2.25V. Performance remains excellent with power supplies ranging from ±2.25 V to ±18 V. Most parameters vary only slightly through this supply voltage range—see Typical Performance Curves. Operation at a very low supply voltage requires careful attention to make sure that the input voltages remain within the linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power-supply voltage. The *Input Common-Mode Range vs Output Voltage* typical characteristics plots, Figure 5-9 and Figure 5-10, show the range of linear operation for ±15-V, ±5-V, and ±2.5-V supplies.

6.1.8 Input Protection

The inputs of the INA141 are individually protected for voltages up to ±40 V. For example, a condition of –40 V on one input and +40 V on the other input does not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors contributes excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value of approximately 1.50 mA to 5 mA. The inputs are protected even if the power supplies are disconnected or turned off.

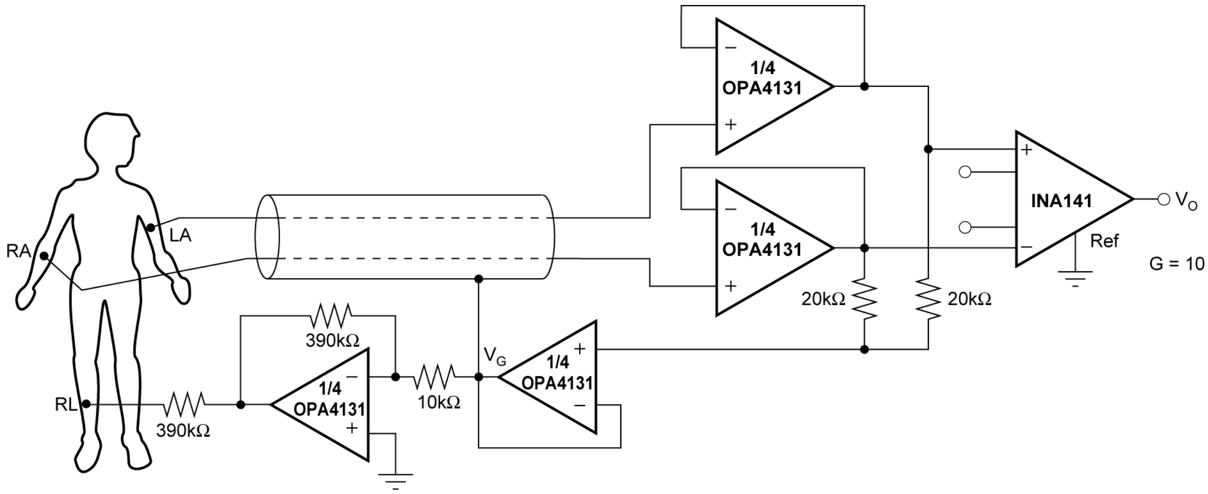


Figure 6-4. ECG Amplifier With Right-Leg Drive

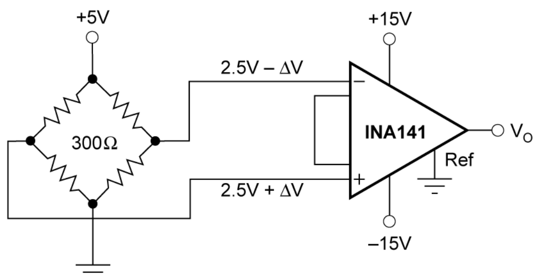


Figure 6-5. Bridge Amplifier

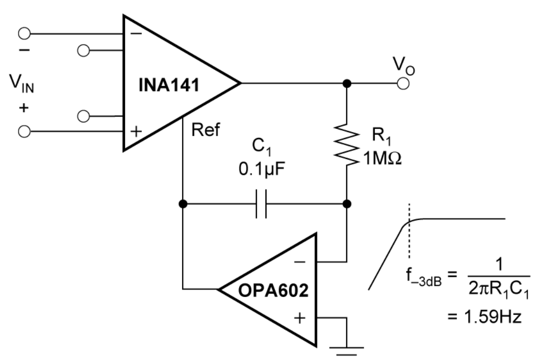
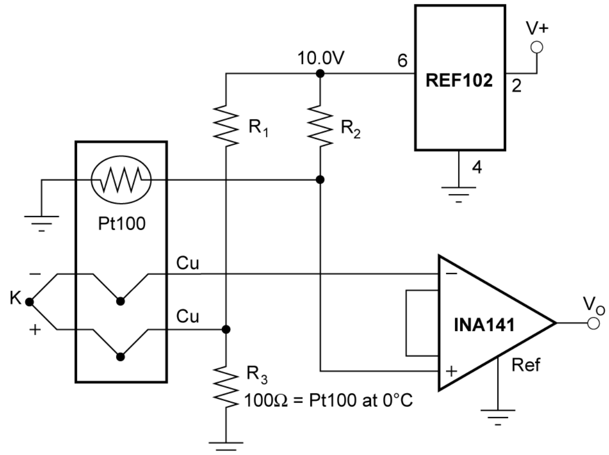
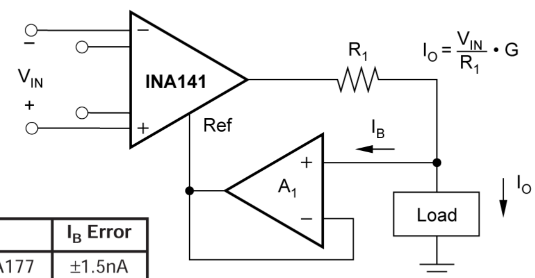


Figure 6-6. AC-Coupled Instrumentation Amplifier



ISA TYPE	MATERIAL	SEEBECK COEFFICIENT (μV/°C)	R_1, R_2
E	+ Chromel – Constantan	58.5	66.5kΩ
J	+ Iron – Constantan	50.2	76.8kΩ
K	+ Chromel – Alumel	39.4	97.6kΩ
T	+ Copper – Constantan	38.0	102kΩ

Figure 6-7. Thermocouple Amplifier With RTD Cold-Junction Compensation



A_1	I_B Error
OPA177	±1.5nA
OPA131	50pA
OPA602	±1pA
OPA128	±75fA

Figure 6-8. Differential Voltage-to-Current Converter

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Device Nomenclature

Table 7-1. Device Nomenclature

Part Number	Definition
INA141U INA141U/2K5 INA141UA INA141UA/2K5	The die is manufactured in CSO: SHE or CSO: TID.
INA141P INA141PA	The die is manufactured in CSO: SHE.

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

7.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

7.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (August 2023) to Revision B (January 2026) **Page**

- Added description of device flow information in the *Specifications* 4
- Added different fabrication process specifications for Offset voltage (RTI) in the *Electrical Characteristics* 5
- Added all chips site origins (CSO) condition to the typical test conditions in the *Electrical Characteristics* 5
- Added different fabrication process specifications for Offset voltage drift (RTI) in the *Electrical Characteristics* 5
- Added different fabrication process specifications for Voltage noise (RTI) in the *Electrical Characteristics* 5
- Added different fabrication process specifications for Current noise f = 10Hz in the *Electrical Characteristics* 5
- Added different fabrication process specifications for Current noise f = 1kHz in the *Electrical Characteristics* 5
- Added different fabrication process specifications for Output voltage in the *Electrical Characteristics* 5
- Added different fabrication process specifications for Bandwidth, -3dB G = 10V/V in the *Electrical Characteristics* 5
- Added different fabrication process specifications for Slew rate in the *Electrical Characteristics* 5
- Added different fabrication process specifications for Quiescent current in the *Electrical Characteristics* 5
- Added *all chips site origins (CSO)* condition to the typical test conditions in the *Typical Characteristics* 8
- Added CSO: SHE to *Gain vs Frequency*, *Common-Mode Rejection vs Frequency*, *Positive Power Supply Rejection vs Frequency*, *Negative Power Supply Rejection vs Frequency*, *Input-Referred Noise vs Frequency*, *Output Voltage Swing vs Power Supply Voltage*, and *Short-circuit Output Current vs Temperature* curves in the *Typical Characteristics* 8
- Added CSO: TID to the *Quiescent Current and Slew Rate vs Temperature*, *Positive Output Voltage Swing vs Output Current*, *Negative Output Voltage Swing vs Output Current*, *Small-Signal Step Response*, and *Large-Signal Step Response* curves in the *Typical Characteristics* 8
- Added *Gain vs Frequency*, *Common-Mode Rejection vs Frequency*, *Positive Power Supply Rejection vs Frequency*, *Negative Power Supply Rejection vs Frequency*, and *Input-Referred Noise vs Frequency* curves for CSO: TID in the *Typical Characteristics* 8
- Added *Quiescent Current and Slew Rate vs Temperature*, *Output Voltage Swing vs Output Current*, *Small-Signal Step Response* and *Large-Signal Step Response* curves for CSO: SHE in the *Typical Characteristics* 8
- Added Part Number flow information table to the *Device Nomenclature* 18

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA141U	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI | Nipdau	Level-3-260C-168 HR	-	INA 141U
INA141U.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	INA 141U
INA141U/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdau	Level-3-260C-168 HR	-	INA 141U
INA141U/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	INA 141U
INA141UA	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI | Nipdau	Level-3-260C-168 HR	-40 to 85	INA 141U A
INA141UA.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	INA 141U A
INA141UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdau	Level-3-260C-168 HR	-40 to 85	INA 141U A
INA141UA/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	INA 141U A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

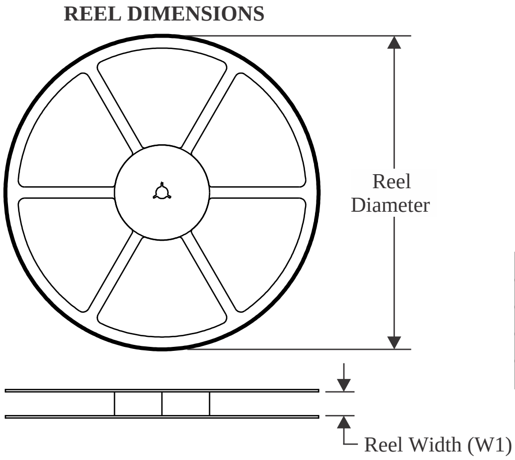
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

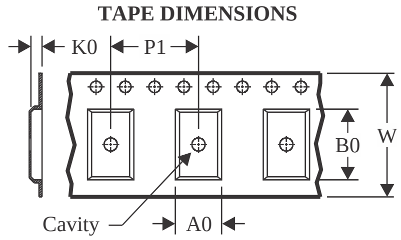
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

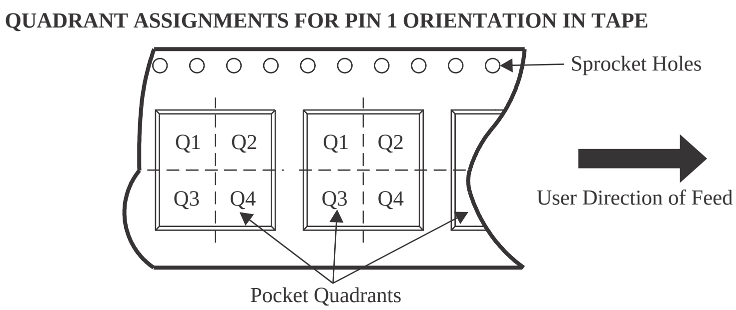
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





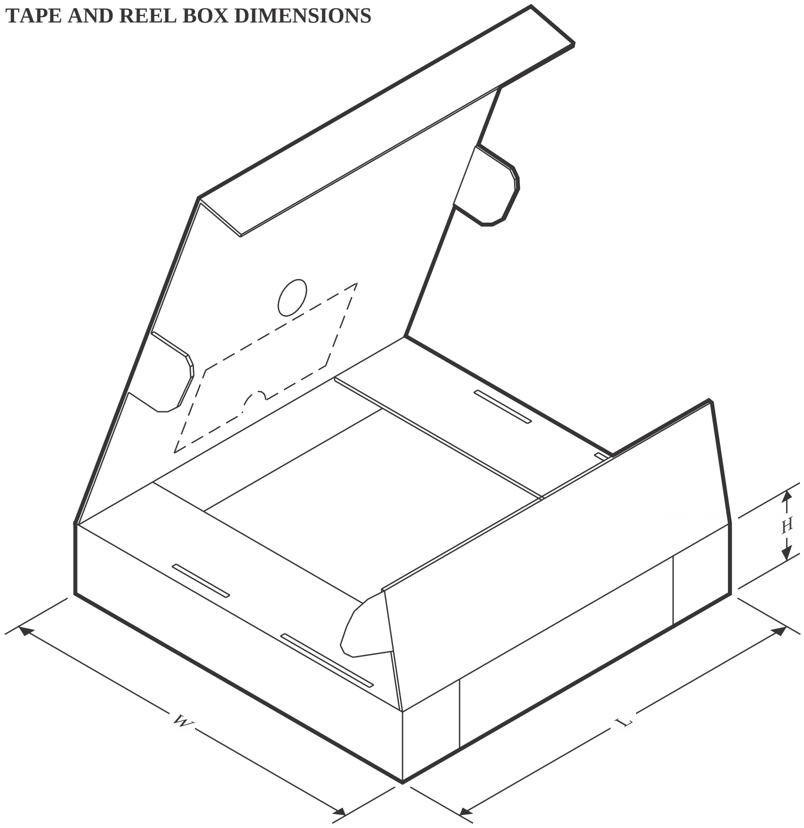
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA141U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA141UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

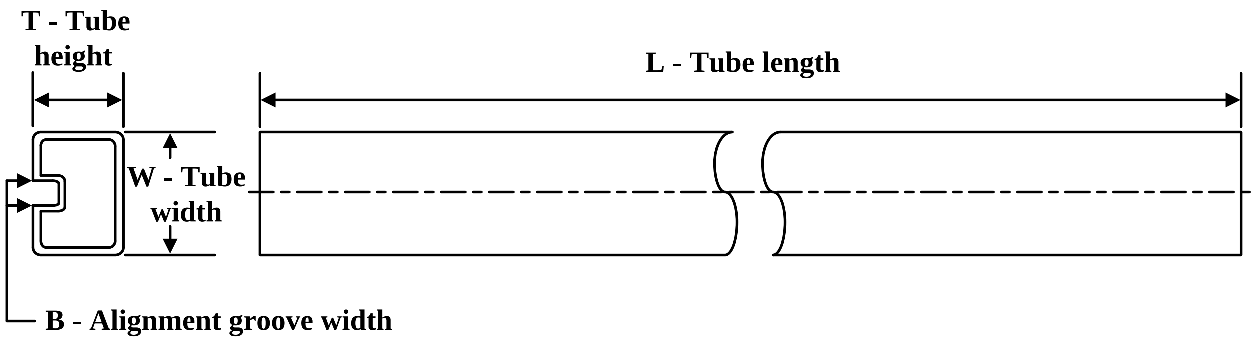
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

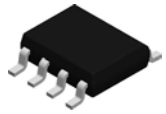
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA141U/2K5	SOIC	D	8	2500	353.0	353.0	32.0
INA141UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA141U	D	SOIC	8	75	506.6	8	3940	4.32
INA141U.B	D	SOIC	8	75	506.6	8	3940	4.32
INA141UA	D	SOIC	8	75	506.6	8	3940	4.32
INA141UA.B	D	SOIC	8	75	506.6	8	3940	4.32

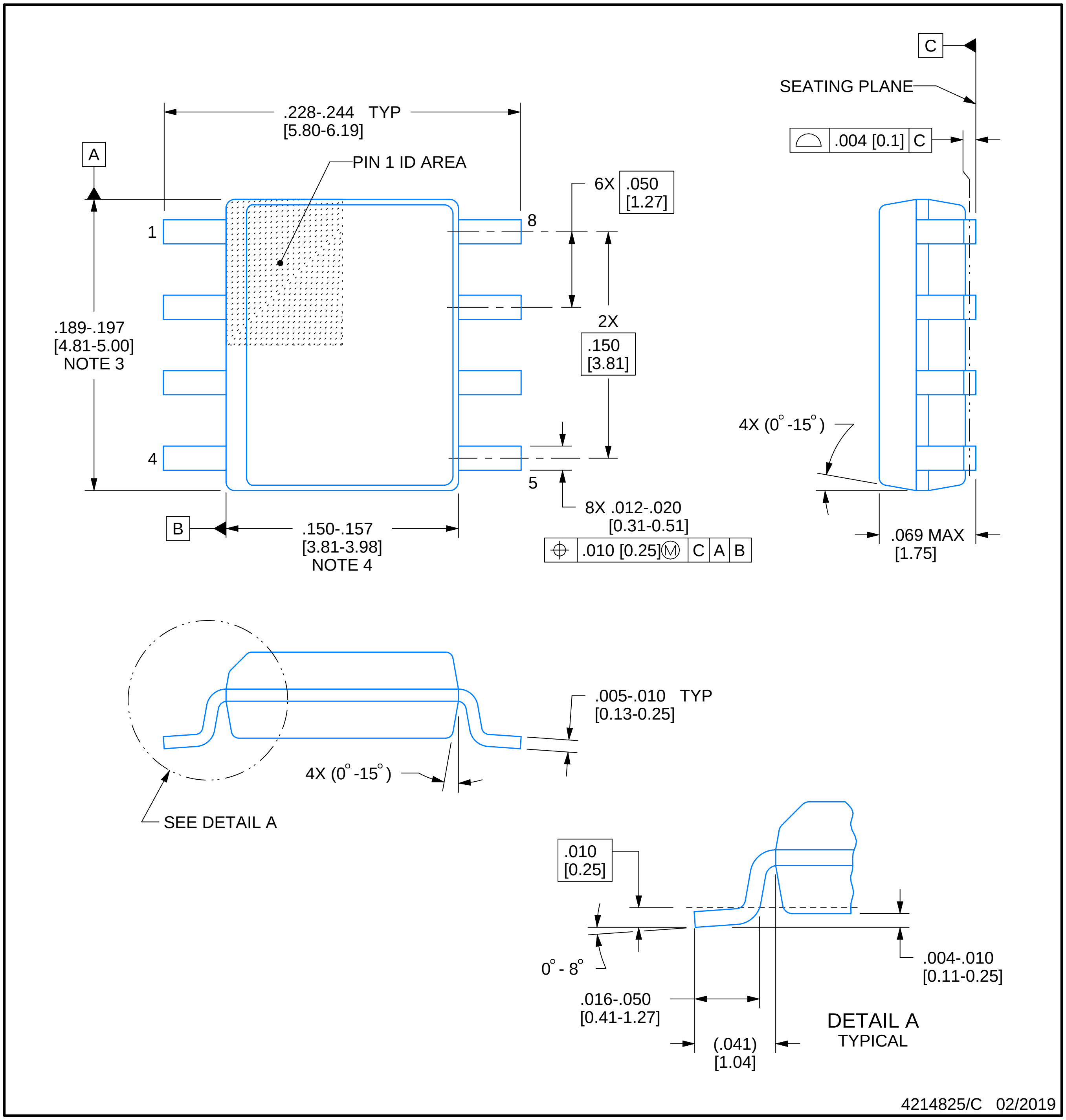


PACKAGE OUTLINE

D0008A

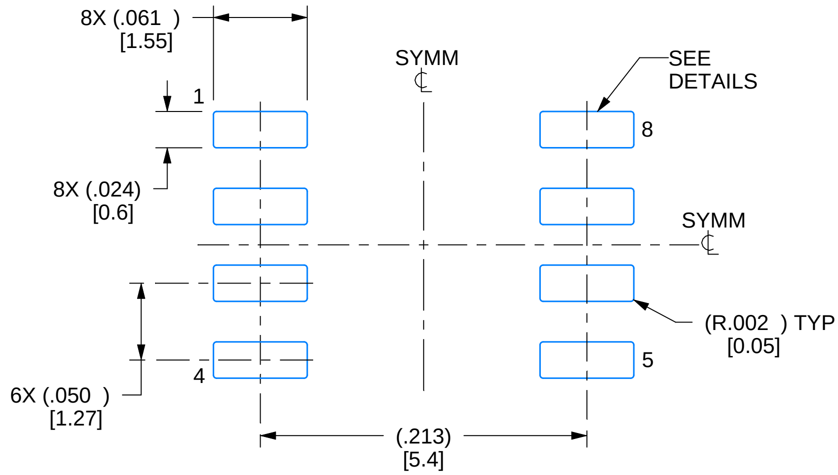
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

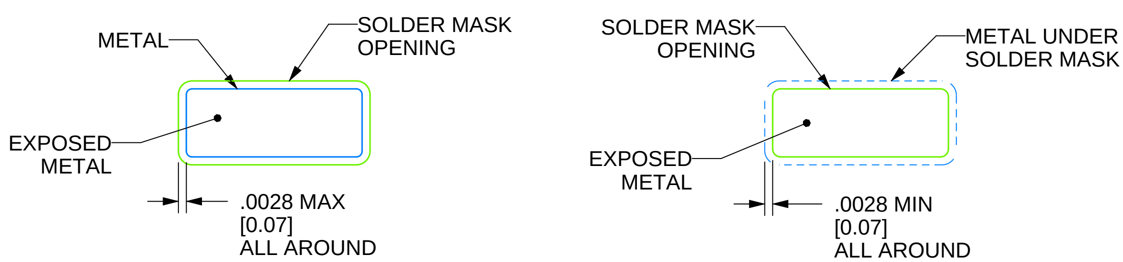


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

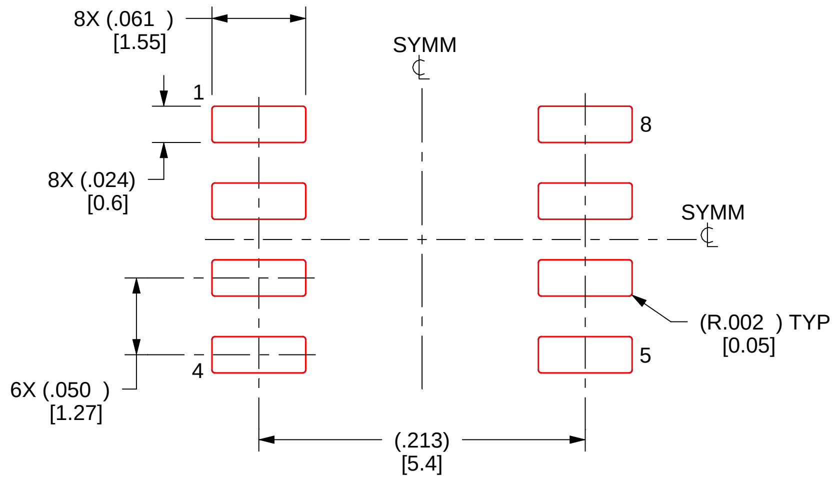
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.