

## ISOx5 Isolated 3.3-V Half- and Full-Duplex RS-485 Transceivers

### 1 Features

- Meets or exceeds TIA/EIA RS-485 requirements
- 1/8 unit load – Up to 256 nodes on a bus
- Signaling rates up to 1 Mbps
- Thermal shutdown protection
- Low bus capacitance – 16 pF (typical)
- 50 kV/μs typical transient immunity
- Fail-safe receiver for bus open, short, idle
- 3.3-V inputs are 5-V tolerant
- Safety and regulatory approvals
  - 4000-V<sub>PK</sub> V<sub>IOTM</sub>, 560-V<sub>PK</sub> V<sub>IORM</sub> per DIN EN IEC 60747-17 (VDE 0884-17)
  - 2500 V<sub>RMS</sub> isolation rating per UL 1577
  - 2500 V<sub>RMS</sub> isolation rating per CSA 62368-1.

### 2 Applications

- Security systems
- Chemical production
- Factory automation
- Motor and motion control
- HVAC and building automation networks
- Networked security stations

### 3 Description

The ISO15 is an isolated half-duplex differential line transceiver while the ISO35 is an isolated full-duplex differential line driver and receiver for TIA/EIA 485/422 applications. The ISO15M and ISO35M have extended ambient temperature ratings of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  while the ISO15 and ISO35 are specified over  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

These devices are ideal for long transmission lines because the ground loop is broken to allow for a much larger common-mode voltage range. The symmetrical barrier of the device is tested to provide isolation of 4000 V<sub>PK</sub> per VDE and 2500 V<sub>RMS</sub> per UL and CSA between the bus-line transceiver and the logic-level interface.

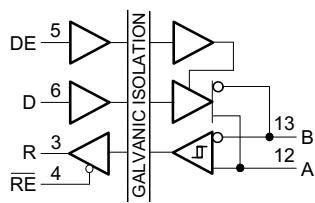
Any cabled I/O can be subjected to electrical noise transients from various sources. These noise transients can cause damage to the transceiver and/or nearby sensitive circuitry if they are of sufficient magnitude and duration. These isolated devices can significantly increase protection and reduce the risk of damage to expensive control circuits.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO15	SOIC (16)	10.30 mm $\times$ 7.50 mm
ISO35		

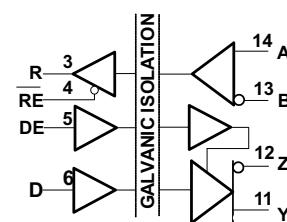
(1) For all available packages, see the orderable addendum at the end of the data sheet.

ISO15x



Simplified Schematic

ISO35x



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision G (March 2015) to Revision H (August 2023)</b>	<b>Page</b>
• Updated the CSA standard to CSA 62368-1, Updated VDE standard to DIN EN IEC 60747-17 (VDE 0884-17).....	<b>1</b>
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	<b>1</b>
• Updated Thermal Characteristics, Safety Limiting Values, and Thermal Derating Curves to provide more accurate system-level thermal calculations.....	<b>7</b>

<b>Changes from Revision F (January 2012) to Revision G (October 2014)</b>	<b>Page</b>
• Added <i>Pin Configuration and Functions</i> section, <i>ESD Rating</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	<b>1</b>
• Changed VDE standard to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12. ....	<b>1</b>

<b>Changes from Revision E (April 2010) to Revision F (January 2012)</b>	<b>Page</b>
• Changed the FEATURES From: 4000-V <sub>peak</sub> 560-V <sub>peak</sub> V <sub>IORM</sub> per IEC....Rev 2) To: 4000-V <sub>PK</sub> V <sub>IOTM</sub> , 560-V <sub>PK</sub> V <sub>IORM</sub> , IEC 60747-5-2 (VDE 0884, Rev 2).....	<b>1</b>
• Changed Description From: The symmetrical isolation.....interface. To; The symmetrical isolation barrier of the device is tested to provide isolation of 4000 V <sub>PK</sub> per VDE and 2500 V <sub>RMS</sub> per UL and CSA between ....interface.....	<b>1</b>
• Updated electrical and switching characteristics to match device performance.....	<b>9</b>

<b>Changes from Revision D (March 2009) to Revision E (April 2010)</b>	<b>Page</b>
• Added devices ISO15M and ISO35M to the data sheet.....	<b>1</b>
• Changed Description - From: The ISO15 and ISO35 are qualified for use from -40°C to 85°C. To: The ISO15M and ISO35M have extended ambient temperature ratings of -55°C to 125°C while the ISO15 and ISO35 are specified over -40°C to 85°C.....	<b>1</b>
• Added the Driver output pins Note for <a href="#">Figure 7-1</a> through <a href="#">Figure 7-4</a> .....	<b>14</b>

- Changed the Driver output pins Note for [Figure 7-5](#) through [Figure 7-6](#) ..... [14](#)

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<b>Changes from Revision B (July 2008) to Revision C (December 2008)</b>	<b>Page</b>
• Added added IEC.....Approved.....	<a href="#">1</a>

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<b>Changes from Revision A (June 2008) to Revision B (July 2008)</b>	<b>Page</b>
• Changed From: 4000-Vpeak Isolation To: 4000-Vpeak Isolation, 560-Vpeak VIORM UL 1577, IEC 60747-5-2 (VDE 0884, Rev 2).....	<a href="#">1</a>
• Changed <a href="#">Figure 7-13</a> , Full-Duplex Common-Mode Transient Immunity Test Circuit.....	<a href="#">14</a>

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## 5 Pin Configuration and Functions

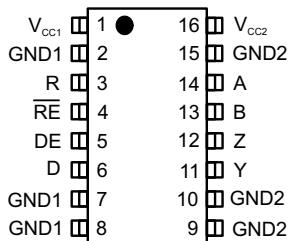


Figure 5-1. ISO35x DW Package  
16-Pin SOIC  
Top View

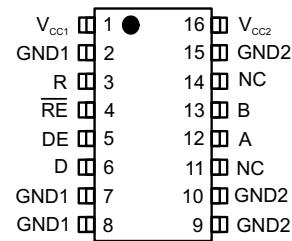


Figure 5-2. ISO15x DW Package  
16-Pin SOIC  
Top View

Table 5-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	ISO15x NO.	ISO35x NO.		
A	12	14	I/O	ISO15x: Noninverting bus input or output
			I	ISO35x: Noninverting bus input
B	13	13	I/O	ISO15x: Inverting bus input or output
			I	ISO35x: Inverting bus input
D	6	6	I	Driver input
DE	5	5	I	Driver logic-high enable input
GND1	2,7,8	2,7,8	—	Logic side ground; internally connected
GND2	9,10,15	9,10,15	—	Bus side ground; internally connected
NC	11,14	—	—	Not connected internally; may be left floating
R	3	3	O	Receiver output
RE	4	4	I	Receiver logic-low enable
V <sub>CC1</sub>	1	1	—	Logic side power supply
V <sub>CC2</sub>	16	16	—	Bus side power supply
Y	—	11	O	Noninverting bus output
Z	—	12	O	Inverting bus output

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC1</sub>	Supply voltage, side 1 <sup>(2)</sup>	-0.3	6	V
V <sub>CC2</sub>	Supply voltage, side 2 <sup>(2)</sup>	-0.3	6	V
V <sub>O</sub>	Voltage at any bus I/O terminal	-9	14	V
V <sub>it</sub>	Voltage input, transient pulse, A, B, Y, and Z (through 100Ω, see Figure 13)	-50	50	V
V <sub>I</sub>	Voltage input at any D, DE or RE terminal	-0.5	6	V
I <sub>O</sub>	Receiver output current	-10	10	mA
T <sub>J</sub>	Junction temperature		150	°C
T <sub>STG</sub>	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	Bus pins and GND1	±6000	V
V <sub>(ESD)</sub>	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	Bus pins and GND2	±16000	V
V <sub>(ESD)</sub>	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	All pins	±4000	V
V <sub>(ESD)</sub>	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>		±1000	V
V <sub>(ESD)</sub>	Machine model ANSI/ESDS5.2-1996		±200	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V <sub>CC1</sub>	Supply Voltage, Side 1	3.15	3.3	3.6	V
V <sub>CC2</sub>	Supply Voltage, Side 2	3.15	3.3	3.6	V
V <sub>OC</sub>	Common Mode voltage at any bus terminal: A or B	-7		12	V
V <sub>IH</sub>	High-level input voltage (D, DE, RE inputs)	2		V <sub>CC1</sub>	V
V <sub>IL</sub>	Low-level input voltage (D, DE, RE inputs)	0		0.8	V
V <sub>ID</sub>	Differential input voltage, A with respect to B	-12		12	V
R <sub>L</sub>	Differential load resistance	54	60		Ω
I <sub>O</sub>	Output current, Driver	-60		60	mA
1/t <sub>UI</sub>	Signaling rate ISO15x and ISO35x			1	Mbps
T <sub>A</sub>	Operating ambient temperature (ISO15 and ISO35)	-40	25	85	°C
	Operating ambient temperature (ISO15M and ISO35M)	-55	25	125	°C

		MIN	TYP	MAX	UNIT
$T_J$	Operating junction temperature (ISO15 and ISO35)	-40		150	°C
	Operating junction temperature (ISO15M and ISO35M)	-55		150	°C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		ISO15, ISO35	UNIT
		DW (SOIC)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	79.6	°C/W
$R_{\theta JC(\text{top})}$	Junction-to-case (top) thermal resistance	39.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.6	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	11.8	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	44	°C/W
$R_{\theta JC(\text{bot})}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

## 6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_D$		$V_{CC1} = V_{CC2} = 3.6$ V, $T_J = 150$ °C, $C_L = 15$ pF, Input a 0.5 MHz 50% duty cycle square wave	220		mW	

## 6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
			DW-16	
CLR	External clearance <sup>(1)</sup>	Shortest terminal-to-terminal distance through air	8	mm
CPG	External creepage <sup>(1)</sup>	Shortest terminal-to-terminal distance across the package surface	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	8	um
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>400	V
	Material group	According to IEC 60664-1	II	
	Overvoltage category per IEC 60664-1	Rated mains voltage $\leq 150$ V <sub>RMS</sub>	I-IV	
		Rated mains voltage $\leq 300$ V <sub>RMS</sub>	I-III	

### DIN EN IEC 60747-17 (VDE 0884-17) <sup>(2)</sup>

$V_{IORM}$	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	560	$V_{PK}$
$V_{IOTM}$	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$ , $t = 60$ s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$ , $t = 1$ s (100% production)	4000	$V_{PK}$
$q_{pd}$	Apparent charge <sup>(3)</sup>	Method b; At routine test (100% production) $V_{ini} = 1.2 \times V_{IOTM}$ , $t_{ini} = 1$ s; $V_{pd(m)} = 1.5 \times V_{IORM}$ , $t_m = 1$ s	$\leq 5$	pC
$C_{IO}$	Barrier capacitance, input to output <sup>(4)</sup>	$V_{IO} = 0.4 \times \sin(2\pi ft)$ , $f = 1$ MHz	2	pF
$C_I$	Input capacitance to ground	$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi ft)$ , $f = 1$ MHz, $V_{CC} = 3.3$ V	2	pF
$R_{IO}$	Isolation resistance <sup>(4)</sup>	$V_{IO} = 500$ V, $T_A = 25$ °C	$>10^{12}$	$\Omega$
		$V_{IO} = 500$ V, $T_S = 150$ °C	$>10^9$	
	Pollution degree		2	
	Climatic Category		40/125/21	
<b>UL 1577</b>				

PARAMETER		TEST CONDITIONS	VALUE DW-16	UNIT
V <sub>ISO</sub>	Maximum withstanding isolation voltage	V <sub>TEST</sub> = V <sub>ISO</sub> , t = 60 s (qualification), V <sub>TEST</sub> = 1.2 x V <sub>ISO</sub> , t = 1 s (100% production)		
			2500	V <sub>RMS</sub>

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.
- (2) This coupler is suitable for *basic electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (4) All pins on each side of the barrier tied together creating a two-terminal device.

## 6.7 Safety-Related Certifications

VDE	CSA	UL
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to IEC 60950-1 and IEC 62368-1	Certified according to UL 1577 Component Recognition Program
Basic insulation, 4000 V <sub>PK</sub> Maximum transient isolation voltage, 560 V <sub>PK</sub> Maximum repetitive peak isolation voltage	2500 V <sub>RMS</sub> Isolation rating, Reinforced insulation per CSA 60950-1 and IEC 60950-1 148V <sub>RMS</sub> working voltage; Basic insulation per CSA 62368-1 and IEC 62368-1 300V <sub>RMS</sub> working voltage	Single protection, 2500 V <sub>RMS</sub>
Certificate number: 40047657	Master contract number: 220991	File number: E181974

## 6.8 Safety Limiting Values

Safety limiting<sup>(1)</sup> intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DW-16 PACKAGE</b>						
I <sub>S</sub>	Safety input, output, or supply current	R <sub>θJA</sub> = 79.6°C/W, V <sub>I</sub> = 3.6 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C.			436	mA
T <sub>S</sub>	Maximum safety temperature				150	°C

- (1) The maximum safety temperature, T<sub>S</sub>, has the same value as the maximum junction temperature, T<sub>J</sub>, specified for the device. The I<sub>S</sub> and P<sub>S</sub> parameters represent the safety current and safety power respectively. The maximum limits of I<sub>S</sub> and P<sub>S</sub> should not be exceeded. These limits vary with the ambient temperature, T<sub>A</sub>.  
The junction-to-air thermal resistance, R<sub>θJA</sub>, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:  
T<sub>J</sub> = T<sub>A</sub> + R<sub>θJA</sub> × P, where P is the power dissipated in the device.  
T<sub>J(max)</sub> = T<sub>S</sub> = T<sub>A</sub> + R<sub>θJA</sub> × P<sub>S</sub>, where T<sub>J(max)</sub> is the maximum allowed junction temperature.  
P<sub>S</sub> = I<sub>S</sub> × V<sub>I</sub>, where V<sub>I</sub> is the maximum input voltage.

## 6.9 Electrical Characteristics: Driver

All typical specs are at  $V_{CC1}=3.3V$ ,  $V_{CC2}=5V$ ,  $T_A=27^\circ C$ , (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$ V_{OD} $ Driver differential-output voltage magnitude	$I_O = 0 \text{ mA}$ , no load	2.5		$V_{CC2}$	V	
	$R_L = 54 \Omega$ , See Figure 3	1.5	2		V	
	$R_L = 100 \Omega$ (RS-422), See Figure 3	2	2.3		V	
	$V_{test}$ from $-7 \text{ V}$ to $+12 \text{ V}$ , See Figure 4	1.5			V	
$\Delta V_{OD} $	Change in differential output voltage between two states	-200		200	mV	
$V_{OC}$	Common-mode output voltage	See Figure 5	1	2.6	3	V
$\Delta V_{OC(ss)}$	change in steady-state common-mode output voltage between two states	See Figure 5	-100	100	mV	
$V_{OC(pp)}$	Peak-to-peak common-mode output voltage	See Figure 5		0.5	V	
$I_I$	Input current	D, DE, $V_I$ at 0 V or $V_{CC1}$	-10	10	$\mu\text{A}$	
$I_{OZ}$ High-impedance state output current	ISO15 See receiver input current					
	ISO35 $V_Y$ or $V_Z = 12 \text{ V}$		90		$\mu\text{A}$	
	ISO35 $V_Y$ or $V_Z = 12 \text{ V}$ , $V_{CC} = 0$		90		$\mu\text{A}$	
	ISO35 $V_Y$ or $V_Z = -7 \text{ V}$	-10			$\mu\text{A}$	
	ISO35 $V_Y$ or $V_Z = -7 \text{ V}$ , $V_{CC} = 0$	-10			$\mu\text{A}$	
$I_{OS}$ Short-circuit output current	$V_A$ or $V_B$ at $-7 \text{ V}$	-250		250	mA	
	$V_A$ or $V_{BAT}$ 12 V	-250		250	mA	
$C_{OD}$	Differential output capacitance	$V_I = 0.4 \sin(4E6\pi t) + 0.5 \text{ V}$ , DE at 0 V		16	$\text{pF}$	
CMTI	Common-mode transient immunity	$V_I = V_{CC}$ or 0 V, See Figure 14 and Figure 15	25	50	$\text{kV}/\mu\text{s}$	

## 6.10 Electrical Characteristics: Receiver

All typical specs are at  $V_{CC1}=3.3V$ ,  $V_{CC2}=5V$ ,  $T_A=27^\circ C$ , (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT+}$	Positive-going input threshold voltage	$I_O = -8 \text{ mA}$		-20	mV
$V_{IT-}$	Negative-going input threshold voltage	$I_O = 8 \text{ mA}$	-200		mV
$V_{hys}$	Input hysteresis ( $V_{IT+} - V_{IT-}$ )			50	mV
$V_O$ Output Voltage	$V_{ID} = 200\text{mV}$ , $I_O = -8\text{mA}$	2.4			V
	$V_{ID} = -200\text{mV}$ , $I_O = 8\text{mA}$			0.4	V
$I_{OZ}$	Output high-impedance current on the R pin	$V_I = -7$ to $12 \text{ V}$ , Other input = 0 V	-1	1	$\mu\text{A}$
$I_A$ or $I_B$ Bus input current	$-55^\circ C \leq T_A \leq 85^\circ C$ $V_A$ or $V_B = 12 \text{ V}$		50	100	$\mu\text{A}$
	$-55^\circ C \leq T_A \leq 85^\circ C$ $V_A$ or $V_B = 12 \text{ V}$ , $V_{CC} = 0$		50	100	$\mu\text{A}$
	$85^\circ C \leq T_A \leq 125^\circ C$ $V_A$ or $V_B = 12 \text{ V}$		200		$\mu\text{A}$
	$85^\circ C \leq T_A \leq 125^\circ C$ $V_A$ or $V_B = 12 \text{ V}$ , $V_{CC} = 0$		200		$\mu\text{A}$
	$-55^\circ C \leq T_A \leq 125^\circ C$ $V_A$ or $V_B = -7 \text{ V}$	-100	-40		$\mu\text{A}$
	$-55^\circ C \leq T_A \leq 125^\circ C$ $V_A$ or $V_B = -7 \text{ V}$ , $V_{CC} = 0$	-100	-30		$\mu\text{A}$
$I_{IH}$	High-level input current, RE	$V_{IH} = 2 \text{ V}$	-10		$\mu\text{A}$

All typical specs are at  $V_{CC1}=3.3V$ ,  $V_{CC2}=5V$ ,  $T_A=27^\circ C$ , (Min/Max specs are over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{IL}$	Low-level input current, RE	$V_{IL} = 0.8 V$	-10			$\mu A$
$R_{ID}$	Differential input resistance	A, B	48			kohm
$C_{ID}$	Differential input capacitance	$V_I = 0.4 \sin(4E6\pi t) + 0.5V$ , DE at 0 V		16		pF

## 6.11 Supply Current

Bus loaded or unloaded (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DRIVER ENABLED, RECEIVER DISABLED</b>					
I <sub>CC1</sub>	ISO35x and ISO15x: RE at 0 V or V <sub>CC</sub> , DE at 0 V, No load (driver disabled)			8	mA
I <sub>CC1</sub>	ISO35x and ISO15x: RE at 0 V or V <sub>CC</sub> , DE at V <sub>CC</sub> , No load (driver enabled)			8	mA
I <sub>CC2</sub>	ISO35x and ISO15x: RE at 0 V or V <sub>CC</sub> , DE at 0 V, No load (driver disabled)			15	mA
I <sub>CC2</sub>	ISO35x and ISO15x: RE at 0 V or V <sub>CC</sub> , DE at V <sub>CC</sub> , No Load (driver enabled)			19	mA

## 6.12 Switching Characteristics: Driver

All typical specs are at  $V_{CC1}=3.3V$ ,  $V_{CC2}=3.3V$ ,  $T_A=27^\circ C$ , (Min/Max specs are over recommended operating conditions unless otherwise noted)

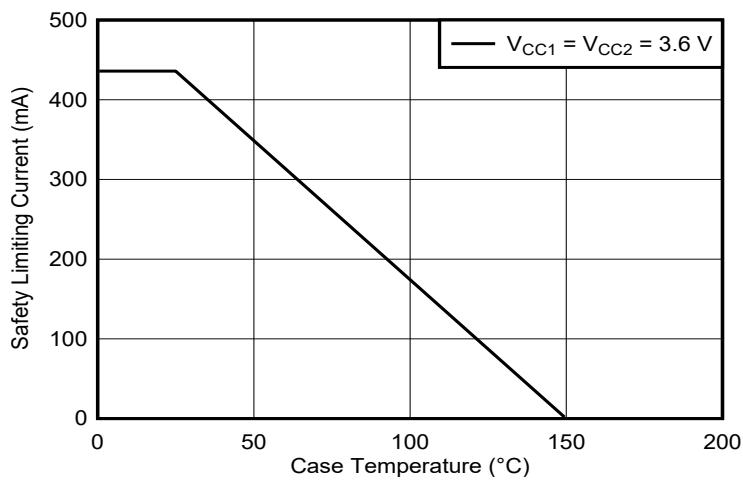
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>500-kbps DEVICES</b>					
$t_r, t_f$	Differential output rise time and fall time	ISO15M and ISO35M	120	180	350
$t_{PHZ}$	Propagation delay, high-level-to-high-impedance output	See Figure 7		205	ns
$t_{PLZ}$	Propagation delay, low-level to high-impedance output	See Figure 8		330	ns
$t_{PZL}$	Propagation delay, standby-to-low-level output	See Figure 8		530	ns
$t_{PHL}, t_{PLH}$	Propagation delay	See Figure 6		340	ns
$tsk(p)$	Pulse skew ( $ t_{PHL} - t_{PLH} $ )	See Figure 6		6	ns
$t_r, t_f$	Differential output rise time and fall time	ISO15 and ISO35	120	180	300
$t_{PZH}$	Propagation delay, high-impedance-to-high-level output	See Figure 7		530	ns

## 6.13 Switching Characteristics: Receiver

All typical specs are at  $V_{CC1}=3.3V$ ,  $V_{CC2}=3.3V$ ,  $T_A=27^\circ C$ , (Min/Max specs are over recommended operating conditions unless otherwise noted)

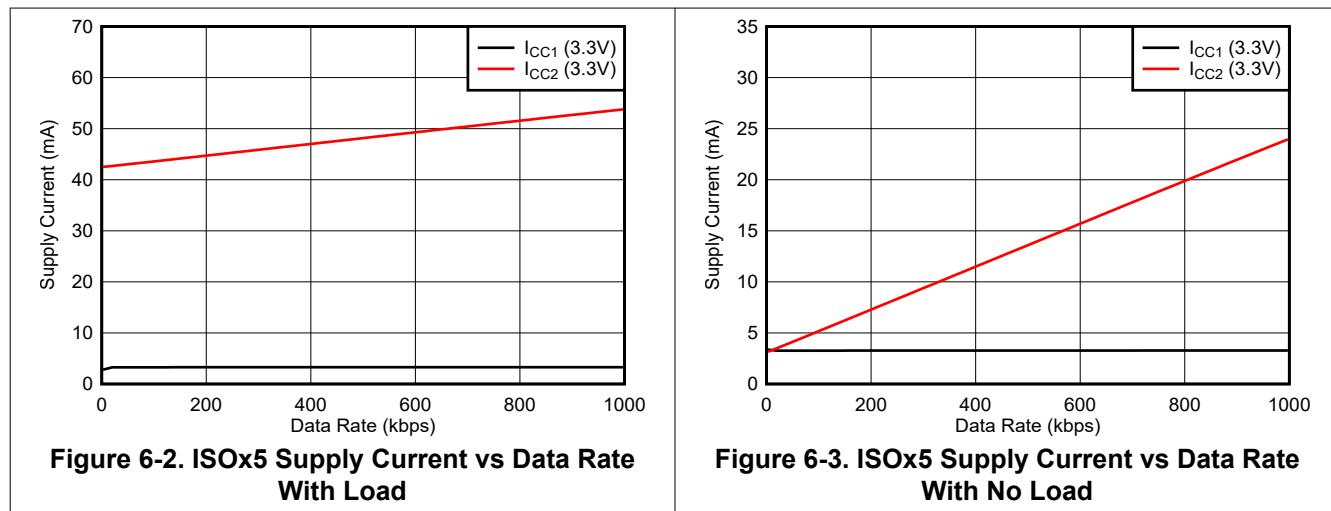
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>500-kbps DEVICES</b>					
$t_{PHL}, t_{PLH}$	Propagation delay	See Figure 10		100	ns
$tsk(p)$	Pulse skew ( $ t_{PHL} - t_{PLH} $ )	ISO15 and ISO35		13	ns
$tsk(p)$	Pulse skew ( $ t_{PHL} - t_{PLH} $ )	ISO15M and ISO35M		18	ns
$t_r, t_f$	Differential output rise time and fall time	ISO15 and ISO35		2	4
$t_r, t_f$	Differential output rise time and fall time	ISO15M and ISO35M		2	6
$t_{PHZ}, t_{PLZ}$	Propagation delay, high-impedance-to-high-level output, Propagation delay, high-impedance-to-low-level output	DE at 0 V, See Figure 11 and Figure 12		13	25
$t_{PZH}, t_{PZL}$	Propagation delay, high-level-to-high-impedance output, Propagation delay, low-level to high-impedance output	DE at 0 V, See Figure 11 and Figure 12		13	25

## 6.14 Insulation Characteristics Curves



**Figure 6-1. Thermal Derating Curve for Safety Limiting Power for DW-16 Package**

## 6.15 Typical Characteristics



## 7 Parameter Measurement Information

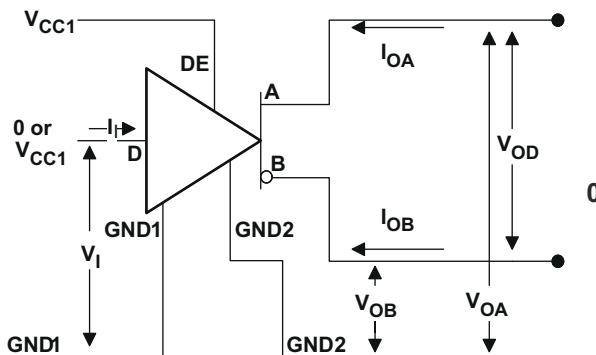


Figure 7-1. Driver  $V_{OD}$  Test and Current Definitions

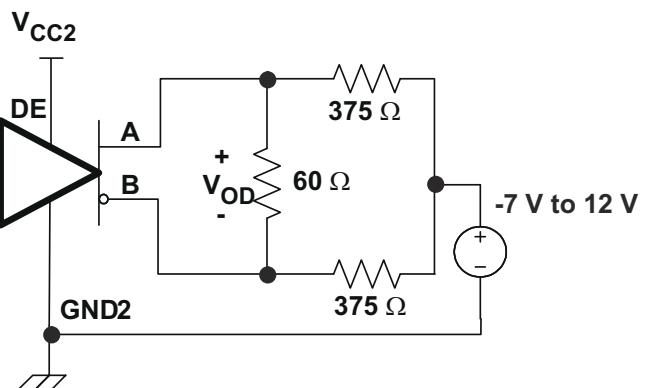


Figure 7-2. Driver  $V_{OD}$  With Common-Mode Loading Test Circuit

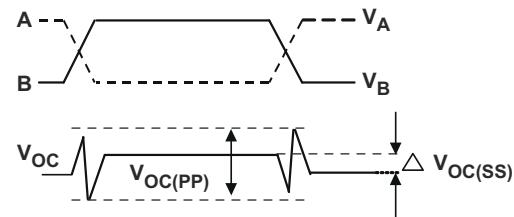
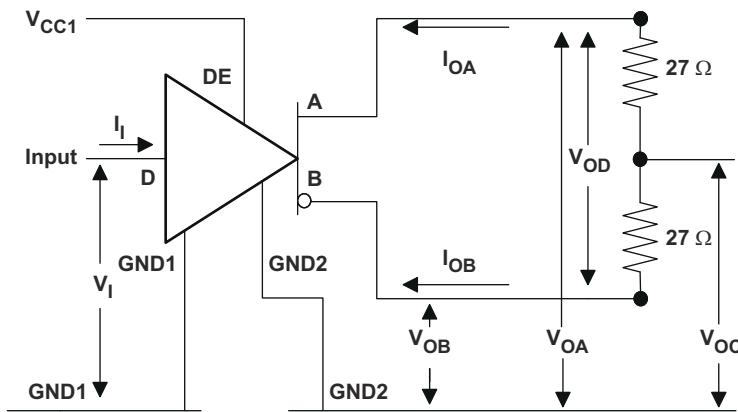
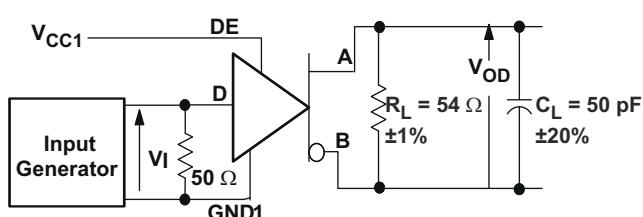


Figure 7-3. Test Circuit and Waveform Definitions for the Driver Common-Mode Output Voltage



Generator: PRR = 500 kHz, 50% duty cycle,  $t_r < 6$  ns,  $t_f < 6$  ns,  $Z_O = 50 \Omega$

$C_L$  includes fixture and Instrumentation Capacitance

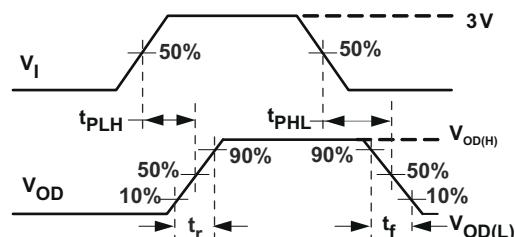


Figure 7-4. Driver Switching Test Circuit and Voltage Waveforms

### Note

Driver output pins are A and B for the ISO15 (see Figure 7-1 through Figure 7-4). These correspond to ISO35 pins Y and Z

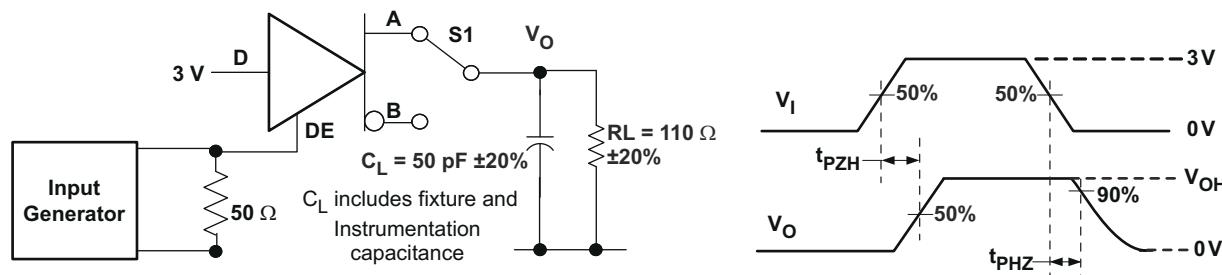


Figure 7-5. Driver High-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

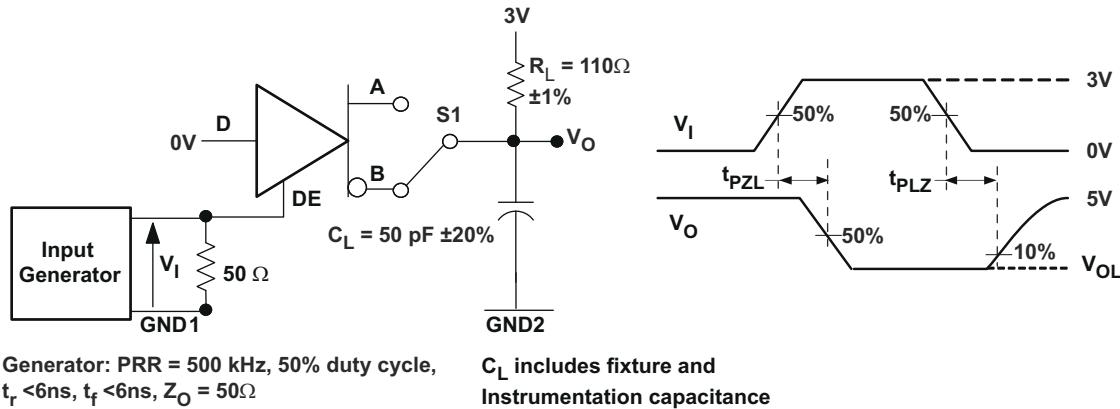


Figure 7-6. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveform

#### Note

Driver output pins are A and B for the ISO15 (see Figure 7-5 through Figure 7-6). These correspond to ISO35 pins Y and Z

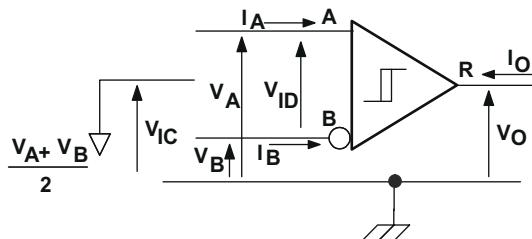


Figure 7-7. Receiver Voltage and Current Definitions

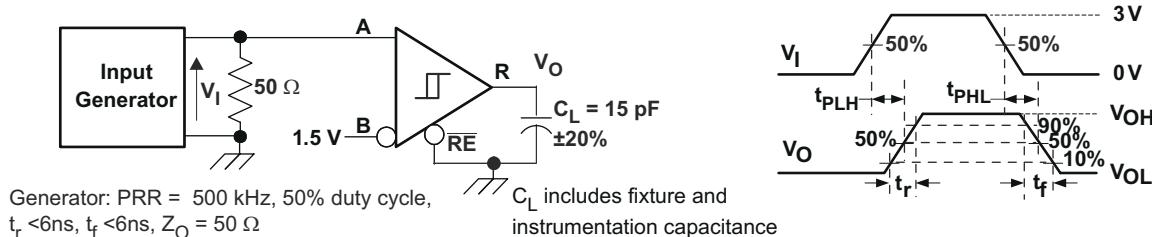


Figure 7-8. Receiver Switching Test Circuit and Waveforms

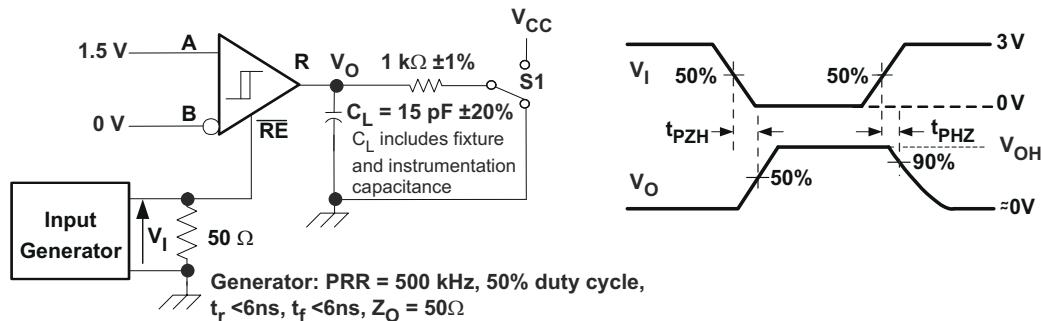


Figure 7-9. Receiver Enable Test Circuit and Waveforms, Data Output High

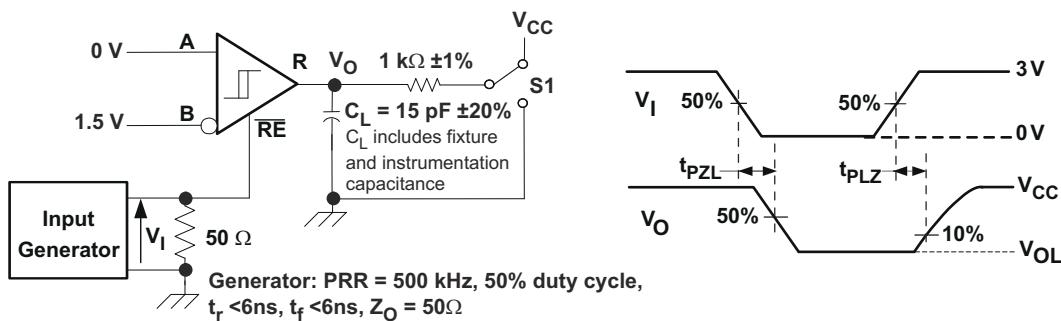
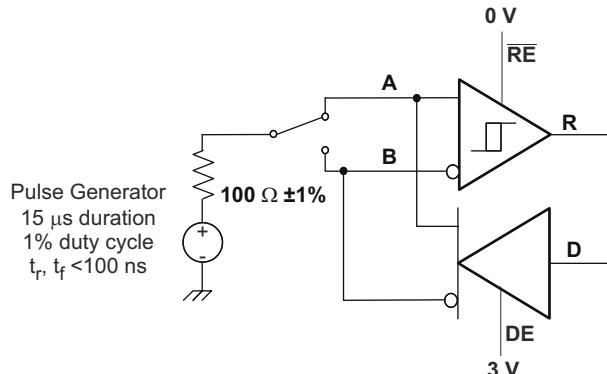


Figure 7-10. Receiver Enable Test Circuit and Waveforms, Data Output Low



Note: This test is conducted to test survivability only.  
Data stability at the R output is not specified.

Figure 7-11. Transient Overvoltage Test Circuit

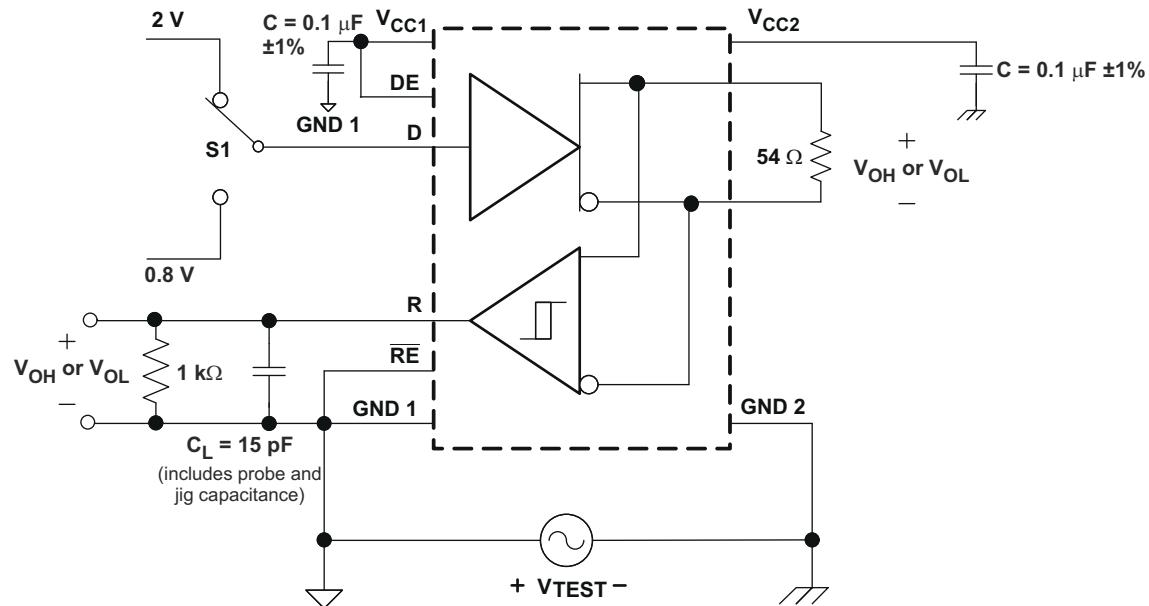
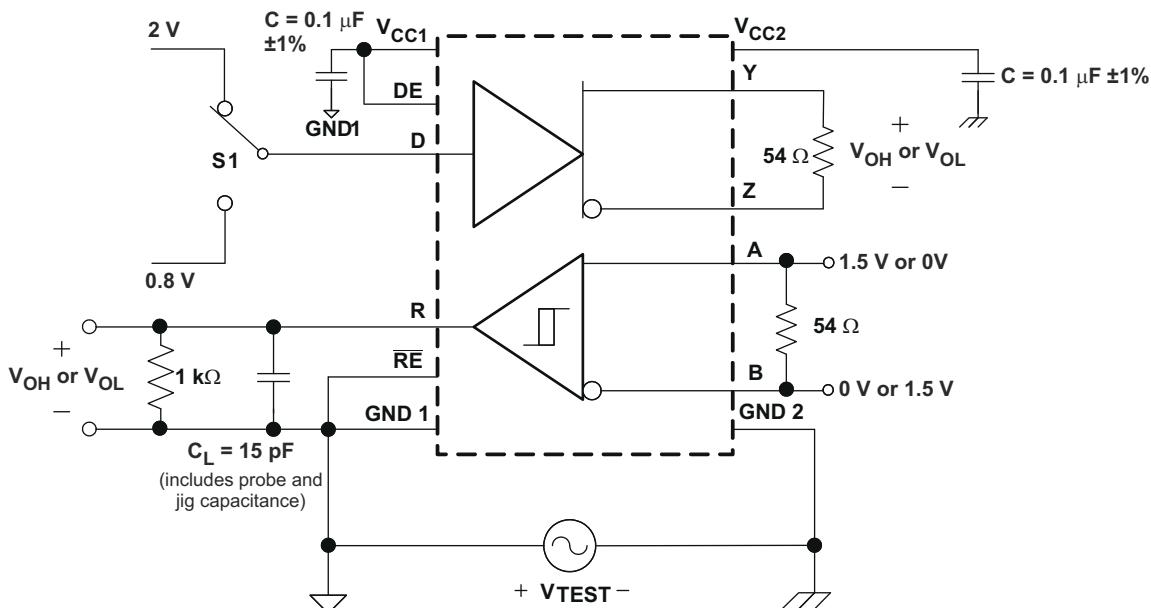


Figure 7-12. Half-Duplex Common-Mode Transient Immunity Test Circuit



**Figure 7-13. Full-Duplex Common-Mode Transient Immunity Test Circuit**

## 8 Detailed Description

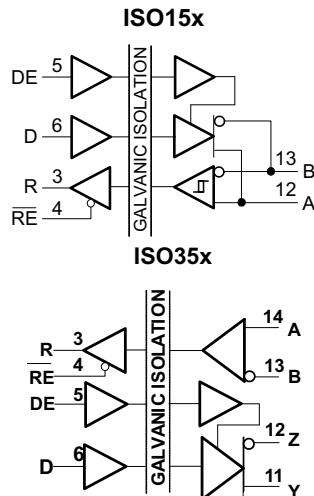
### 8.1 Overview

The ISO15 and ISO15M are isolated half-duplex differential line drivers and receivers while the ISO35 and ISO35M are isolated full-duplex differential line transceivers for TIA/EIA 485/422 applications. They are rated to provide galvanic isolation of up to 2500 V<sub>rms</sub> for 60 sec as per the standard. They have active-high driver enables and active-low receiver enables to control the data flow.

When the driver enable pin, DE, is logic high, the differential outputs Y and Z follow the logic states at data input D. A logic high at D causes Y to turn high and Z to turn low. In this case the differential output voltage defined as  $V_{OD} = V_{(Y)} - V_{(Z)}$  is positive. When D is low, the output states reverse, Z turns high, Y becomes low, and  $V_{OD}$  is negative. When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pulldown resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pullup resistor to V<sub>CC</sub>, thus, when left open while the driver is enabled, output Y turns high and Z turns low.

When the receiver enable pin, RE, is logic low, the receiver is enabled. When the differential input voltage defined as  $V_{ID} = V_{(A)} - V_{(B)}$  is positive and higher than the positive input threshold,  $V_{IT+}$ , the receiver output, R, turns high. When  $V_{ID}$  is negative and less than the negative and lower than the negative input threshold,  $V_{IT-}$ , the receiver output, R, turns low. If  $V_{ID}$  is between  $V_{IT+}$  and  $V_{IT-}$  the output is indeterminate. When RE is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of  $V_{ID}$  are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

### 8.2 Functional Block Diagrams



### 8.3 Device Functional Modes

Table 8-1. Driver Function Table<sup>(2)</sup>

V <sub>CC1</sub>	V <sub>CC2</sub>	INPUT (D)	ENABLE INPUT (DE)	OUTPUTS <sup>(1)</sup>	
				Y / A	Z / B
PU	PU	H	H	H	L
PU	PU	L	H	L	H
PU	PU	X	L	Hi-Z	Hi-Z
PU	PU	X	OPEN	Hi-Z	Hi-Z
PU	PU	OPEN	H	H	L
PD	PU	X	X	Hi-Z	Hi-Z
PU	PD	X	X	Hi-Z	Hi-Z

**Table 8-1. Driver Function Table<sup>(2)</sup> (continued)**

<b>V<sub>CC1</sub></b>	<b>V<sub>CC2</sub></b>	<b>INPUT (D)</b>	<b>ENABLE INPUT (DE)</b>	<b>OUTPUTS<sup>(1)</sup></b>	
				<b>Y / A</b>	<b>Z / B</b>
PD	PD	X	X	Hi-Z	Hi-Z

(1) Driver output pins are Y and Z for full-duplex devices and A & B for half-duplex devices.

(2) PU = Powered Up; PD = Powered Down; H = Logic High; L = Logic Low; X = Irrelevant, Hi-Z = High Impedance (off)

**Table 8-2. Receiver Function Table<sup>(1)</sup>**

<b>V<sub>cc1</sub></b>	<b>V<sub>cc2</sub></b>	<b>DIFFERENTIAL INPUT V<sub>ID</sub> = (V<sub>A</sub> – V<sub>B</sub>)</b>	<b>ENABLE (R̄E)</b>	<b>OUTPUT (R)</b>
PU	PU	–0.01 V ≤ V <sub>ID</sub>	L	H
PU	PU	–0.2 V < V <sub>ID</sub> < –0.01 V	L	?
PU	PU	V <sub>ID</sub> ≤ –0.2 V	L	L
PU	PU	X	H	Hi-Z
PU	PU	X	OPEN	Hi-Z
PU	PU	Open circuit	L	H
PU	PU	Short Circuit	L	H
PU	PU	Idle (terminated) bus	L	H
PD	PU	X	X	Hi-Z
PU	PD	X	L	H

(1) PU = Powered Up; PD = Powered Down; H = Logic High; L = Logic Low; X = Irrelevant, Hi-Z = High Impedance (off), ? = Indeterminate

### 8.3.1 Device I/O Schematics

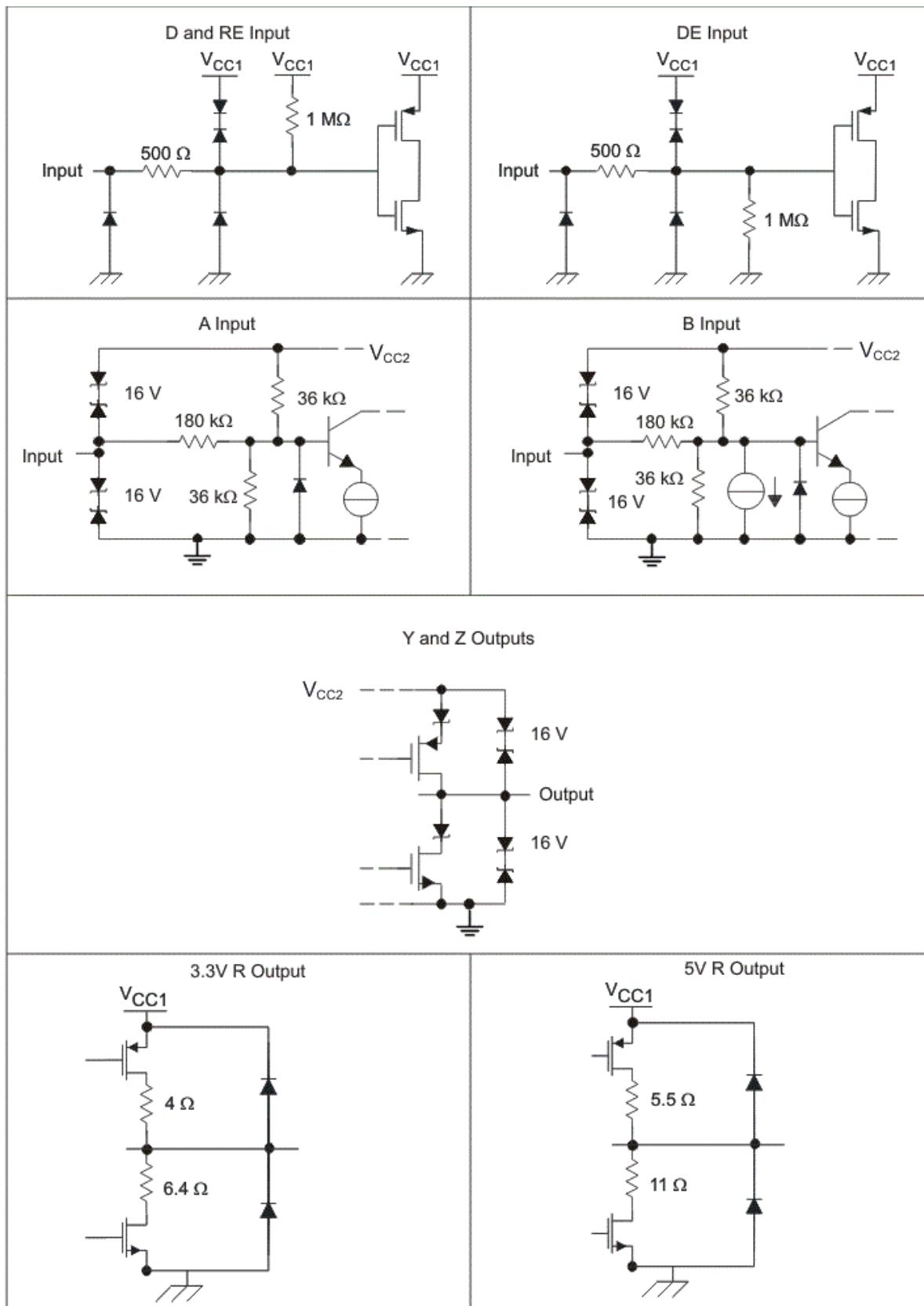


Figure 8-1. Device I/O Schematics

## 9 Application and Implementation

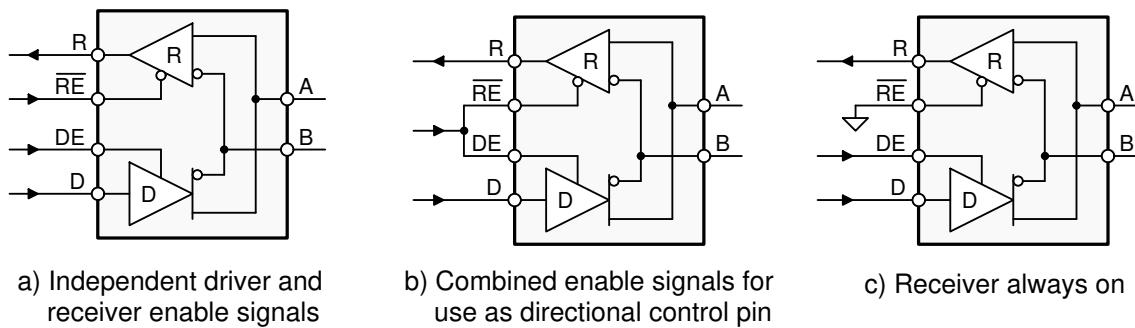
### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

The ISO15x and ISO35x family consists of RS-485 transceivers commonly used for asynchronous data transmissions. Full-duplex implementation requires two signal pairs (four wires), and allows each node to transmit data on one pair while simultaneously receiving data on the other pair. For half-duplex transmission there is only one pair which is shared for both transmission and reception of data. To eliminate line reflections, each cable end is terminated with a termination resistor,  $R(T)$ , whose value matches the characteristic impedance,  $Z_0$ , of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

### 9.2 Typical Application



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Figure 9-1. Half-Duplex Transceiver Configurations

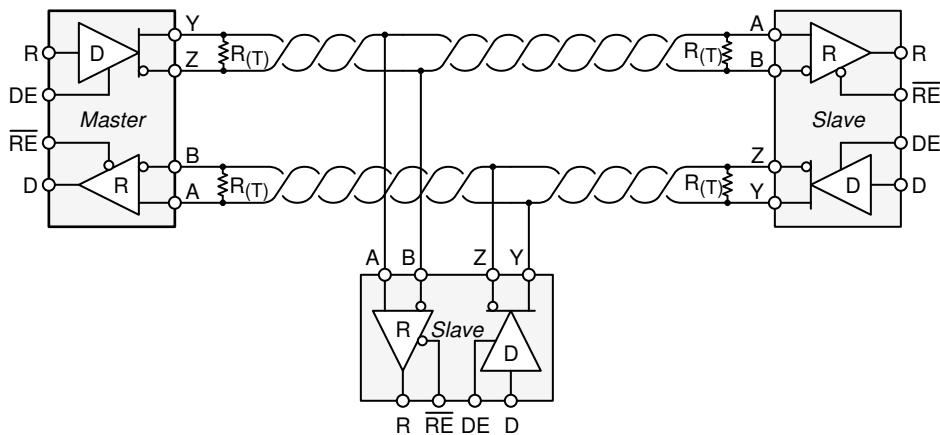


Figure 9-2. Typical RS-485 Network With Full-Duplex Transceivers

### 9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

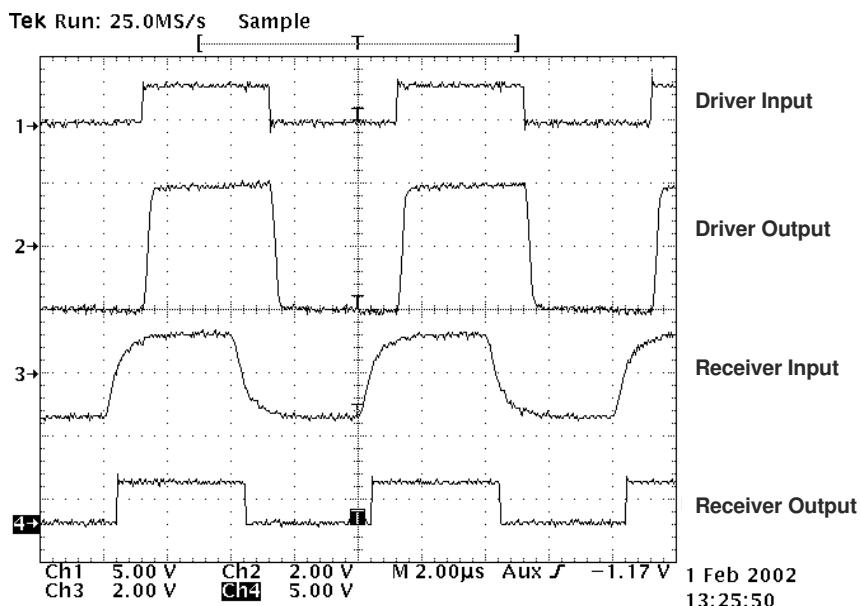
**Table 9-1. Design Parameters**

PARAMETER	VALUE
Pullup and Pulldown Resistors	1 kΩ to 10 kΩ
Decoupling Capacitors	100 nF

### 9.2.2 Detailed Design Procedure

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable length. When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a nonterminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver. The RS-485 standard specifies that a compliant driver must be able to drive 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because these devices consist of 1/8 UL transceivers, connecting up to 256 receivers to the bus is possible.

### 9.2.3 Application Curve



**Figure 9-3. Typical Input and Output Waveforms**

## Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, a 0.1- $\mu$ F bypass capacitor is recommended at input and output supply pins ( $V_{CC1}$  and  $V_{CC2}$ ). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501. For such applications, detailed power supply design and transformer selection recommendations are available in SN6501 data sheet ([SLLSEA0](#)).

## 10 Layout

### 10.1 Layout Guidelines

On-chip IEC-ESD protection is good for laboratory and portable equipment but never sufficient for EFT and surge transients occurring in industrial environments. Therefore robust and reliable bus node design requires the use of external transient protection devices. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3-MHz to 3-GHz, highfrequency layout techniques must be applied during PCB design. A minimum of four layers is required to accomplish a low EMI PCB design (see [Figure 10-1](#)).

- Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.
- Place the protection circuitry close to the bus connector to prevent noise transients from penetrating the board.
- Use VCC and ground planes to provide low-inductance. High-frequency currents might follow the path of least inductance and not necessarily the path of least resistance.
- Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
- Apply 100-nF to 220-nF bypass capacitors as close as possible to the VCC-pins of transceiver, UART, controller ICs on the board (see [Figure 10-1](#)).
- Use at least two vias for VCC and ground connections of bypass capacitors and protection devices to minimize effective via-inductance (see [Figure 10-1](#)).
- Use 1-k $\Omega$  to 10-k $\Omega$  pullup and pulldown resistors for enable lines to limit noise currents in these lines during transient events (see [Figure 10-1](#)).
- Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up (see [Figure 10-1](#)).
- While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.
- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in<sup>2</sup>.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

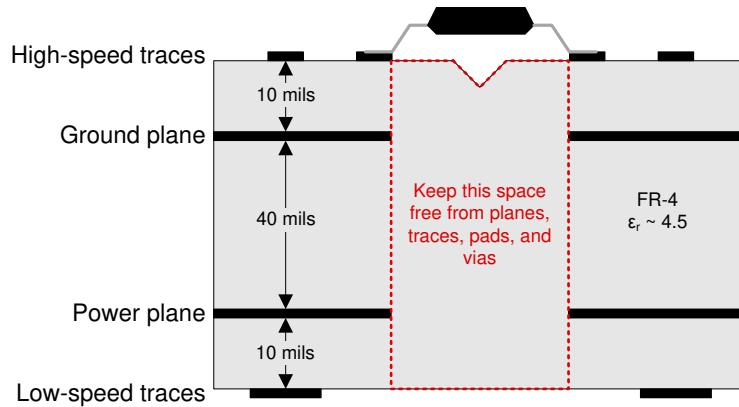
If an additional supply voltage plane or signal layer is needed, add a second power and ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

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#### Note

For detailed layout recommendations, see Application Note [SLLA284, Digital Isolator Design Guide](#).

## 10.2 Layout Example



**Figure 10-1. Recommended Layer Stack**

## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Digital Isolator Design Guide](#) data sheet
- Texas Instruments, [Transformer Driver for Isolated Power Supplies](#) application report
- Texas Instruments, [Isolation Glossary](#) application report

### 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 11.4 Trademarks

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### 11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO15DW	Obsolete	Production	SOIC (DW)   16	-	-	Call TI	Call TI	-40 to 85	ISO15
ISO15DWR	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO15
ISO15DWR.A	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO15
ISO15MDW	Obsolete	Production	SOIC (DW)   16	-	-	Call TI	Call TI	-55 to 125	ISO15M
ISO15MDWR	Obsolete	Production	SOIC (DW)   16	-	-	Call TI	Call TI	-55 to 125	ISO15M
ISO35DW	Obsolete	Production	SOIC (DW)   16	-	-	Call TI	Call TI	-40 to 85	ISO35
ISO35DWR	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO35
ISO35DWR.A	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO35
ISO35MDW	Obsolete	Production	SOIC (DW)   16	-	-	Call TI	Call TI	-55 to 125	ISO35M
ISO35MDWR	Obsolete	Production	SOIC (DW)   16	-	-	Call TI	Call TI	-55 to 125	ISO35M

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

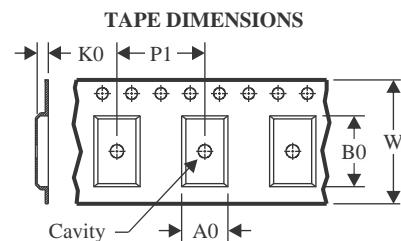
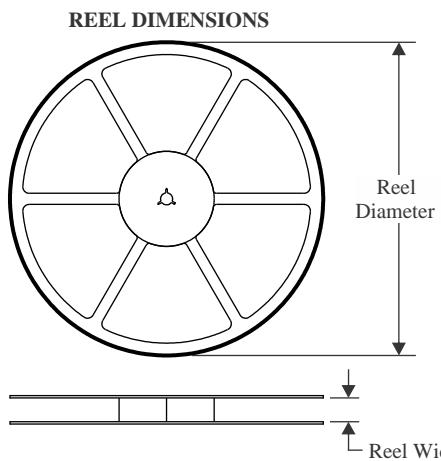
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

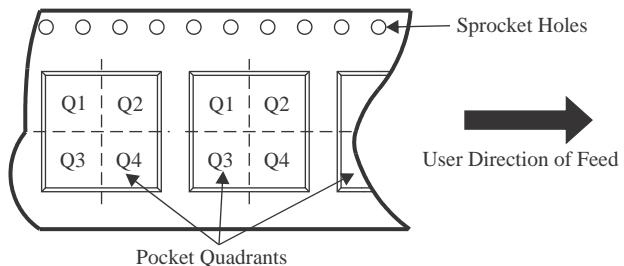
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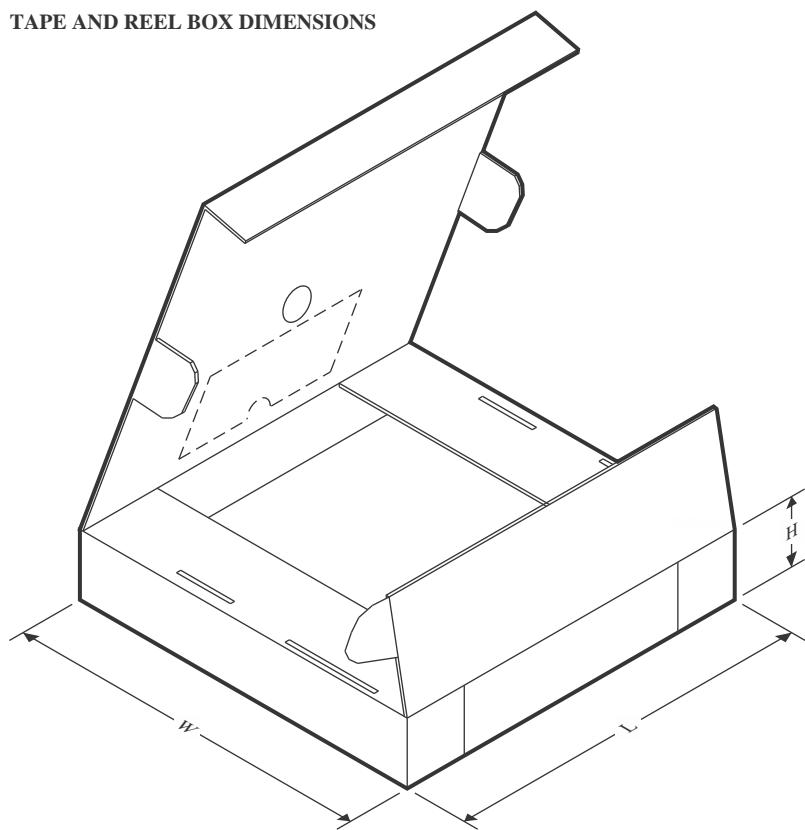
**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO15DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO35DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO15DWR	SOIC	DW	16	2000	353.0	353.0	32.0
ISO35DWR	SOIC	DW	16	2000	353.0	353.0	32.0

# GENERIC PACKAGE VIEW

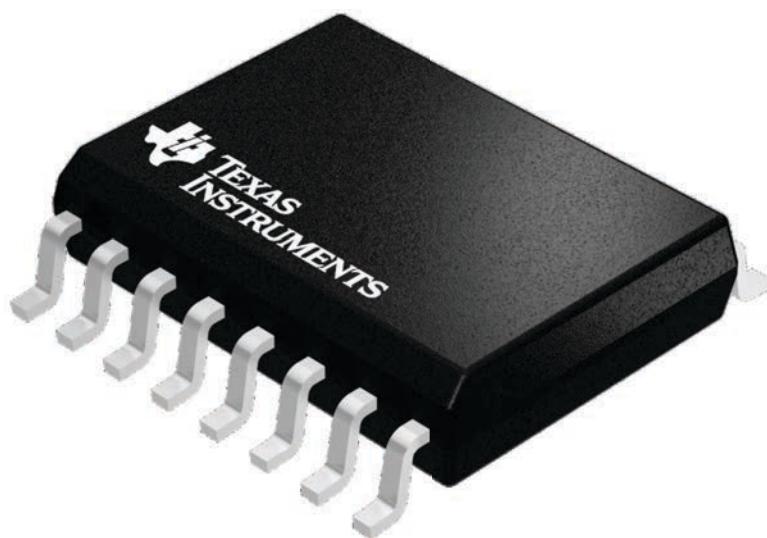
**DW 16**

**SOIC - 2.65 mm max height**

**7.5 x 10.3, 1.27 mm pitch**

**SMALL OUTLINE INTEGRATED CIRCUIT**

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



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Last updated 10/2025