# ISO672x-Q1 General Purpose Reinforced and Basic Dual-Channel Automotive Digital Isolators With Robust EMC

## 1 Features

- Functional Safety-Capable
  - Documentation available to aid functional safety system design: ISO6720-Q1, ISO6721-Q1
- AEC-Q100 qualified with the following results:
  - Device temperature Grade 1: –40°C to +125°C ambient operating temperature range
- Meets VDA320 isolation requirements
- 50Mbps data rate
- Robust isolation barrier:
  - High lifetime at $1060V_{RMS}$ working voltage
  - Up to $5000V_{RMS}$ isolation rating
  - ±150kV/µs typical CMTI
- Wide supply range: 1.71V to 1.89V and 2.25V to 5.5V
- 1.71V to 5.5V level translation
- Default output *High* (ISO672x-Q1) and *Low* (ISO672xF-Q1) Options
- 1.8mA per channel typical at 1Mbps
- Low propagation delay: 11ns typical
- Robust electromagnetic compatibility (EMC)
  - System-Level ESD, EFT, and surge immunity
  - ±8kV IEC 61000-4-2 contact discharge protection across isolation barrier
  - Low emissions
- Narrow-SOIC (D-8) and Wide-SOIC (DWV-8) package
- Safety-Related Certifications:
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL 1577 component recognition program
  - IEC 62368-1, IEC 61010-1, IEC 60601-1
  - GB 4943.1

## 2 Applications

- Hybrid, electric and power train system (EV/HEV)
  - Battery management system (BMS)
  - On-board charger
  - Traction inverter
  - DC/DC converter
  - Inverter and motor control
- Power supplies
- Grid, Electricity meter
- Appliances

**Device Information**

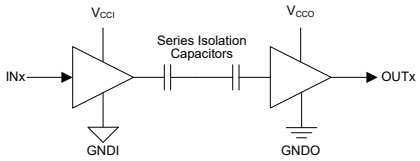
| PART NUMBER | PACKAGE (1) | PACKAGE SIZE(2) | BODY SIZE (NOM) |
|---|---|---|---|
| ISO6720B-Q1, ISO6720FB-Q1 | D (SOIC, 8) | 4.90mm × 6.00mm | 4.90mm × 3.91mm |
| ISO6721B-Q1, ISO6721FB-Q1 | | | |
| ISO6721RB-Q1, ISO6721RFB-Q1 | | | |
| ISO6720-Q1, ISO6720F-Q1 | DWV (SOIC, 8) | 5.85mm × 11.50mm | 5.85mm × 7.50mm |
| ISO6721-Q1, ISO6721F-Q1 | | | |

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

## 3 Description

The ISO672x-Q1 devices are high-performance, dual-channel digital isolators designed for cost sensitive applications requiring up to 5000$V_{RMS}$ (DWV package) and 3000$V_{RMS}$ (D package) isolation ratings per UL 1577. These devices are also certified by VDE, TUV, CSA, and CQC.

The ISO672x-Q1 devices provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by TI's double capacitive silicon dioxide ($SiO_2$) insulation barrier. The ISO6720-Q1 device has 2 isolation channels with both channels in the same direction. The ISO6721-Q1 device has 2 isolation channels with 1 channel in each direction. In the event of input power or signal loss, the default output is *high* for devices without suffix F and *low* for devices with suffix F. See Device Functional Modes section for further details.




$V_{CCI}$=Input supply, $V_{CCO}$=Output supply
GNDI=Input ground, GNDO=Output ground

**Simplified Schematic**

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# 4 Pin Configuration and Functions

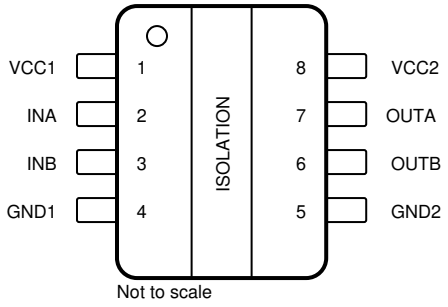



**Figure 4-1. ISO6720-Q1 D and DWV Package 8-Pin SOIC Top View**

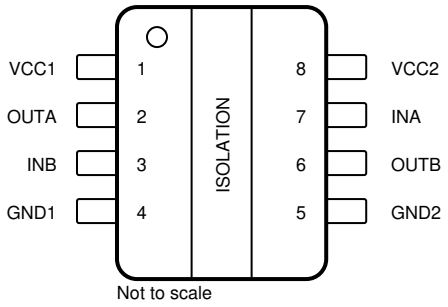



**Figure 4-2. ISO6721-Q1 D and DWV Package 8-Pin SOIC Top View**

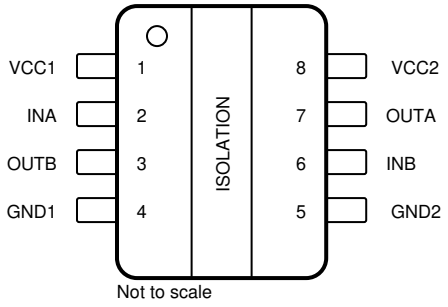



**Figure 4-3. ISO6721RB-Q1 D Package 8-Pin SOIC Top View**

**Table 4-1. Pin Functions**

| PIN | | | | TYPE[1] | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | D and DWV PACKAGE | | D PACKAGE | | |
| | ISO6720-Q1 | ISO6721-Q1 | ISO6721RB-Q1 | | |
| GND1 | 4 | 4 | 4 | — | Ground connection for $V_{CC1}$ |
| GND2 | 5 | 5 | 5 | — | Ground connection for $V_{CC2}$ |
| INA | 2 | 7 | 2 | I | Input, channel A |
| INB | 3 | 3 | 6 | I | Input, channel B |
| OUTA | 7 | 2 | 7 | O | Output, channel A |
| OUTB | 6 | 6 | 3 | O | Output, channel B |
| $V_{CC1}$ | 1 | 1 | 1 | — | Power supply, $V_{CC1}$ |
| $V_{CC2}$ | 8 | 8 | 8 | — | Power supply, $V_{CC2}$ |

(1) I = Input; O = Output

# 5 Specifications

## 5.1 Absolute Maximum Ratings

See(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply Voltage (2) | $V_{CC1}$ to GND1 | -0.5 | 6 | V |
| | $V_{CC2}$ to GND2 | -0.5 | 6 | |
| Input/Output Voltage | INx to GNDx | -0.5 | $V_{CCX}$ + 0.5 (3) | V |
| | OUTx to GNDx | -0.5 | $V_{CCX}$ + 0.5 (3) | |
| Output Current | Io | -15 | 15 | mA |
| Temperature | Operating junction temperature, $T_J$ | | 150 | °C |
| | Storage temperature, $T_{stg}$ | -65 | 150 | °C |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values
(3) Maximum voltage must not exceed 6 V.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±6000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±1500 | |
| | | Contact discharge per IEC 61000-4-2; Isolation barrier withstand test(3) (4) | ±8000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.
(4) Testing is carried out in air or oil to determine the intrinsic contact discharge capability of the device.

## 5.3 Recommended Operating Conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC1}$ (1) | Supply Voltage Side 1 | $V_{CC}$ = 1.8V (3) | 1.71 | | 1.89 | V |
| $V_{CC1}$ (1) | Supply Voltage Side 1 | $V_{CC}$ = 2.5V to 5V (3) | 2.25 | | 5.5 | V |
| $V_{CC2}$ (1) | Supply Voltage Side 2 | $V_{CC}$ = 1.8V (3) | 1.71 | | 1.89 | V |
| $V_{CC2}$ (1) | Supply Voltage Side 2 | $V_{CC}$ = 2.5V to 5V (3) | 2.25 | | 5.5 | V |
| $V_{CC}$ (UVLO+) | UVLO threshold when supply voltage is rising | | | 1.53 | 1.71 | V |
| $V_{CC}$ (UVLO-) | UVLO threshold when supply voltage is falling | | 1.1 | 1.41 | | V |
| Vhys (UVLO) | Supply voltage UVLO hysteresis | | 0.08 | 0.13 | | V |
| $V_{IH}$ | High level Input voltage | | 0.7 × $V_{CCI}$ (2) | | $V_{CCI}$ | V |
| $V_{IL}$ | Low level Input voltage | | 0 | | 0.3 × $V_{CCI}$ | V |
| $I_{OH}$ | High level output current | $V_{CCO}$ (2) = 5V | -4 | | | mA |
| | | $V_{CCO}$ = 3.3V | -2 | | | mA |
| | | $V_{CCO}$ = 2.5V | -1 | | | mA |
| | | $V_{CCO}$ = 1.8 V | -1 | | | mA |
| $I_{OL}$ | Low level output current | $V_{CCO}$ = 5V | | | 4 | mA |
| | | $V_{CCO}$ = 3.3V | | | 2 | mA |
| | | $V_{CCO}$ = 2.5V | | | 1 | mA |
| | | $V_{CCO}$ = 1.8V | | | 1 | mA |
| DR | Data Rate | | 0 | | 50 | Mbps |
| $T_A$ | Ambient temperature | | -40 | 25 | 125 | °C |

(1) $V_{CC1}$ and $V_{CC2}$ can be set independent of one another
(2) $V_{CCI}$ = Input-side $V_{CC}$; $V_{CCO}$ = Output-side $V_{CC}$
(3) The channel outputs are in undetermined state when 1.89 V < $V_{CC1}$, $V_{CC2}$ < 2.25 V and 1.05 V < $V_{CC1}$, $V_{CC2}$ < 1.71 V

## 5.4 Thermal Information

| THERMAL METRIC [1] | | ISO672x | ISO672xB | ISO6721RB | UNIT |
|---|---|---|---|---|---|
| | | DWV (SOIC) | D (SOIC) | D (SOIC) | |
| | | 8 PINS | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 84.3 | 104.6 | 98.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 36.3 | 48.9 | 33.8 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 47.0 | 52.9 | 47 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 7.4 | 7.9 | 2.3 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 45.1 | 52.1 | 46.2 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | n/a | n/a | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

## 5.5 Power Ratings

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ISO6720** | | | | | | |
| $P_D$ | Maximum power dissipation (both sides) | $V_{CC1}$ = $V_{CC2}$ = 5.5V, $T_J$ = 150°C, $C_L$ = 15pF, Input a 25MHz 50% duty cycle square wave | | | 72 | mW |
| $P_{D1}$ | Maximum power dissipation (side-1) | | | | 20 | mW |
| $P_{D2}$ | Maximum power dissipation (side-2) | | | | 52 | mW |
| **ISO6721** | | | | | | |
| $P_D$ | Maximum power dissipation (both sides) | $V_{CC1}$ = $V_{CC2}$ = 5.5V, $T_J$ = 150°C, $C_L$ = 15pF, Input a 25MHz 50% duty cycle square wave | | | 73 | mW |
| $P_{D1}$ | Maximum power dissipation (side-1) | | | | 37 | mW |
| $P_{D2}$ | Maximum power dissipation (side-2) | | | | 37 | mW |
| **ISO6721RB** | | | | | | |
| $P_D$ | Maximum power dissipation (both sides) | $V_{CC1}$ = $V_{CC2}$ = 5.5V, $T_J$ = 150°C, $C_L$ = 15pF, Input a 25MHz 50% duty cycle square wave | | | 86 | mW |
| $P_{D1}$ | Maximum power dissipation (side-1) | | | | 43 | mW |
| $P_{D2}$ | Maximum power dissipation (side-2) | | | | 43 | mW |

## 5.6 Insulation Specifications

| PARAMETER | | TEST CONDITIONS | VALUE 8-DWV | VALUE 8-D | UNIT |
|---|---|---|---|---|---|
| **IEC 60664-1** | | | | | |
| CLR | External clearance(1) | Side 1 to side 2 distance through air | >8.5 | >4 | mm |
| CPG | External creepage(1) | Side 1 to side 2 distance across package surface | >8.5 | >4 | mm |
| DTI | Distance through the insulation | Minimum internal gap (internal clearance) | >17 | >17 | µm |
| CTI | Comparative tracking index | IEC 60112; UL 746A | >600 | >400 | V |
| | Material Group | According to IEC 60664-1 | I | II | |
| | Overvoltage category | Rated mains voltage ≤ 150$V_{RMS}$ | I–IV | I-IV | |
| | | Rated mains voltage ≤ 300$V_{RMS}$ | I–IV | I-III | |
| | | Rated mains voltage ≤ 600$V_{RMS}$ | I–IV | n/a | |
| | | Rated mains voltage ≤ 1000$V_{RMS}$ | I-III | n/a | |
| **DIN EN IEC 60747-17 (VDE 0884-17)(2)** | | | | | |
| $V_{IORM}$ | Maximum repetitive peak isolation voltage | AC voltage (bipolar) | 1500 | 637 | $V_{PK}$ |
| $V_{IOWM}$ | Maximum isolation working voltage | AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test. See Figure 8-9 | 1060 | 450 | $V_{RMS}$ |
| | | DC voltage | 1500 | 637 | $V_{DC}$ |
| $V_{IOTM}$ | Maximum transient isolation voltage | $V_{TEST}$ = $V_{IOTM}$ , t = 60s (qualification); $V_{TEST}$ = 1.2 × $V_{IOTM}$, t = 1s (100% production) | 7071 | 4242 | $V_{PK}$ |
| $V_{IMP}$ | Maximum impulse voltage(3) | Tested in air, 1.2/50-µs waveform per IEC 62368-1 | 7692 | 5000 | $V_{PK}$ |
| $V_{IOSM}$ | Maximum surge isolation voltage (4) | $V_{IOSM}$ ≥ 1.3 x $V_{IMP}$; tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1 | 10000 | 6500 | $V_{PK}$ |
| $q_{pd}$ | Apparent charge(5) | Method a: After I/O safety test subgroup 2/3, $V_{ini}$ = $V_{IOTM}$, $t_{ini}$ = 60s; $V_{pd(m)}$ = 1.2 × $V_{IORM}$ , $t_m$ = 10s | ≤5 | ≤5 | pC |
| | | Method a: After environmental tests subgroup 1, $V_{ini}$ = $V_{IOTM}$, $t_{ini}$ = 60s; **DWV:** $V_{pd(m)}$ = 1.6 × $V_{IORM}$ , $t_m$ = 10s **D:** $V_{pd(m)}$ = 1.2 × $V_{IORM}$ , $t_m$ = 10s | ≤5 | ≤5 | |
| | | At routine test (100% production), Method b1: $V_{ini}$ = 1.2 x $V_{IOTM}$, $t_{ini}$ = 1s, **DWV:** $V_{pd(m)}$ = 1.875 × $V_{IORM}$ , $t_m$ = 1s **D:** $V_{pd(m)}$ = 1.5 × $V_{IORM}$ , $t_m$ = 1s, or Method b2: $V_{pd(m)}$ = $V_{ini}$, $t_m$ = $t_{ini}$ | ≤5 | ≤5 | |
| $C_{IO}$ | Barrier capacitance, input to output(6) | $V_{IO}$ = 0.4 × sin (2 πft), f = 1MHz | ≅0.5 | ≅0.5 | pF |
| $R_{IO}$ | Insulation resistance, input to output(6) | $V_{IO}$ = 500V, $T_A$ = 25°C | >$10^{12}$ | >$10^{12}$ | Ω |
| | | $V_{IO}$ = 500V, 100°C ≤ $T_A$ ≤ 125°C | >$10^{11}$ | >$10^{11}$ | |
| | | $V_{IO}$ = 500V at $T_S$ = 150°C | >$10^{9}$ | >$10^{9}$ | |
| | Pollution degree | | 2 | 2 | |
| | Climatic category | | 40/125/21 | 40/125/21 | |
| **UL 1577** | | | | | |

| PARAMETER | | TEST CONDITIONS | VALUE | VALUE | UNIT |
|---|---|---|---|---|---|
| | | | 8-DWV | 8-D | |
| $V_{ISO}$ | Withstand isolation voltage | $V_{TEST} = V_{ISO}$ , t = 60s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$ , t = 1s (100% production) | 5000 | 3000 | $V_{RMS}$ |

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation (ISO672x)* and *basic electrical insulation (ISO672xB)* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier tied together creating a two-pin device.

## 5.7 Safety-Related Certifications

| VDE | CSA | UL | CQC | TUV |
|---|---|---|---|---|
| Certified according to DIN EN IEC 60747-17 (VDE 0884-17) | Certified according to IEC 62368-1, IEC 61010-1 and IEC 60601-1 | Certified according to UL 1577 Component Recognition Program | Certified according to GB 4943.1 | Certified according to EN 61010-1 and EN 62368-1 |
| Certificates:<br>Reinforced: 40040142<br>Basic: 40047657 | Master contract number: 220991 | File number: E181974 | Certificates:<br>CQC18001199096 (DWV-8)<br>CQC21001305151 (D-8) | Client ID number: 77311 |

## 5.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **D-8 PACKAGE - ISO672xB** | | | | | | |
| $I_S$ | Safety input, output, or supply current (1) | $R_{\theta JA}$ =104.6°C/W, $V_I$ = 5.5V, $T_J$ = 150°C, $T_A$ = 25°C See Figure 5-1 | | | 217.2 | mA |
| | | $R_{\theta JA}$ = 104.6°C/W, $V_I$ = 3.6V, $T_J$ = 150°C, $T_A$ = 25°C See Figure 5-1 | | | 332 | mA |
| | | $R_{\theta JA}$ = 104.6°C/W, $V_I$ = 2.75V, $T_J$ = 150°C, $T_A$ = 25°C See Figure 5-1 | | | 434.5 | mA |
| | | $R_{\theta JA}$ = 104.6°C/W, $V_I$ = 1.89V, $T_J$ = 150°C, $T_A$ = 25°C See Figure 5-1 | | | 628.9 | mA |
| $P_S$ | Safety input, output, or total power (1) | $R_{\theta JA}$ = 104.6°C/W, $T_J$ = 150°C, $T_A$ = 25°C See Figure 5-2 | | | 1195 | mW |
| $T_S$ | Maximum safety temperature (1) | | | | 150 | °C |
| **D-8 PACKAGE - ISO6721RB** | | | | | | |
| $I_S$ | Safety input, output, or supply current (1) | $R_{\theta JA}$ = 98.5°C/W, $V_I$ = 5.5V, $T_J$ = 150°C, $T_A$ = 25°C See Figure 5-3 | | | 230.7 | mA |
| $I_S$ | Safety input, output, or supply current (1) | $R_{\theta JA}$ = 98.5°C/W, $V_I$ = 3.6V, $T_J$ = 150°C, $T_A$ = 25°C See Figure 5-3 | | | 352.5 | mA |
| $I_S$ | Safety input, output, or supply current (1) | $R_{\theta JA}$ = 98.5°C/W, $V_I$ = 2.75V, $T_J$ = 150°C, $T_A$ = 25°C See Figure 5-3 | | | 461.5 | mA |
| $I_S$ | Safety input, output, or supply current (1) | $R_{\theta JA}$ = 98.5°C/W, $V_I$ = 1.89V, $T_J$ = 150°C, $T_A$ = 25°C See Figure 5-3 | | | 671.4 | mA |
| $P_S$ | Safety input, output, or total power (1) | $R_{\theta JA}$ = 98.5°C/W, $T_J$ = 150°C, $T_A$ = 25°C See Figure 5-4 | | | 1269 | mW |
| $T_S$ | Maximum safety temperature (1) | | | | 150 | °C |

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DWV-8 PACKAGE** | | | | | | |
| $I_S$ | Safety input, output, or supply current (1) | $R_{\theta JA}$ =84.3°C/W, $V_I$ = 5.5V, $T_J$ = 150°C, $T_A$ = 25°C See Figure 5-5 | | | 270 | mA |
| $I_S$ | | $R_{\theta JA}$ = 84.3.6°C/W, $V_I$ = 3.6V, $T_J$ = 150°C, $T_A$ = 25°C See Figure 5-5 | | | 412 | mA |
| $I_S$ | | $R_{\theta JA}$ = 84.3°C/W, $V_I$ = 2.75V, $T_J$ = 150°C, $T_A$ = 25°C See Figure 5-5 | | | 539 | mA |
| $I_S$ | | $R_{\theta JA}$ = 84.3°C/W, $V_I$ = 1.89V, $T_J$ = 150°C, $T_A$ = 25°C See Figure 5-5 | | | 790 | mA |
| $P_S$ | Safety input, output, or total power (1) | $R_{\theta JA}$ = 84.3°C/W, $T_J$ = 150°C, $T_A$ = 25°C See Figure 5-5 | | | 1483 | mW |
| $T_S$ | Maximum safety temperature (1) | | | | 150 | °C |

(1) The maximum safety temperature, $T_S$, has the same value as the maximum junction temperature, $T_J$, specified for the device. The $I_S$ and $P_S$ parameters represent the safety current and safety power respectively. The maximum limits of $I_S$ and $P_S$ should not be exceeded. These limits vary with the ambient temperature, $T_A$.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where $V_I$ is the maximum input voltage.

## 5.9 Electrical Characteristics—5-V Supply

$V_{CC1}$ = $V_{CC2}$ = 5 V ± 10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = -4mA; See Figure 6-1 | $V_{CCO}$ - 0.4 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 4mA; See Figure 6-1 | | | 0.4 | V |
| $V_{IT+(IN)}$ | Rising input switching threshold | | | | 0.7 × $V_{CCI}$ (1) | V |
| $V_{IT-(IN)}$ | Falling input switching threshold | | 0.3 × $V_{CCI}$ | | | V |
| $V_{I(HYS)}$ | Input threshold voltage hysteresis | | 0.1 × $V_{CCI}$ | | | V |
| $I_{IH}$ | High-level input current | $V_{IH}$ = $V_{CCI}$ (1) at INx | | | 10 | µA |
| $I_{IL}$ | Low-level input current | $V_{IL}$ = 0V at INx | -10 | | | µA |
| CMTI | Common mode transient immunity | $V_I$ = $V_{CC}$ or 0V, $V_{CM}$ = 1200V | 100 | 150 | | kV/µs |
| $C_i$ | Input Capacitance (2) | $V_I$ = $V_{CC}$/ 2 + 0.4×sin(2πft), f = 2MHz, $V_{CC}$ = 5V ; See Figure 6-3 | | 2.8 | | pF |

(1) $V_{CCI}$ = Input-side $V_{CC}$; $V_{CCO}$ = Output-side $V_{CC}$
(2) Measured from input pin to same side ground.

## 5.10 Supply Current Characteristics—5-V Supply

$V_{CC1}$ = $V_{CC2}$ = 5 V ± 10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SUPPLY CURRENT | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ISO6720** | | | | | | | |
| Supply current - DC signal | $V_I$ = $V_{CCI}$ (1)(ISO6720), $V_I$ = 0V (ISO6720 with F suffix) | | $I_{CC1}$ | | 1.1 | 1.7 | mA |
| | | | $I_{CC2}$ | | 1.3 | 2.1 | |
| | $V_I$ = 0V (ISO6720), $V_I$ = $V_{CC1}$ (ISO6720 with F suffix) | | $I_{CC1}$ | | 3.2 | 4.6 | |
| | | | $I_{CC2}$ | | 1.4 | 2.3 | |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L$ = 15pF | 1Mbps | $I_{CC1}$ | | 2.1 | 3.1 | |
| | | | $I_{CC2}$ | | 1.5 | 2.3 | |
| | | 10Mbps | $I_{CC1}$ | | 2.2 | 3.2 | |
| | | | $I_{CC2}$ | | 2.7 | 3.6 | |
| | | 50Mbps | $I_{CC1}$ | | 2.5 | 3.6 | |
| | | | $I_{CC2}$ | | 7.9 | 9.5 | |
| **ISO6721** | | | | | | | |
| Supply current - DC signal | $V_I$ = $V_{CCI}$ (1)(ISO6721); $V_I$ = 0V (ISO6721 with F suffix) | | $I_{CC1}$, $I_{CC2}$ | | 1.2 | 2.1 | mA |
| | $V_I$ = 0V (ISO6721); $V_I$ = $V_{CCI}$ (ISO6721 with F suffix) | | $I_{CC1}$, $I_{CC2}$ | | 2.3 | 3.5 | |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L$ = 15pF | 1Mbps | $I_{CC1}$, $I_{CC2}$ | | 1.9 | 2.9 | |
| | | 10Mbps | $I_{CC1}$, $I_{CC2}$ | | 2.5 | 3.6 | |
| | | 50Mbps | $I_{CC1}$, $I_{CC2}$ | | 5.2 | 6.7 | |

$V_{CC1}$ = $V_{CC2}$ = 5 V ± 10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SUPPLY CURRENT | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ISO6721RB** | | | | | | | |
| Supply current - DC signal | $V_I$ = $V_{CCI}$ (1)(ISO6721R); $V_I$ = 0V (ISO6721R with F suffix) | | $I_{CC1}$ , $I_{CC2}$ | | 2.1 | 3.3 | mA |
| | $V_I$ = 0V (ISO6721R); $V_I$ = $V_{CCI}$ (ISO6721R with F suffix) | | $I_{CC1}$ , $I_{CC2}$ | | 3.2 | 4.7 | |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L$ = 15pF | 1Mbps | $I_{CC1}$, $I_{CC2}$ | | 2.7 | 4.1 | |
| | | 10Mbps | $I_{CC1}$, $I_{CC2}$ | | 3.3 | 4.7 | |
| | | 50Mbps | $I_{CC1}$, $I_{CC2}$ | | 6.0 | 7.7 | |

(1) $V_{CCI}$ = Input-side $V_{CC}$

## 5.11 Electrical Characteristics—3.3-V Supply

$V_{CC1}$ = $V_{CC2}$ = 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = -2mA ; See Figure 6-1 | $V_{CCO}$ - 0.2 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 2mA ; See Figure 6-1 | | | 0.2 | V |
| $V_{IT+(IN)}$ | Rising input switching threshold | | | | 0.7× $V_{CCI}$ (1) | V |
| $V_{IT-(IN)}$ | Falling input switching threshold | | 0.3 × $V_{CCI}$ | | | V |
| $V_{I(HYS)}$ | Input threshold voltage hysteresis | | 0.1 × $V_{CCI}$ | | | V |
| $I_{IH}$ | High-level input current | $V_{IH}$ = $V_{CCI}$ (1) at INx | | | 10 | µA |
| $I_{IL}$ | Low-level input current | $V_{IL}$ = 0V at INx | -10 | | | µA |
| CMTI | Common mode transient immunity | $V_I$ = $V_{CC}$ or 0V, $V_{CM}$ = 1200V | 100 | 150 | | kV/µs |
| $C_i$ | Input Capacitance(2) | $V_I$ = $V_{CC}$/ 2 + 0.4×sin(2πft), f = 2MHz, $V_{CC}$ = 3.3V ; See Figure 6-3 | | 2.8 | | pF |

(1) $V_{CCI}$ = Input-side $V_{CC}$; $V_{CCO}$ = Output-side $V_{CC}$
(2) Measured from input pin to same side ground.

## 5.12 Supply Current Characteristics—3.3-V Supply

$V_{CC1}$ = $V_{CC2}$ = 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SUPPLY CURRENT | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ISO6720** | | | | | | | |
| Supply current - DC signal | $V_I$ = $V_{CCI}$ (1)(ISO6720), $V_I$ = 0V (ISO6720 with F suffix) | | $I_{CC1}$ | | 1.1 | 1.6 | mA |
| | | | $I_{CC2}$ | | 1.3 | 2 | |
| | $V_I$ = 0V (ISO6720), $V_I$ = $V_{CC1}$ (ISO6720 with F suffix) | | $I_{CC1}$ | | 3.2 | 4.5 | |
| | | | $I_{CC2}$ | | 1.4 | 2.2 | |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L$ = 15pF | 1Mbps | $I_{CC1}$ | | 2.1 | 3.1 | |
| | | | $I_{CC2}$ | | 1.4 | 2.2 | |
| | | 10Mbps | $I_{CC1}$ | | 2.2 | 3.1 | |
| | | | $I_{CC2}$ | | 2.3 | 3.2 | |
| | | 50Mbps | $I_{CC1}$ | | 2.4 | 3.4 | |
| | | | $I_{CC2}$ | | 6 | 7.3 | |
| **ISO6721** | | | | | | | |
| Supply current - DC signal | $V_I$ = $V_{CCI}$ (1)(ISO6721); $V_I$ = 0V (ISO6721 with F suffix) | | $I_{CC1}$, $I_{CC2}$ | | 1.2 | 2.1 | mA |
| | $V_I$ = 0V (ISO6721); $V_I$ = $V_{CCI}$ (ISO6721 with F suffix) | | $I_{CC1}$, $I_{CC2}$ | | 2.3 | 3.5 | |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L$ = 15pF | 1Mbps | $I_{CC1}$, $I_{CC2}$ | | 1.8 | 2.8 | |
| | | 10Mbps | $I_{CC1}$, $I_{CC2}$ | | 2.3 | 3.3 | |
| | | 50Mbps | $I_{CC1}$, $I_{CC2}$ | | 4.2 | 5.5 | |

$V_{CC1}$ = $V_{CC2}$ = 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SUPPLY CURRENT | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ISO6721RB** | | | | | | | |
| Supply current - DC signal | $V_I$ = $V_{CCI}$ (1)(ISO6721R); $V_I$ = 0V (ISO6721R with F suffix) | | $I_{CC1}$ , $I_{CC2}$ | | 2.1 | 3.3 | mA |
| | $V_I$ = 0V (ISO6721R); $V_I$ = $V_{CCI}$ (ISO6721R with F suffix) | | $I_{CC1}$ , $I_{CC2}$ | | 3.2 | 4.7 | |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L$ = 15pF | 1Mbps | $I_{CC1}$, $I_{CC2}$ | | 2.7 | 4.0 | |
| | | 10Mbps | $I_{CC1}$, $I_{CC2}$ | | 3.1 | 4.5 | |
| | | 50Mbps | $I_{CC1}$, $I_{CC2}$ | | 5.0 | 6.7 | |

(1) $V_{CCI}$ = Input-side $V_{CC}$

## 5.13 Electrical Characteristics—2.5-V Supply

$V_{CC1}$ = $V_{CC2}$ = 2.5 V ± 10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = -1mA ; See Figure 6-1 | $V_{CCO}$ - 0.1 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 1mA ; See Figure 6-1 | | | 0.1 | V |
| $V_{IT+(IN)}$ | Rising input switching threshold | | | | 0.7 × $V_{CCI}$ (1) | V |
| $V_{IT-(IN)}$ | Falling input switching threshold | | 0.3 × $V_{CCI}$ | | | V |
| $V_{I(HYS)}$ | Input threshold voltage hysteresis | | 0.1 × $V_{CCI}$ | | | V |
| $I_{IH}$ | High-level input current | $V_{IH}$ = $V_{CCI}$ (1) at INx | | | 10 | µA |
| $I_{IL}$ | Low-level input current | $V_{IL}$ = 0V at INx | -10 | | | µA |
| CMTI | Common mode transient immunity | $V_I$ = $V_{CC}$ or 0 V, $V_{CM}$ = 1200 V | 100 | 150 | | kV/µs |
| $C_i$ | Input Capacitance(2) | $V_I$ = $V_{CC}$/ 2 + 0.4×sin(2πft), f = 2MHz, $V_{CC}$ = 2.5V ; See Figure 6-3 | | 2.8 | | pF |

(1) $V_{CCI}$ = Input-side $V_{CC}$; $V_{CCO}$ = Output-side $V_{CC}$
(2) Measured from input pin to same side ground.

## 5.14 Supply Current Characteristics—2.5-V Supply

$V_{CC1}$ = $V_{CC2}$ = 2.5 V ± 10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SUPPLY CURRENT | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ISO6720** | | | | | | | |
| Supply current - DC signal | $V_I$ = $V_{CCI}$ (1)(ISO6720), $V_I$ = 0V (ISO6720 with F suffix) | | $I_{CC1}$ | | 1.1 | 1.6 | mA |
| | | | $I_{CC2}$ | | 1.3 | 2 | |
| | $V_I$ = 0V (ISO6720), $V_I$ = $V_{CC1}$ (ISO6720 with F suffix) | | $I_{CC1}$ | | 3.1 | 4.5 | |
| | | | $I_{CC2}$ | | 1.4 | 2.2 | |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L$ = 15pF | 1Mbps | $I_{CC1}$ | | 2.1 | 3.1 | |
| | | | $I_{CC2}$ | | 1.4 | 2.2 | |
| | | 10Mbps | $I_{CC1}$ | | 2.1 | 3.1 | |
| | | | $I_{CC2}$ | | 2 | 2.9 | |
| | | 50Mbps | $I_{CC1}$ | | 2.3 | 3.3 | |
| | | | $I_{CC2}$ | | 4.8 | 6 | |
| **ISO6721** | | | | | | | |
| Supply current - DC signal | $V_I$ = $V_{CCI}$ (1)(ISO6721); $V_I$ = 0V (ISO6721 with F suffix) | | $I_{CC1}$, $I_{CC2}$ | | 1.2 | 2.1 | mA |
| | $V_I$ = 0V (ISO6721); $V_I$ = $V_{CCI}$ (ISO6721 with F suffix) | | $I_{CC1}$, $I_{CC2}$ | | 2.3 | 3.5 | |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L$ = 15pF | 1Mbps | $I_{CC1}$, $I_{CC2}$ | | 1.8 | 2.8 | |
| | | 10Mbps | $I_{CC1}$, $I_{CC2}$ | | 2.1 | 3.2 | |
| | | 50Mbps | $I_{CC1}$, $I_{CC2}$ | | 3.6 | 4.9 | |

$V_{CC1}$ = $V_{CC2}$ = 2.5 V ± 10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SUPPLY CURRENT | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ISO6721RB** | | | | | | | |
| Supply current - DC signal | $V_I$ = $V_{CCI}$ (1)(ISO6721R); $V_I$ = 0V (ISO6721R with F suffix) | | $I_{CC1}$ , $I_{CC2}$ | | 2.1 | 3.3 | mA |
| | $V_I$ = 0V (ISO6721R); $V_I$ = $V_{CCI}$ (ISO6721R with F suffix) | | $I_{CC1}$ , $I_{CC2}$ | | 3.2 | 4.7 | |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L$ = 15pF | 1Mbps | $I_{CC1}$, $I_{CC2}$ | | 2.7 | 4.0 | |
| | | 10Mbps | $I_{CC1}$, $I_{CC2}$ | | 3.0 | 4.4 | |
| | | 50Mbps | $I_{CC1}$, $I_{CC2}$ | | 4.4 | 6 | |

(1) $V_{CCI}$ = Input-side $V_{CC}$

## 5.15 Electrical Characteristics—1.8-V Supply

$V_{CC1}$ = $V_{CC2}$ = 1.8 V ± 5% (over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = -1mA ; See Figure 6-1 | $V_{CCO}$ - 0.1 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 1mA ; See Figure 6-1 | | | 0.1 | V |
| $V_{IT+(IN)}$ | Rising input switching threshold | | | | 0.7 × $V_{CCI}$ (1) | V |
| $V_{IT-(IN)}$ | Falling input switching threshold | | 0.3 × $V_{CCI}$ | | | V |
| $V_{I(HYS)}$ | Input threshold voltage hysteresis | | 0.1 × $V_{CCI}$ | | | V |
| $I_{IH}$ | High-level input current | $V_{IH}$ = $V_{CCI}$ (1) at INx | | | 10 | µA |
| $I_{IL}$ | Low-level input current | $V_{IL}$ = 0V at INx | -10 | | | µA |
| CMTI | Common mode transient immunity | $V_I$ = $V_{CC}$ or 0V, $V_{CM}$ = 1200V | 100 | 150 | | kV/µs |
| $C_i$ | Input Capacitance(2) | $V_I$ = $V_{CC}$/ 2 + 0.4×sin(2πft), f = 2MHz, $V_{CC}$ = 1.8V ; See Figure 6-3 | | 2.8 | | pF |

(1) $V_{CCI}$ = Input-side $V_{CC}$; $V_{CCO}$ = Output-side $V_{CC}$
(2) Measured from input pin to same side ground.

## 5.16 Supply Current Characteristics—1.8-V Supply

$V_{CC1}$ = $V_{CC2}$ = 1.8 V ± 5% (over recommended operating conditions unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SUPPLY CURRENT | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ISO6720** | | | | | | | |
| Supply current - DC signal | $V_I$ = $V_{CCI}$ (1)(ISO6720), $V_I$ = 0V (ISO6720 with F suffix) | | $I_{CC1}$ | | 0.8 | 1.5 | mA |
| | | | $I_{CC2}$ | | 1.2 | 2.1 | |
| | $V_I$ = 0V (ISO6720), $V_I$ = $V_{CC1}$ (ISO6720 with F suffix) | | $I_{CC1}$ | | 2.8 | 4.3 | |
| | | | $I_{CC2}$ | | 1.3 | 2.2 | |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L$ = 15pF | 1Mbps | $I_{CC1}$ | | 1.8 | 2.9 | |
| | | | $I_{CC2}$ | | 1.3 | 2.2 | |
| | | 10Mbps | $I_{CC1}$ | | 1.8 | 2.9 | |
| | | | $I_{CC2}$ | | 1.8 | 2.7 | |
| | | 50Mbps | $I_{CC1}$ | | 2 | 3.1 | |
| | | | $I_{CC2}$ | | 3.8 | 4.9 | |
| **ISO6721** | | | | | | | |
| Supply current - DC signal | $V_I$ = $V_{CCI}$ (1)(ISO6721); $V_I$ = 0V (ISO6721 with F suffix) | | $I_{CC1}$, $I_{CC2}$ | | 1.1 | 2 | mA |
| | $V_I$ = 0V (ISO6721); $V_I$ = $V_{CCI}$ (ISO6721 with F suffix) | | $I_{CC1}$, $I_{CC2}$ | | 2.1 | 3.4 | |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L$ = 15pF | 1Mbps | $I_{CC1}$, $I_{CC2}$ | | 1.6 | 2.7 | |
| | | 10Mbps | $I_{CC1}$, $I_{CC2}$ | | 1.9 | 3 | |
| | | 50Mbps | $I_{CC1}$, $I_{CC2}$ | | 3 | 4.2 | |

$V_{CC1}$ = $V_{CC2}$ = 1.8 V ± 5% (over recommended operating conditions unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SUPPLY CURRENT | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ISO6721RB** | | | | | | | |
| Supply current - DC signal | $V_I$ = $V_{CCI}$ (1)(ISO6721R); $V_I$ = 0V (ISO6721R with F suffix) | | $I_{CC1}$ , $I_{CC2}$ | | 1.8 | 3.1 | mA |
| | $V_I$ = 0V (ISO6721R); $V_I$ = $V_{CCI}$ (ISO6721R with F suffix) | | $I_{CC1}$ , $I_{CC2}$ | | 2.9 | 4.5 | |
| Supply current - AC signal | All channels switching with square wave clock input; $C_L$ = 15pF | 1Mbps | $I_{CC1}$, $I_{CC2}$ | | 2.4 | 3.8 | |
| | | 10Mbps | $I_{CC1}$, $I_{CC2}$ | | 2.6 | 4.1 | |
| | | 50Mbps | $I_{CC1}$, $I_{CC2}$ | | 3.7 | 5.3 | |

(1) $V_{CCI}$ = Input-side $V_{CC}$

## 5.17 Switching Characteristics—5-V Supply

$V_{CC1}$ = $V_{CC2}$ = 5 V ± 10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation delay time | See Figure 6-1 | | 11 | 18 | ns |
| $t_{P(dft)}$ | Propagation delay drift | | | 8 | | ps/°C |
| $t_{UI}$ | Minimum pulse width | See Figure 6-1 | 20 | | | ns |
| PWD | Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$ | See Figure 6-1 | | 0.2 | 7 | ns |
| $t_{sk(o)}$ | Channel-to-channel output skew time (2) | Same direction channels | | | 6 | ns |
| $t_{sk(p-p)}$ | Part-to-part skew time (3) | | | | 6 | ns |
| $t_r$ | Output signal rise time | See Figure 6-1 | | 2.6 | 4.5 | ns |
| $t_f$ | Output signal fall time | | | 2.6 | 4.5 | ns |
| $t_{PU}$ | Time from UVLO to valid output data | | | | 300 | µs |
| $t_{DO}$ | Default output delay time from input power loss | Measured from the time $V_{CC}$ goes below 1.2V. See Figure 6-2 | | 0.1 | 0.3 | µs |
| $t_{ie}$ | Time interval error | $2^{16}$ – 1 PRBS data at 50Mbps | | 1 | | ns |

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

## 5.18 Switching Characteristics—3.3-V Supply

$V_{CC1}$ = $V_{CC2}$ = 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation delay time | See Figure 6-1 | | 11 | 18 | ns |
| $t_{P(dft)}$ | Propagation delay drift | | | 9.2 | | ps/°C |
| $t_{UI}$ | Minimum pulse width | See Figure 6-1 | 20 | | | ns |
| PWD | Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$ | See Figure 6-1 | | 0.5 | 7 | ns |
| $t_{sk(o)}$ | Channel-to-channel output skew time (2) | Same direction channels | | | 6 | ns |
| $t_{sk(p-p)}$ | Part-to-part skew time (3) | | | | 6 | ns |
| $t_r$ | Output signal rise time | See Figure 6-1 | | 1.6 | 3.2 | ns |
| $t_f$ | Output signal fall time | | | 1.6 | 3.2 | ns |
| $t_{PU}$ | Time from UVLO to valid output data | | | | 300 | µs |
| $t_{DO}$ | Default output delay time from input power loss | Measured from the time $V_{CC}$ goes below 1.2V. See Figure 6-2 | | 0.1 | 0.3 | µs |
| $t_{ie}$ | Time interval error | $2^{16}$ – 1 PRBS data at 50Mbps | | 1 | | ns |

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

## 5.19 Switching Characteristics—2.5-V Supply

$V_{CC1}$ = $V_{CC2}$ = 2.5 V ± 10% (over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation delay time | See Figure 6-1 | | 12 | 20.5 | ns |
| $t_{P(dft)}$ | Propagation delay drift | | | 14.3 | | ps/°C |
| $t_{UI}$ | Minimum pulse width | See Figure 6-1 | 20 | | | ns |
| PWD | Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$ | See Figure 6-1 | | 0.6 | 7.1 | ns |
| $t_{sk(o)}$ | Channel-to-channel output skew time(2) | Same direction channels | | | 6 | ns |
| $t_{sk(p-p)}$ | Part-to-part skew time(3) | | | | 6.1 | ns |
| $t_r$ | Output signal rise time | See Figure 6-1 | | 2 | 4 | ns |
| $t_f$ | Output signal fall time | | | 2 | 4 | ns |
| $t_{PU}$ | Time from UVLO to valid output data | | | | 300 | µs |
| $t_{DO}$ | Default output delay time from input power loss | Measured from the time $V_{CC}$ goes below 1.2V. See Figure 6-2 | | 0.1 | 0.3 | µs |
| $t_{ie}$ | Time interval error | $2^{16}$ – 1 PRBS data at 50Mbps | | 1 | | ns |

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

## 5.20 Switching Characteristics—1.8-V Supply

$V_{CC1}$ = $V_{CC2}$ = 1.8 V ± 5% (over recommended operating conditions unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation delay time | See Figure 6-1 | | 15 | 24 | ns |
| $t_{P(dft)}$ | Propagation delay drift | | | 15.2 | | ps/°C |
| $t_{UI}$ | Minimum pulse width | See Figure 6-1 | 20 | | | ns |
| PWD | Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$ | See Figure 6-1 | | 0.7 | 8.2 | ns |
| $t_{sk(o)}$ | Channel-to-channel output skew time(2) | Same direction channels | | | 6 | ns |
| $t_{sk(p-p)}$ | Part-to-part skew time(3) | | | | 8.8 | ns |
| $t_r$ | Output signal rise time | See Figure 6-1 | | 2.7 | 5.3 | ns |
| $t_f$ | Output signal fall time | | | 2.7 | 5.3 | ns |
| $t_{PU}$ | Time from UVLO to valid output data | | | | 300 | µs |
| $t_{DO}$ | Default output delay time from input power loss | Measured from the time $V_{CC}$ goes below 1.2V. See Figure 6-2 | | 0.1 | 0.3 | µs |
| $t_{ie}$ | Time interval error | $2^{16}$ – 1 PRBS data at 50Mbps | | 1 | | ns |

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

## 5.21 Insulation Characteristics Curves

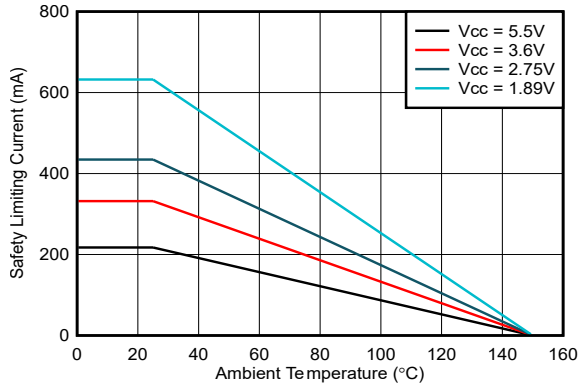



**Figure 5-1. Thermal Derating Curve for Safety Limiting Current for D-8 Package - ISO672x**

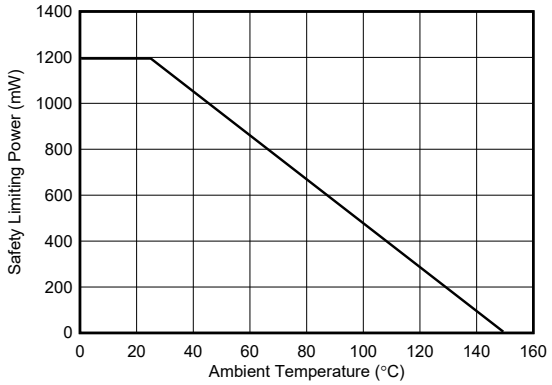



**Figure 5-2. Thermal Derating Curve for Safety Limiting Power for D-8 Package - ISO672x**

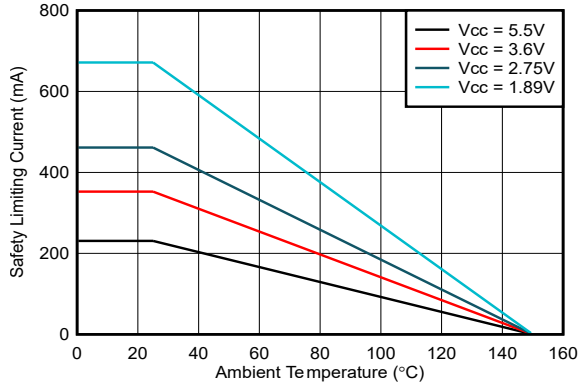



**Figure 5-3. Thermal Derating Curve for Safety Limiting Current for D-8 Package - ISO6721R**

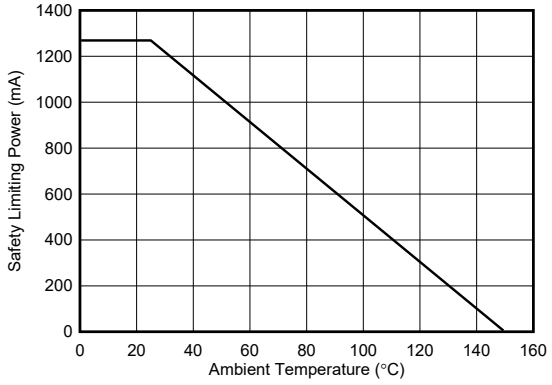



**Figure 5-4. Thermal Derating Curve for Safety Limiting Power for D-8 Package - ISO6721R**

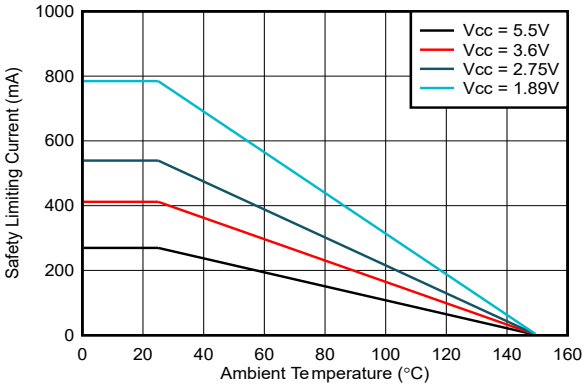



**Figure 5-5. Thermal Derating Curve for Safety Limiting Current for DWV-8 Package - ISO672x**

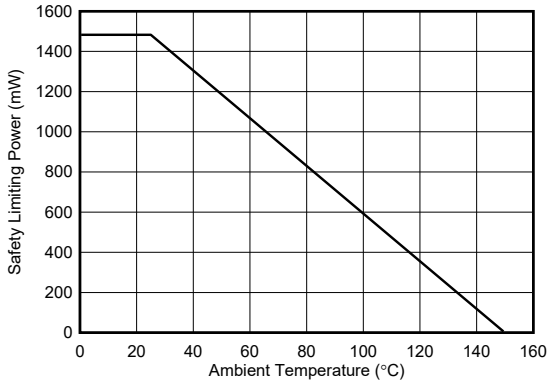



**Figure 5-6. Thermal Derating Curve for Safety Limiting Power for DWV-8 Package - ISO672x**

## 5.22 Typical Characteristics

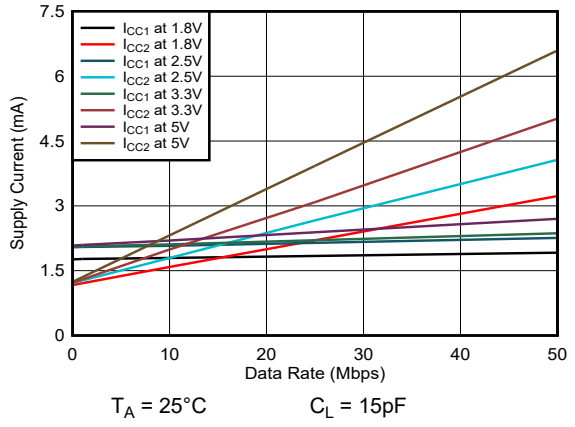



**Figure 5-7. ISO6720 Supply Current vs Data Rate (With 15pF Load)**

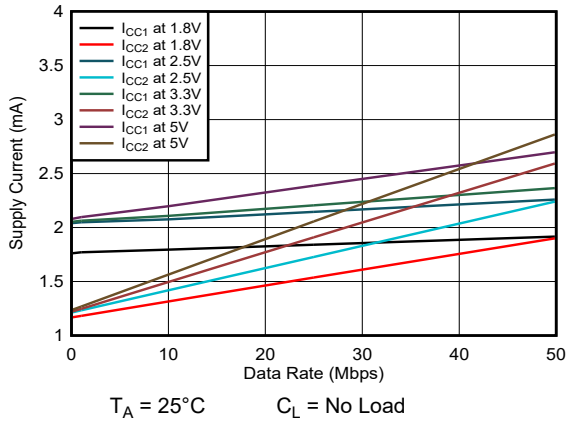



**Figure 5-8. ISO6720 Supply Current vs Data Rate (With No Load)**

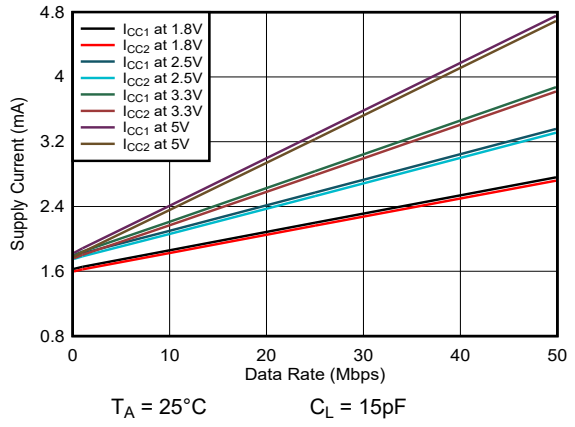



**Figure 5-9. ISO6721 Supply Current vs Data Rate (With 15pF Load)**

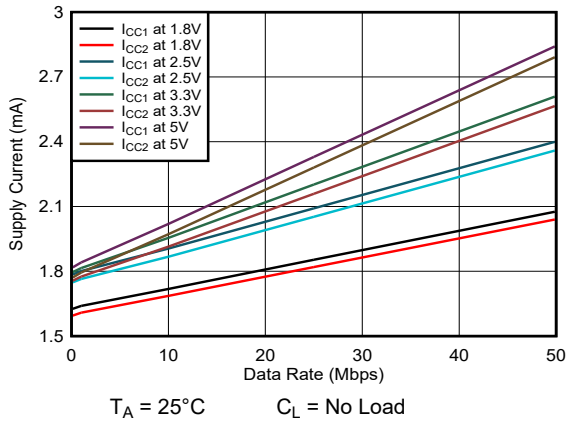



**Figure 5-10. ISO6721 Supply Current vs Data Rate (With No Load)**

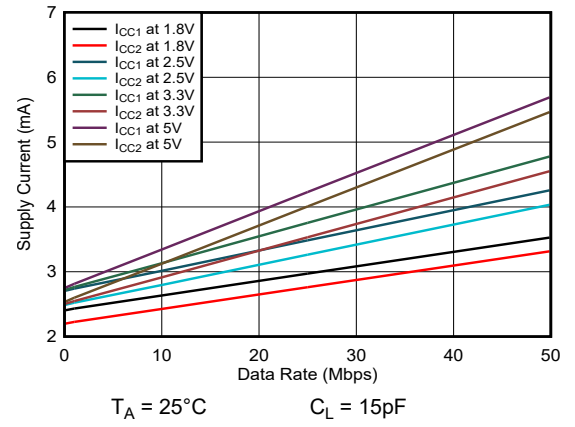



**Figure 5-11. ISO6721RB Supply Current vs Data Rate (With 15pF Load)**

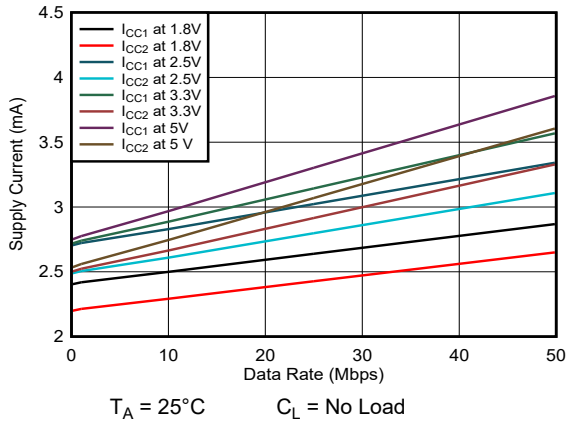



**Figure 5-12. ISO6721RB Supply Current vs Data Rate (With No Load)**

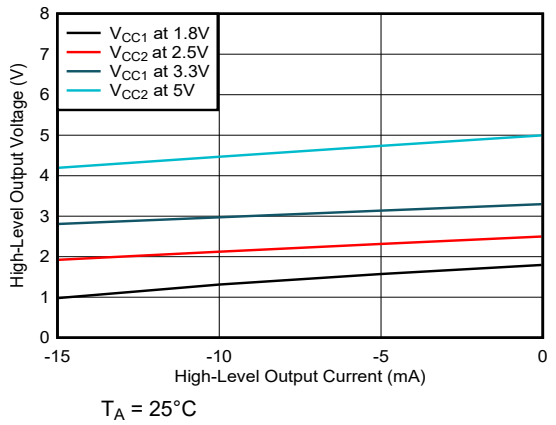



**Figure 5-13. High-Level Output Voltage vs High-level Output Current**

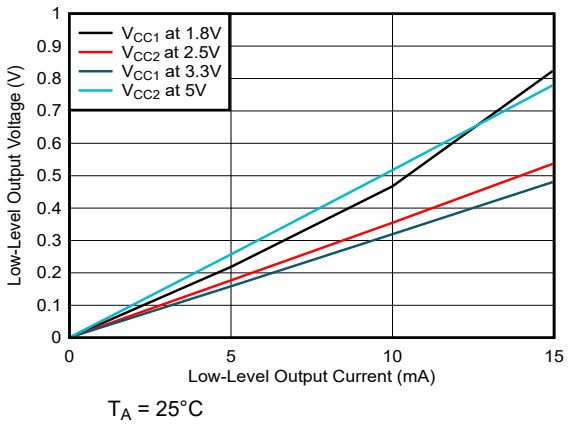



**Figure 5-14. Low-Level Output Voltage vs Low-Level Output Current**

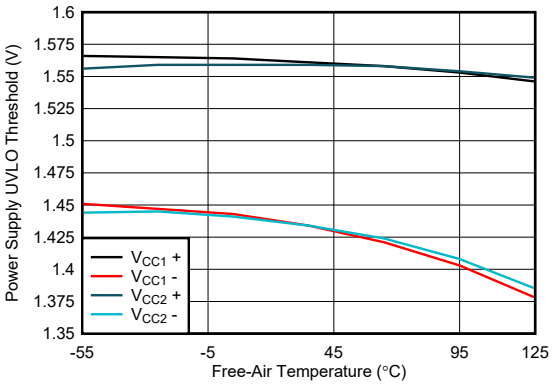



**Figure 5-15. Power Supply Undervoltage Threshold vs Free-Air Temperature**

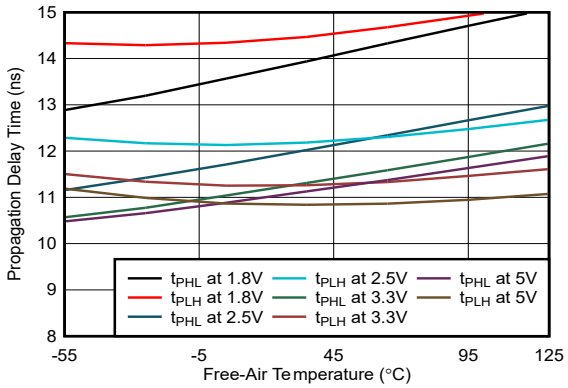
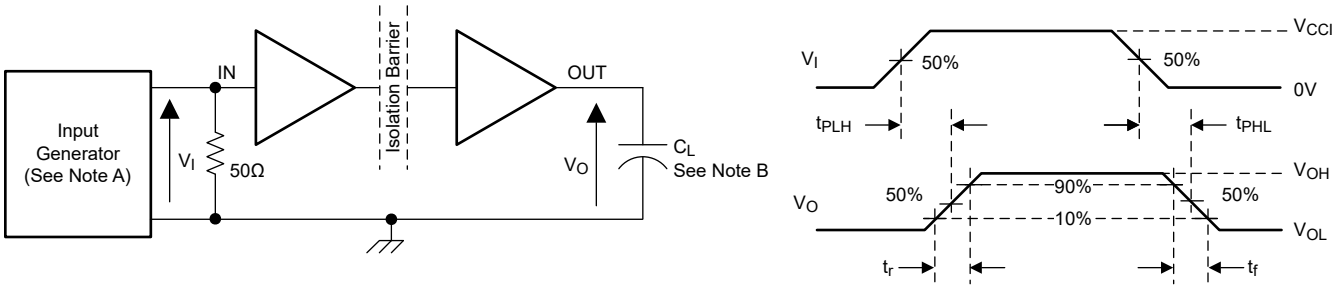



**Figure 5-16. Propagation Delay Time vs Free-Air Temperature**

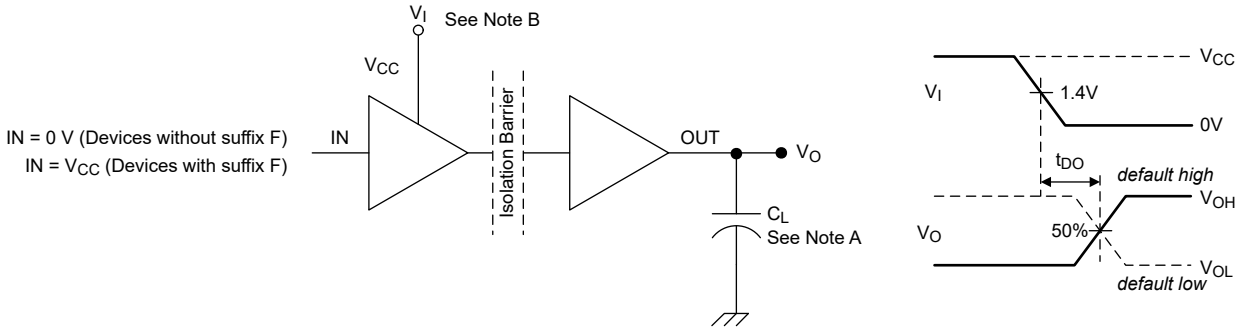
# 6 Parameter Measurement Information




A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50kHz, 50% duty cycle, $t_r$ ≤ 3ns, $t_f$ ≤ 3ns, $Z_O$ = 50Ω. At the input, 50Ω resistor is required to terminate Input Generator signal. The 50Ω resistor not needed in actual application.

B. $C_L$ = 15pF and includes instrumentation and fixture capacitance within ±20%.

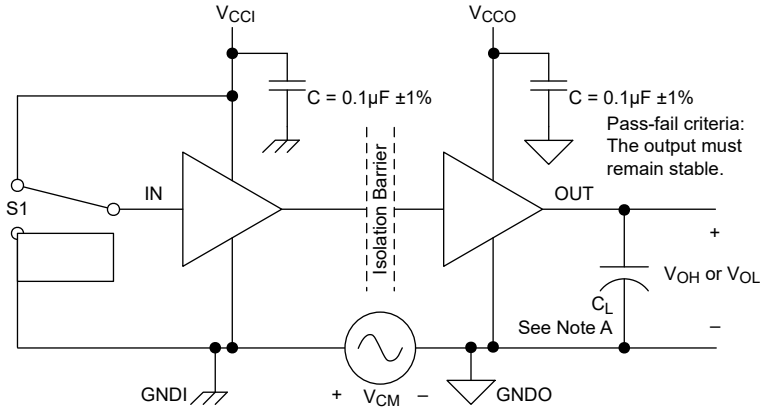
**Figure 6-1. Switching Characteristics Test Circuit and Voltage Waveforms**




A. $C_L$ = 15pF and includes instrumentation and fixture capacitance within ±20%.

B. Power Supply Ramp Rate = 10mV/ns

**Figure 6-2. Default Output Delay Time Test Circuit and Voltage Waveforms**




A. $C_L$ = 15pF and includes instrumentation and fixture capacitance within ±20%.

**Figure 6-3. Common-Mode Transient Immunity Test Circuit**

# 7 Detailed Description

## 7.1 Overview

The ISO672x-Q1family of devices has an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. These devices also incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, Figure 7-1, shows a functional block diagram of a typical channel.

## 7.2 Functional Block Diagram

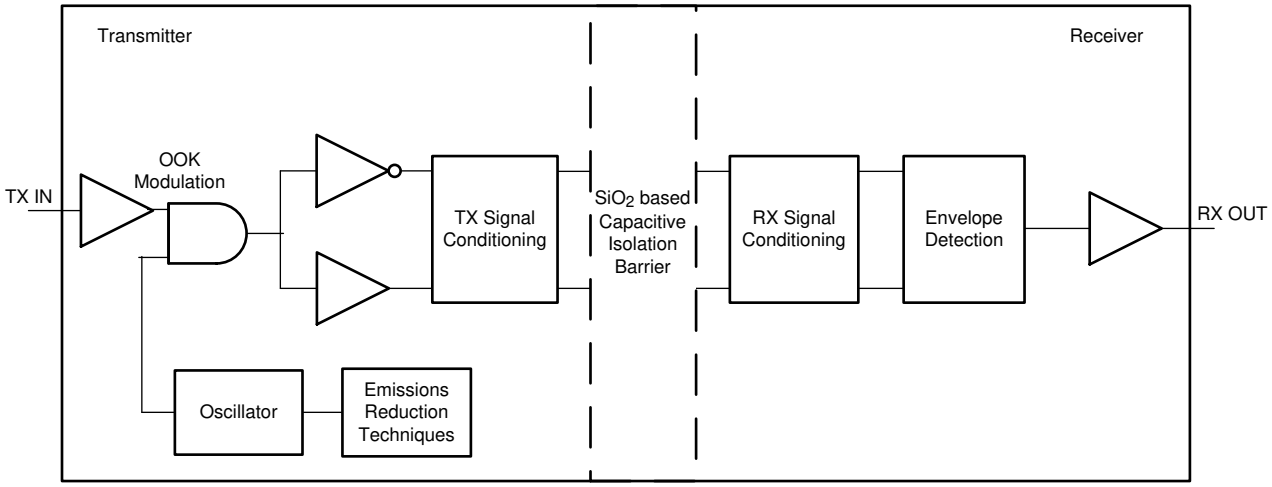



**Figure 7-1. Conceptual Block Diagram of a Digital Capacitive Isolator**

Figure 7-2 shows a conceptual detail of how the OOK scheme works.

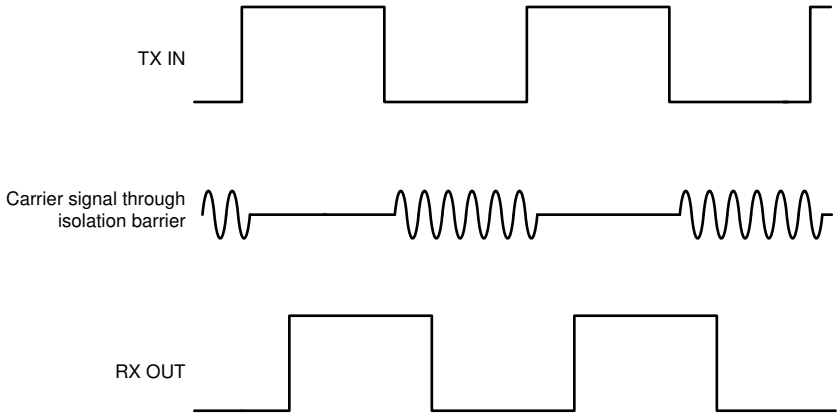



**Figure 7-2. On-Off Keying (OOK) Based Modulation Scheme**

## 7.3 Feature Description

The ISO672x-Q1 family of devices is available in two channel configurations and default output state options to enable a variety of application uses. Table 7-1 lists the device features of the ISO672x-Q1 devices.

**Table 7-1. Device Features**

| PART NUMBER | MAXIMUM DATA RATE | CHANNEL DIRECTION | DEFAULT OUTPUT STATE | PACKAGE | RATED ISOLATION(1) |
|---|---|---|---|---|---|
| ISO6720B-Q1 | 50Mbps | 2 Forward, 0 Reverse | High | D-8 | $3000V_{RMS}$ / $4242V_{PK}$ |
| ISO6720FB-Q1 | 50Mbps | 2 Forward, 0 Reverse | Low | D-8 | $3000V_{RMS}$ / $4242V_{PK}$ |
| ISO6721B-Q1 | 50Mbps | 1 Forward, 1 Reverse | High | D-8 | $3000V_{RMS}$ / $4242V_{PK}$ |
| ISO6721FB-Q1 | 50Mbps | 1 Forward, 1 Reverse | Low | D-8 | $3000V_{RMS}$ / $4242V_{PK}$ |
| ISO6721RB-Q1 | 50Mbps | 1 Forward, 1 Reverse | High | D-8 | $3000V_{RMS}$ / $4242V_{PK}$ |
| ISO6721RFB-Q1 | 50Mbps | 1 Forward, 1 Reverse | Low | D-8 | $3000V_{RMS}$ / $4242V_{PK}$ |
| ISO6720-Q1 | 50Mbps | 2 Forward, 0 Reverse | High | DWV-8 | $5000V_{RMS}$ / $7071V_{PK}$ |
| ISO6720F-Q1 | 50Mbps | 2 Forward, 0 Reverse | Low | DWV-8 | $5000V_{RMS}$ / $7071V_{PK}$ |
| ISO6721-Q1 | 50Mbps | 1 Forward, 1 Reverse | High | DWV-8 | $5000V_{RMS}$ / $7071V_{PK}$ |
| ISO6721F-Q1 | 50Mbps | 1 Forward, 1 Reverse | Low | DWV-8 | $5000V_{RMS}$ / $7071V_{PK}$ |

(1) See *Safety-Related Certifications* for detailed isolation ratings.

### *7.3.1 Electromagnetic Compatibility (EMC) Considerations*

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 25 . Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO672x-Q1 family of devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by providing purely differential internal operation.

## 7.4 Device Functional Modes

Table 7-2 lists the functional modes for the ISO672x-Q1 devices.

**Table 7-2. Function Table**

| $V_{CCI}$ (1) | $V_{CCO}$ | INPUT (INx)(2) | OUTPUT (OUTx) | COMMENTS |
|---|---|---|---|---|
| PU | PU | H | H | Normal Operation: A channel output assumes the logic state of the input. |
| | | L | L | |
| | | Open | Default | Default mode: When INx is open, the corresponding channel output goes to the default logic state. The default is *High* for ISO672x-Q1 and *Low* for ISO672x-Q1 with F suffix. |
| PD | PU | X | Default | Default mode: When $V_{CCI}$ is unpowered, a channel output assumes the logic state based on the selected default option. The default is *High* for ISO672x-Q1 and *Low* for ISO672x-Q1 with F suffix.<br>When $V_{CCI}$ transitions from unpowered to powered-up, a channel output assumes the logic state of the input.<br>When $V_{CCI}$ transitions from powered-up to unpowered, channel output assumes the selected default state. |
| X | PD | X | Undetermined | When $V_{CCO}$ is unpowered, a channel output is undetermined(3).<br>When $V_{CCO}$ transitions from unpowered to powered-up, a channel output assumes the logic state of the input |

(1) $V_{CCI}$ = Input-side $V_{CC}$; $V_{CCO}$ = Output-side $V_{CC}$; PU = Powered up ($V_{CC}$ ≥ 1.71V); PD = Powered down ($V_{CC}$ ≤ 1.05V); X = Irrelevant; H = High level; L = Low level
(2) A strongly driven input signal can weakly power the floating $V_{CC}$ using an internal protection diode and cause undetermined output.
(3) The outputs are in undetermined state when 1.89V < $V_{CCI}$, $V_{CCO}$ < 2.25V and 1.05V < $V_{CCI}$, $V_{CCO}$ < 1.71V

### 7.4.1 Device I/O Schematics

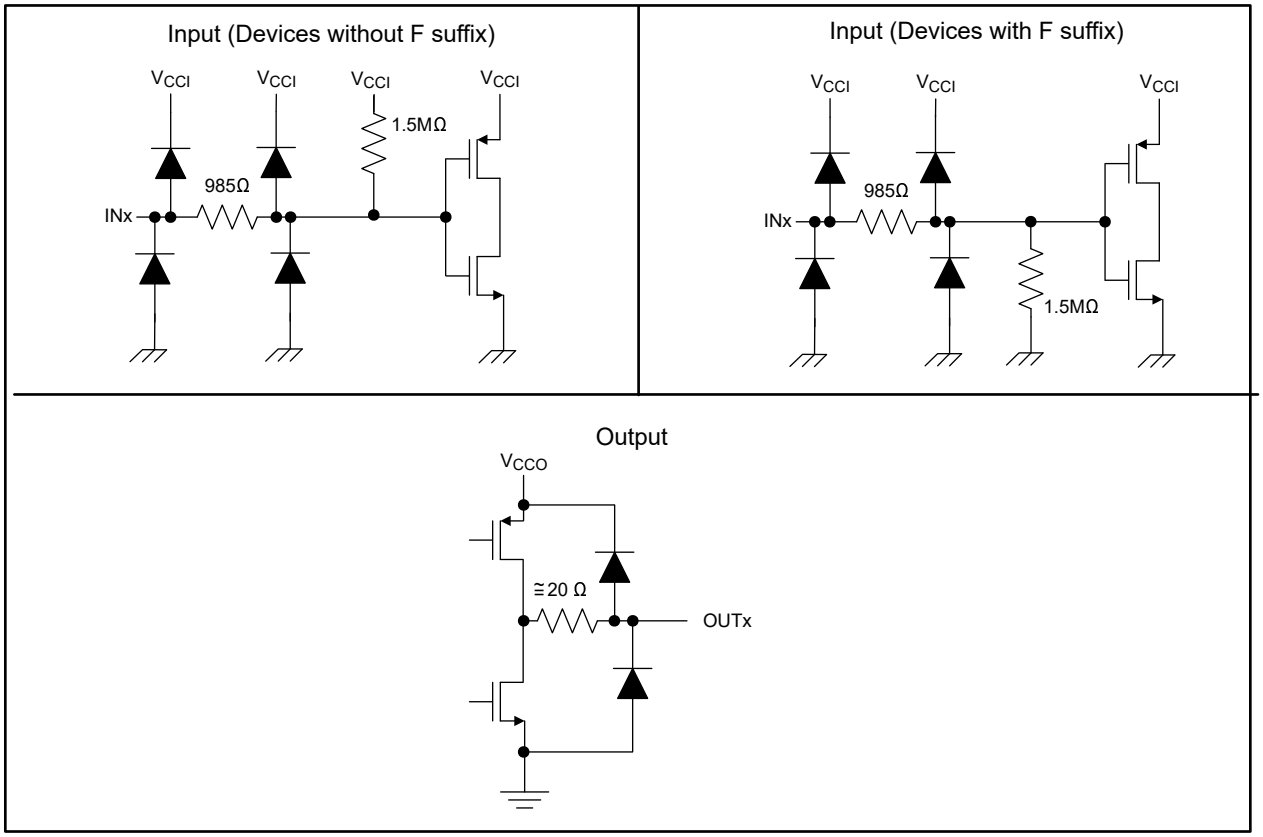



**Figure 7-3. Device I/O Schematics**

# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant the accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The ISO672x-Q1 devices are high-performance, dual-channel digital isolators. The devices use single-ended CMOS-logic switching technology. The supply voltage range is from 1.71V to 5.5V for both supplies, $V_{CC1}$ and $V_{CC2}$. Since an isolation barrier separates the two sides, each side can be sourced independently with any voltage within recommended operating conditions. As an example, supplying ISO672x-Q1 $V_{CC1}$ with 3.3V (which is within 1.71V to 1.89V and 2.25V to 5V) and $V_{CC2}$ with 5V (which is also within 1.71V to 1.89V and 2.25V to 5V) is possible. You can use the digital isolator as a logic-level translator in addition to providing isolation. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, MCU or FPGA), and a data converter or a line transceiver, regardless of the interface type or standard.

## 8.2 Typical Application

For automotive applications, the ISO672x-Q1 device can also be used with Texas Instruments' Piccolo™ microcontroller, CAN transceiver, transformer driver, and voltage regulator to create an isolated CAN interface.

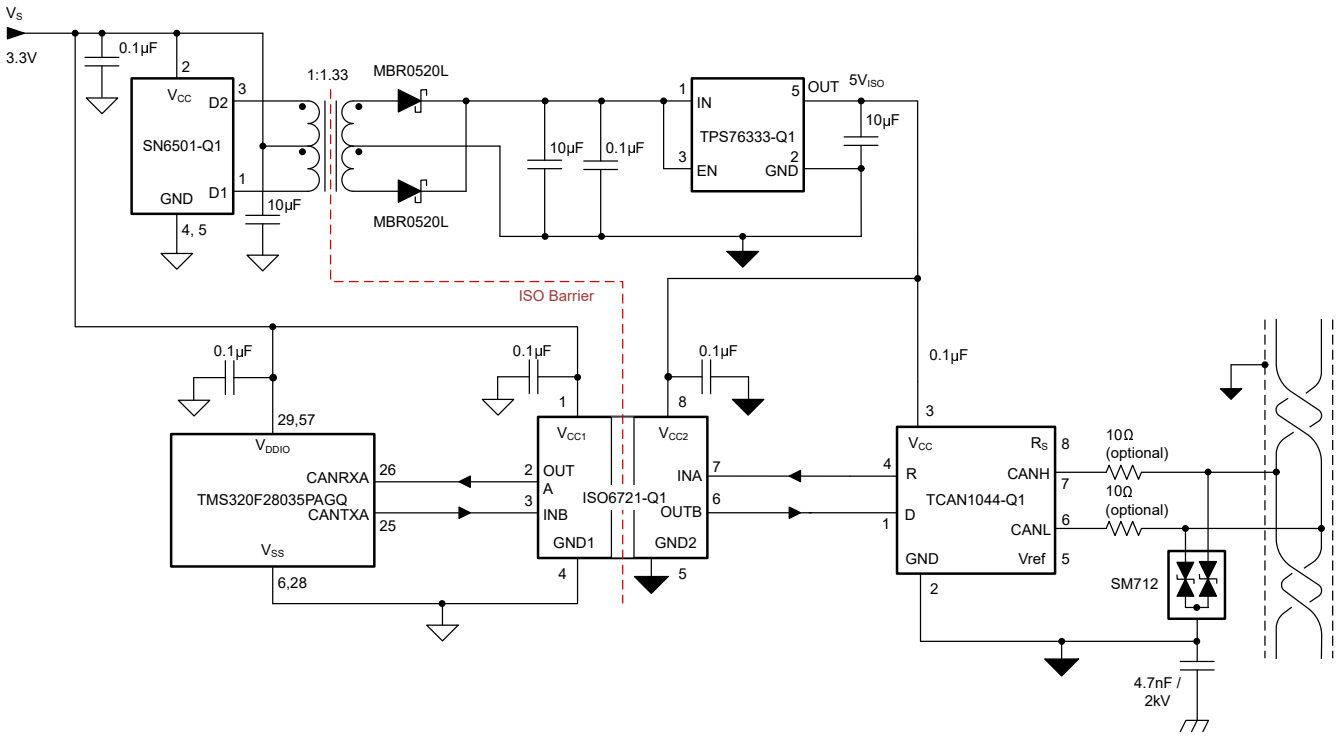



**Figure 8-1. Typical Isolated CAN Application Circuit**

### 8.2.1 Design Requirements

To design with these devices, use the parameters listed in Table 8-1.

**Table 8-1. Design Parameters**

| PARAMETER | VALUE |
|---|---|
| Supply voltage, $V_{CC1}$ and $V_{CC2}$ | 1.71V to 1.89V and 2.25V to 5.5V |
| Decoupling capacitor between $V_{CC1}$ and GND1 | 0.1µF |
| Decoupling capacitor from $V_{CC2}$ and GND2 | 0.1µF |

### 8.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO672x-Q1 devices only require two external bypass capacitors to operate.

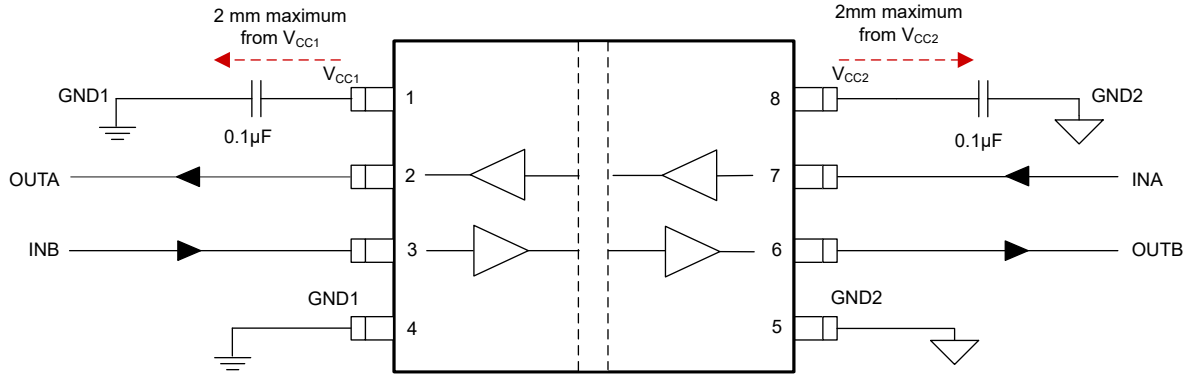



**Figure 8-2. Typical ISO672x-Q1 Circuit Hook-up**

### 8.2.3 Application Curve

The following typical eye diagrams of the ISO672x-Q1 family of devices indicate low jitter and wide open eye at the maximum data rate of 50Mbps.

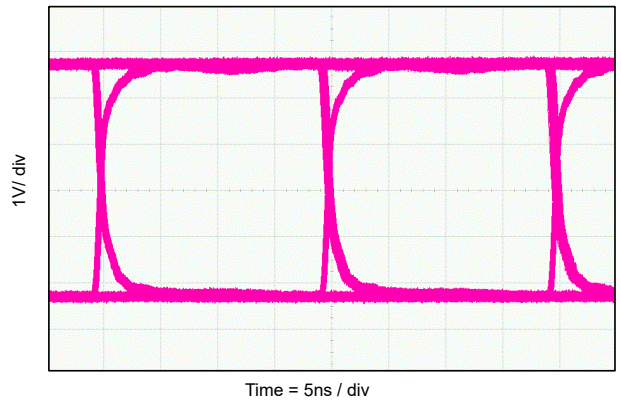



**Figure 8-3. Eye Diagram at 50Mbps PRBS $2^{16}$ – 1, 5V and 25°C**

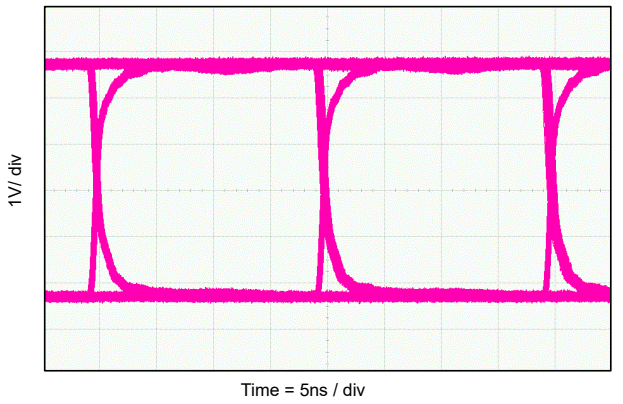



**Figure 8-4. Eye Diagram at 50Mbps PRBS $2^{16}$ – 1, 3.3V and 25°C**

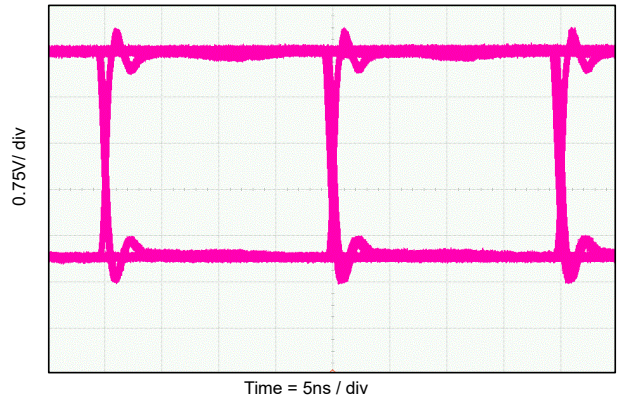



**Figure 8-5. Eye Diagram at 50Mbps PRBS $2^{16}$ – 1, 2.5V and 25°C**

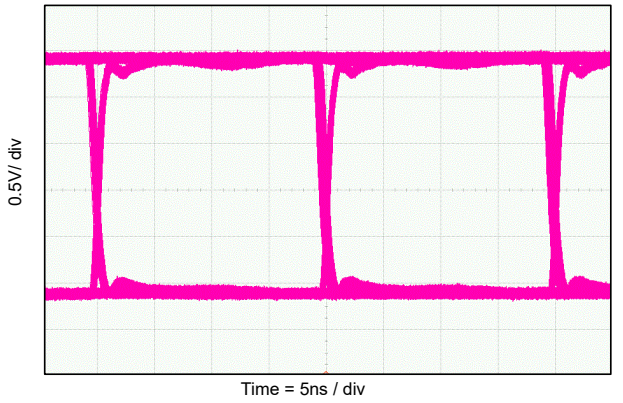



**Figure 8-6. Eye Diagram at 50Mbps PRBS $2^{16}$ – 1, 1.8V and 25°C**

#### 8.2.3.1 *Insulation Lifetime*

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See Figure 8-7 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60Hz over temperature. For basic insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1000 part per million (ppm). For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm).

Even though the expected minimum insulation lifetime is 20 years, at the specified working isolation voltage, VDE basic and reinforced certifications require additional safety margin of 20% for working voltage. For basic certification, device lifetime requires a safety margin of 20% translating to a minimum required insulation lifetime of 24 years at a working voltage that is 20% higher than the specified value. For reinforced insulation, device lifetime requires a safety margin of 50% translating to a minimum required insulation lifetime of 30 years at a working voltage that is 20% higher than the specified value

Figure 8-8 and Figure 8-9 show the intrinsic capability of the isolation barrier to withstand high voltage stress over the lifetime of the barrier. Based on the TDDB data, the intrinsic capability of the insulation is $1060V_{RMS}$ in the 8-DWV package and $450V_{RMS}$ in the 8D package with a lifetime of >100 years. Other factors, such as package size, pollution degree, material group, and so forth. can further limit the working voltage of the component.

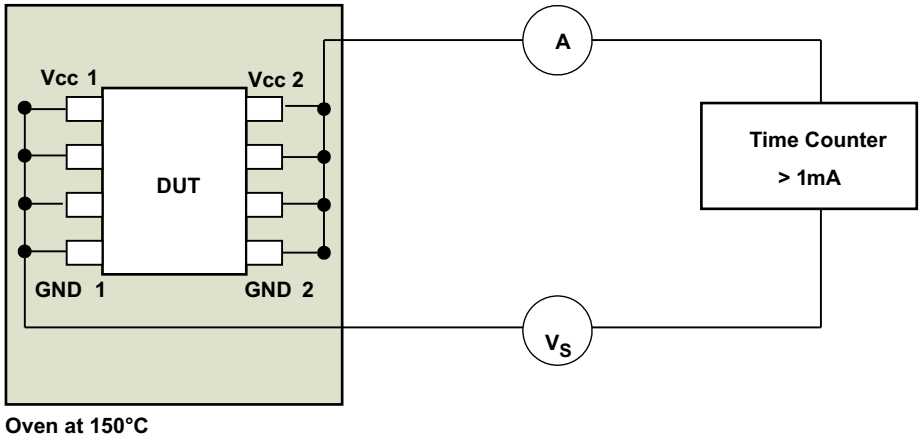



**Figure 8-7. Test Setup for Insulation Lifetime Measurement**

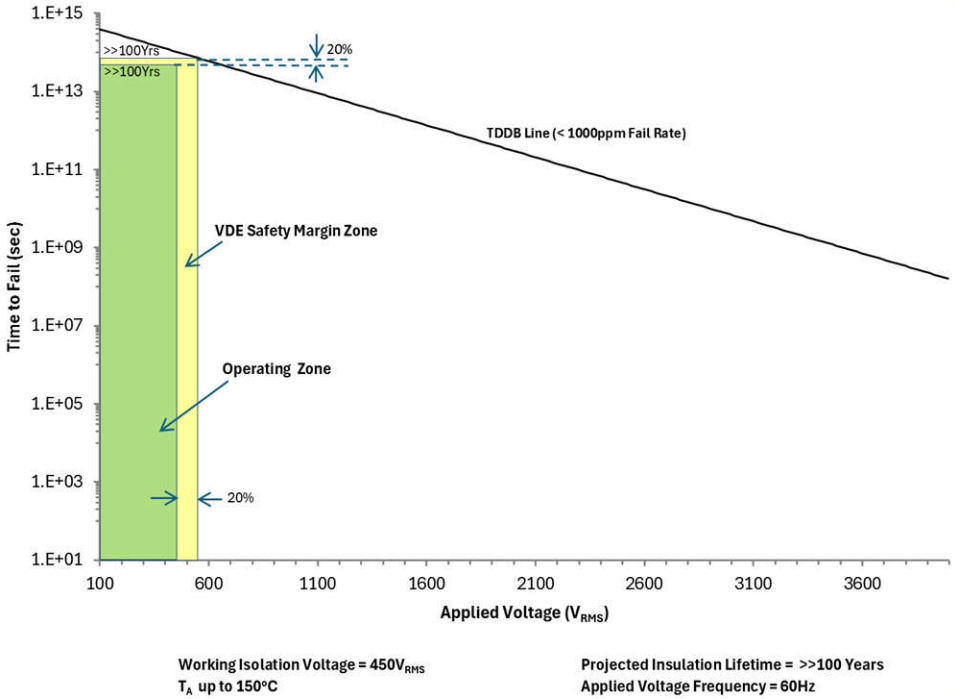



**Figure 8-8. Insulation Lifetime Projection Data for 8D Package**

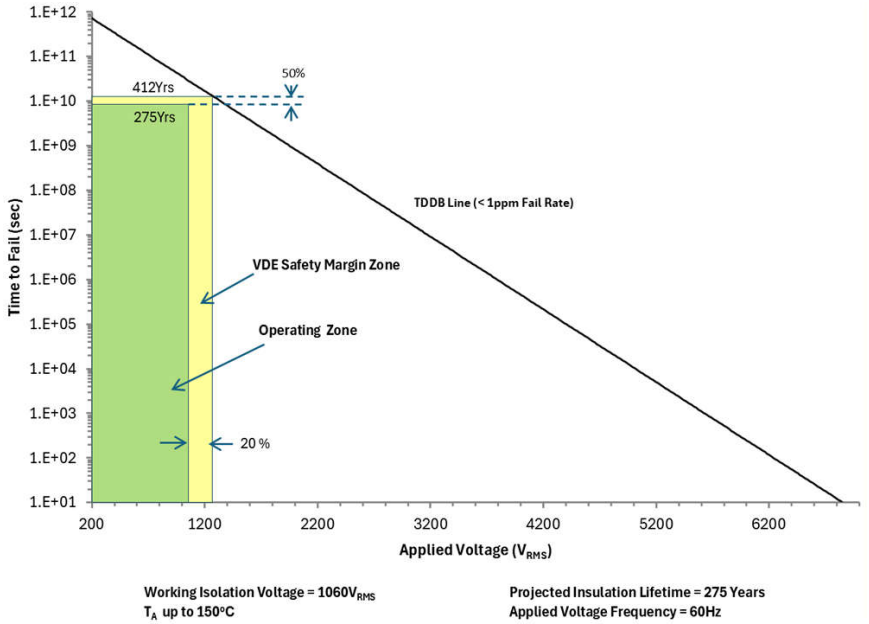



**Figure 8-9. Insulation Lifetime Projection Data for 8-DWV Package**

## 8.3 Power Supply Recommendations

To help provide reliable operation at data rates and supply voltages, a 0.1µF bypass capacitor is recommended at the input and output supply pins ($V_{CC1}$ and $V_{CC2}$). The capacitors must be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver. For automotive applications, please use SN6501-Q1 or SN6505B-Q1. For such applications, detailed power supply design and transformer selection recommendations are available in *SN6501-Q1 Transformer Driver for Isolated Power Supplies* or *SN6505B-Q1 Automotive, low-noise, 1A, 420kHz transformer driver with soft start for isolated power supplies* .

## 8.4 Layout

### *8.4.1 Layout Guidelines*

A minimum of two layers is required to accomplish a cost optimized and low EMI PCB design. To further improve EMI, a four layer board can be used (see Section 8.4.2). Layer stacking for a four layer board must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of the inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100pF/in$^2$.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links typically have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep the planes symmetrical. This makes the stack mechanically stable and prevents warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the *Digital Isolator Design Guide*.

#### 8.4.1.1 PCB Material

For digital circuit boards operating at less than 150Mbps, (or rise and fall times greater than 1ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

### 8.4.2 Layout Example

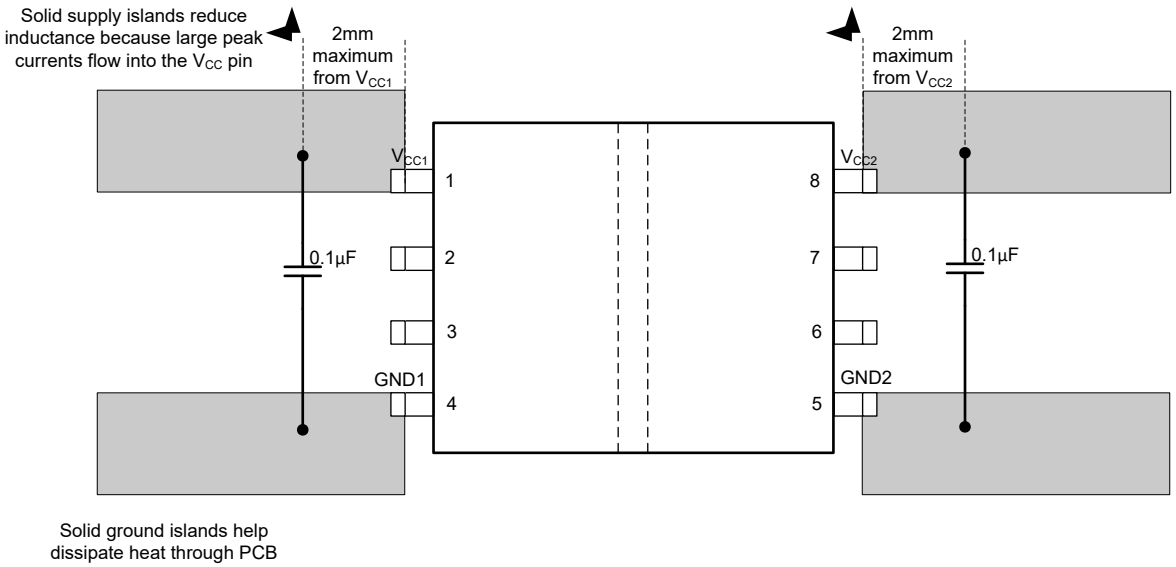



**Figure 8-10. Layout Example**

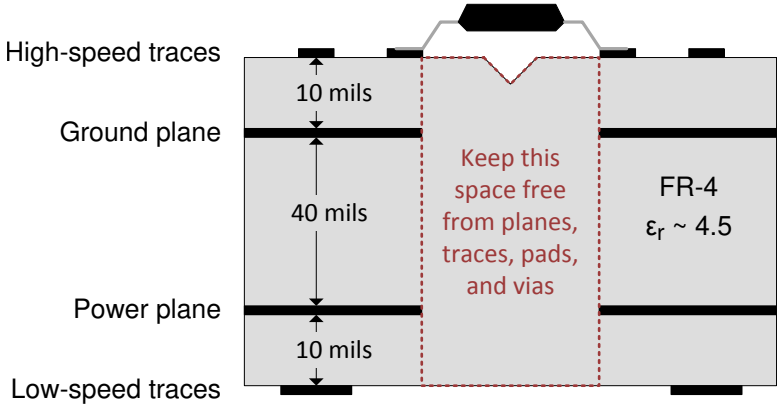



**Figure 8-11. Four Layer Board Layout Example**

# 9 Device and Documentation Support

## 9.1 Device Support

### 9.1.1 Development Support

For development support, refer to:

- Isolated CAN Flexible Data (FD) Rate Repeater Reference Design
- Isolated 16-Channel AC Analog Input Module Reference Design Using Dual Simultaneously Sampled ADCs
- Polyphase Shunt Metrology with Isolated AFE Reference Design
- Reference Design for Power-Isolated Ultra-Compact Analog Output Module

## 9.2 Documentation Support

### 9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Digital Isolator Design Guide*
- Texas Instruments, *How to use isolation to improve ESD, EFT and Surge immunity in industrial systems* application note
- Texas Instruments, *Isolation Glossary*
- Texas Instruments, *Enabling high voltage signal isolation quality and reliability*
- Texas Instruments, *SN6501-Q1 Transformer Driver for Isolated Power Supplies* datasheet
- Texas Instruments, SN65HVD231Q *3.3V CAN Transceivers* datasheet
- Texas Instruments, *TPS763xx-Q1 Low-Power, 150mA, Low-Dropout Linear Regulators* datasheet
- Texas Instruments, *TMS320F2803x Piccolo™ Microcontrollers* datasheet

## 9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 9.5 Trademarks

Piccolo™ is a trademark of Texas Instruments.
TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.7 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

## 10 Revision History

**Changes from Revision H (May 2022) to Revision I (August 2026)** **Page**

- Updated the certification information in the *Features* and throughout the document ..... 1
- Updated the number formatting for tables, figures, and cross-references throughout the document ..... 2
- Added maximum impulse voltage ($V_{IMP}$) parameter per IEC 60747-17. $V_{IMP}$ value is 7692 $V_{PK}$ for 8-DWV package and 5000 $V_{PK}$ for 8-D package. ..... 8
- Changed $V_{IOSM}$ value From: 6250 $V_{PK}$ To: 10000 $V_{PK}$ for 8-DWV package and From: 5000 $V_{PK}$ To: 6500 $V_{PK}$ for 8-D package per IEC 60747-17 ..... 8
- Updated *Insulation Lifetime Projection Data* image and the *Insulation Lifetime* section ..... 34

**Changes from Revision G (January 2022) to Revision H (May 2022)** **Page**

- Updated CMTI typical to 150 kV/us and minimum to 100 kV/us ..... 5

**Changes from Revision F (November 2021) to Revision G (January 2022)** **Page**

- Added missing DWV Insulation Specification. ..... 5

**Changes from Revision E (July 2021) to Revision F (November 2021)** **Page**

- Added ISO6721RBD to the data sheet ..... 2

**Changes from Revision D (April 2021) to Revision E (July 2021)** **Page**

- Updated Safety-Related Certifications table ..... 5
- Updated test conditions in all Switching Characteristics tables ..... 5
- Updated *Insulation Lifetime Projection Data* image ..... 34
- Updated *Power Supply Recommendations* document references ..... 36

**Changes from Revision C (March 2021) to Revision D (April 2021)** **Page**

- Updated device status to "Production Data" ..... 2

**Changes from Revision B (January 2021) to Revision C (March 2021)** **Page**

- Added the *Device Support* section ..... 38

**Changes from Revision A (December 2020) to Revision B (January 2021)** **Page**

- Changed device status to Production Data ..... 1
- Added the *Receiving Notification of Documentation Updates* section ..... 38
- Changed the *Electrostatic Discharge Caution* statement ..... 38

| Changes from Revision * (July 2020) to Revision A (December 2020) | Page |
|---|---|
| • Pre-RTM updates | 1 |

## 11 Mechanical, Packaging, and Orderable Information

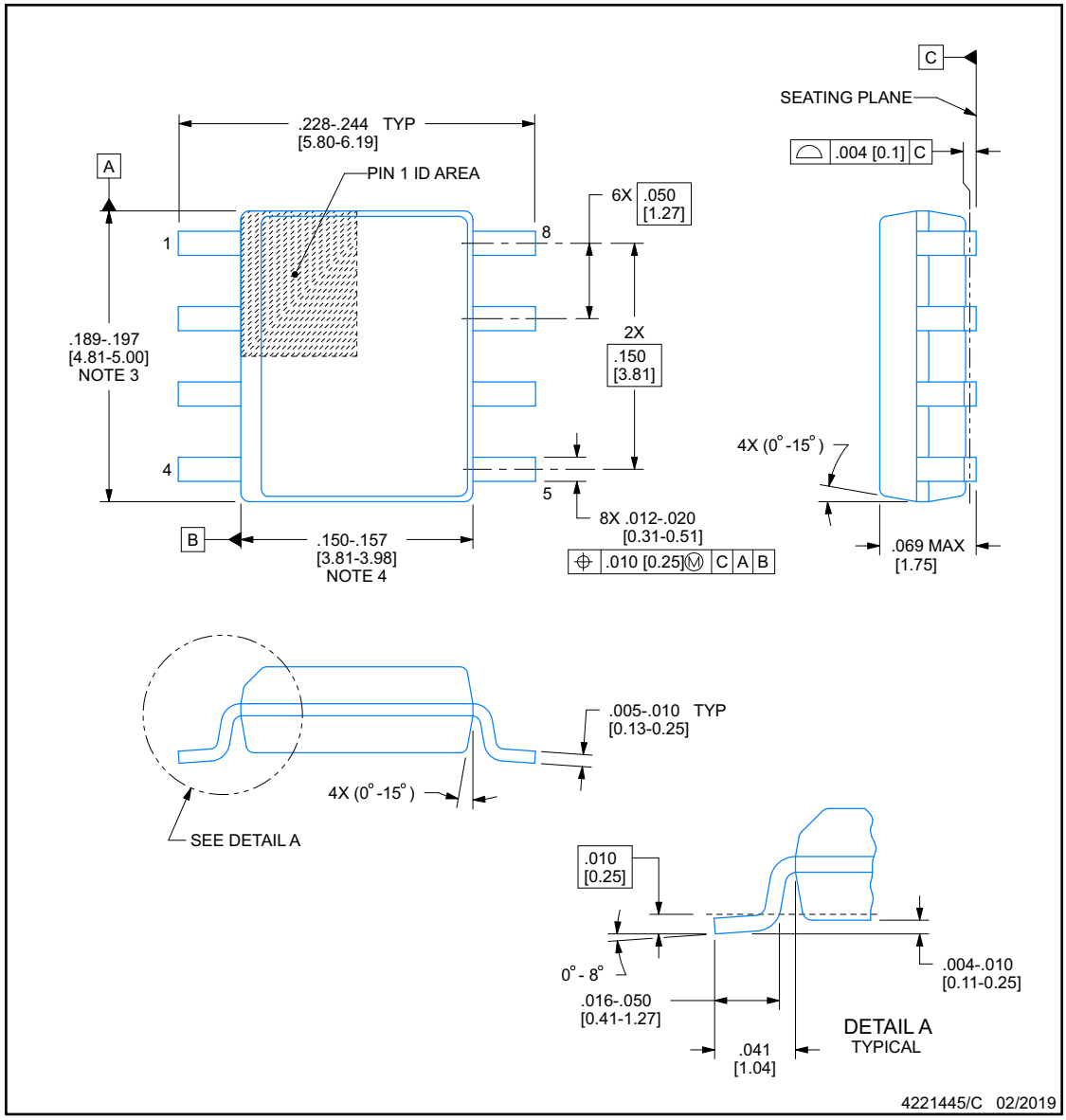
The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

# PACKAGE OUTLINE

## D0008B

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




NOTES:

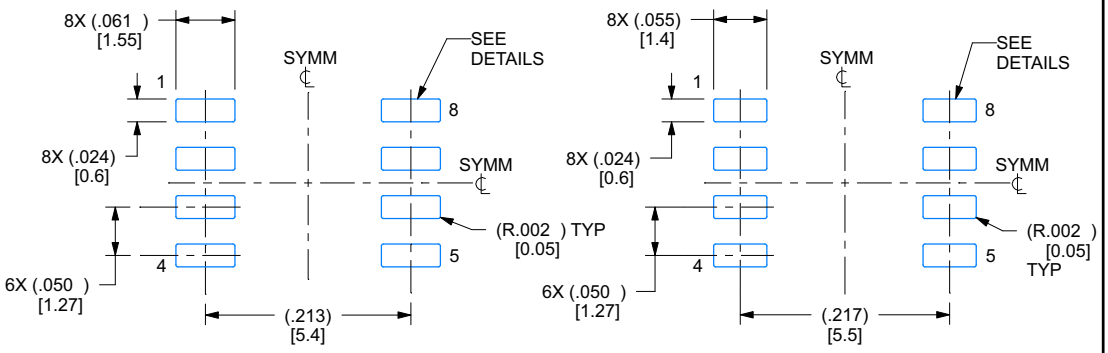
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15], per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

## EXAMPLE BOARD LAYOUT

### D0008B

### SOIC - 1.75 mm max height

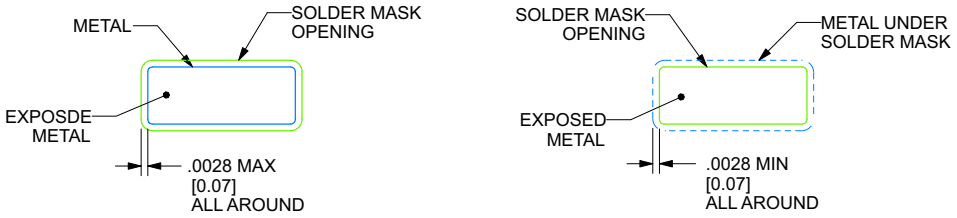
SMALL OUTLINE INTEGRATED CIRCUIT




IPC-7351 NOMINAL
.150 [3.85] CLEARANCE / CREEPAGE

HV / ISOLATION OPTION
.162 [4.1] CLEARANCE / CREEPAGE

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X




NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4221445/C 02/2019

NOTES: (continued)

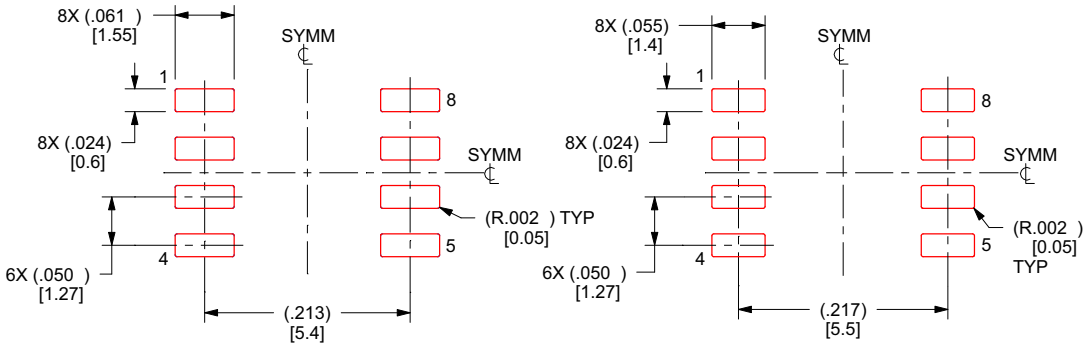
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008B

### SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




IPC-7351 NOMINAL
.150 [3.85] CLEARANCE / CREEPAGE

HV / ISOLATION OPTION
.162 [4.1] CLEARANCE / CREEPAGE

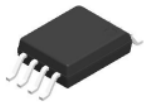
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:6X

4221445/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

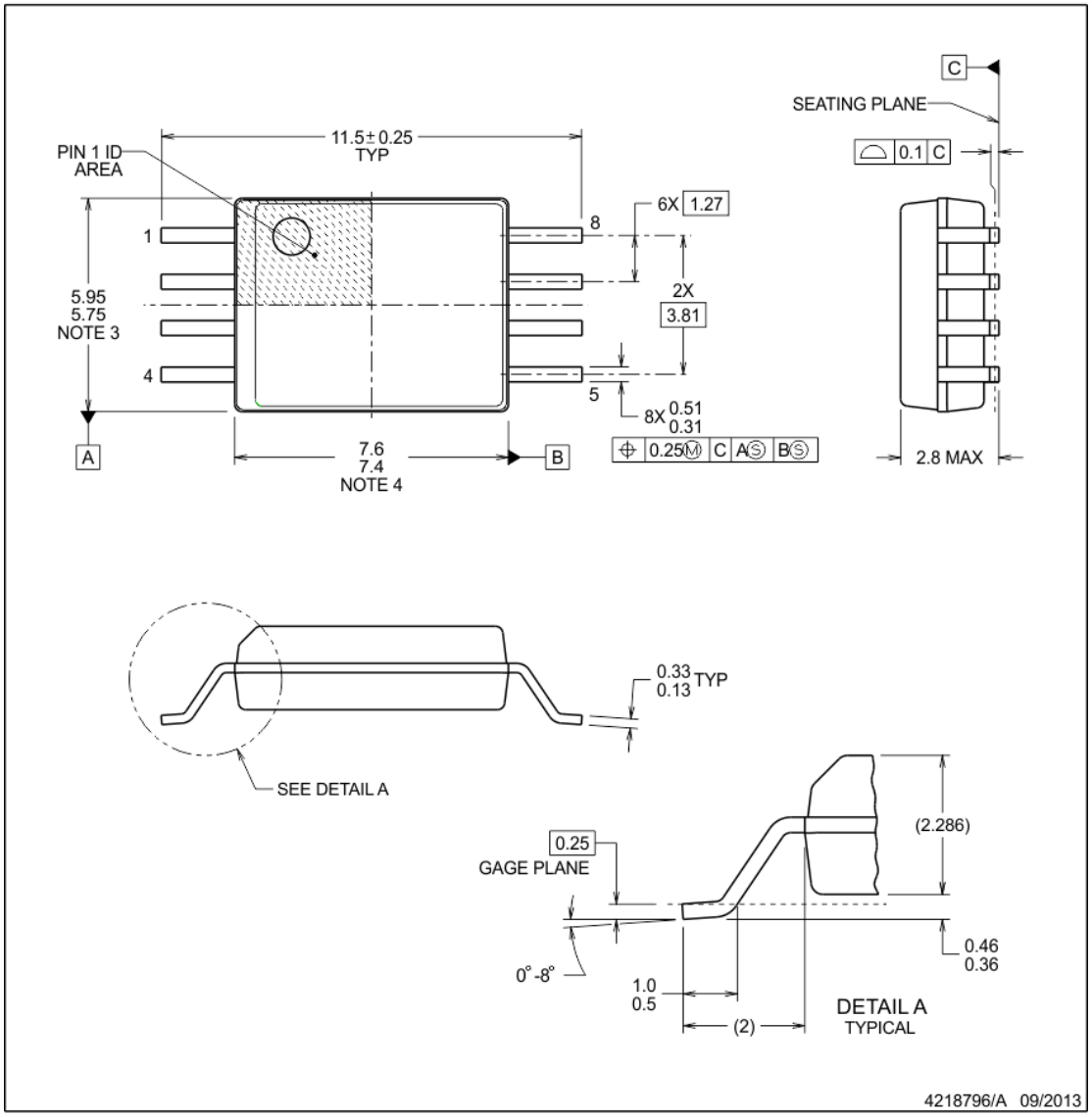
# PACKAGE OUTLINE



## DWV0008A

SOIC - 2.8 mm max height

SOIC



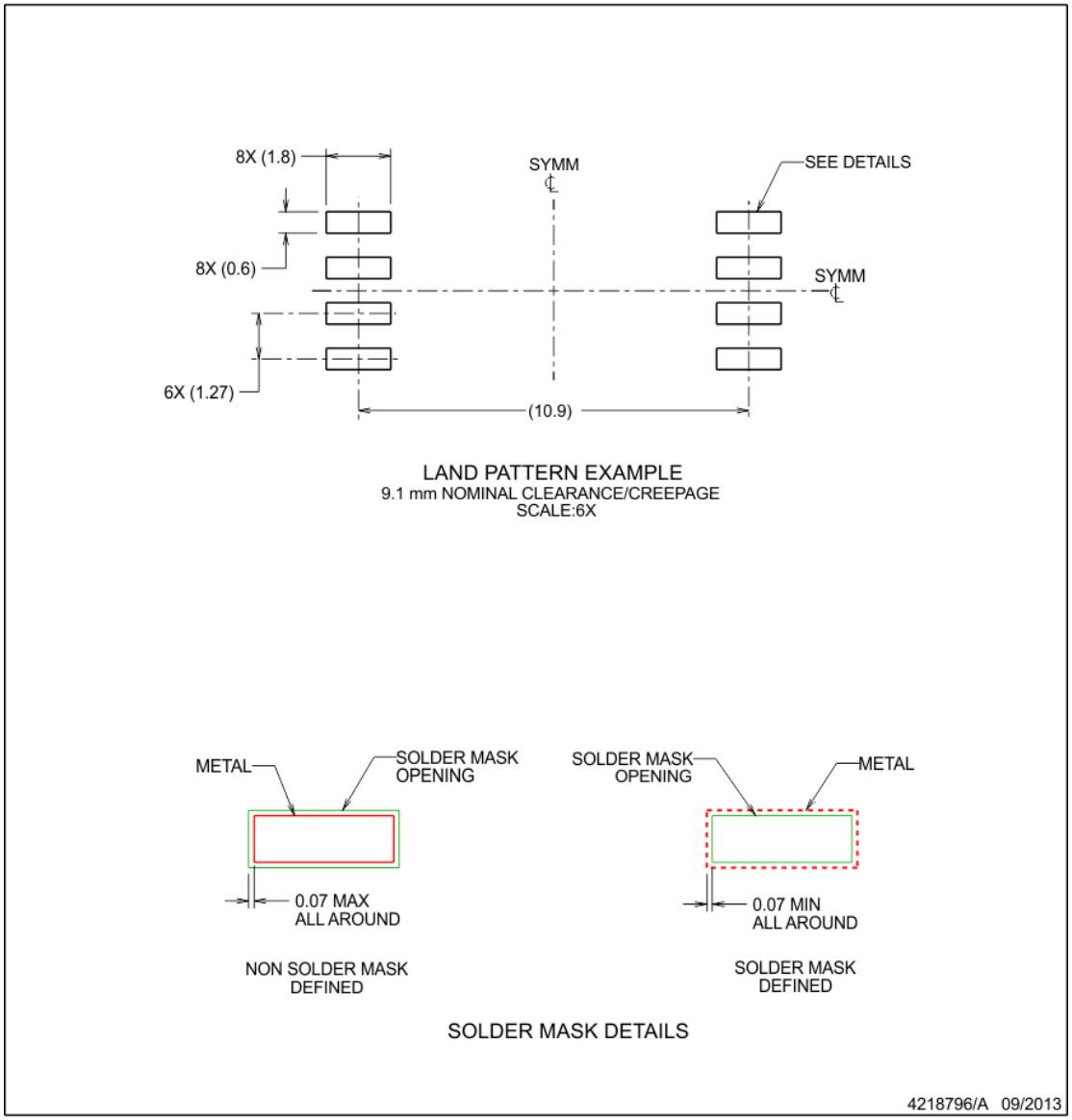

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

## DWV0008A — SOIC - 2.8 mm max height

SOIC



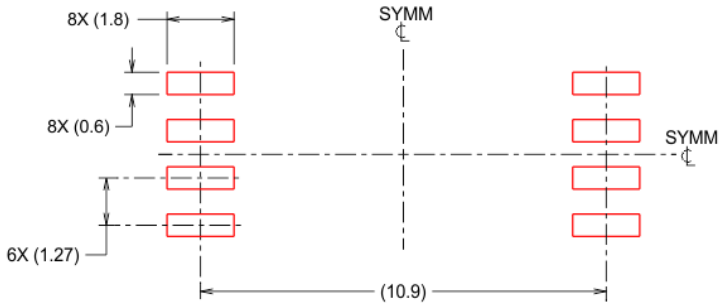

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DWV0008A — SOIC - 2.8 mm max height

SOIC




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

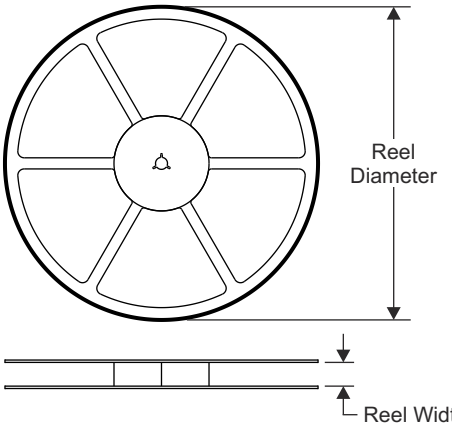
## 11.1 Package Option Addendum

### Packaging Information

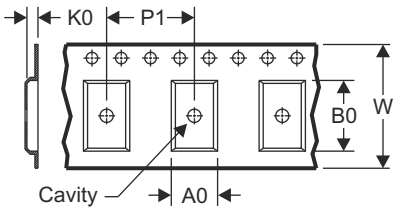
| Orderable Device | Status(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan(2) | Lead/Ball Finish(6) | MSL Peak Temp(3) | Op Temp (°C) | Device Marking(4) (5) |
|---|---|---|---|---|---|---|---|---|---|---|
| ISO6720QDWVRQ1 | ACTIVE | SOIC | DWV | 8 | 1000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 6720 |
| ISO6720FQDWVRQ1 | ACTIVE | SOIC | DWV | 8 | 1000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 6720F |
| ISO6721QDWVRQ1 | ACTIVE | SOIC | DWV | 8 | 1000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 6721 |
| ISO6721FQDWVRQ1 | ACTIVE | SOIC | DWV | 8 | 1000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 6721F |
| ISO6720BQDRQ1 | ACTIVE | SOIC | D | 8 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 6720B |
| ISO6720FBQDRQ1 | ACTIVE | SOIC | D | 8 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 6720FB |
| ISO6721BQDRQ1 | ACTIVE | SOIC | D | 8 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 6721B |
| ISO6721FBQDRQ1 | ACTIVE | SOIC | D | 8 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 6721FB |
| ISO6721RBQDRQ1 | ACTIVE | SOIC | D | 8 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 21RB |
| ISO6721RFBQDRQ | ACTIVE | SOIC | D | 8 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 21RFB |

## 11.2 Tape and Reel Information

REEL DIMENSIONS

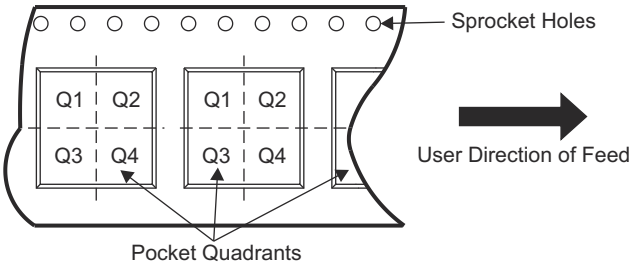



TAPE DIMENSIONS



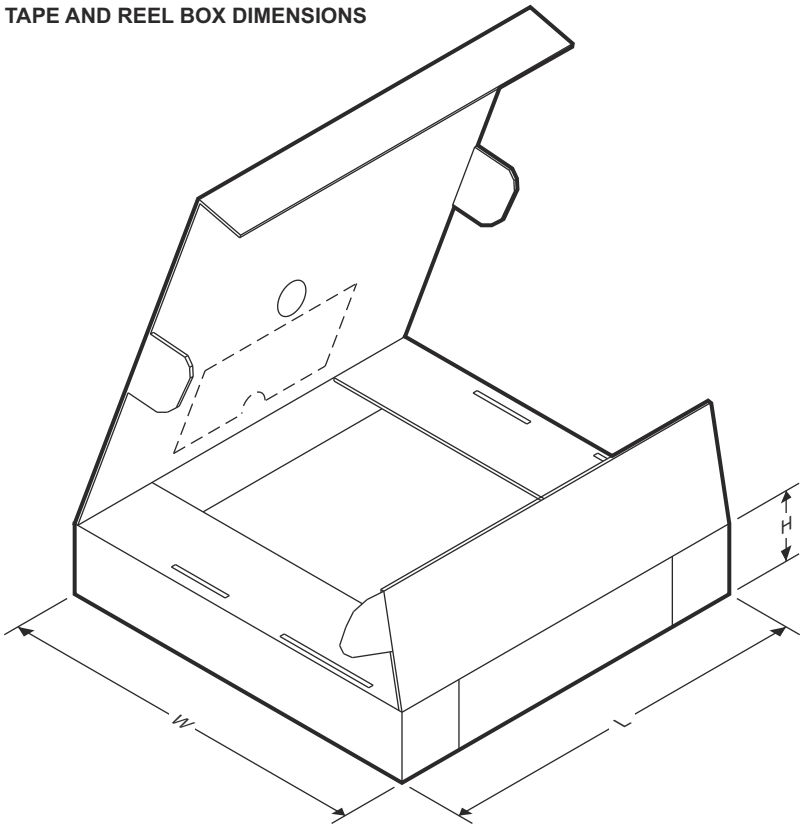

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ISO6720QDWVRQ1 | SOIC | DWV | 8 | 1000 | 330.0 | 16.4 | 12.05 | 6.15 | 3.3 | 16.0 | 16.0 | Q1 |
| ISO6720FQDWVRQ1 | SOIC | DWV | 8 | 1000 | 330.0 | 16.4 | 12.05 | 6.15 | 3.3 | 16.0 | 16.0 | Q1 |
| ISO6721QDWVRQ1 | SOIC | DWV | 8 | 1000 | 330.0 | 16.4 | 12.05 | 6.15 | 3.3 | 16.0 | 16.0 | Q1 |
| ISO6721FQDWVRQ1 | SOIC | DWV | 8 | 1000 | 330.0 | 16.4 | 12.05 | 6.15 | 3.3 | 16.0 | 16.0 | Q1 |
| ISO6720BQDRQ1 | SOIC | D | 8 | 3000 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| ISO6720FBQDRQ1 | SOIC | D | 8 | 3000 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| ISO6721BQDRQ1 | SOIC | D | 8 | 3000 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| ISO6721FBQDRQ1 | SOIC | D | 8 | 3000 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| ISO6721RBQDRQ1 | SOIC | D | 8 | 3000 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| ISO6721RFBQDRQ | SOIC | D | 8 | 3000 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**




| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| ISO6720QDWVRQ1 | SOIC | DWV | 8 | 1000 | 350.0 | 350.0 | 43.0 |
| ISO6720FQDWVRQ1 | SOIC | DWV | 8 | 1000 | 350.0 | 350.0 | 43.0 |
| ISO6721QDWVRQ1 | SOIC | DWV | 8 | 1000 | 350.0 | 350.0 | 43.0 |
| ISO6721FQDWVRQ1 | SOIC | DWV | 8 | 1000 | 350.0 | 350.0 | 43.0 |
| ISO6720BQDRQ1 | SOIC | D | 8 | 3000 | 367.0 | 367.0 | 35.0 |
| ISO6720FBQDRQ1 | SOIC | D | 8 | 3000 | 367.0 | 367.0 | 35.0 |
| ISO6721BQDRQ1 | SOIC | D | 8 | 3000 | 367.0 | 367.0 | 35.0 |
| ISO6721FBQDRQ1 | SOIC | D | 8 | 3000 | 367.0 | 367.0 | 35.0 |
| ISO6721RBQDRQ1 | SOIC | D | 8 | 3000 | 367.0 | 367.0 | 35.0 |
| ISO6721RFBQDRQ | SOIC | D | 8 | 3000 | 367.0 | 367.0 | 35.0 |

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| ISO6720BQDRQ1 | Active | Production | SOIC (D) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 6720B |
| ISO6720BQDRQ1.A | Active | Production | SOIC (D) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 6720B |
| ISO6720FBQDRQ1 | Active | Production | SOIC (D) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 6720FB |
| ISO6720FBQDRQ1.A | Active | Production | SOIC (D) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 6720FB |
| ISO6720FQDWVRQ1 | Active | Production | SOIC (DWV) \| 8 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 6720F |
| ISO6720FQDWVRQ1.A | Active | Production | SOIC (DWV) \| 8 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 6720F |
| ISO6720QDWVRQ1 | Active | Production | SOIC (DWV) \| 8 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 6720 |
| ISO6720QDWVRQ1.A | Active | Production | SOIC (DWV) \| 8 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 6720 |
| ISO6721BQDRQ1 | Active | Production | SOIC (D) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 6721B |
| ISO6721BQDRQ1.A | Active | Production | SOIC (D) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 6721B |
| ISO6721FBQDRQ1 | Active | Production | SOIC (D) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 6721FB |
| ISO6721FBQDRQ1.A | Active | Production | SOIC (D) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 6721FB |
| ISO6721FQDWVRQ1 | Active | Production | SOIC (DWV) \| 8 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 6721F |
| ISO6721FQDWVRQ1.A | Active | Production | SOIC (DWV) \| 8 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 6721F |
| ISO6721QDWVRQ1 | Active | Production | SOIC (DWV) \| 8 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 6721 |
| ISO6721QDWVRQ1.A | Active | Production | SOIC (DWV) \| 8 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 6721 |
| ISO6721RBQDRQ1 | Active | Production | SOIC (D) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 21RB |
| ISO6721RBQDRQ1.A | Active | Production | SOIC (D) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 21RB |
| ISO6721RFBQDRQ1 | Active | Production | SOIC (D) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 21RFB |
| ISO6721RFBQDRQ1.A | Active | Production | SOIC (D) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 21RFB |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

**(4) Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.



**OTHER QUALIFIED VERSIONS OF ISO6720-Q1, ISO6721-Q1, ISO6721R-Q1 :**

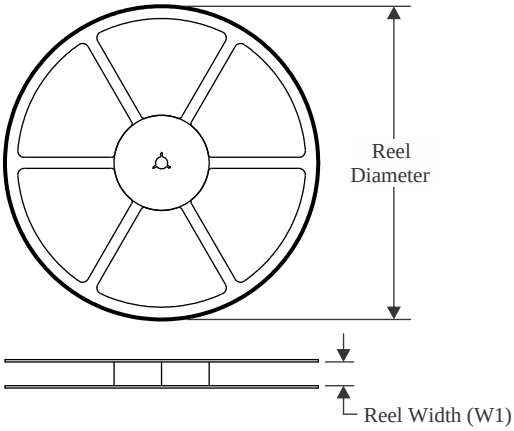
- Catalog : ISO6720, ISO6721, ISO6721R

NOTE: Qualified Version Definitions:

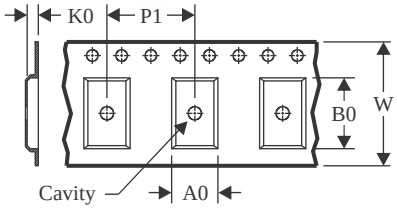
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

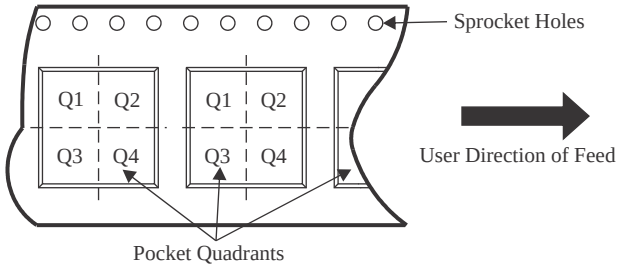



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

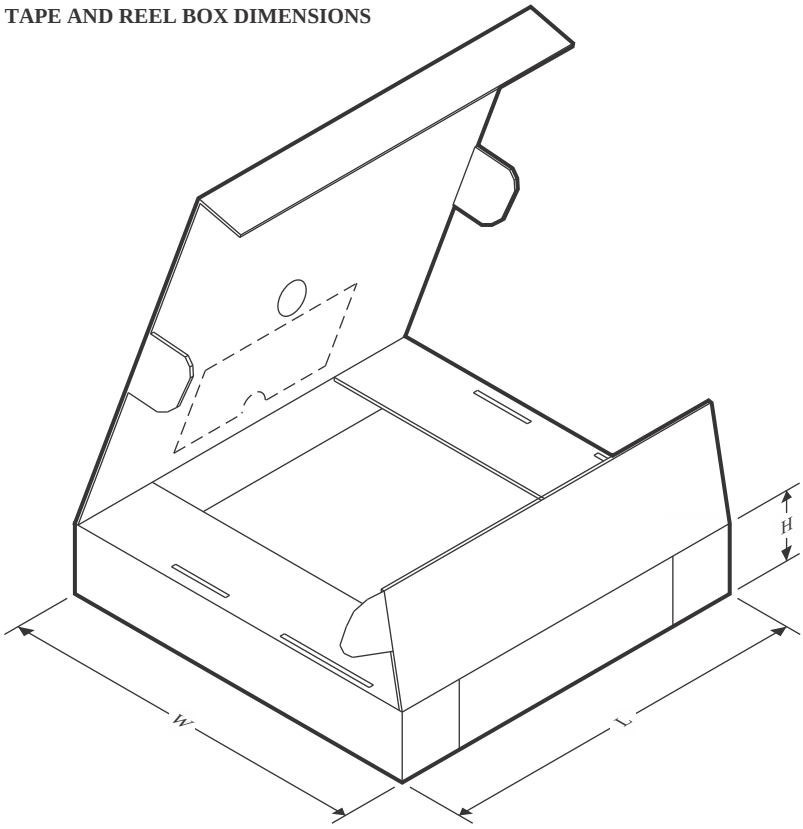



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ISO6720BQDRQ1 | SOIC | D | 8 | 3000 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| ISO6720BQDRQ1 | SOIC | D | 8 | 3000 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| ISO6720FBQDRQ1 | SOIC | D | 8 | 3000 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| ISO6720FBQDRQ1 | SOIC | D | 8 | 3000 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| ISO6720FQDWVRQ1 | SOIC | DWV | 8 | 1000 | 330.0 | 16.4 | 12.05 | 6.15 | 3.3 | 16.0 | 16.0 | Q1 |
| ISO6720FQDWVRQ1 | SOIC | DWV | 8 | 1000 | 330.0 | 16.4 | 12.15 | 6.2 | 3.05 | 16.0 | 16.0 | Q1 |
| ISO6720QDWVRQ1 | SOIC | DWV | 8 | 1000 | 330.0 | 16.4 | 12.15 | 6.2 | 3.05 | 16.0 | 16.0 | Q1 |
| ISO6721BQDRQ1 | SOIC | D | 8 | 3000 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| ISO6721BQDRQ1 | SOIC | D | 8 | 3000 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| ISO6721FBQDRQ1 | SOIC | D | 8 | 3000 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| ISO6721FBQDRQ1 | SOIC | D | 8 | 3000 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| ISO6721FQDWVRQ1 | SOIC | DWV | 8 | 1000 | 330.0 | 16.4 | 12.15 | 6.2 | 3.05 | 16.0 | 16.0 | Q1 |
| ISO6721QDWVRQ1 | SOIC | DWV | 8 | 1000 | 330.0 | 16.4 | 12.15 | 6.2 | 3.05 | 16.0 | 16.0 | Q1 |
| ISO6721RBQDRQ1 | SOIC | D | 8 | 3000 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |
| ISO6721RBQDRQ1 | SOIC | D | 8 | 3000 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| ISO6721RFBQDRQ1 | SOIC | D | 8 | 3000 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

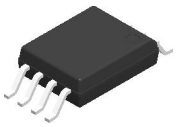
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ISO6721RFBQDRQ1 | SOIC | D | 8 | 3000 | 330.0 | 12.4 | 6.5 | 5.4 | 2.0 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

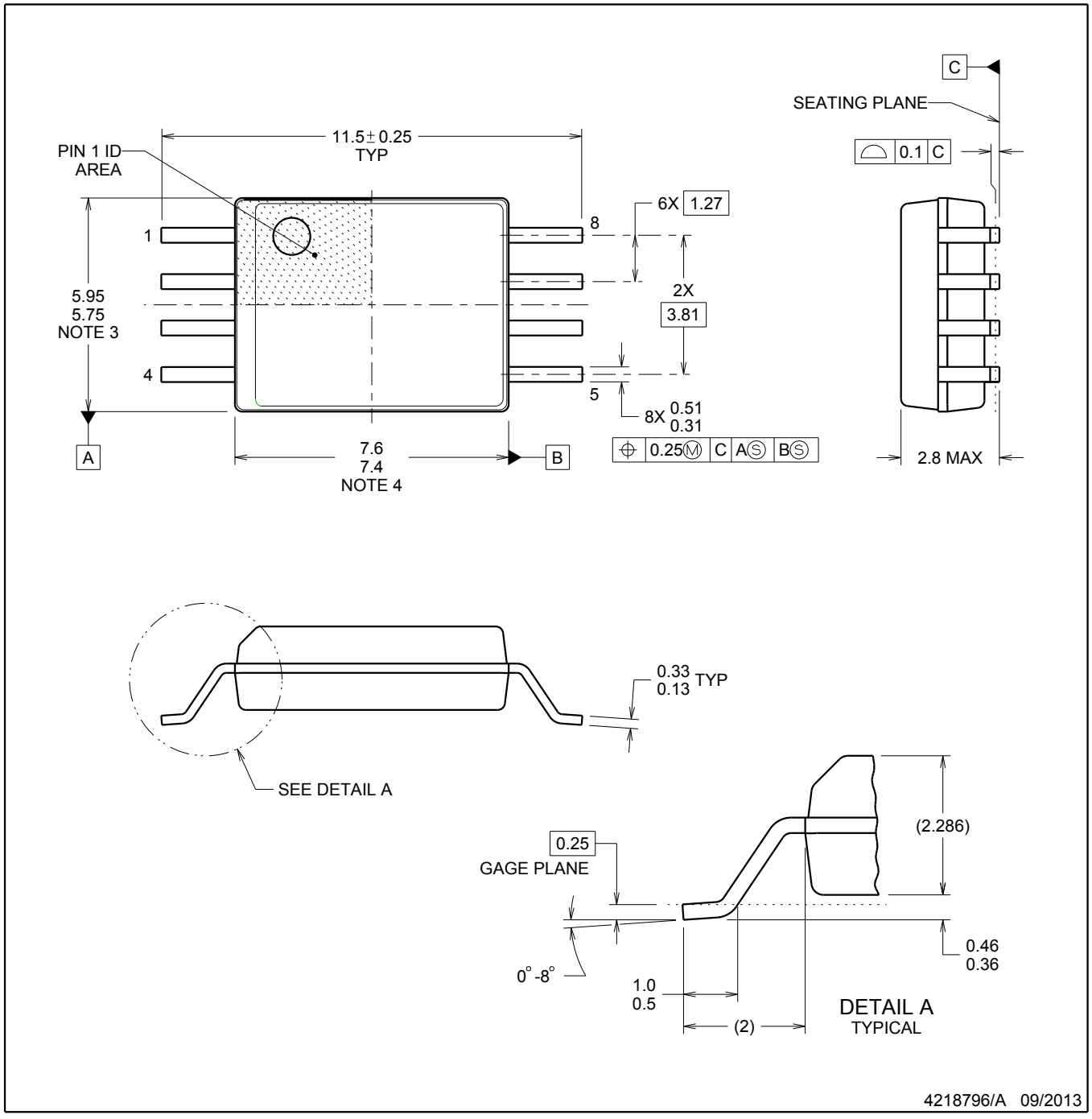
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| ISO6720BQDRQ1 | SOIC | D | 8 | 3000 | 356.0 | 356.0 | 36.0 |
| ISO6720BQDRQ1 | SOIC | D | 8 | 3000 | 353.0 | 353.0 | 32.0 |
| ISO6720FBQDRQ1 | SOIC | D | 8 | 3000 | 356.0 | 356.0 | 36.0 |
| ISO6720FBQDRQ1 | SOIC | D | 8 | 3000 | 353.0 | 353.0 | 32.0 |
| ISO6720FQDWVRQ1 | SOIC | DWV | 8 | 1000 | 350.0 | 350.0 | 43.0 |
| ISO6720FQDWVRQ1 | SOIC | DWV | 8 | 1000 | 353.0 | 353.0 | 32.0 |
| ISO6720QDWVRQ1 | SOIC | DWV | 8 | 1000 | 353.0 | 353.0 | 32.0 |
| ISO6721BQDRQ1 | SOIC | D | 8 | 3000 | 353.0 | 353.0 | 32.0 |
| ISO6721BQDRQ1 | SOIC | D | 8 | 3000 | 356.0 | 356.0 | 36.0 |
| ISO6721FBQDRQ1 | SOIC | D | 8 | 3000 | 356.0 | 356.0 | 36.0 |
| ISO6721FBQDRQ1 | SOIC | D | 8 | 3000 | 353.0 | 353.0 | 32.0 |
| ISO6721FQDWVRQ1 | SOIC | DWV | 8 | 1000 | 353.0 | 353.0 | 32.0 |
| ISO6721QDWVRQ1 | SOIC | DWV | 8 | 1000 | 353.0 | 353.0 | 32.0 |
| ISO6721RBQDRQ1 | SOIC | D | 8 | 3000 | 356.0 | 356.0 | 36.0 |
| ISO6721RBQDRQ1 | SOIC | D | 8 | 3000 | 353.0 | 353.0 | 32.0 |
| ISO6721RFBQDRQ1 | SOIC | D | 8 | 3000 | 353.0 | 353.0 | 32.0 |
| ISO6721RFBQDRQ1 | SOIC | D | 8 | 3000 | 356.0 | 356.0 | 36.0 |



# DWV0008A

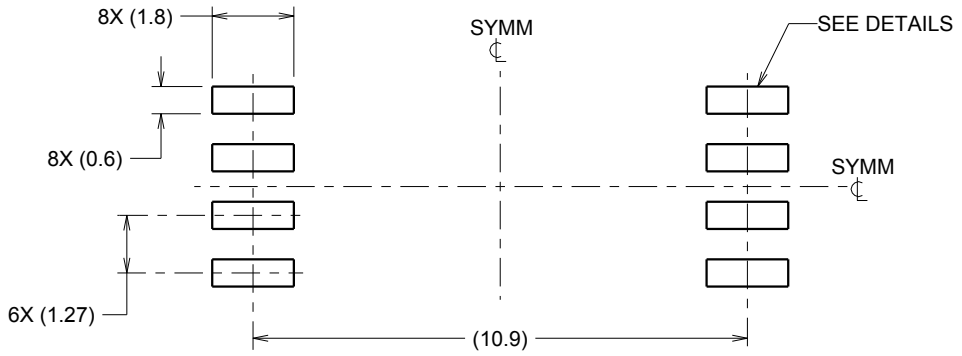
## SOIC - 2.8 mm max height

SOIC

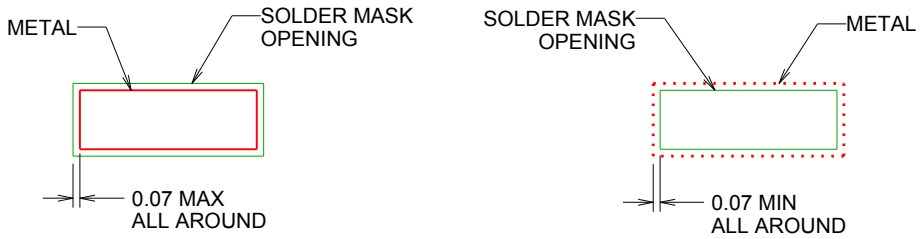



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.




LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X




SOLDER MASK DETAILS

4218796/A 09/2013

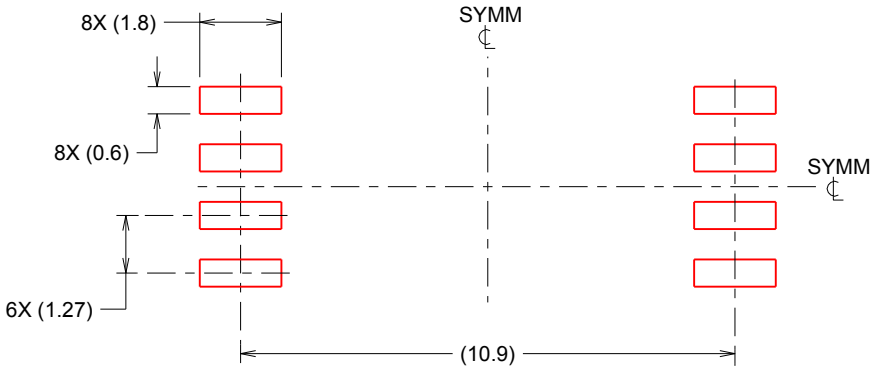
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DWV0008A

SOIC - 2.8 mm max height

SOIC

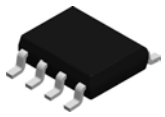



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

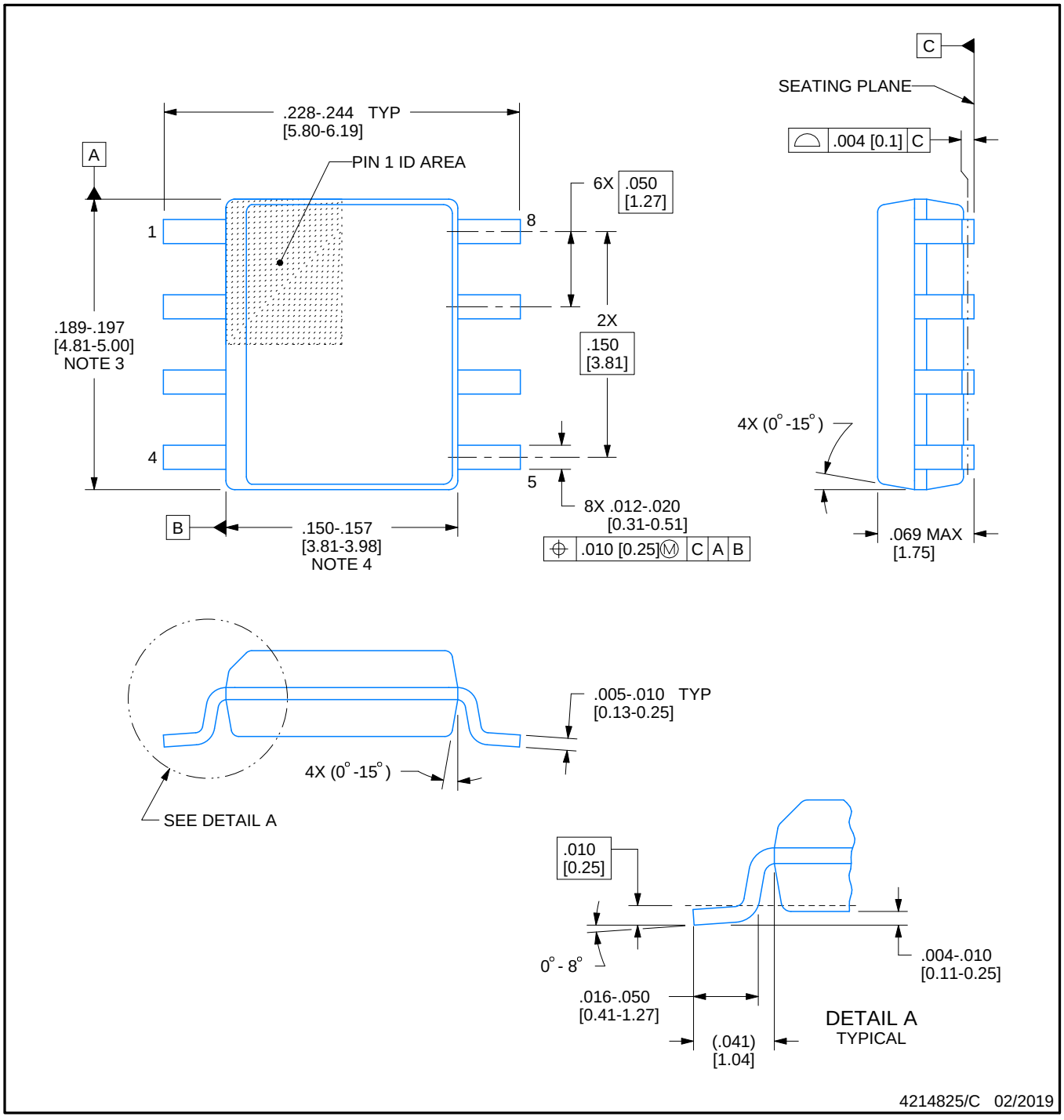


# PACKAGE OUTLINE

## D0008A

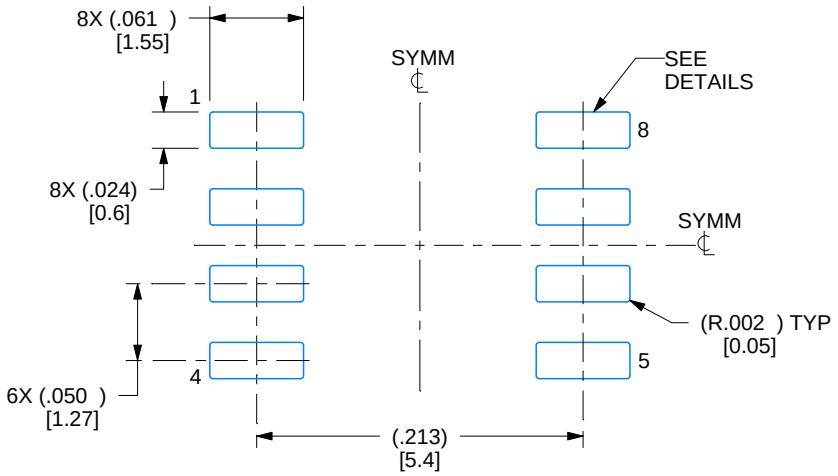
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

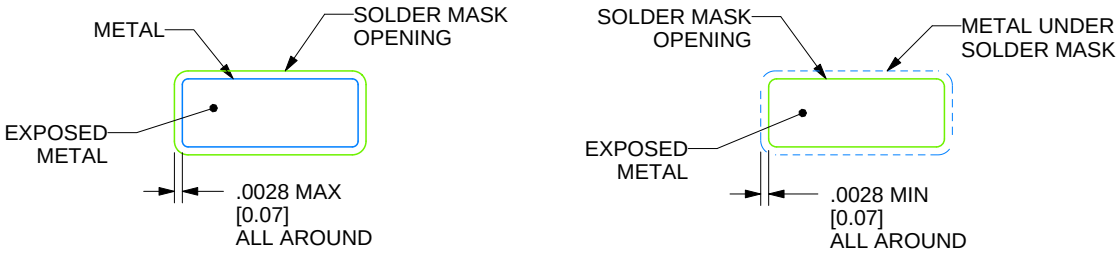



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

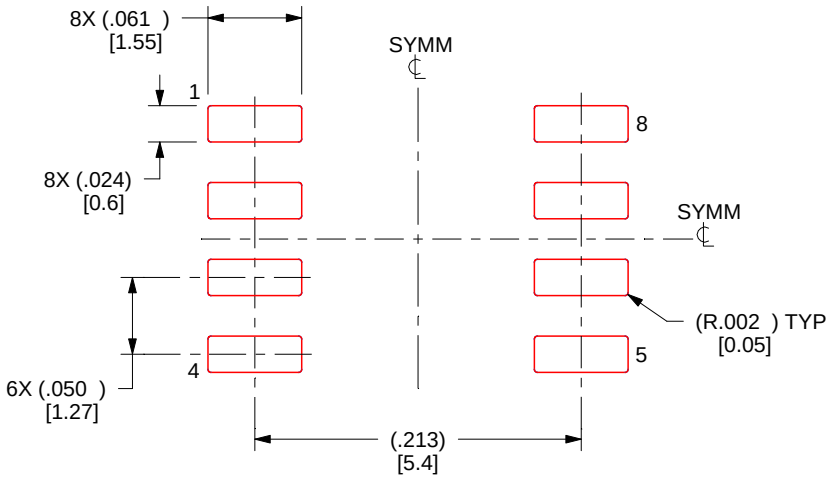
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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