ISO7840x High-Performance, 8000V_{PK} Reinforced Quad-Channel Digital Isolator

1 Features

- Signaling Rate: Up to 100Mbps
- Wide Supply Range: 2.25V to 5.5V
- 2.25V to 5.5V Level Translation
- Wide Temperature Range: –55°C to 125°C
- Low-Power Consumption, Typical 1.7mA per Channel at 1Mbps
- Low Propagation Delay: 11ns Typical (5V Supplies)
- Industry leading CMTI (Min): ±100kV/µs
- Robust Electromagnetic Compatibility (EMC)
- System-Level ESD, EFT, and Surge Immunity
- Low Emissions
- Isolation Barrier Life: >40 Years
- Wide Body SOIC-16 Package and Extra-Wide Body SOIC-16 Package Options
- Safety and Regulatory Approvals:
  - 8000V_{PK} Reinforced Isolation per DIN EN IEC 60747-17 (VDE 0884-17)
  - 5.7kV_{RMS} Isolation for 1 Minute per UL 1577
  - IEC 61010-1, IEC 62368-1, IEC 60601-1, and GB 4943.1 certifications

2 Applications

- Industrial Automation
- Motor Control
- Power Supplies
- Solar Inverters
- Medical Equipment
- Hybrid Electric Vehicles

3 Description

The ISO7840x device is a high-performance, quad-channel digital isolator with a 8000V_{PK} isolation voltage. This device has reinforced isolation certifications according to VDE, CSA, CQC, and TUV. The isolator provides high electromagnetic immunity and low emissions at low-power consumption while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by a silicon-dioxide (SiO_2) insulation barrier.

This device comes with enable pins that can be used to put the respective outputs in high impedance for multi-controller driving applications and to reduce power consumption. The ISO7840 device has four forward and zero reverse-direction channels. If the input power or signal is lost, the default output is *high* for the ISO7840 device and *low* for the ISO7840F device. See the *Device Functional Modes* section for further details.

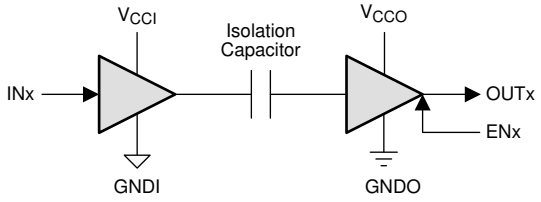
Used in conjunction with isolated power supplies, this device helps prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. Through remarkable chip design and layout techniques, electromagnetic compatibility of the ISO7840 device has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance.

The ISO7840 device is available in 16-pin SOIC wide-body (DW) and extra-wide body (DWW) packages.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE (NOM)
ISO7840 ISO7840F	DW (16, SOIC)	10.30mm × 10.30mm	10.30mm × 7.50mm
	DWW (16, SOIC)	10.30mm × 17.25mm	10.30mm × 14.0mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



V_{CCI} and GNDI are supply and ground connections respectively for the input channels.
V_{CCO} and GNDO are supply and ground connections respectively for the output channels.

Simplified Schematic

Table of Contents

4 Pin Configuration and Functions

Pin Functions

PIN		Type[1]	DESCRIPTION
NAME	NO.		
EN2	10	I	Output enable 2. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low.
GND1	2	—	Ground connection for V_{CC1}
	8		
GND2	9	—	Ground connection for V_{CC2}
	15		
INA	3	I	Input, channel A
INB	4	I	Input, channel B
INC	5	I	Input, channel C
IND	6	I	Input, channel D
NC	7	—	Not connected
OUTA	14	O	Output, channel A
OUTB	13	O	Output, channel B
OUTC	12	O	Output, channel C
OUTD	11	O	Output, channel D
V_{CC1}	1	—	Power supply, V_{CC1}
V_{CC2}	16	—	Power supply, V_{CC2}

(1) I = Input, O = Output

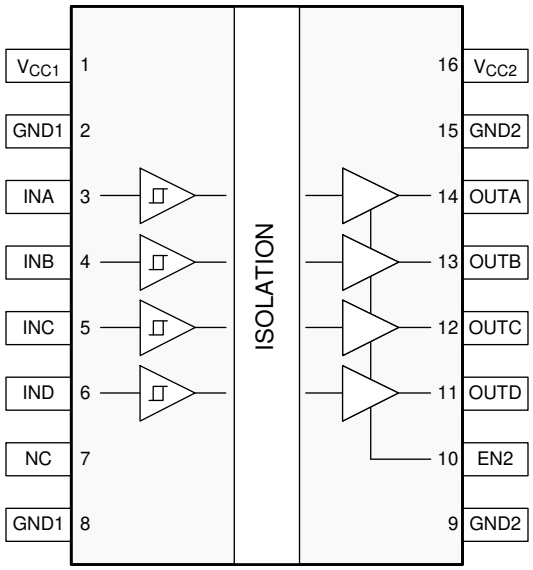


Figure 4-1. DW and DWW Packages 16-Pin SOIC Top View

5 Specifications

5.1 Absolute Maximum Ratings

See (1)

			MIN	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage(2)		–0.5	6	V
	Voltage	INx	–0.5	V_{CCX} + 0.5(3)	V
		OUTx	–0.5	V_{CCX} + 0.5(3)	
		EN2	–0.5	V_{CCX} + 0.5(3)	
I_O	Output current		–15	15	mA
	Surge immunity			12.8	kV
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 6V

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±6000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage		2.25		5.5	V
I_{OH}	High-level output current	V_{CCO} (2) = 5V	-4			mA
		V_{CCO} (2) = 3.3V	-2			
		V_{CCO} (2) = 2.5V	-1			
I_{OL}	Low-level output current	V_{CCO} (2) = 5V		4		mA
		V_{CCO} (2) = 3.3V		2		
		V_{CCO} (2) = 2.5V		1		
V_{IH}	High-level input voltage		0.7 × V_{CCI} (2)		V_{CCI} (2)	V
V_{IL}	Low-level input voltage		0		0.3 × V_{CCI} (2)	V
DR	Signaling Rate		0		100	Mbps
T_J	Junction temperature(1)		-55		150	°C
T_A	Ambient temperature		-55	25	125	°C

(1) To maintain the recommended operating conditions for T_J, see *Section 5.4*.
(2) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

5.4 Thermal Information

THERMAL METRIC[1]		ISO7840		UNIT
		DW (SOIC)	DWW (SOIC)	
		16 Pins	16 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	78.9	78.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	41.6	41.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.6	49.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	15.5	15.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	43.1	48.8	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Power Ratings

V_{CC1} = V_{CC2} = 5.5V, T_J = 150°C, C_L = 15pF, input a 50MHz 50% duty cycle square wave

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation by ISO7840x				200	mW
P_{D1}	Maximum power dissipation by side-1 of ISO7840x				40	mW
P_{D2}	Maximum power dissipation by side-2 of ISO7840x				160	mW

5.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	SPECIFICATION		UNIT
			DW	DWW	
GENERAL					
CLR	External clearance(1)	Shortest pin-to-pin distance through air	>8.15	>14.5	mm
		Shortest pin-to-pin distance through air (typical)		15.0	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	>8.15	>14.5	mm
		Shortest pin-to-pin distance across the package surface (typical)		15.0	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>21	>21	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112; UL 746A	>600	>600	V
	Material group		I	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600V_{RMS}	I–IV	I–IV	
		Rated mains voltage ≤ 1000V_{RMS}	I–III	I–IV	
DIN EN IEC 60747-17 (VDE 0884-17)(2)					
V_{IORM}	Maximum repetitive peak isolation voltage		2121	2828	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); Time dependent dielectric breakdown (TDDB) Test, see Figure 5-1 and Figure 5-2	1500	2000	V_{RMS}
		DC voltage	2121	2828	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification) $V_{TEST} = 1.2 \times V_{IOTM}$, t= 1s (100% production)	8000	8000	V_{PK}
V_{IMP}	Maximum impulse voltage (3)	Tested in air, 1.2/50µs waveform per IEC 62368-1	9800	9800	V_{PK}
V_{IOSM}	Maximum surge isolation voltage (4)	$V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	12800	12800	V_{PK}
q_{pd}	Apparent charge (5)	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IOTM} = 2545V_{PK}$ (DW) and $3394V_{PK}$ (DWW), t_m = 10s	≤5	≤5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.6 \times V_{IORM} = 3394V_{PK}$ (DW) and $4525V_{PK}$ (DWW), t_m = 10s	≤5	≤5	
		Method b: At routine test (100% production); $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s (method b1) or $V_{pd(m)} = V_{ini}$, $t_m = t_{ini}$ (method b2)	≤5	≤5	
C_{IO}	Barrier capacitance, input to output(6)	V_{IO} = 0.4 × sin (2πft), f = 1MHz	2	2	pF
R_{IO}	Isolation resistance, input to output (6)	V_{IO} = 500V, T_A = 25°C	$>10^{12}$	$>10^{12}$	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	$>10^{11}$	
		V_{IO} = 500V at T_S = 150°C	$>10^{9}$	$>10^{9}$	
	Pollution degree		2	2	
	Climatic category		55/125/21	55/125/21	
UL 1577					
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO} = 5700V_{RMS}$, t = 60s (qualification), $V_{TEST} = 1.2 \times V_{ISO} = 6840V_{RMS}$, t = 1s (100% production)	5700	5700	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal

in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.

(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

(3) Testing is carried out in air to determine the surge immunity of the package.

(4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.

(5) Apparent charge is electrical discharge caused by a partial discharge (pd).

(6) All pins on each side of the barrier tied together creating a two-terminal device.

5.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to IEC 62368-1 and IEC 60601-1	Certified according to UL 1577 Component Recognition Program	Certified according to GB 4943.1	Certified according to EN 61010-1 and EN 62368-1
Certificate number: 40040142	Master contract number: 220991	File number: E181974	Certificate number: CQC15001121716	Client ID number: 77311

5.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 78.9°C/W, V_I = 5.5V, T_J = 150°C, T_A = 25°C			288	mA
		$R_{\theta JA}$ = 78.9°C/W, V_I = 3.6V, T_J = 150°C, T_A = 25°C			440	
		$R_{\theta JA}$ = 78.9°C/W, V_I = 2.75V, T_J = 150°C, T_A = 25°C			576	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 78.9°C/W, T_J = 150°C, T_A = 25°C			1584	mW
T_S	Maximum safety temperature				150	°C

The maximum safety temperature is the maximum junction temperature specified for the device. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Section 5.4* is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

5.9 Electrical Characteristics—5V Supply

V_{CC1} = V_{CC2} = 5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4mA; see Figure 6-1	V_{CCO} (1) – 0.4	V_{CCO} (1) – 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 4mA; see Figure 6-1		0.2	0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 × V_{CCI} (1)			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx or EN2			10	µA
I_{IL}	Low-level input current	V_{IL} = 0V at INx or EN2	–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI} (1) or 0V, V_{CM} = 1500V; see Figure 6-4	100			kV/µs
C_I	Input capacitance	V_I = V_{CC}/2 + 0.4 × sin (2πft), f = 1MHz, V_{CC} = 5V		2		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

5.10 Supply Characteristics—5V Supply

V_{CC1} = V_{CC2} = 5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS			SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current	Disable	EN2 = 0V, V_I = 0V (ISO7840F), V_I = V_{CCI} (1) (ISO7840)		I_{CC1}		1.3	2	mA
				I_{CC2}		0.4	0.6	
		EN2 = 0V, V_I = V_{CCI} (1) (ISO7840F), V_I = 0V (ISO7840) EN2 = 0V		I_{CC1}		6	8.5	mA
				I_{CC2}		0.4	0.6	
	DC signal	V_I = 0V (ISO7840F), V_I = V_{CCI} (1) (ISO7840)		I_{CC1}		1.3	2	mA
				I_{CC2}		2.2	3.1	
		V_I = V_{CCI} (1) (ISO7840F), V_I = 0V (ISO7840)		I_{CC1}		5.9	8.6	mA
				I_{CC2}		2.5	3.3	
	All channels switching with square wave clock input; C_L = 15pF	1Mbps		I_{CC1}		3.6	5.3	mA
				I_{CC2}		2.6	3.7	
		10Mbps		I_{CC1}		3.8	5.4	mA
				I_{CC2}		4.5	5.9	
		100Mbps	DW package	I_{CC1}		5.1	5.9	mA
				I_{CC2}		23.8	27.4	
			DWW package	I_{CC1}		5.1	5.9	mA
				I_{CC2}		23.8	28.5	

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

5.11 Electrical Characteristics—3.3V Supply

V_{CC1} = V_{CC2} = 3.3V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2mA; see Figure 6-1	V_{CCO} (1) – 0.4	V_{CCO} (1) – 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 2mA; see Figure 6-1		0.2	0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 × V_{CCI} (1)			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx or EN2			10	µA
I_{IL}	Low-level input current	V_{IL} = 0V at INx or EN2	–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI} (1) or 0V, V_{CM} = 1500V; see Figure 6-4	100			kV/µs

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

5.12 Supply Current Characteristics—3.3V Supply

V_{CC1} = V_{CC2} = 3.3V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current	Disable	EN2 = 0V, V_I = 0V (ISO7840F), V_I = V_{CCI} (1) (ISO7840)	I_{CC1}		1.3	2	mA
			I_{CC2}		0.4	0.6	
		EN2 = 0V, V_I = V_{CCI} (1) (ISO7840F), V_I = 0V (ISO7840)	I_{CC1}		6	8.5	mA
			I_{CC2}		0.4	0.6	
	DC signal	V_I = 0V (ISO7840F), V_I = V_{CCI} (1) (ISO7840)	I_{CC1}		1.3	2	mA
			I_{CC2}		2.2	3	
		V_I = V_{CCI} (1) (ISO7840F), V_I = 0V (ISO7840)	I_{CC1}		5.9	8.6	mA
			I_{CC2}		2.4	3.3	
	All channels switching with square wave clock input; C_L = 15pF	1Mbps	I_{CC1}		3.6	5.3	mA
			I_{CC2}		2.5	3.6	
		10Mbps	I_{CC1}		3.7	5.3	mA
			I_{CC2}		3.9	5.1	
		100Mbps	I_{CC1}		4.5	5.8	mA
			I_{CC2}		17.7	20.6	

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

5.13 Electrical Characteristics—2.5V Supply

V_{CC1} = V_{CC2} = 2.5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1mA; see Figure 6-1	V_{CCO} (1) – 0.4	V_{CCO} (1) – 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 1mA; see Figure 6-1		0.2	0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 × V_{CCI} (1)			V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx or EN2			10	µA
I_{IL}	Low-level input current	V_{IL} = 0V at INx or EN2	–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI} (1) or 0V, V_{CM} = 1500V; see Figure 6-4	100			kV/µs

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

5.14 Supply Current Characteristics—2.5V Supply

V_{CC1} = V_{CC2} = 2.5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current	Disable	EN2 = 0V, V_I = 0V (Devices with suffix F), V_I = V_{CCI} (1) (Devices without suffix F)	I_{CC1}		1.3	2	mA
			I_{CC2}		0.4	0.6	
		EN2 = 0V, V_I = V_{CCI} (1) (Devices with suffix F), V_I = 0V (Devices without suffix F)	I_{CC1}		6	8.5	mA
			I_{CC2}		0.4	0.6	
	DC signal	V_I = 0V (Devices with suffix F), V_I = V_{CCI} (1) (Devices without suffix F)	I_{CC1}		1.3	2	mA
			I_{CC2}		2.2	3	
		V_I = V_{CCI} (1) (Devices with suffix F), V_I = 0V (Devices without suffix F)	I_{CC1}		5.9	8.6	mA
			I_{CC2}		2.4	3.3	
	All channels switching with square wave clock input; C_L = 15pF	1Mbps	I_{CC1}		3.6	5.3	mA
			I_{CC2}		2.5	3.5	
		10Mbps	I_{CC1}		3.7	5.3	mA
			I_{CC2}		3.5	4.7	
		100Mbps	I_{CC1}		4.4	5.7	mA
			I_{CC2}		13.9	16.4	

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

5.15 Switching Characteristics—5V Supply

V_{CC1} = V_{CC2} = 5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 6-1	6	11	16	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.55	4.1	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			2.5	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				4.5	ns
t_r	Output signal rise time	See Figure 6-1		1.7	3.9	ns
t_f	Output signal fall time			1.9	3.9	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Figure 6-2		12	20	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			12	20	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO7840			10	20	ns
	Enable propagation delay, high impedance-to-high output for ISO7840F			2	2.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO7840			2	2.5	µs
	Enable propagation delay, high impedance-to-low output for ISO7840F			10	20	ns
t_{fs}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7V. See Figure 6-3		0.2	9	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100Mbps		0.90		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

5.16 Switching Characteristics—3.3V Supply

V_{CC1} = V_{CC2} = 3.3V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 6-1	6	10.8	16	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.7	4.2	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			2.2	ns
$t_{sk(pp)}$	Part-to-part skew time				4.5	ns
t_r	Output signal rise time	See Figure 6-1		0.8	3	ns
t_f	Output signal fall time			0.8	3	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Figure 6-2		17	32	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			17	32	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO7840			17	32	ns
	Enable propagation delay, high impedance-to-high output for ISO7840F			2	2.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO7840			2	2.5	µs
	Enable propagation delay, high impedance-to-low output for ISO7840F			17	32	ns
t_{fs}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7V. See Figure 6-3		0.2	9	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100Mbps		0.91		ns

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

5.17 Switching Characteristics—2.5V Supply

V_{CC1} = V_{CC2} = 2.5V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 6-1	7.5	11.7	17.5	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.66	4.2	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction Channels			2.2	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				4.5	ns
t_r	Output signal rise time	See Figure 6-1		1	3.5	ns
t_f	Output signal fall time			1.2	3.5	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Figure 6-2		22	45	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			22	45	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO7840			18	45	ns
	Enable propagation delay, high impedance-to-high output for ISO7840F			2	2.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO7840			2	2.5	µs
	Enable propagation delay, high impedance-to-low output for ISO7840F			18	45	ns
t_{fs}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7V. See Figure 6-3		0.2	9	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100Mbps		0.91		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

5.18 Insulation Characteristics Curves

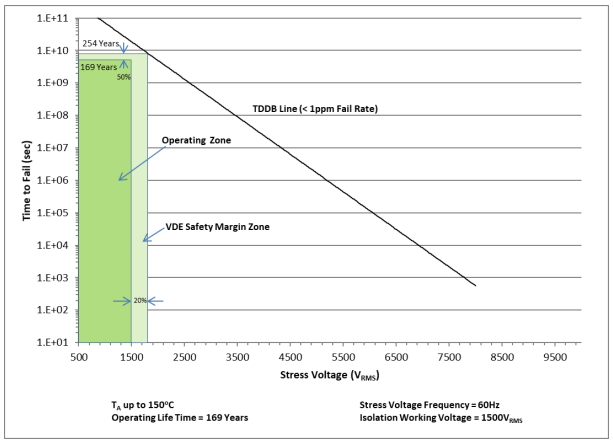


Figure 5-1. Reinforced Isolation Capacitor Life Time Projection for Devices in DW Package

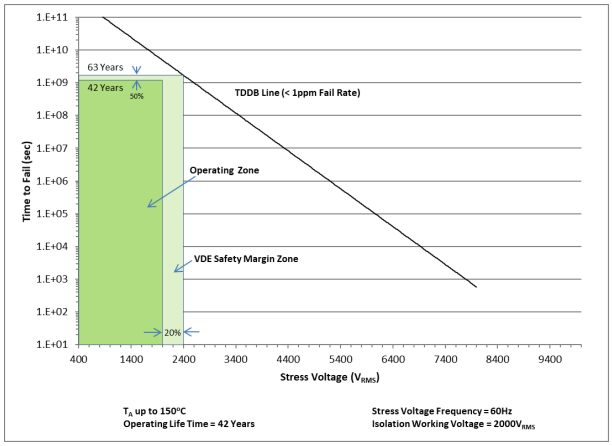


Figure 5-2. Reinforced Isolation Capacitor Life Time Projection for Devices in DWW Package

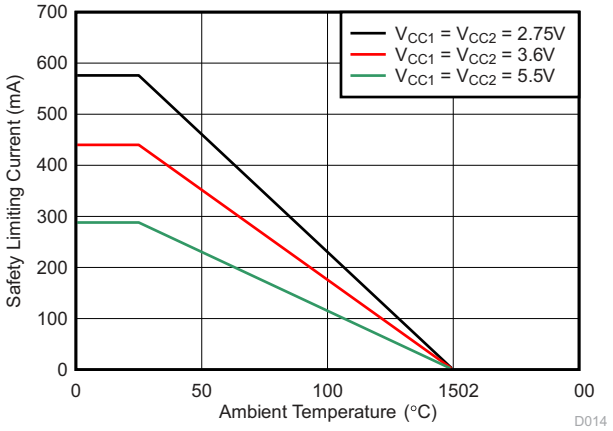


Figure 5-3. Thermal Derating Curve for Limiting Current per VDE

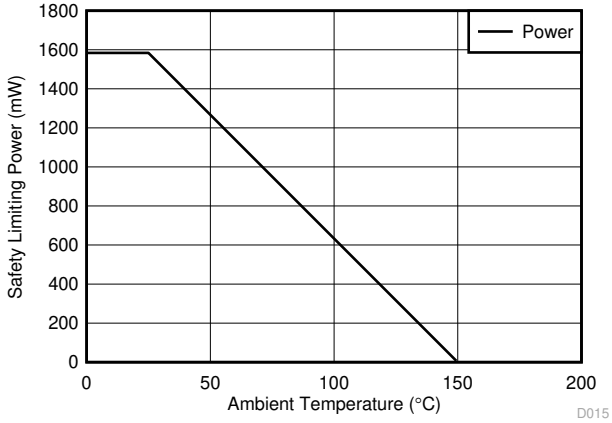
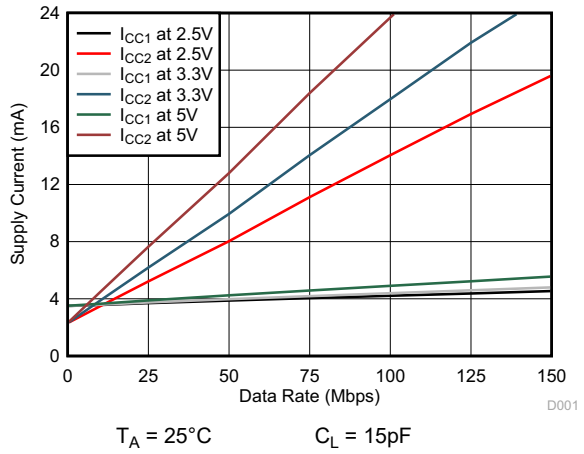


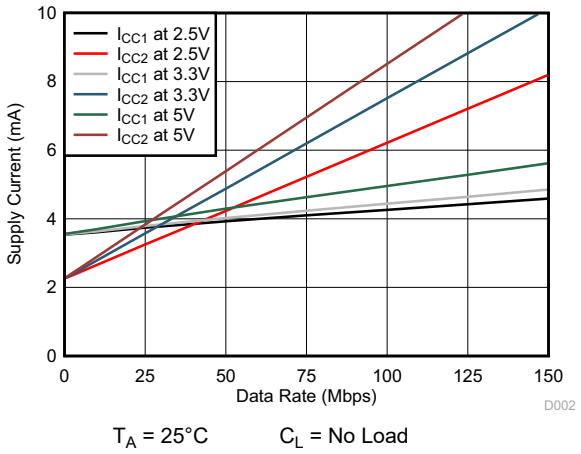
Figure 5-4. Thermal Derating Curve for Limiting Power per VDE

5.19 Typical Characteristics



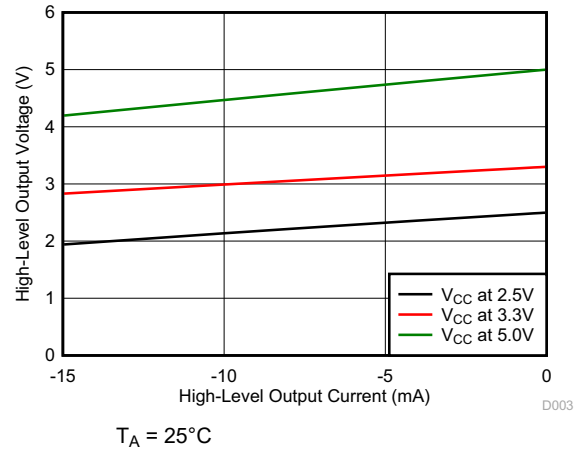
T_A = 25°C C_L = 15pF

Figure 5-5. Supply Current vs Data Rate (With 15pF Load)



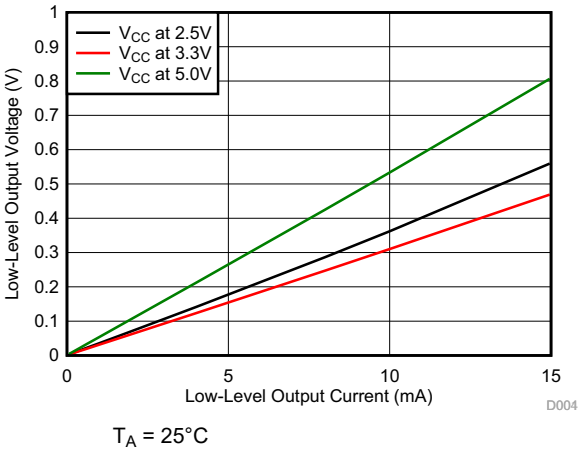
T_A = 25°C C_L = No Load

Figure 5-6. Supply Current vs Data Rate (With No Load)



T_A = 25°C

Figure 5-7. High-Level Output Voltage vs High-level Output Current



T_A = 25°C

Figure 5-8. Low-Level Output Voltage vs Low-Level Output Current

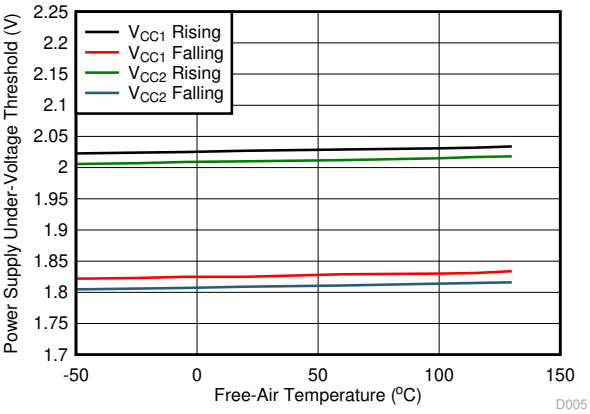


Figure 5-9. Power Supply Undervoltage Threshold vs Free-Air Temperature

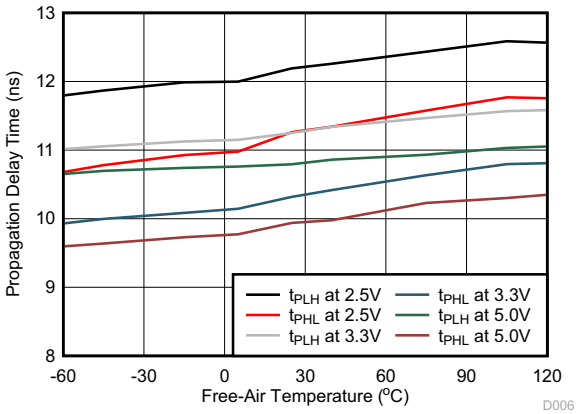
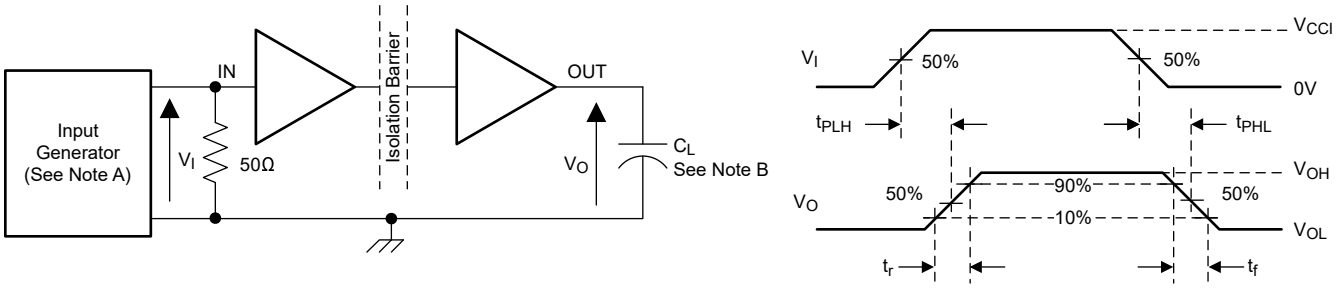


Figure 5-10. Propagation Delay Time vs Free-Air Temperature

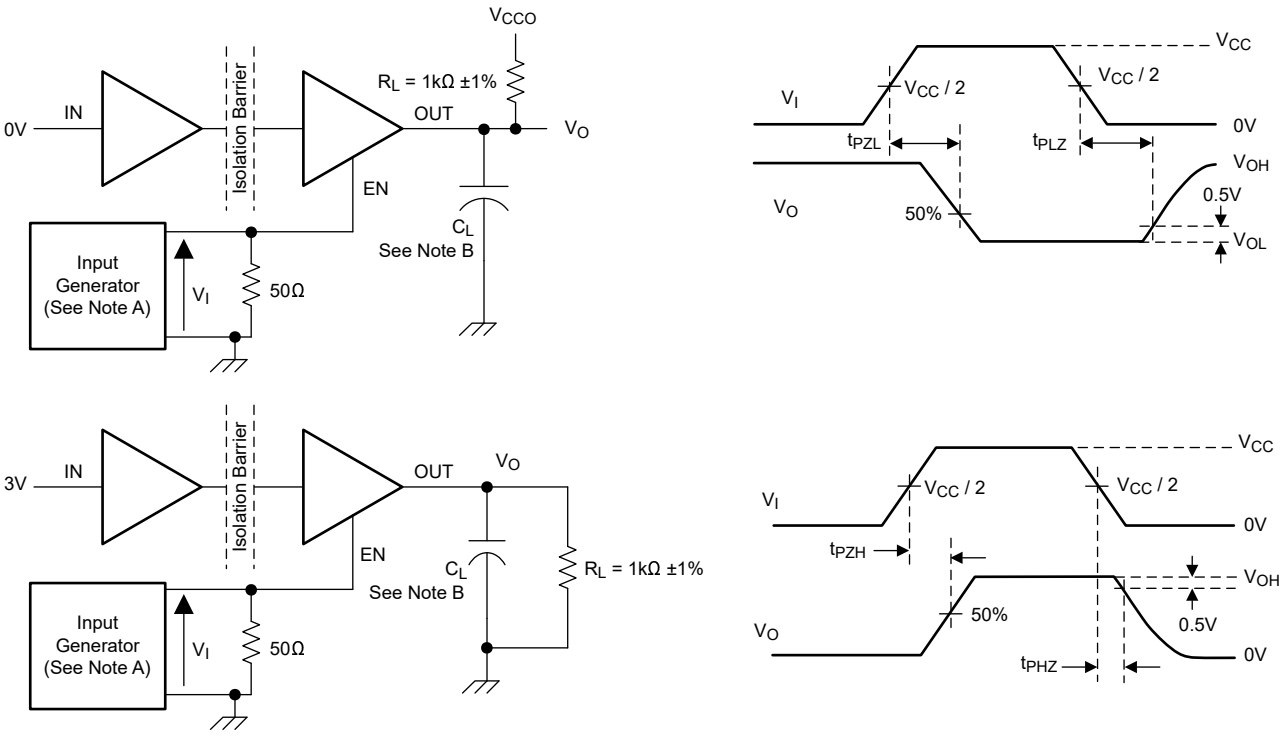
6 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50kHz, 50% duty cycle, t_r ≤ 3ns, t_f ≤ 3ns, Z_O = 50Ω. At the input, a 50Ω resistor is required to terminate Input Generator signal. The 50Ω resistor is not needed in actual application.

B. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

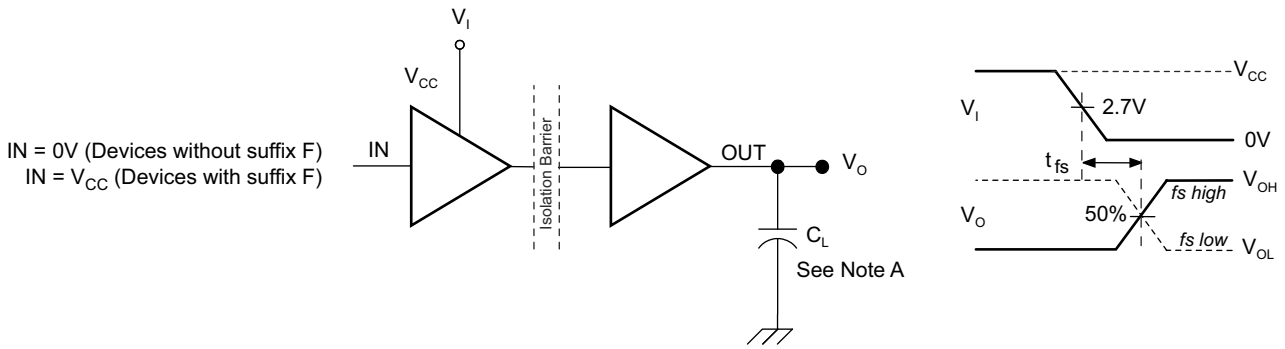
Figure 6-1. Switching Characteristics Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 10kHz, 50% duty cycle, t_r ≤ 3ns, t_f ≤ 3ns, Z_O = 5Ω.

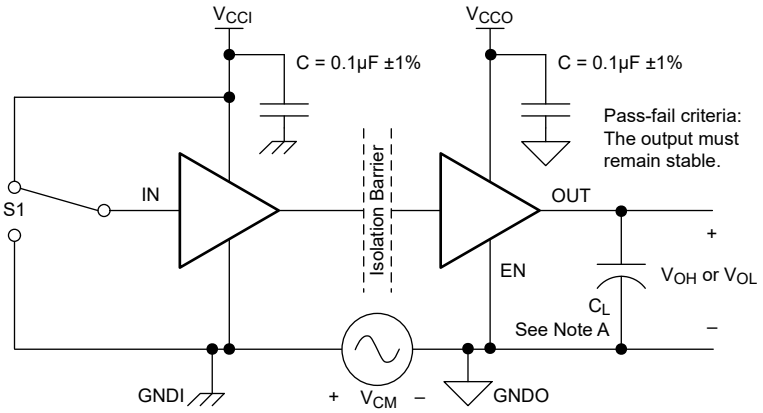
B. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

Figure 6-2. Enable/Disable Propagation Delay Time Test Circuit and Waveform



A. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

Figure 6-3. Default Output Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15pF and includes instrumentation and fixture capacitance within ±20%.

Figure 6-4. Common-Mode Transient Immunity Test Circuit

7 Detailed Description

7.1 Overview

The ISO7840 device uses an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon-dioxide based isolation barrier. The transmitter sends a high-frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. If the EN pin is low then the output goes to high impedance. The ISO7840 device also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions because of the high-frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, Figure 7-1, shows a functional block diagram of a typical channel.

7.2 Functional Block Diagram

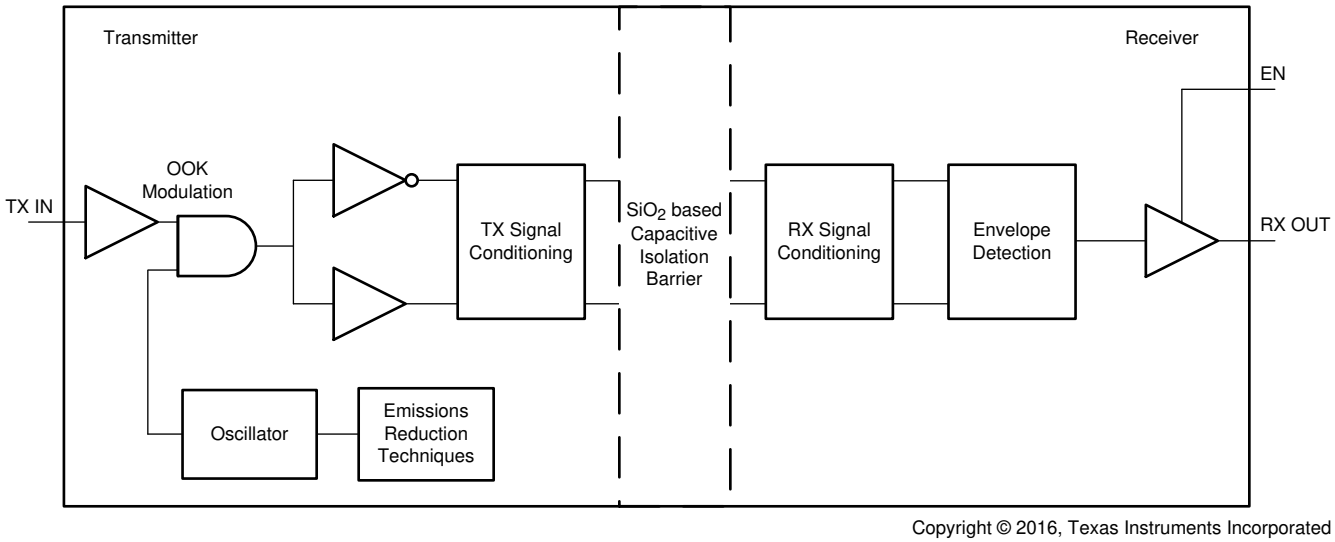


Figure 7-1. Conceptual Block Diagram of a Digital Capacitive Isolator

Figure 7-2 shows a conceptual detail of how the ON-OFF keying scheme works.

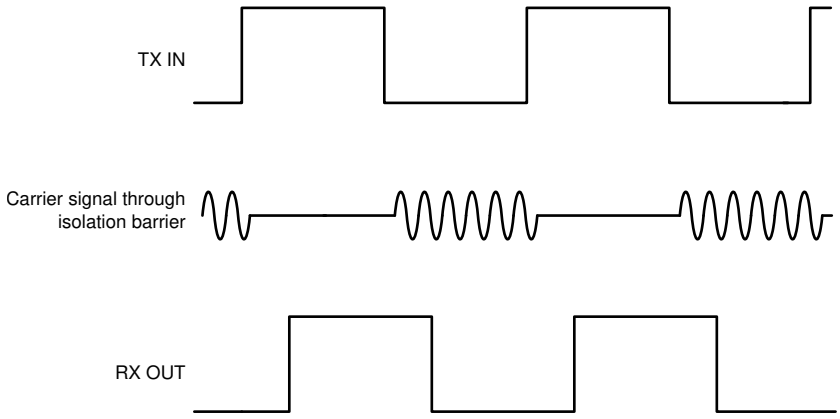


Figure 7-2. On-Off Keying (OOK) Based Modulation Scheme

7.3 Feature Description

Table 7-1 lists the device features.

Table 7-1. Device Features

PART NUMBER	CHANNEL DIRECTION	RATED ISOLATION	MAXIMUM DATA RATE	DEFAULT OUTPUT
ISO7840	4 Forward, 0 Reverse	5700V_{RMS} / 8000V_{PK} (1)	100Mbps	High
ISO7840F	4 Forward, 0 Reverse	5700V_{RMS} / 8000V_{PK} (1)	100Mbps	Low

(1) See *Insulation Specifications* for detailed isolation ratings.

7.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge, and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO7840 device incorporates many chip-level design improvements for overall system robustness. Some of these improvements include

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by providing purely differential internal operation.

7.4 Device Functional Modes

Table 7-2 lists the ISO7840 functional modes.

Table 7-2. Function Table

V_{CCI}	V_{CCO}	INPUT (INx)(2)	OUTPUT ENABLE (EN2)	OUTPUT (OUTx)	COMMENTS
PU	PU	H	H or open	H	Normal Operation: A channel output assumes the logic state of the input.
		L	H or open	L	
		Open	H or open	Default	Default mode: When INx is open, the corresponding channel output goes to the default logic state. Default= High for ISO7840 and Low for ISO7840F.
X	PU	X	L	Z	A low value of Output Enable causes the outputs to be high-impedance
PD	PU	X	H or open	Default	Default mode: When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. Default= High for IISO7840 and Low for ISO7840F. When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	X	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined (1). When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of the input

(1) The outputs are undetermined when 1.7V < V_{CCI}, V_{CCO} < 2.25V.
(2) A strongly driven input signal can weakly power the floating V_{CC} through an internal protection diode and cause undetermined output.

7.4.1 Device I/O Schematics

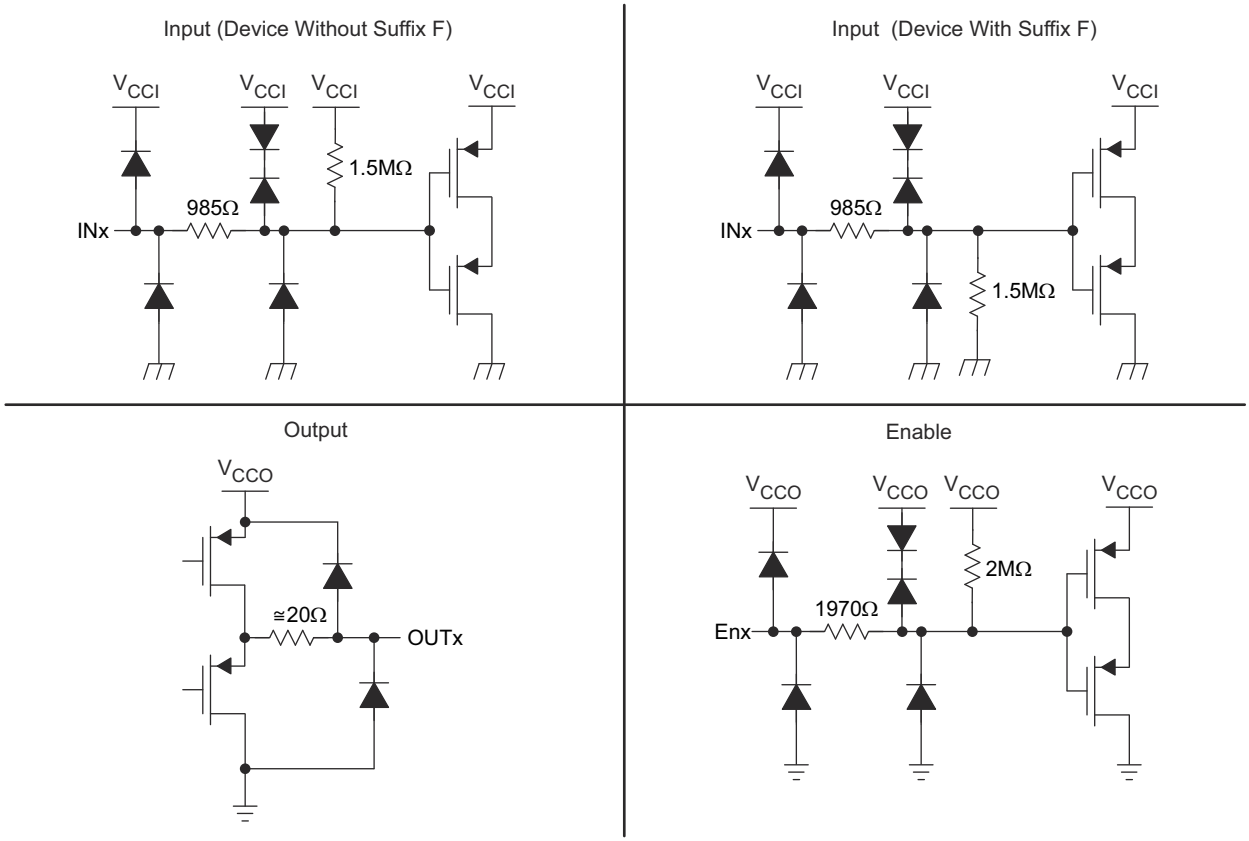


Figure 7-3. Device I/O Schematics

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The ISO7840 device is a high-performance, quad-channel digital isolator with a 5.7kV$_{RMS}$ isolation voltage . The device comes with enable pins on each side that can be used to put the respective outputs in high impedance for multi-controller driving applications and reduce power consumption. The ISO7840 device uses single-ended CMOS-logic switching technology. The supply voltage range is from 2.25V to 5.5V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

8.2 Typical Application

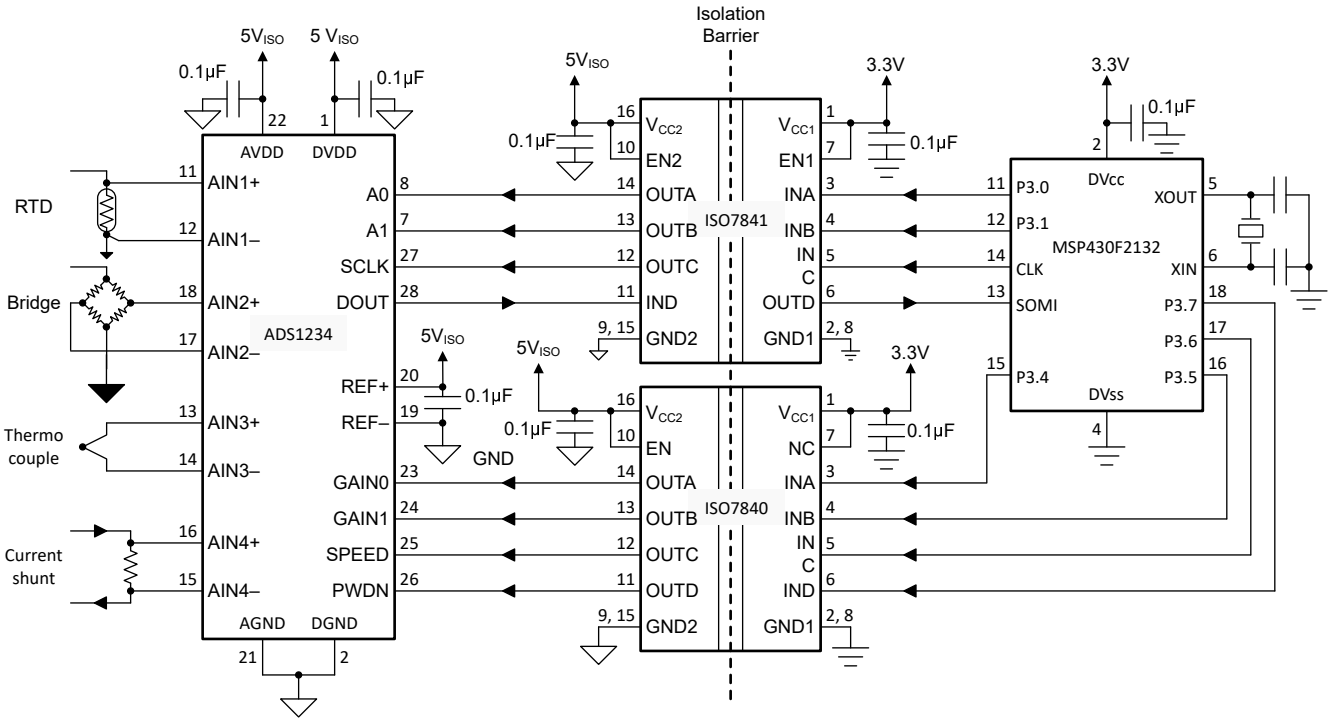


Figure 8-1. Isolated Data Acquisition System for Process Control

8.2.1 Design Requirements

For this design example, use the parameters shown in Table 8-1.

Table 8-1. Design Parameters

PARAMETER	VALUE
Supply voltage	2.25V to 5.5V
Decoupling capacitor between V_{CC1} and GND1	0.1µF
Decoupling capacitor from V_{CC2} and GND2	0.1µF

8.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO7840 device only requires two external bypass capacitors to operate.

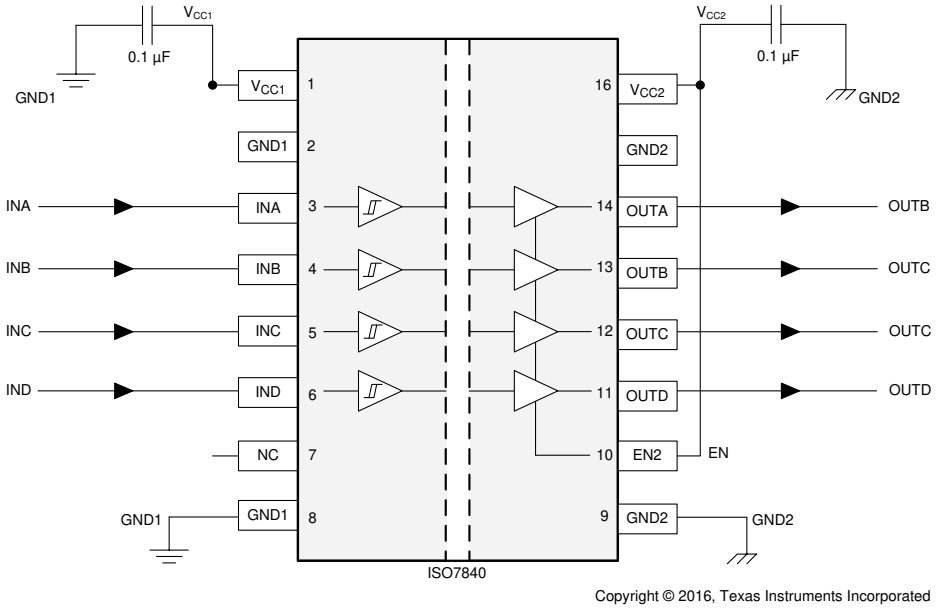


Figure 8-2. Typical ISO7840 Circuit Hook-Up

8.2.3 Application Curve

The typical eye diagram of the ISO7840 device indicates low jitter and wide open eye at the maximum data rate of 100Mbps.

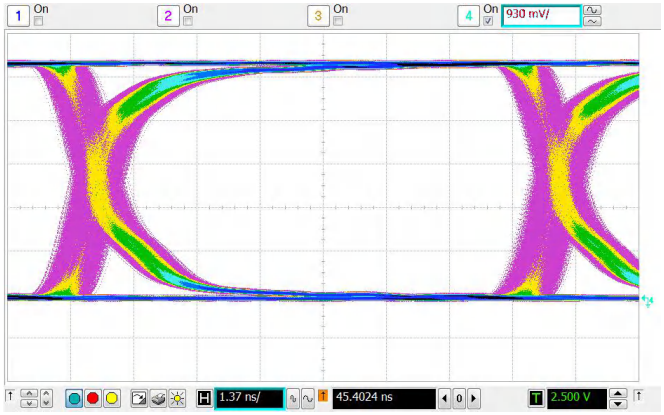


Figure 8-3. Eye Diagram at 100Mbps PRBS, 5V and 25°C

8.3 Power Supply Recommendations

To help provide reliable operation at data rates and supply voltages, a 0.1µF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors must be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments SN6501. For such applications, detailed power supply design and transformer selection recommendations are available in SN6501 Transformer Driver for Isolated Power Supplies.

8.4 Layout

8.4.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 8-4). Layer stacking must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of the inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100pF/inch^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links typically have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep the planes symmetrical. This makes the stack mechanically stable and prevents warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to *Digital Isolator Design Guide*.

8.4.1.1 PCB Material

For digital circuit boards operating at less than 150Mbps, (or rise and fall times greater than 1ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

8.4.2 Layout Example

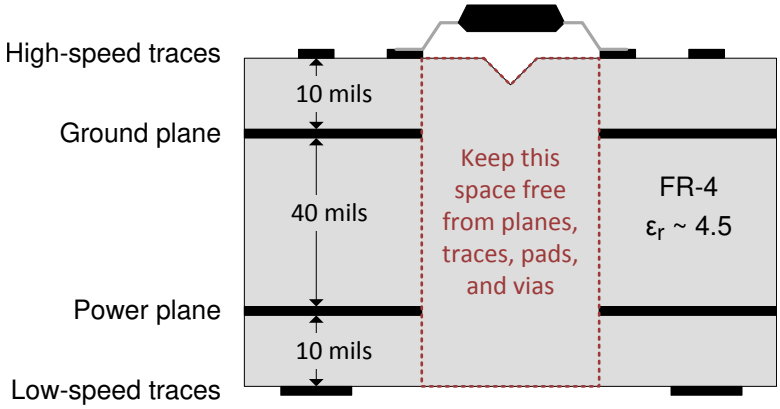


Figure 8-4. Layout Example Schematic

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *DS123x 2- and 4-Channel, 24-Bit, Delta-Sigma ADCs for Bridge Sensors*, data sheet
- Texas Instruments, *Digital Isolator Design Guide*, application note
- Texas Instruments, *Isolation Glossary*, application note
- Texas Instruments, *MSP430G2x32, MSP430G2x02 Mixed Signal Microcontrollers*, data sheet
- Texas Instruments, *Transformer Driver for Isolated Power Supplies*, data sheet

9.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 9-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ISO7840	Click here	Click here	Click here	Click here	Click here
ISO7840F	Click here	Click here	Click here	Click here	Click here

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2016) to Revision C (July 2025)	Page
• Added 15mm typical specification for CLR/CPG in *Insulation Specification*	6

- Added the *Receiving Notification of Documentation Updates* section....24

Changes from Revision A (March 2016) to Revision B (April 2016) **Page**

- Added *Features* 2.25V to 5.5V Level Translation....1
- Changed the number of years for the isolation barrier life in the *Features* section 1
- VDE certification is now complete 1
- Changed the input-to-output test voltage parameter to apparent charge in the *Insulation Specifications* 6
- Changed V_{CCO} to V_{CCI} for the minimum value of the input threshold voltage hysteresis parameter in all electrical characteristics tables....8
- Added V_{CM} to the test condition of the common-mode transient immunity parameter in all electrical characteristics tables....8
- Added the lifetime projection graphs for DW and DWW packages to the *Safety Limiting Values* section 14

Changes from Revision * (July 2015) to Revision A (February 2016) **Page**

- Changed *Features* From: Industry leading CMTI To: Industry leading CMTI (MIN) 1
- Changed the Safety and Regulatory Approvals list of *Features* 1
- Added *Features* "TUV Certification per EN 61010-1 and EN 60950-1"....1
- Changed text in the first paragraph of the *Description* From: "certifications according to VDE, CSA, and CQC". To: "certifications according to VDE, CSA, CQC, and TUV." 1
- Added the DWW package to the *Section 5.4* 5
- Changed *Package Insulation and Safety-Related Specifications*, added the 16-DWW Package information....6
- Added the DWW package information, added "Climatic category", and deleted Note 1 in *Insulation Characteristics* 6
- Added Note 1 to *Insulation Characteristics* 6
- Changed *IEC 60664-1 Ratings Table* 6
- Added the TUV and DWW package information to the *Regulatory Information* section and Regulatory Information. Deleted Note 1 in Regulatory Information....7
- Changed the Supply Current section of *Supply Characteristics—5V Supply* 8
- Changed the Supply Current section of *Supply Current Characteristics—3.3V Supply* 9
- Changed the Supply Current section of*Supply Current Characteristics—2.5V Supply* 10
- Changed Device I/O Schematics 20

11 Mechanical, Packaging, and Orderable Information

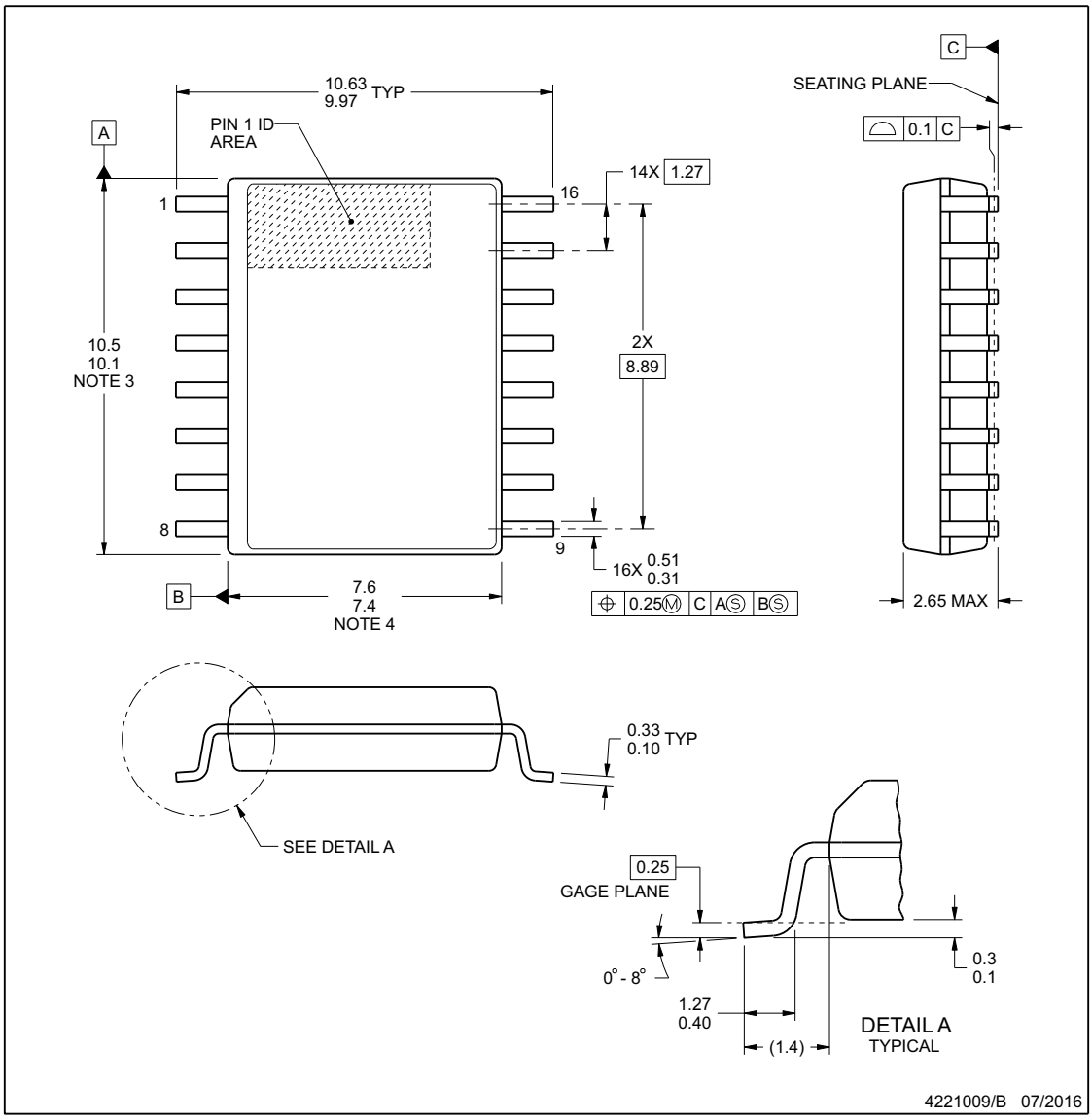
The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES:

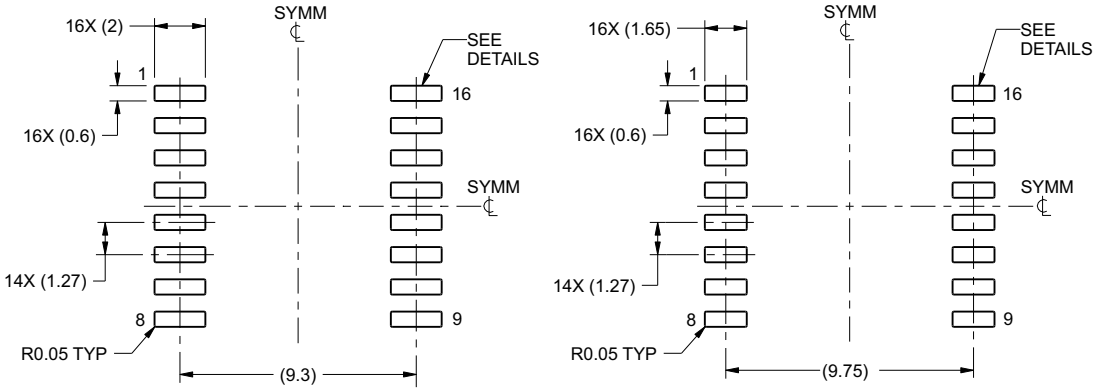
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

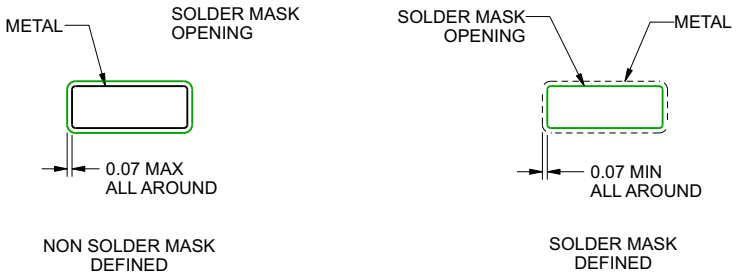
DW0016B

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:4X



SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

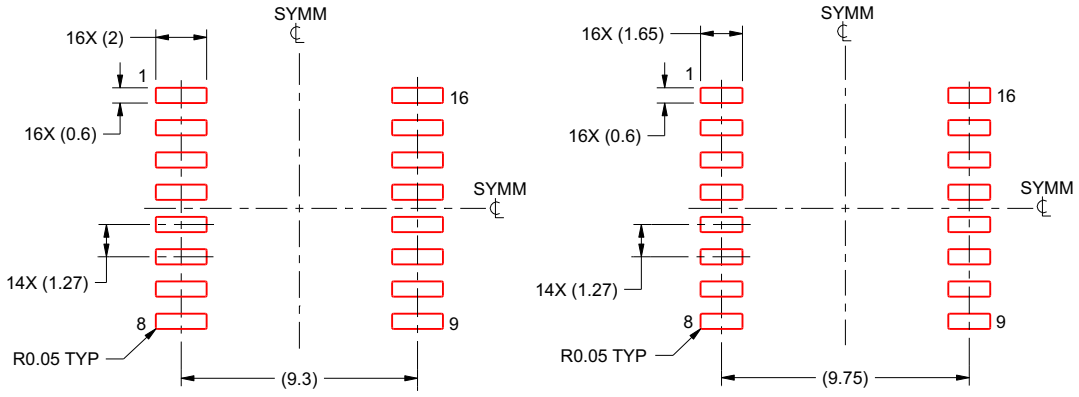
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

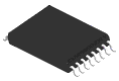
4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

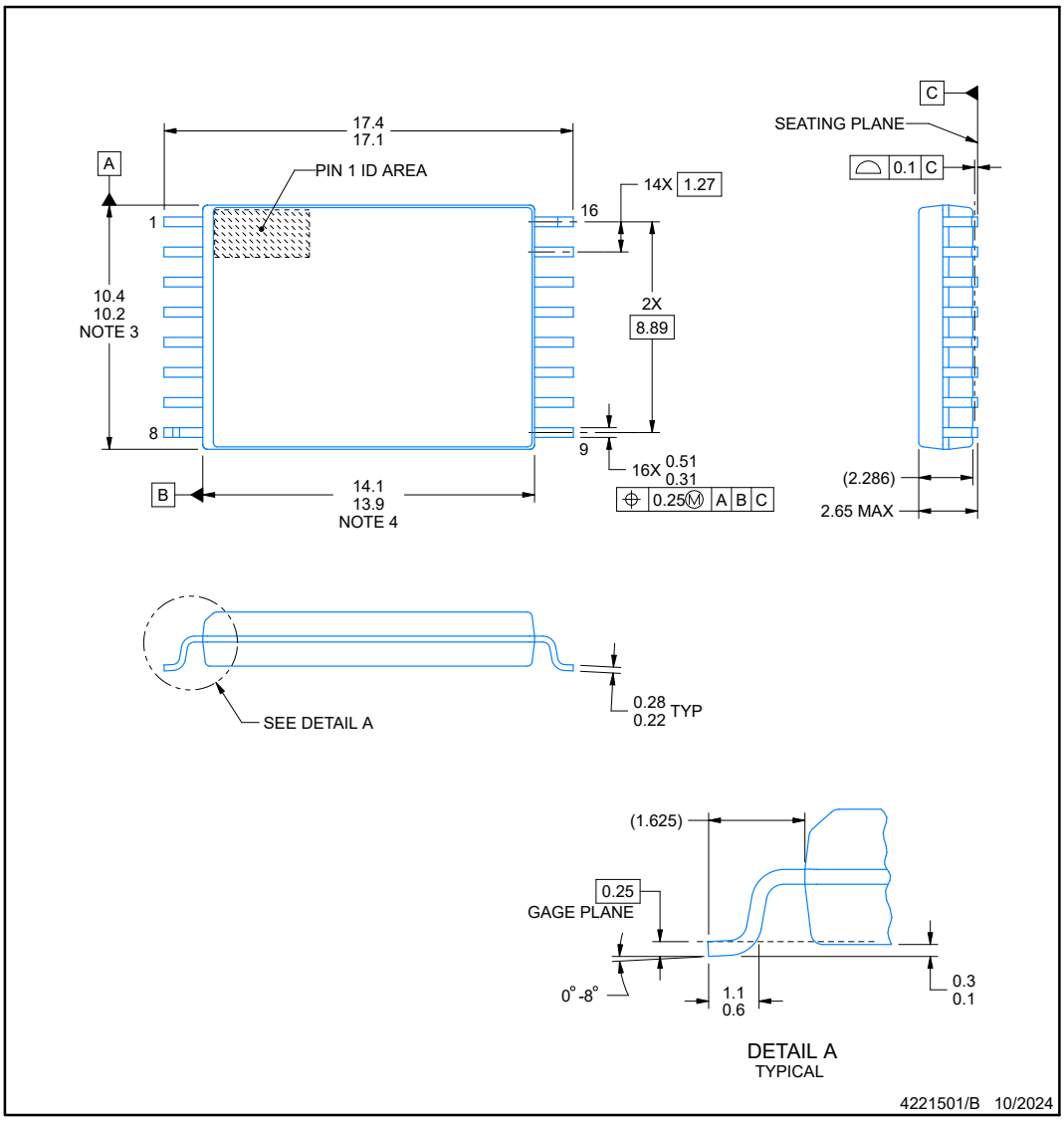
PACKAGE OUTLINE

DWW0016A



SOIC - 2.65 mm max height

PLASTIC SMALL OUTLINE



NOTES:

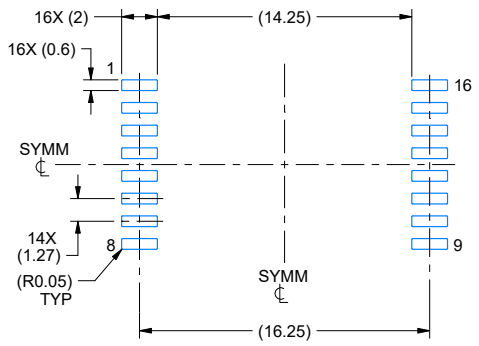
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 mm per side.
4. This dimension does not include interlead flash.

EXAMPLE BOARD LAYOUT

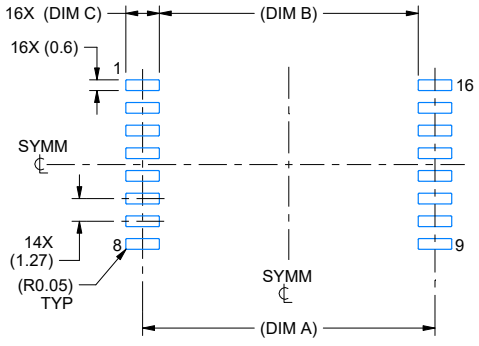
DWW0016A

SOIC - 2.65 mm max height

PLASTIC SMALL OUTLINE

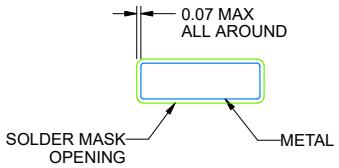


LAND PATTERN EXAMPLE
STANDARD
SCALE:3X

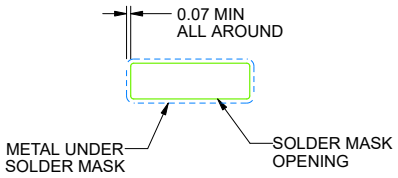


LAND PATTERN EXAMPLE
PCB CLEARANCE & CREEPAGE OPTIMIZED
SCALE:3X

OPTION	DIM A	DIM B	DIM C
01	16.375	14.5	1.875
02	16.625	15	1.625
03	16.725	15.2	1.525



NON SOLDER MASK
DEFINED
(PREFERRED)



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4221501/B 10/2024

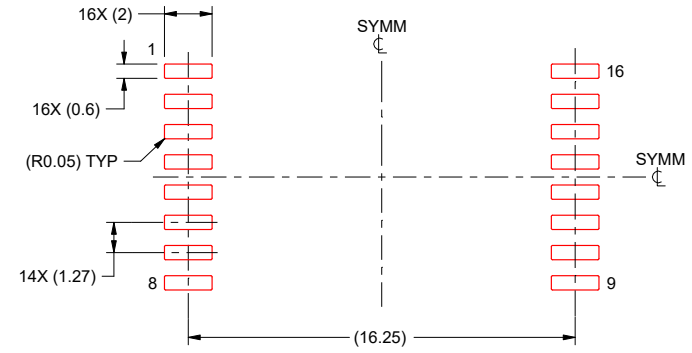
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

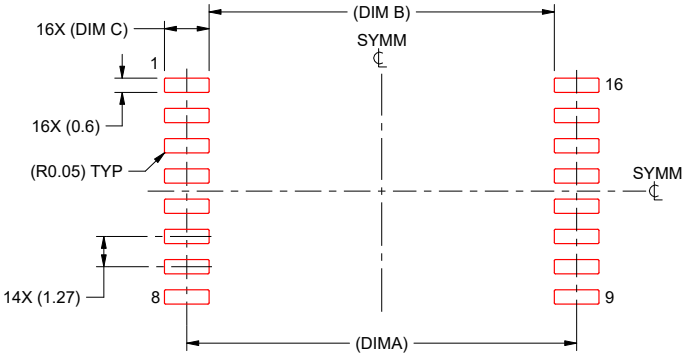
EXAMPLE STENCIL DESIGN

DWW0016A — **SOIC - 2.65 mm max height**

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
STANDARD
BASED ON 0.125 mm THICK STENCIL
SCALE:4X



SOLDER PASTE EXAMPLE
PCB CLEARANCE & CREEPAGE OPTIMIZED
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

OPTION	DIM A	DIM B	DIM C
01	16.375	14.5	1.875
02	16.625	15	1.625
03	16.725	15.2	1.525

4221501/B 10/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO7840DW	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7840
ISO7840DW.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7840
ISO7840DWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7840
ISO7840DWR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7840
ISO7840DWW	Active	Production	SOIC (DWW) | 16	45 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7840
ISO7840DWW.A	Active	Production	SOIC (DWW) | 16	45 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7840
ISO7840DWWR	Active	Production	SOIC (DWW) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7840
ISO7840DWWR.A	Active	Production	SOIC (DWW) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7840
ISO7840FDW	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7840F
ISO7840FDW.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7840F
ISO7840FDWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7840F
ISO7840FDWR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7840F
ISO7840FDWRG4	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7840F
ISO7840FDWRG4.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7840F
ISO7840FDWW	Active	Production	SOIC (DWW) | 16	45 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7840F
ISO7840FDWW.A	Active	Production	SOIC (DWW) | 16	45 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7840F
ISO7840FDWWR	Active	Production	SOIC (DWW) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7840F
ISO7840FDWWR.A	Active	Production	SOIC (DWW) | 16	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7840F

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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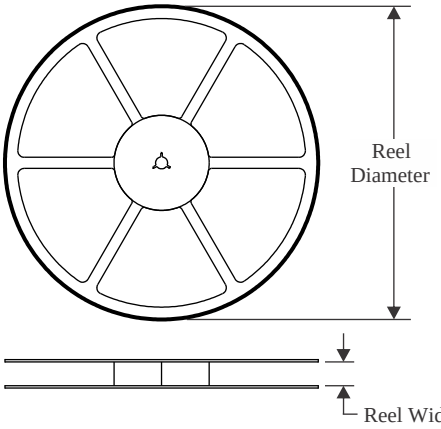
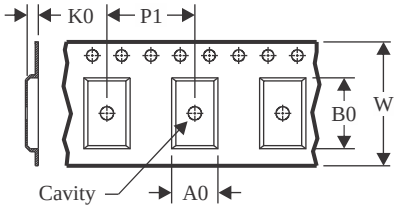
TAPE AND REEL INFORMATION

REEL DIMENSIONS

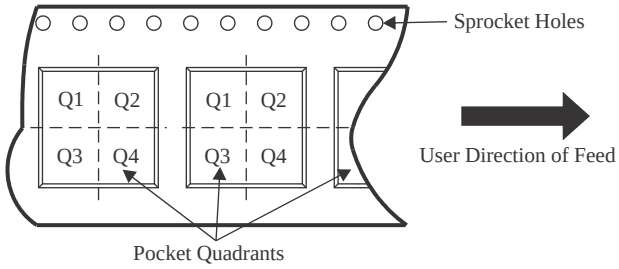


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

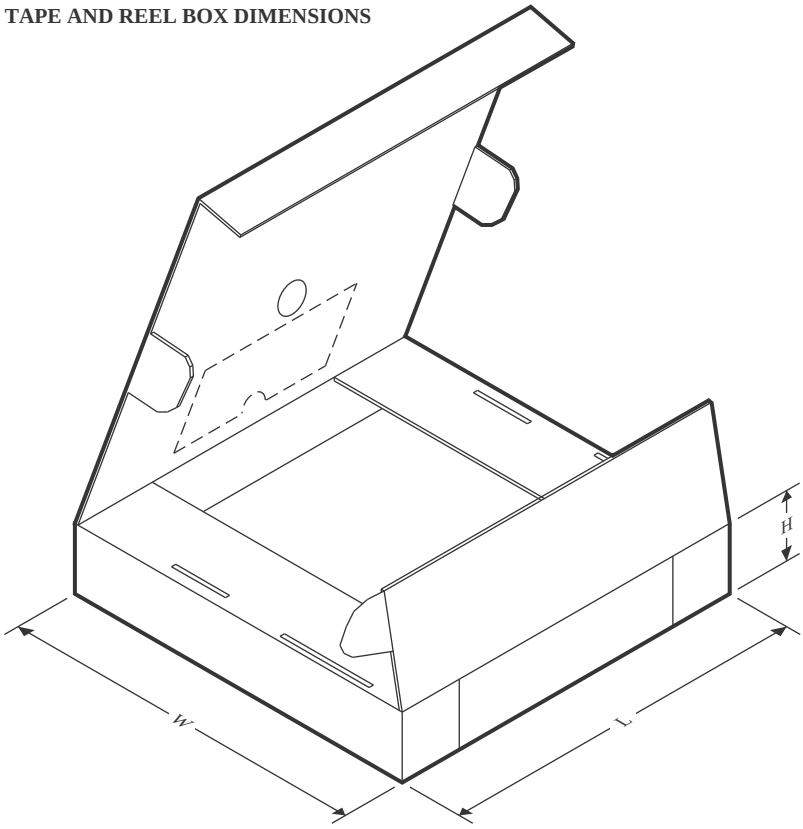
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7840DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7840DWWR	SOIC	DWW	16	1000	330.0	24.4	18.0	10.0	3.0	20.0	24.0	Q1
ISO7840FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7840FDWRG4	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7840FDWWR	SOIC	DWW	16	1000	330.0	24.4	18.0	10.0	3.0	20.0	24.0	Q1

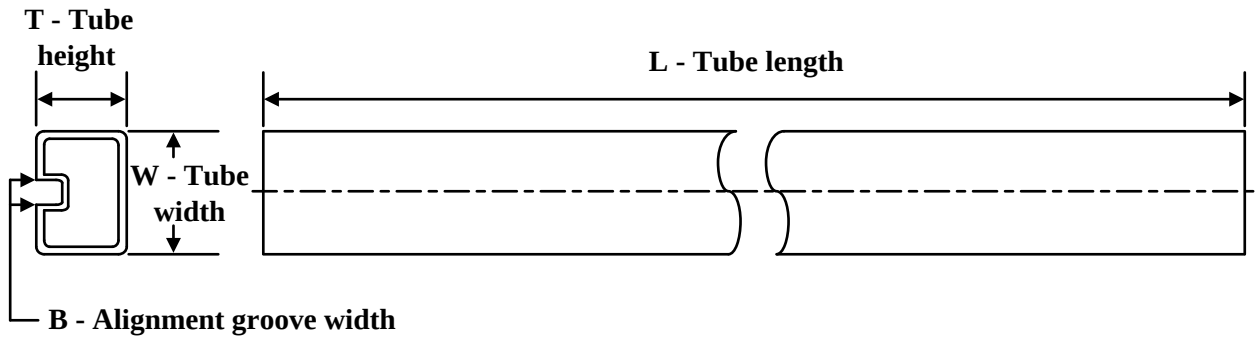
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7840DWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7840DWWR	SOIC	DWW	16	1000	350.0	350.0	43.0
ISO7840FDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7840FDWRG4	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7840FDWWR	SOIC	DWW	16	1000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO7840DW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7840DW.A	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7840DWW	DWW	SOIC	16	45	507	20	5000	9
ISO7840DWW.A	DWW	SOIC	16	45	507	20	5000	9
ISO7840FDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7840FDW.A	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7840FDWW	DWW	SOIC	16	45	507	20	5000	9
ISO7840FDWW.A	DWW	SOIC	16	45	507	20	5000	9

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Last updated 10/2025