ISOM871x 3.75kV$_{RMS}$, High-Speed Single-Channel Opto-Emulator

1 Features

- Drop-in replacement and pin-to-pin upgrade to industry standard high-speed digital optocouplers
- Single-channel diode-emulator input
- Output options:
  - ISOM8710: CMOS
  - ISOM8711: Open-collector
- Wide supply range (V_{CC}): 2.7V to 5.5V
- High data rate: up to 25Mbps
  - Maximum propagation delay: 52ns
  - Maximum pulse width distortion: 17ns
  - Maximum propagation delay skew: 15ns
- Robust isolation barrier:
  - Isolation rating: up to 3750V$_{RMS}$
  - Working voltage: 500V$_{RMS}$
  - Surge capability: up to 10kV
  - Minimum transient immunity: ±125kV/µs
- Wide temperature range: –40°C to +125°C
- Small SOIC-5 package
- Safety-related certifications:
  - UL 1577 recognition, 3750V$_{RMS}$ isolation
  - DIN EN IEC 60747-17 (VDE 0884-17) conformity per VDE
  - IEC 62368-1, IEC 61010-1
  - CQC GB 4943.1

2 Applications

- Power supplies
- Grid, Electricity meter
- Motor drives
- Factory automation and control
- Building automation
- Lighting
- Appliances

3 Description

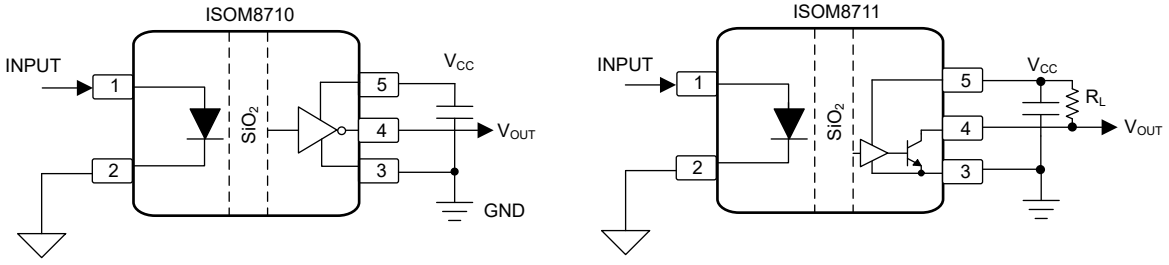
The ISOM871x devices are single-channel opto-emulators with diode-emulator inputs and digital outputs. The devices are pin-compatible and drop-in replaceable for many traditional optocouplers, allowing enhancement to industry-standard packages with no PCB redesign. These devices can transmit data rates up to 25Mbps and can output 3.3V and 5V signals with two logic-output options: CMOS-compatible output (ISOM8710) and open-collector output (ISOM8711).

ISOM871x opto-emulators offer significant reliability and performance advantages compared to optocouplers, including high common mode transient immunity (CMTI), low propagation delay, small pulse width distortion (PWD), low power consumption, wider temperature ranges, and tight process controls resulting in small part-to-part skew. Since there is no aging effect to compensate for, the emulated diode-input stage consumes less power than optocouplers. ISOM871x devices are offered in a small SOIC-5 package, supporting a 3.75kV$_{RMS}$ isolation rating. The high performance and reliability of the device enable the use in motor drives, I/O modules in industrial controllers, factory automation applications, and more. To learn more about the advantages of opto-emulator technology, please read *Introduction to Opto-emulators*.

Package Information

PART NUMBER	OUTPUT STAGE	PACKAGE (1)	PACKAGE SIZE (2)
ISOM8710	CMOS	DFF (SOIC, 5)	3.51mm × 7mm
ISOM8711	OPEN COLLECTOR		

(1) For more information, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Application Examples

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4 Device Comparison

Table 4-1. Device Comparison Table

DEVICE NAME	OUTPUT STAGE TYPE	CHANNEL COUNT	PACKAGE	NOMINAL BODY SIZE (mm)
ISOM8710	CMOS	1	DFF (SOIC, 5)	3.51mm × 4.8mm
ISOM8711	OPEN COLLECTOR			

5 Pin Configuration and Functions

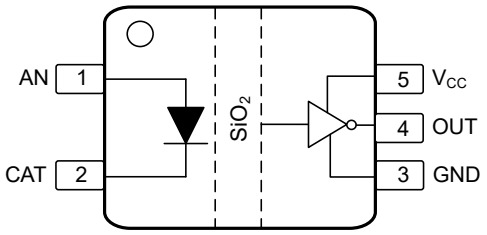


Figure 5-1. ISOM8710 DFF Package, 5-Pin SOIC (Top View)

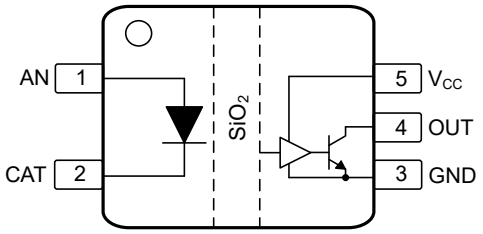


Figure 5-2. ISOM8711 DFF Package, 5-Pin SOIC (Top View)

Table 5-1. Pin Functions

PIN		TYPE(1)	Description
NAME	NO.		
AN	1	I	Anode connection of diode emulator
CAT	2	O	Cathode connection of diode emulator
GND	3	GND	Ground reference for V_{CC} and OUT
OUT	4	O	Digital data output. For ISOM8711, pull this pin up to V_{CC} using a resistor, R_L.
V_{CC}	5	P	Output power supply

(1) I = input, O = output, P = power, GND = ground

6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted).(1)

		MIN	MAX	UNIT
Supply voltage(2)	V_{CC}	-0.3	6	V
Input reverse voltage(3)	V_R		5	V
Output collector voltage, ISOM8711 only	V_{OC}	–0.3	V_{CC} + 0.5	V
Input forward current	I_F		25	mA
Peak transient input current(4)	I_{FT}		1	A
Output current, ISOM8710 only	I_O	-15	15	mA
Output collector current, ISOM8711 only	I_O		50	mA
Input power dissipation	P_{DI}		75	mW
Output collector power dissipation, ISOM8711 only	P_{DO}		85	mW
Operating junction temperature	T_J		150	°C
Storage temperature	T_{stg}	-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground potential and are peak voltage values
(3) Input reverse voltage is measured from CAT pin with respect to the AN pin
(4) <1 µs pulse width, 300 pulses per second

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2.7		5.5	V
$V_{F(OFF)}$	Input OFF-state voltage	0		0.8	V
$I_{F(ON)}$	Input ON-state forward current	2		20	mA
$I_{F(OFF)}$	Input OFF-state forward current(1)	0		250	µA
I_{OH}	HIGH-state output current	-4			mA
I_{OL}	LOW-state output current, ISOM8710 only			4	mA
I_{OS}	LOW-state open-collector sink current, ISOM8711 only			13	mA
DR	Data rate at 2 mA ≤ I_F < 3 mA	0		5	Mbps
	Data rate at 3 mA ≤ I_F < 6 mA	0		10	Mbps
	Data rate at I_F ≥ 6 mA	0		25	Mbps
T_J	Junction temperature	-40		130	°C
T_A	Ambient temperature	-40		125	°C

(1) The OFF condition is also specified by V_F ≤ 0.8 V.

6.4 Thermal Information

THERMAL METRIC[1]		ISOM871x DFF (SOIC) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	215.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	124.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	156.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	91.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	154.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	I_F = 20 mA, V_{CC} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 2-MHz 50% duty cycle square wave			70	mW
P_{D1}	Maximum power dissipation (side-1)				50	mW
P_{D2}	Maximum power dissipation (side-2)				20	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
			5-DFF	
IEC 60664-1				
CLR	External clearance(1)	Side 1 to side 2 distance through air	>5	mm
CPG	External creepage(1)	Side 1 to side 2 distance across package surface	>5	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	µm
CTI	Comparative tracking index	IEC 60112; UL 746A	>400	V
	Material Group	According to IEC 60664-1	II	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V_{RMS}	I-IV	
		Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 500 V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	707	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test; see Insulation Lifetime	500	V_{RMS}
		DC voltage	707	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production)	5303	V_{PK}
V_{IMP}	Maximum impulse voltage(3)	Tested in air, 1.2/50-us waveform per IEC 62368-1	7200	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(4)	$V_{IOSM} \geq 1.3 \times V_{IMP}$; tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	10000	V_{PK}
q_{pd}	Apparent charge(5)	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤5	
		Method b: At routine test (100% production), $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s (method b1) or $V_{pd(m)} = V_{ini}$, $t_m = t_{ini}$ (method b2)	≤5	
C_{IO}	Barrier capacitance, input to output(6)	V_{IO} = 0.4 × sin (2 πft), f = 1 MHz	1	pF
R_{IO}	Insulation resistance, input to output(6)	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	3750	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care must be taken during board design so that the mounting pads of the isolator on the printed-circuit board (PCB) do not reduce creepage and clearance. Inserting grooves, ribs or both can help increase creepage distance on the PCB.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier tied together creating a two-pin device.

6.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to IEC 62368-1 and IEC 61010-1	Certified according to UL 1577 Component Recognition Program	Certified according to GB4943.1	Certified according to EN 61010-1 and EN 62368-1
Certificate: 40040142	Master contract number: 220991	File number: E181974	Certificate: CQC24001426995	Client ID number: 77311

6.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SO5 PACKAGE						
I_S	Safety input, output, or supply current (1)	$R_{\theta JA}$ = 215.9°C/W, V_I = 5.5 V, T_J = 135°C, T_A = 25°C			90	mA
		$R_{\theta JA}$ = 215.9°C/W, V_I = 3.6 V, T_J = 135°C, T_A = 25°C			135	mA
		$R_{\theta JA}$ = 215.9°C/W, V_I = 2.7 V, T_J = 135°C, T_A = 25°C			185	mA
		$R_{\theta JA}$ = 215.9°C/W, V_I = 2 V, T_J = 135°C, T_A = 25°C			250	mA
P_S	Safety input, output, or total power (1)	$R_{\theta JA}$ = 215.9°C/W, T_J = 135°C, T_A = 25°C			500	mW
T_S	Maximum safety temperature (1)				135	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

6.9 Electrical Characteristics—DC

Over recommended operating conditions unless otherwise noted. All typical specifications are at T_A = 25 °C and V_{CC} = 3.3 V unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_F	Input forward voltage	I_F = 6 mA	1.3	1.5	1.8	V
I_{CCH}	Logic HIGH output supply current	Figure 7-2 or Figure 7-3, I_F = 0 mA			2	mA
I_{CCL}	Logic LOW output supply current	Figure 7-2 or Figure 7-3, I_F = 6 mA			2	mA
I/O						
V_{OH}	Logic HIGH output voltage, ISOM8710	Figure 7-1, I_F = 0, I_O = -4 mA, V_{CC} = 2.7 V	V_{CC} - 0.4	V_{CC} - 0.2		V
		Figure 7-1, I_F = 0, I_O = -4 mA, V_{CC} = 4.5 V	V_{CC} - 0.3	V_{CC} - 0.1		V
V_{OL}	Logic LOW output voltage, ISOM8710	Figure 7-1, I_F = 6 mA, I_O = 4 mA, V_{CC} = 2.7 V		0.06	0.2	V
		Figure 7-1, I_F = 6 mA, I_O = 4 mA, V_{CC} = 4.5 V		0.04	0.2	V
	Logic LOW output voltage, ISOM8711	Figure 7-3, I_F = 6 mA, V_{CC} = 4.5 V, R_L = 348 Ω; I_{OL} (sinking) = 13 mA		0.15	0.6	V
		Figure 7-3, I_F = 6 mA, V_{CC} = 2.7 V, R_L = 208 Ω; I_{OL} (sinking) = 13 mA		0.22	0.6	V
I_{OH}	Logic HIGH output current, ISOM8711	Figure 7-3, I_F = 0 mA, V_{OUT} = V_{CC} = 2.7 V			100	µA
		Figure 7-3, I_F = 0 mA, V_{OUT} = V_{CC} = 4.5 V			100	µA
I_{TH}	Input threshold current		0.6	1	2	mA
I_{HYS}	Input current hysteresis			0.26		mA
I_R	Input reverse current	V_R = 5 V, T_A = 25 ºC			10	µA
C_I	Input capacitance	Anode to Cathode capacitance at f = 1 MHz, V_F = 0 V		4		pF

6.10 Switching Characteristics, ISOM8710

Over recommended operating conditions unless otherwise noted. V_{CC} = 2.7 V to 5.5 V. All typical specifications are at T_A = 25 °C and V_{CC} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output signal rise time	Figure 7-2, C_L = 15 pF			10	ns
t_f	Output signal fall time	Figure 7-2, C_L = 15 pF			10	ns
t_{PLH}	Propagation delay time for output LOW to HIGH transition	Figure 7-2, I_F = 6 mA to 0 mA, C_L = 15 pF. T_r = T_f = 5 ns			52	ns
t_{PHL}	Propagation delay time for output HIGH to LOW transition	Figure 7-2, I_F = 0 mA to 6 mA, C_L = 15 pF. T_r = T_f = 5 ns			52	ns
PWD	Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	Figure 7-2, I_F = 6 mA, C_L = 15 pF. T_r = T_f = 5 ns		4.7	17	ns
t_{psk}	Part-to-part delay skew	I_F = 6 mA, C_L = 15 pF. T_r = T_f = 5 ns			15	ns
$\lvert CMTI_L \rvert$	Common mode transient immunity with a static LOW output	Figure 7-5, V_{CM} = 1200 V_{p-p}, I_F = 6 mA, output = LOW	±125	±150		kV/µs
$\lvert CMTI_H \rvert$	Common mode transient immunity with a static HIGH output	Figure 7-5, V_{CM} = 1200 V_{p-p}, I_F = 0 mA, output = HIGH	±800	±1000		kV/µs
TIE	Time Interval Error	2^{16} – 1 PRBS data at 20 Mbps, I_F = 6 mA		4.2	12	ns

6.11 Switching Characteristics, ISOM8711

Over recommended operating conditions unless otherwise noted. V_{CC} = 2.7 V to 5.5 V. R_L = 300 Ω unless otherwise specified. All typical specifications are at T_A = 25 °C and V_{CC} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output signal rise time	Figure 7-3, R_L = 300 Ω, C_L = 15 pF			15	ns

Over recommended operating conditions unless otherwise noted. V_{CC} = 2.7 V to 5.5 V. R_L = 300 Ω unless otherwise specified. All typical specifications are at T_A = 25 °C and V_{CC} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_f	Output signal fall time	Figure 7-3, R_L = 300 Ω, C_L = 15 pF			15	ns
t_{PLH}	Propagation delay time for output LOW to HIGH transition	Figure 7-3, I_F = 6 mA to 0 mA, C_L = 15 pF. T_r = T_f = 5 ns, R_L = 300 Ω			54	ns
t_{PHL}	Propagation delay time for output HIGH to LOW transition	Figure 7-3, I_F = 0 mA to 6 mA, C_L = 15 pF. T_r = T_f = 5 ns, R_L = 300 Ω			54	ns
PWD	Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	Figure 7-3, I_F = 6 mA, C_L = 15 pF. T_r = T_f = 5 ns		4.8	26	ns
t_{psk}	Part-to-part delay skew	I_F = 6 mA, C_L = 15 pF. T_r = T_f = 5 ns			15	ns
$\lvert CMTI_L \rvert$	Common mode transient immunity with a static LOW output	Figure 7-6, V_{CM} = 1200 V_{p-p}, I_F = 6 mA, Output = LOW	±125	±150		kV/µs
$\lvert CMTI_H \rvert$	Common mode transient immunity with a static HIGH output	Figure 7-6, V_{CM} = 1200 V_{p-p}, I_F = 0 mA, Output = HIGH	±800	±1000		kV/µs
TIE	Time Interval Error	2^{16} – 1 PRBS data at 20 Mbps, I_F = 6 mA		3.7	12	ns

6.12 Typical Characteristics

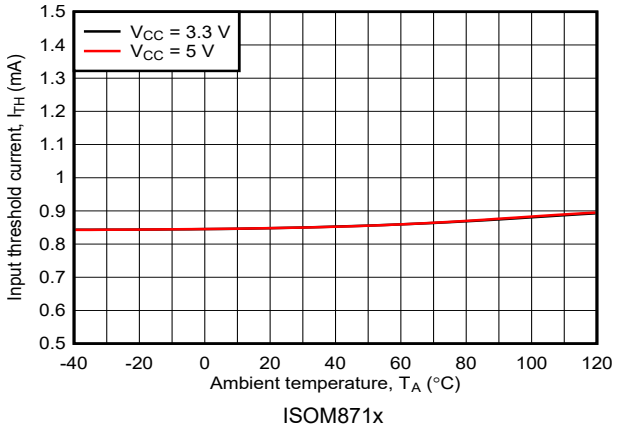


Figure 6-1. Input Threshold Current vs Ambient Temperature

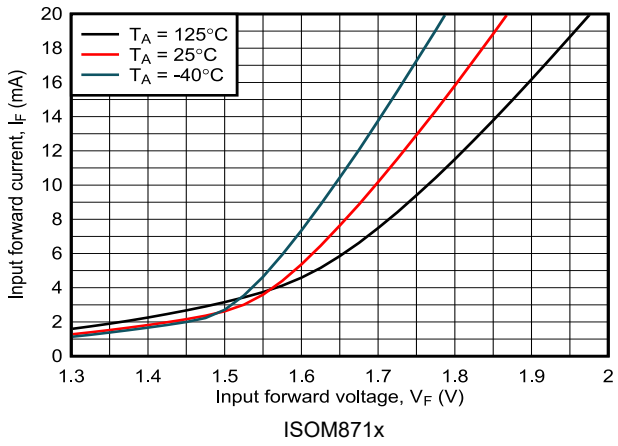


Figure 6-2. Input Forward Current vs Input Forward Voltage

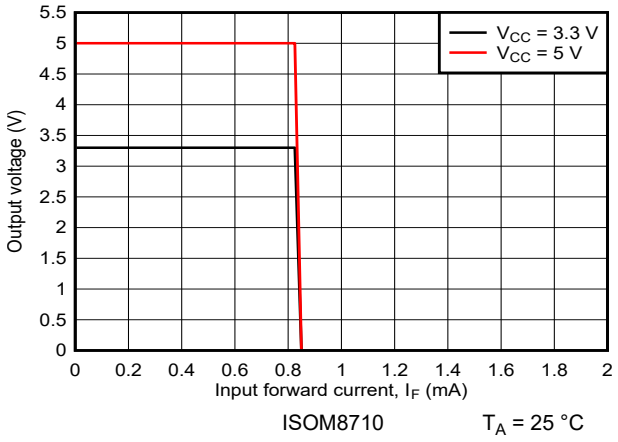


Figure 6-3. Output Voltage vs Input Forward Current

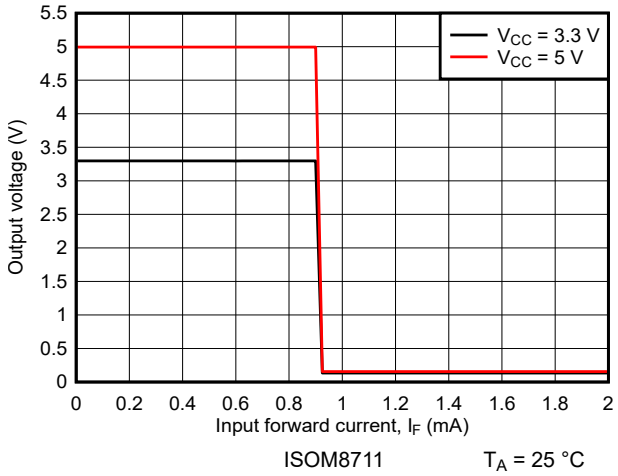


Figure 6-4. Output Voltage vs Input Forward Current

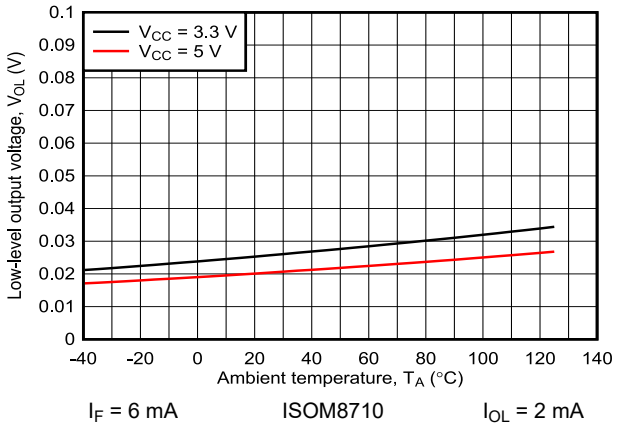


Figure 6-5. Low-Level Output Voltage vs Ambient Temperature

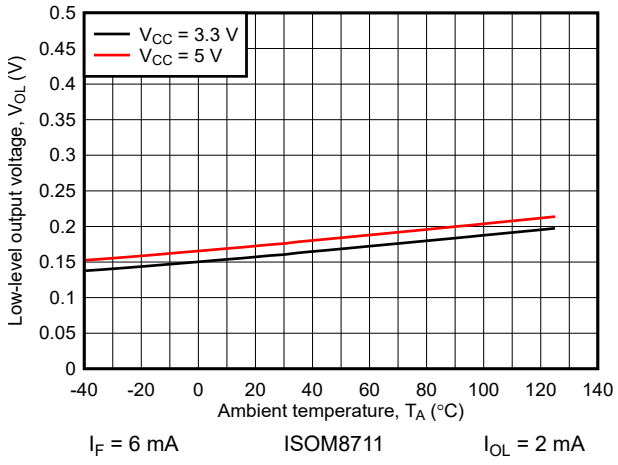


Figure 6-6. Low-Level Output Voltage vs Ambient Temperature

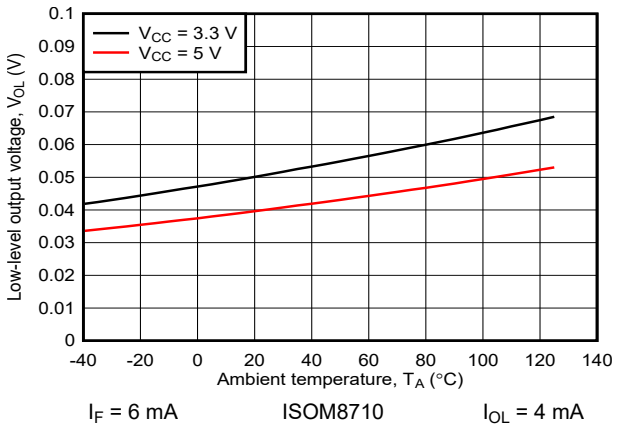


Figure 6-7. Low-Level Output Voltage vs Ambient Temperature

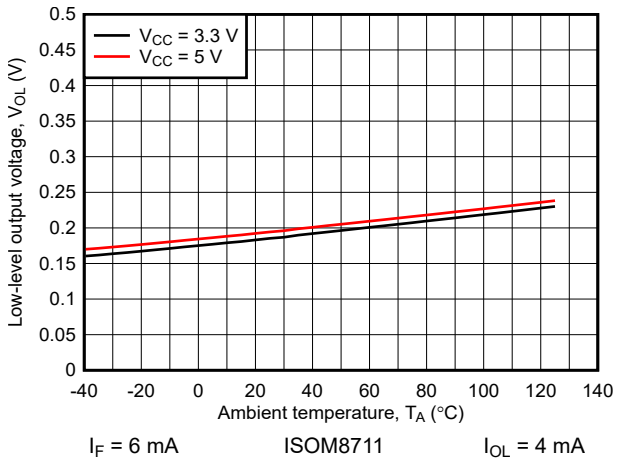


Figure 6-8. Low-Level Output Voltage vs Ambient Temperature

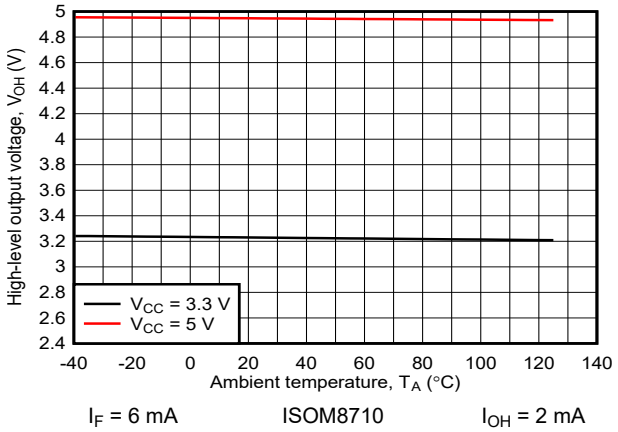


Figure 6-9. High-Level Output Voltage vs Ambient Temperature

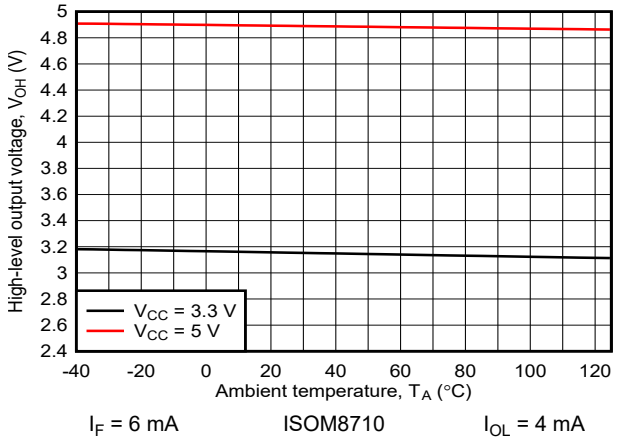


Figure 6-10. High-Level Output Voltage vs Ambient Temperature

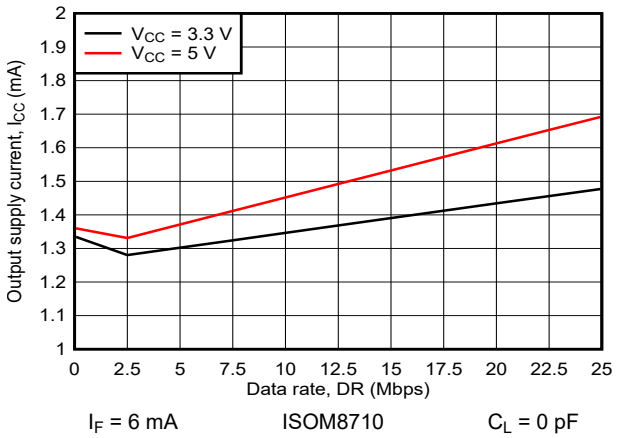


Figure 6-11. Output Supply Current vs Data Rate

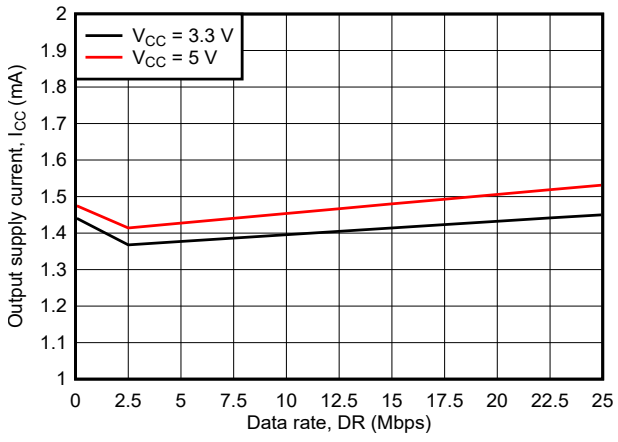


Figure 6-12. Output Supply Current vs Data Rate

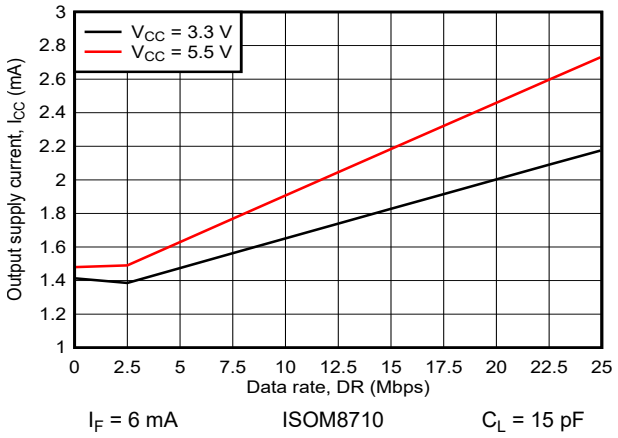


Figure 6-13. Output Supply Current vs Data Rate

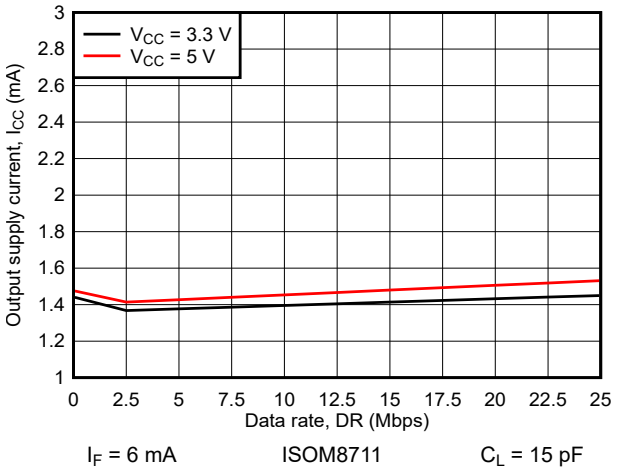


Figure 6-14. Output Supply Current vs Data Rate

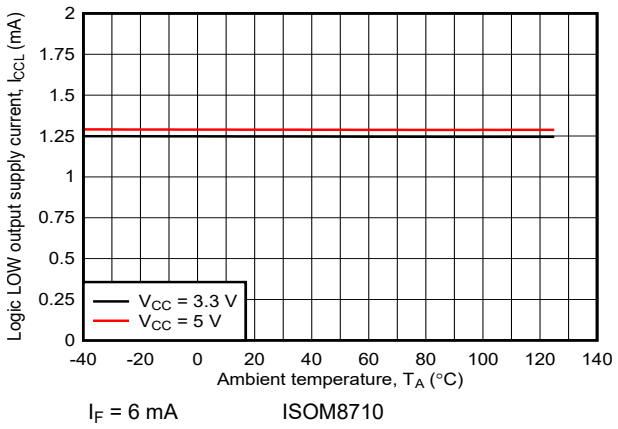


Figure 6-15. Logic LOW Output Supply Current vs Ambient Temperature

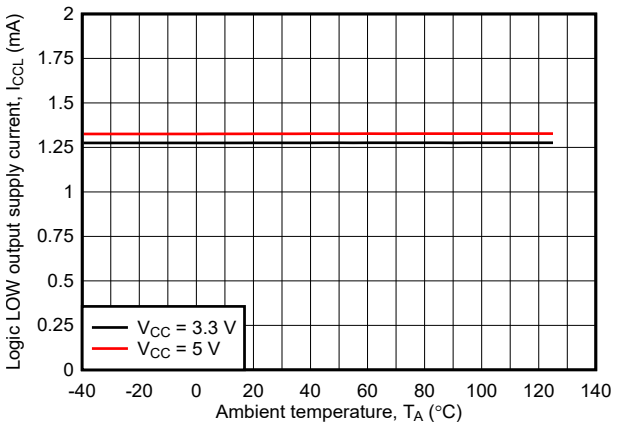


Figure 6-16. Logic LOW Output Supply Current vs Ambient Temperature

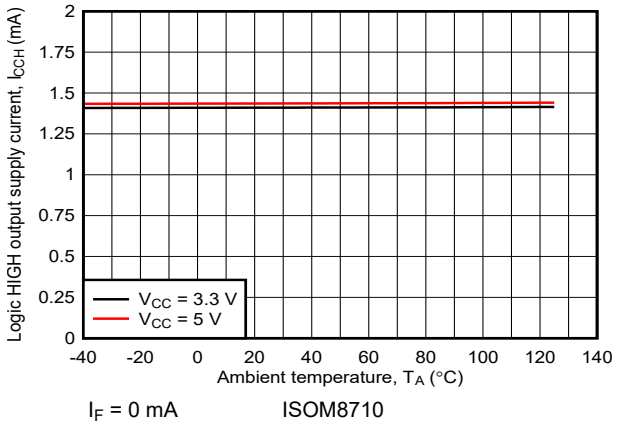


Figure 6-17. Logic HIGH Output Supply Current vs Ambient Temperature

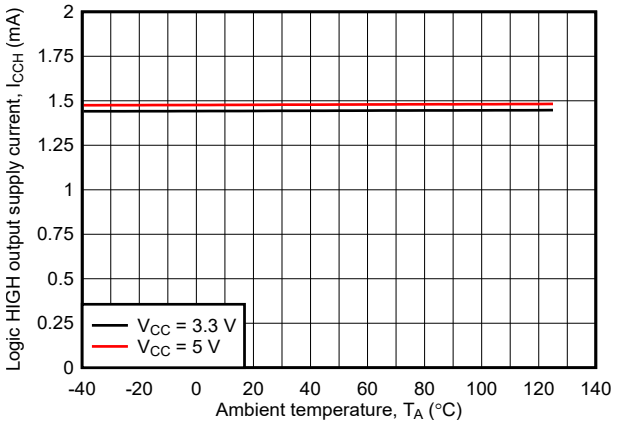


Figure 6-18. Logic HIGH Output Supply Current vs Ambient Temperature

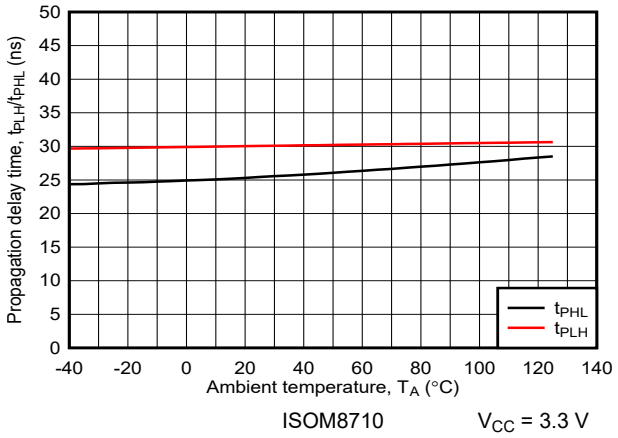


Figure 6-19. Propagation Delay Time vs Ambient Temperature

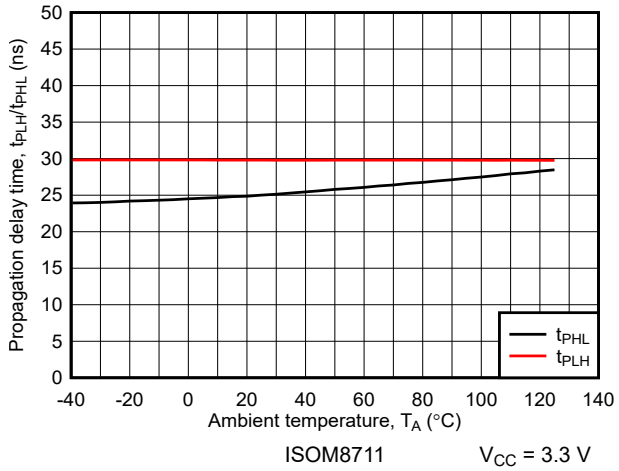


Figure 6-20. Propagation Delay Time vs Ambient Temperature

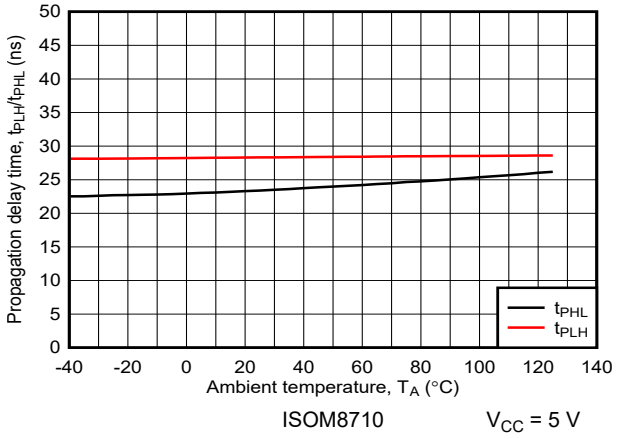


Figure 6-21. Propagation Delay Time vs Ambient Temperature

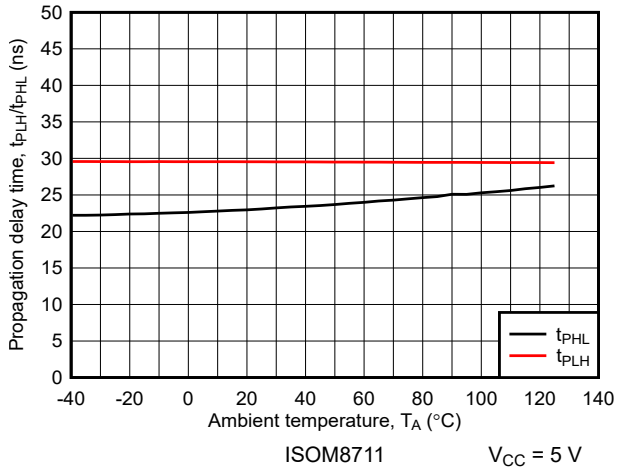


Figure 6-22. Propagation Delay Time vs Ambient Temperature

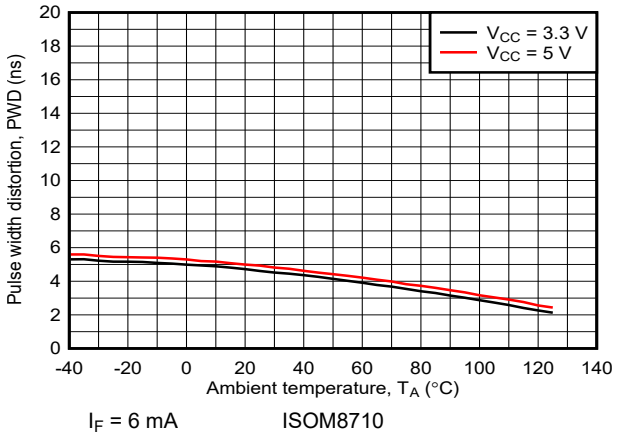


Figure 6-23. Pulse Width Distortion vs Ambient Temperature

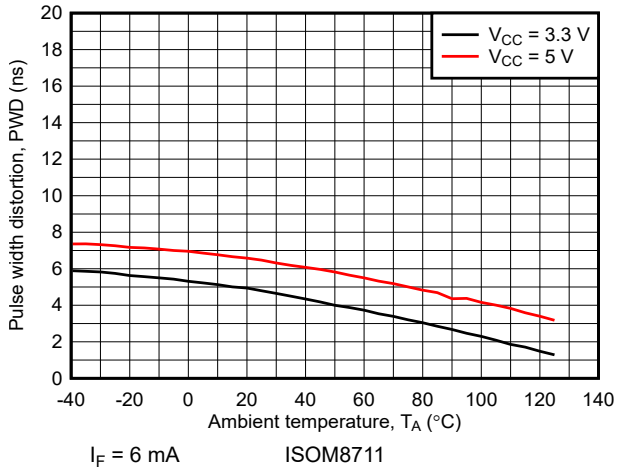


Figure 6-24. Pulse Width Distortion vs Ambient Temperature

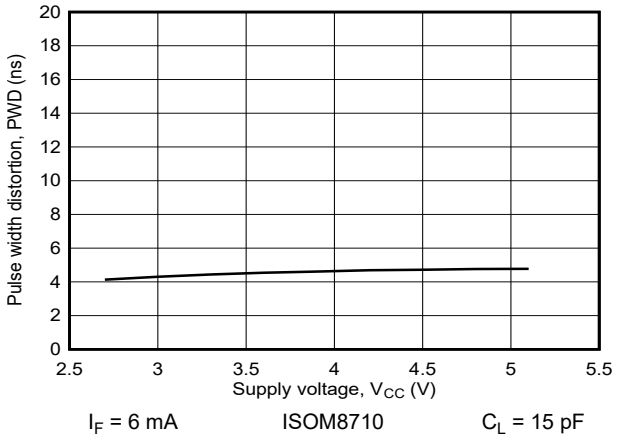


Figure 6-25. Pulse Width Distortion vs Supply Voltage

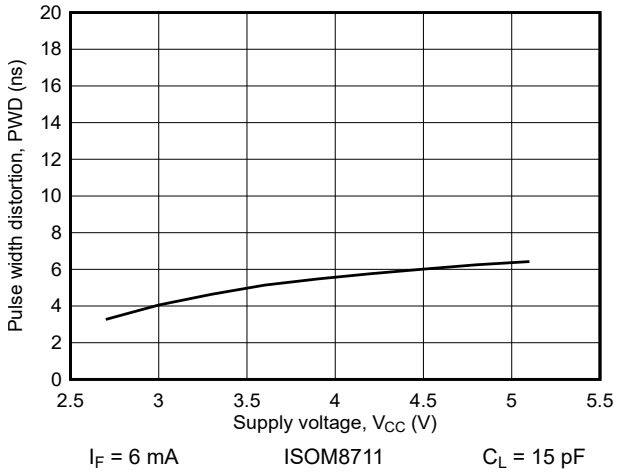


Figure 6-26. Pulse Width Distortion vs Supply Voltage

7 Parameter Measurement Information

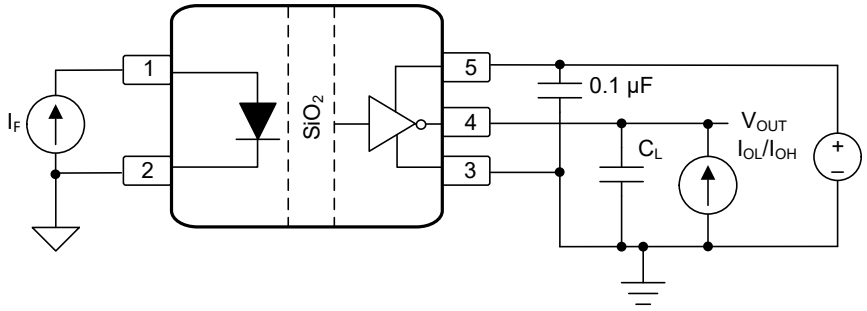


Figure 7-1. ISOM8710 Current-Source Test Circuit for V_{OL} and V_{OH}

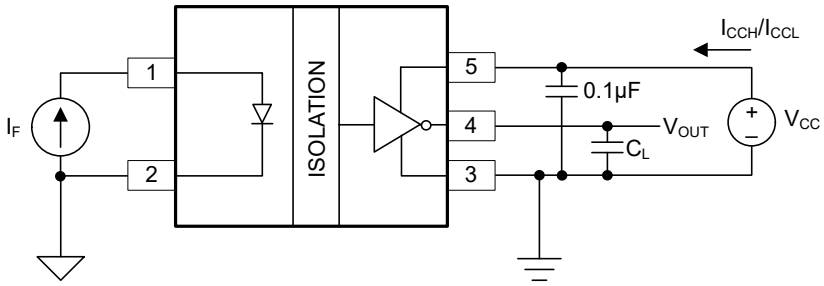


Figure 7-2. ISOM8710 Current-Source Test Circuit for I_{CCL}, I_{CCH}, and Switching Timing

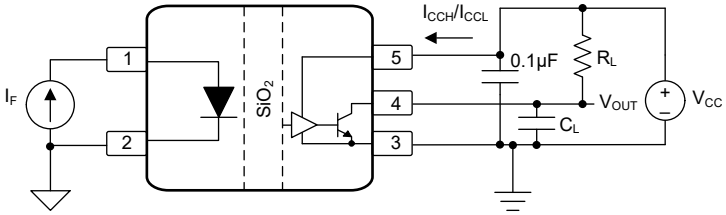


Figure 7-3. ISOM8711 Current-Source Test Circuit for Electrical and Switching Timing

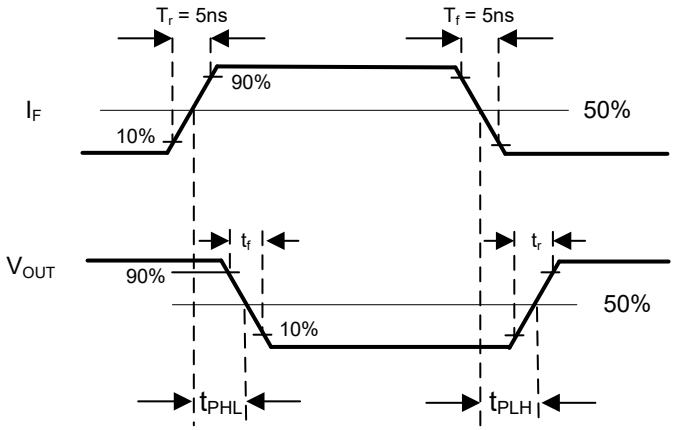


Figure 7-4. Switching Timing Waveforms

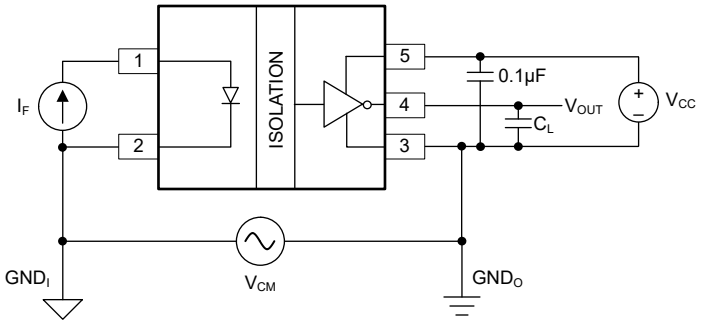


Figure 7-5. ISOM8710 Test Circuit for Common-Mode Transient Immunity

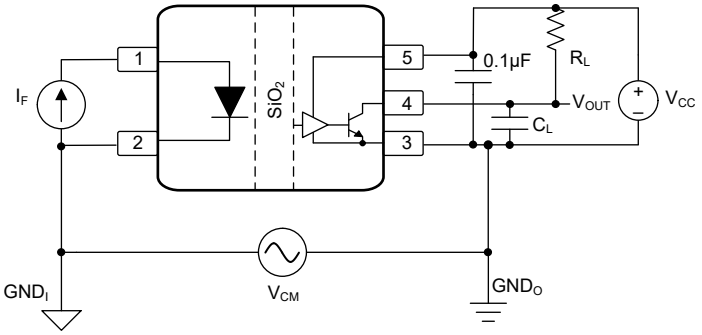


Figure 7-6. ISOM8711 Test Circuit for Common-Mode Transient Immunity

8 Detailed Description

8.1 Overview

The ISOM871x family of devices are opto-emulators that provide isolation for digital signals of data rates up to 25Mbps and are single-channel, pin-compatible, drop-in replacements for optocouplers. While standard optocouplers use an LED as the input stage, ISOM871x uses an emulated diode as the input stage. The input stage is isolated from the driver stage by TI's proprietary silicon dioxide-based (SiO_2) isolation barrier, which not only provides robust isolation, but also offers best-in-class common mode transient immunity. Ordering options include CMOS output and open collector output options.

ISOM871x devices isolate high speed digital signals and offer performance, reliability, and flexibility advantages not available with traditional optocouplers. The devices are based on CMOS isolation technology for low-power and high-speed operation, therefore the devices are resistant to the wear-out effects found in optocouplers that degrade performance with increasing temperature, forward current, and device age.

The functional block diagram of ISOM871x devices is shown in *Section 8.2*. The input signal is transmitted across the isolation barrier using an on-off keying (OOK) modulation scheme. The transmitter sends a high-frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the signal through the output stage. These devices also incorporate advanced circuit techniques to maximize CMTI performance and minimize radiated emissions. Figure 8-2 shows conceptual detail of how the OOK scheme works.

8.2 Functional Block Diagram

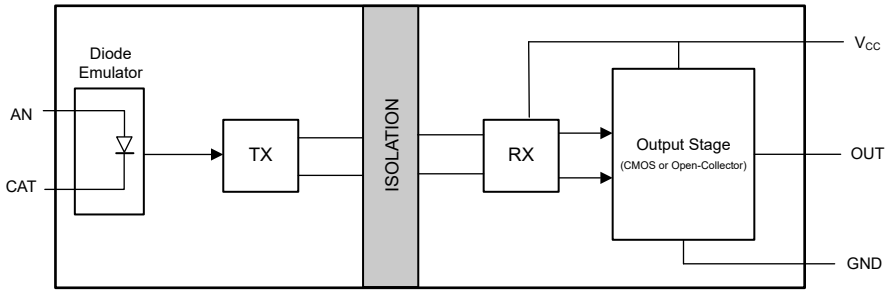


Figure 8-1. Conceptual Block Diagram of an Opto-emulator

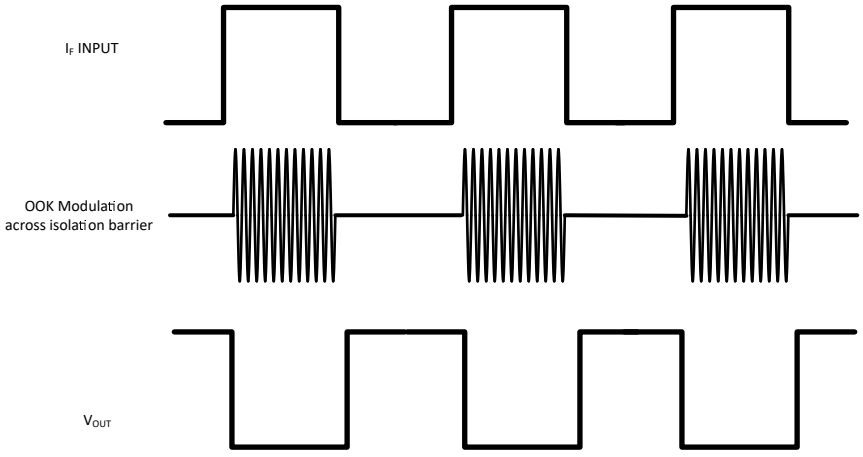


Figure 8-2. On-off Keying (OOK) Based Modulation Scheme

8.3 Feature Description

The ISOM871x devices receive current input and provide isolated voltage outputs. ISOM8710 has an output buffer on the receiver side which is capable of providing enough current to drive most logic-input devices. ISOM8711 has an open-collector output driven by an output buffer. Both devices are capable of isolating signals of up to 25Mbps data-rates and have an isolation voltage rating of 3750V_{RMS} between side 1 and side 2.

8.4 Device Functional Modes

Table 8-1 lists the functional modes for the ISOM871x devices.

Table 8-1. Function Table

V_{CC} STATE(2)	INPUT CURRENT I_F (1)	OUTPUT	COMMENTS
PU	> I_{TH}	L	Channel output assumes the inverse logic state of channel input.
	< I_{TH}	H	
PD	X	Undetermined	When V_{CC} is unpowered, the output is undetermined(2). When V_{CC} transitions from unpowered to powered up, the channel output assumes the corresponding logic state based on the logic state of the input.

(1) V_{CC} = Output power supply; PU = Powered up (V_{CC} ≥ 2.7V); PD = Powered down (V_{CC} ≤ 2V); X = Irrelevant; H = High level; L = Low level

(2) The outputs are in an undetermined state when 2V < V_{CC} < 2.7V.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISOM871x devices are single-channel opto-emulators with diode-emulator inputs and digital outputs. The devices use on-off keying modulation to transmit data across the isolation barrier. Since an isolation barrier separates the two sides of these devices, each side can be sourced independently with voltages and currents within recommended operating conditions. As an example, supplying the ISOM871x V_{CC} pin with 3.3V (which is within the 2.7V to 5.5V range for V_{CC}) and driving the diode-emulator input with 5mA (which is also within the 2mA to 20mA range for I_F) is possible.

The opto-emulator can also be used as a current-to-voltage translator or voltage level-translator in addition to providing isolation. Opto-emulators do not conform to any specific interface standard and are intended for isolating single-ended digital signal lines. Isolation devices like ISOM871x are typically placed between a data controller (that is, an MCU or FPGA), and a sensor, data converter, or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

For industrial applications, the ISOM871x devices can be used with a Texas Instruments mixed signal microcontroller, digital-to-analog converter, transformer driver, CAN transceiver, buffer, and voltage regulator to create an isolated CAN communication system. The different components of this typical schematic, like the microcontroller, transceiver, optional buffer, and power supply, can be replaced to create isolated RS-485, UART, SPI, GPIO, and other isolated signal communication systems. Additionally, ISOM871x devices can be used to isolate other signals within the *Recommended Operating Conditions*, including PWM power supply feedback signals.

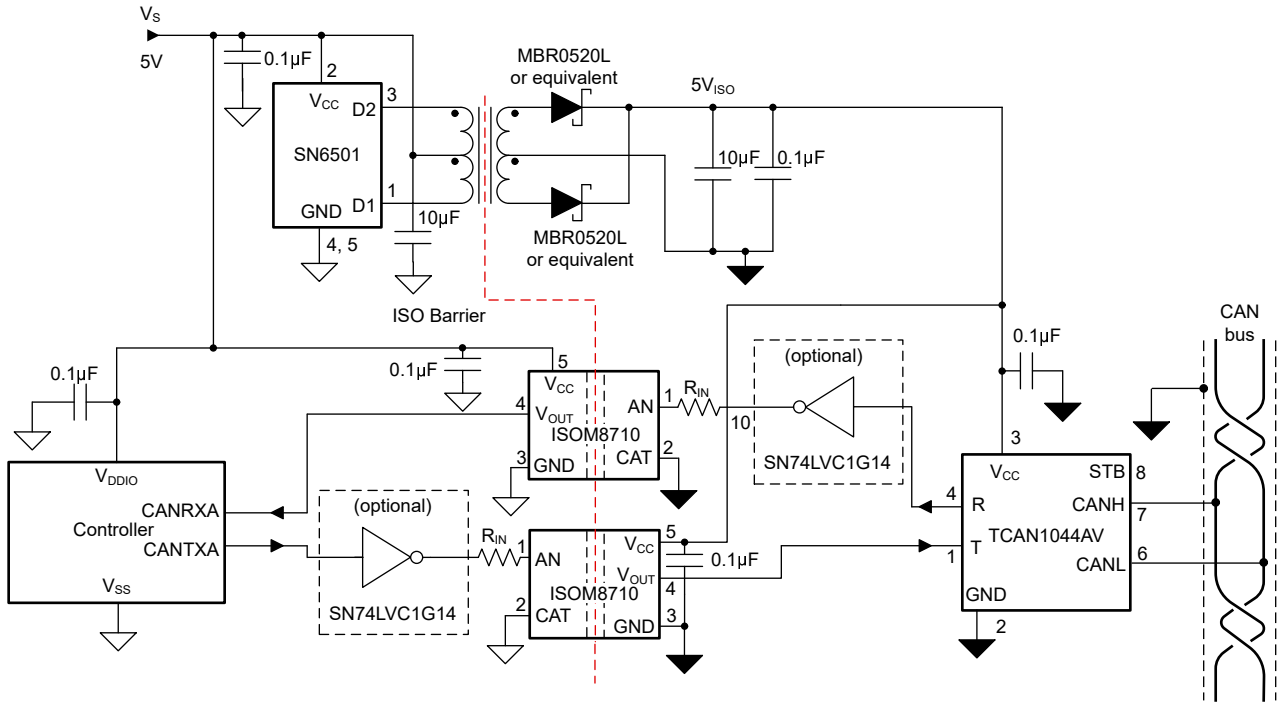


Figure 9-1. Typical Isolated CAN Application Using ISOM8710

9.2.1 Design Requirements

To design with ISOM871x devices, use the parameters listed in Table 9-1.

Table 9-1. Design Parameters

PARAMETER	VALUE	EXAMPLE VALUE
Supply voltage, V_{CC}	2.7V to 5.5V	3.3V or 5V
Input forward current, I_F, for up to 5Mbps data rates	2mA to 20mA	2mA
Input forward current, I_F, for up to 10Mbps data rates	3mA to 20mA	5mA
Input forward current, I_F, for up to 25Mbps data rates	6mA to 20mA	10mA
Decoupling capacitor between V_{CC} and GND	0.1µF	0.1µF
Pull-up resistor value, R_L, between OUT and V_{CC} for ISOM8711	750Ω to 50kΩ	4.7kΩ

9.2.2 Detailed Design Procedure

This section presents the design procedure for using the ISOM871x opto-emulators. External components must be selected to operate ISOM871x within the *Recommended Operating Conditions*. The following recommendations on components selection focus on the design of a typical isolated signal circuit with considerations for input current and data rate.

9.2.2.1 Sizing R_{IN}

The input side of ISOM871x is current-driven. To limit the amount of current flowing into the AN pin, use a series resistor, R_{IN}, in series with the input as shown in Figure 9-1.

R_{IN} can be sized to minimize current flow and power consumption through the ISOM871x input-side, or the resistor can be sized to enable higher data rates, depending on the application requirements. Regardless of the requirements, R_{IN} must be a value that limits the input forward current to be within the *Recommended Operating Conditions* for ISOM871x. The equation to calculate R_{IN} for a given input voltage, V_{IN}, and desired input forward current, I_F, is shown in Equation 1 where V_F is the maximum spec for the ISOM871x input forward voltage:

$$R_{IN} = \frac{V_{IN} - V_{F\,[MAX]}}{I_F} \quad (1)$$

For example, with a 24V input and 10mA desired I_F, R_{IN} can be calculated as:

$$R_{IN} = \frac{24\ V - 1.8\ V}{10\ mA} = 2.22\ k\Omega \quad (2)$$

9.2.2.2 Driving the Input with a Buffer

The input of ISOM871x can be driven by an inverting buffer or non-inverting buffer to change the truth table of the ISOM871x or provide sufficient input forward current to drive the device. Using a buffer is optional. If a buffer is used, the equation for R_{IN} remains the same as shown above.

Sizing R_{IN} based on the output voltage of the buffer, V_{BUF}, and the desired forward input current, I_F, Equation 1 becomes:

$$R_{IN} = \frac{V_{BUF} - V_{F\,[MAX]}}{I_F} \quad (3)$$

For example, using a buffer with a 5V output, and a desired I_F of 5mA, R_{IN} is calculated as:

$$R_{IN} = \frac{5\ V - 1.8\ V}{5\ mA} = 640\ \Omega \quad (4)$$

9.2.2.3 Calculating R_L for ISOM8711

An R_L component is not necessary if using ISOM8710. Since ISOM8711 features an open-collector OUT pin, a pull-up resistor, R_L, connecting OUT to V_{CC} is necessary for transmission of logic-HIGH signals. This pull-up resistor pulls the line HIGH when the line is not driven LOW by the open-collector OUT pin. The value of R_L is an important design consideration for systems using ISOM8711 since a value that is too low (strong pull-up) can result in excessive power dissipation while a value that is too high (weak pull-up) can lead to signal loss at high frequencies. Below are equations for the pullup resistor calculation.

Step 1: Calculate the Minimum R_L

An R_L value that is too small can prevent the OUT pin of the ISOM8711 from being able to drive LOW signals. Thus, the equation for minimum R_L is a function of V_{CC}, the maximum voltage level that can be read as a LOW signal by the input buffers of the connected device, V_{IL}, and the maximum current OUT can sink in LOW signal states, I_{OS}, as shown in Equation 5.

$$R_{L\,[MIN]} = \frac{V_{CC} - V_{IL\,[MAX]}}{I_{OS\,[MAX]}} \quad (5)$$

Most CMOS-input devices have maximum V_{IL} thresholds as a function of the supply, like 30% the V_{CC} level, while TTL-input devices can have a fixed V_{IL} threshold regardless of the supply, like 0.8V.

For an example V_{CC} = 3.3V, a maximum V_{IL} of 0.99V, and maximum I_{OS} of 13mA, minimum R_L is calculated as:

$$R_{L\,[MIN]} = \frac{3.3\ V - 0.99\ V}{13\ mA} = 178\ \Omega \quad (6)$$

Step 2: Calculate the Maximum R_L

The maximum pullup resistance is limited by the load and trace capacitance, C_L, of the OUT signal line due to standard rise time specifications. If the pullup resistor value is too high, the signal line cannot rise to a logical HIGH before being pulled LOW again. Thus, to calculate the maximum appropriate R_L value, the maximum allowable rise time, t_R, must first be calculated using Equation 7 and the maximum allowable rise time as a percentage of the data rate period and the maximum data rate of the signal to be transmitted.

$$t_R = 2 \times \frac{\text{rise time \%}}{\text{data rate}_{[MAX]}} \quad (7)$$

This rise time can be set equal to the time constant factor needed for a 10% to 90% transition to occur and solved for the resistor value, as shown in Equation 8:

$$R_{L\,[MAX]} = \frac{t_R}{2.2 \times C_L} \quad (8)$$

For example, if rise time can occupy 15% of the period for a 10Mbps signal, rise time in seconds is calculated as:

$$t_R = 2 \times \frac{15\ \%}{10\text{Mbps}} = 30\text{ns} \quad (9)$$

With a 30ns rise-time and a typical load capacitance of 2pF, maximum R_L is estimated as:

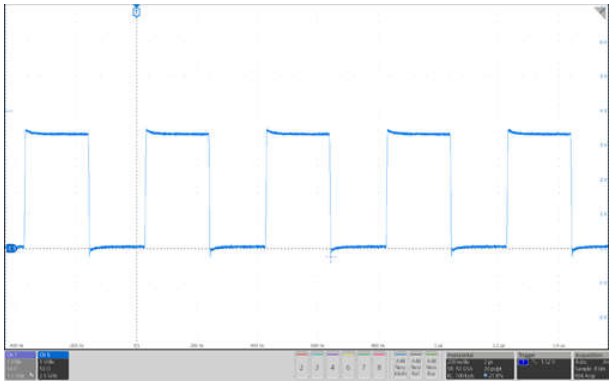
$$R_{L\,[MAX]} = \frac{30\text{ns}}{2.2 \times 2\text{pF}} = 6.82\text{k}\Omega \quad (10)$$

Step 3: Select R_L to be Between $R_{L\,(min)}$ and $R_{L\,(max)}$

The selected R_L value must be between the calculated $R_{L\,[min]}$ and $R_{L\,[max]}$ values to meet the design criteria. A lower value enables faster signal transmission or higher load and trace capacitances while a higher value consumes less power.

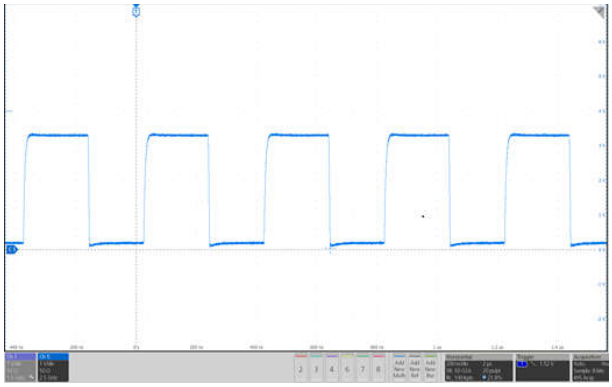
9.2.3 Application Curves

The following typical switching curve shows data transmission using the ISOM871x.



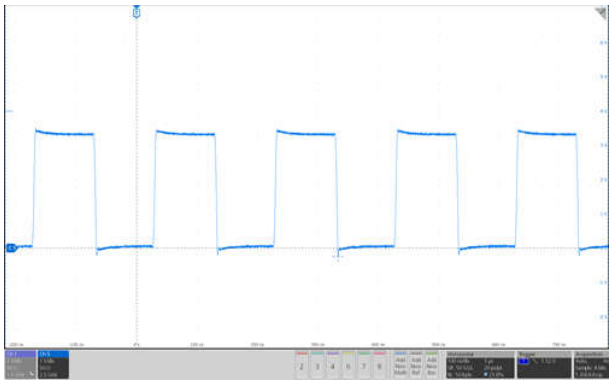
DR = 5Mbps ISOM8710 V_{CC} = 3.3V C_L = 15pF

Figure 9-2. Typical Output Waveform at I_F = 2mA



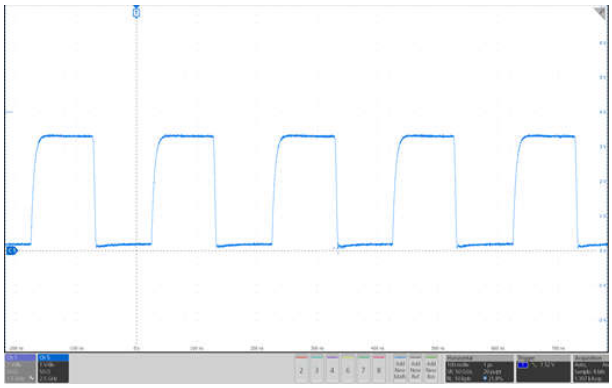
DR = 5Mbps ISOM8711 V_{CC} = 3.3V C_L = 15pF

Figure 9-3. Typical Output Waveform at I_F = 2mA



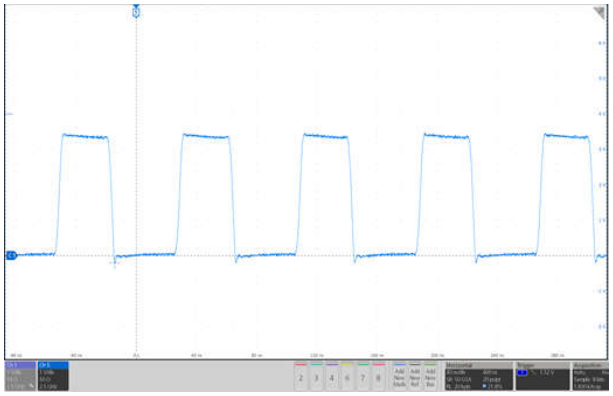
DR = 10Mbps ISOM8710 V_{CC} = 3.3V C_L = 15pF

Figure 9-4. Typical Output Waveform at I_F = 3mA



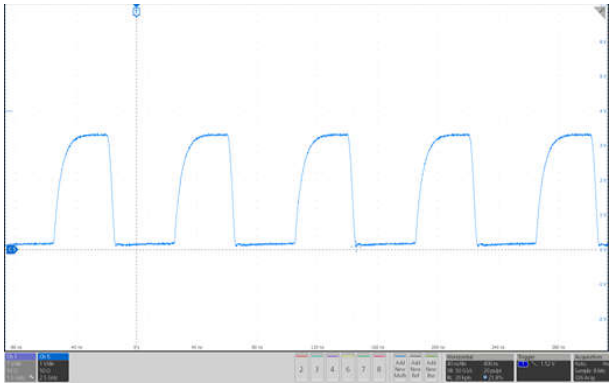
DR = 10Mbps ISOM8711 V_{CC} = 3.3V C_L = 15pF

Figure 9-5. Typical Output Waveform at I_F = 3mA



DR = 25Mbps ISOM8710 V_{CC} = 3.3V C_L = 15pF

Figure 9-6. Typical Output Waveform at I_F = 6mA



DR = 25Mbps ISOM8711 V_{CC} = 3.3V C_L = 15pF

Figure 9-7. Typical Output Waveform at I_F = 6mA

9.2.4 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; see Figure 9-8 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 50% for lifetime which translates into minimum required insulation lifetime of 30 years at a working voltage that's 20% higher than the specified value.

Figure 9-9 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over the lifetime of the barrier. Based on the TDDB data, the intrinsic capability of the insulation is 500V_{RMS} with a lifetime of 44. Other factors such as package size, pollution degree, and material group can further limit the working voltage of a component.

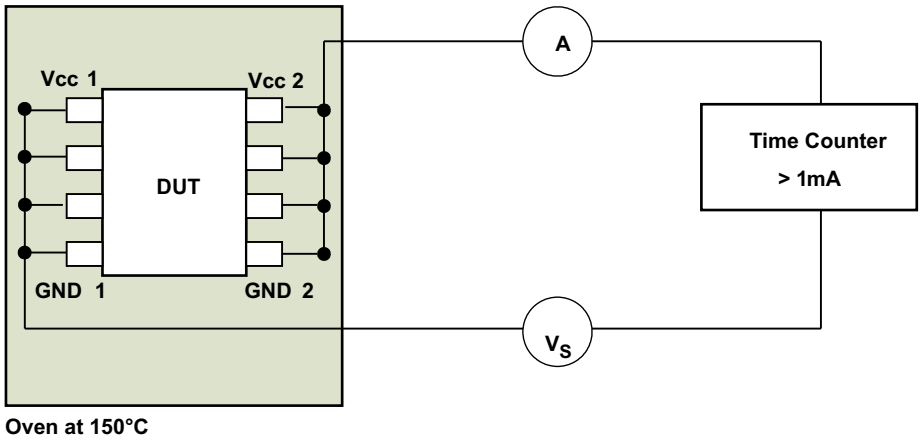


Figure 9-8. Test Setup for Insulation Lifetime Measurement

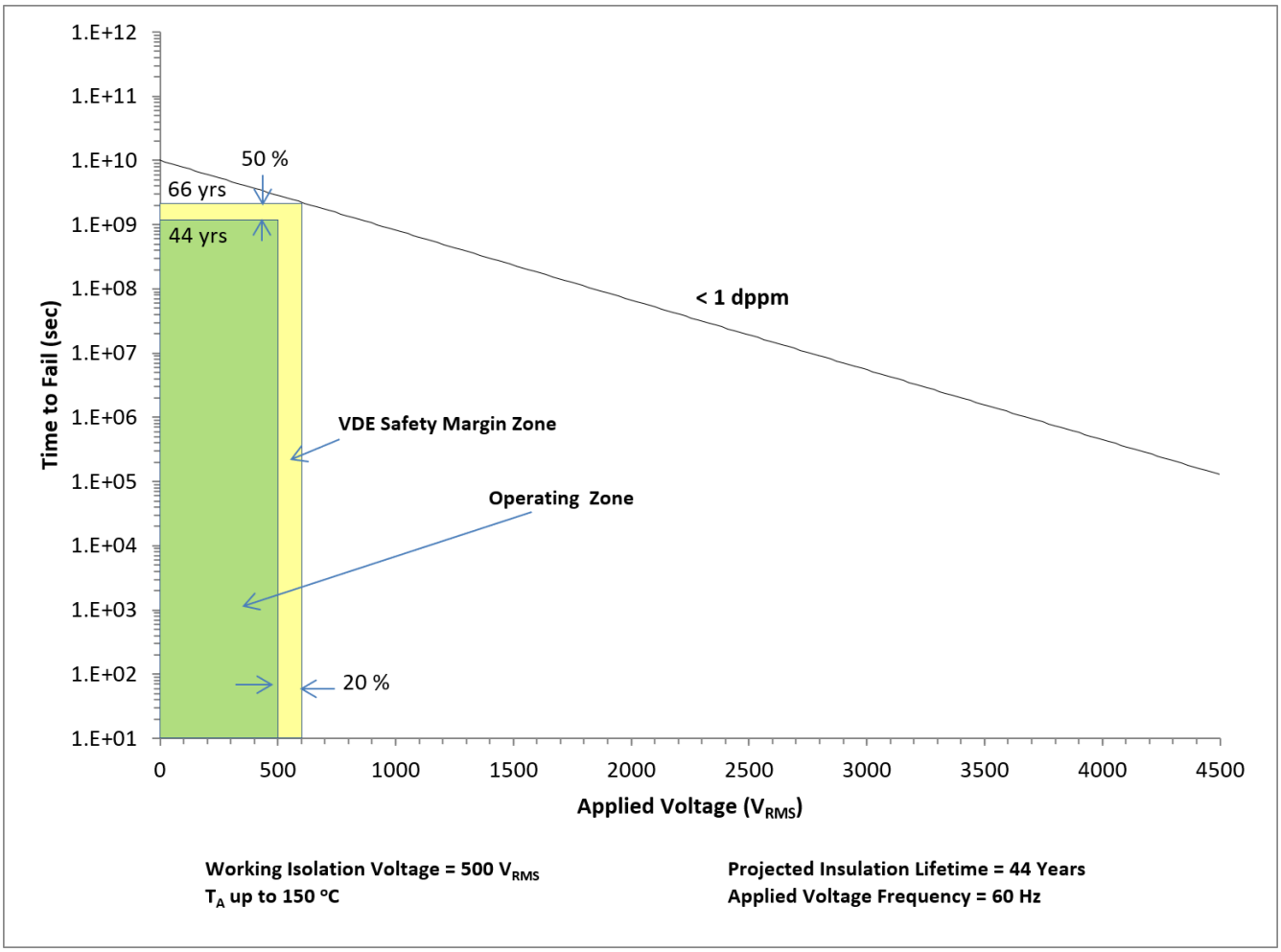


Figure 9-9. Insulation Lifetime Projection Data

9.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.7V and 5.5V. To help facilitate reliable operation at data rates and supply voltages, a 0.1µF bypass capacitor is recommended on the V_{CC} power supply pin. Place the capacitor within 2mm of the V_{CC} pin and as close to the V_{CC} pin as possible.

If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of an isolation transformer driver, such as Texas Instruments' SN6501, SN6505A/B, or SN6507. For such applications, detailed power supply design and transformer selection recommendations are available in the data sheets for each of these products and the respective product webpages on TI.com.

9.4 Layout

9.4.1 Layout Guidelines

- Bypass the V_{CC} pin to ground with a low-ESR ceramic bypass capacitor. The typical recommended bypass capacitance is 0.1µF when using a ceramic capacitor with an X5R- or X7R-rated dielectric. The capacitor must be placed as close to the V_{CC} pin as possible in the PCB layout and on the same layer. The capacitor must have a voltage rating greater than the V_{CC} voltage level.
- The device connections to ground must be tied to the PCB ground plane using a direct connection or two vias to help minimize inductance.
- The connections of capacitors and other components to the PCB ground plane must use a direct connection or two vias for minimum inductance.

9.4.2 Layout Example

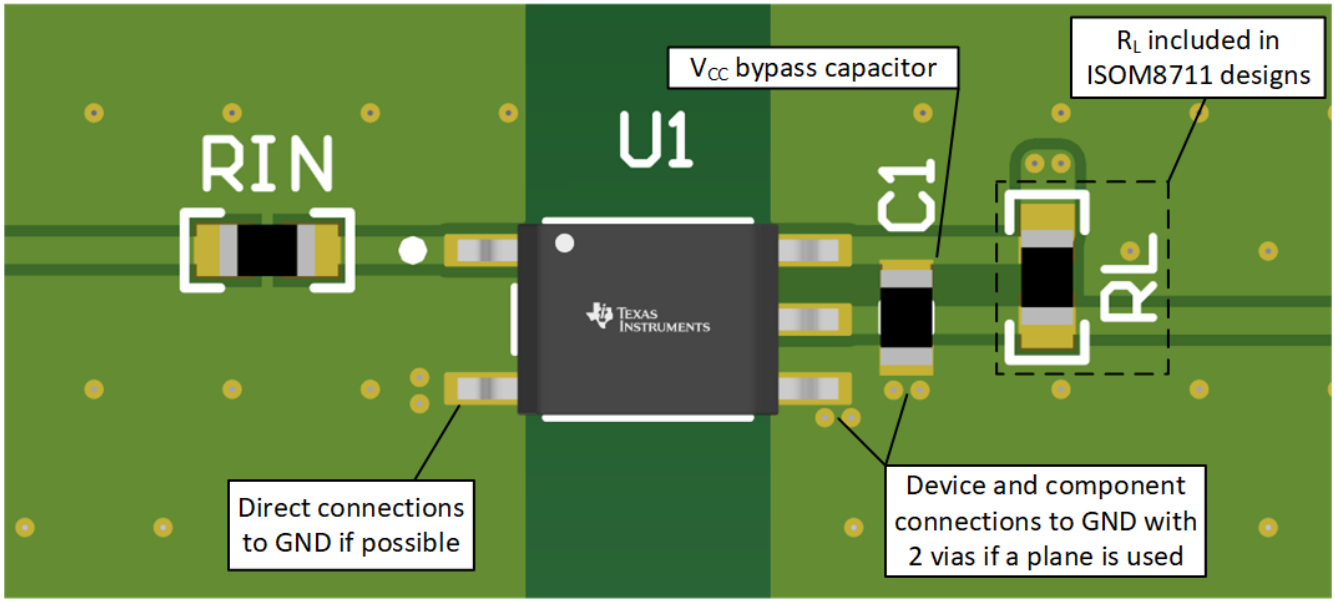


Figure 9-10. Layout Example of ISOM871x With a 2-Layer Board

10 Device and Documentation Support

10.1 Documentation Support

For related documentation see the following:

- Texas Instruments, *Isolation Glossary*
- Texas Instruments, *Introduction to Opto-Emulators* application note
- Texas Instruments, *ISOM8710 High-Speed Single-Channel Opto-Emulator Evaluation Module* user's guide
- Texas Instruments, *SN6501 Transformer Driver for Isolated Power Supplies* data sheet
- Texas Instruments, *SN6505x Low-Noise 1A Transformer Drivers for Isolated Power Supplies* data sheet
- Texas Instruments, *SN6507 Low-Emissions, 36V Push-Pull Transformer Driver with Duty Cycle Control for Isolated Power Supplies* data sheet
- Texas Instruments, *TCAN1044A-Q1 and TCAN1044AV-Q1 Automotive Fault-Protected CAN FD Transceiver with Standby mode* data sheet

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need. Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (September 2023) to Revision D (August 2025)	Page
• Updated certification information and removed "planned"	1
• Changed to 500 VRMS to match VIOWM	7
• Changed 'Plan to certify' to 'Certified' and added certificate numbers	8

Changes from Revision B (July 2023) to Revision C (September 2023)	Page
• Made editorial corrections and modifications throughout the document	1
• Updated ISOM871x images to read "SiO_2" instead of "ISOLATION" throughout the document	1
• Updated ISOM8711 device status to Production Data	1

- Updated application waveforms.....23

Changes from Revision A (June 2023) to Revision B (July 2023) **Page**

- Updated ISOM8711 device status to Advanced Information.....1

Changes from Revision * (March 2023) to Revision A (June 2023) **Page**

- Updated device status to Production Data.....1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISOM8710DFFR	Active	Production	SOIC (DFF) | 5	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8710
ISOM8710DFFR.A	Active	Production	SOIC (DFF) | 5	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8710
ISOM8711DFFR	Active	Production	SOIC (DFF) | 5	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8711
ISOM8711DFFR.A	Active	Production	SOIC (DFF) | 5	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8711

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

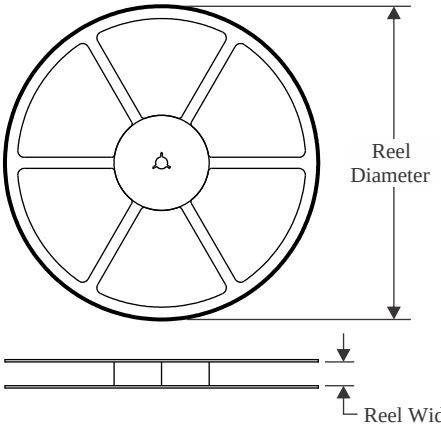
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

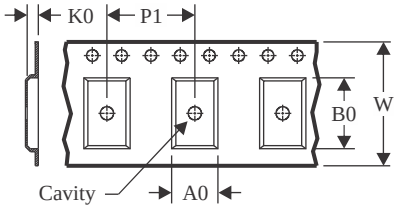
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

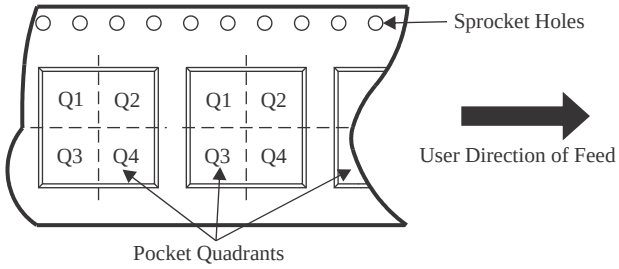


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

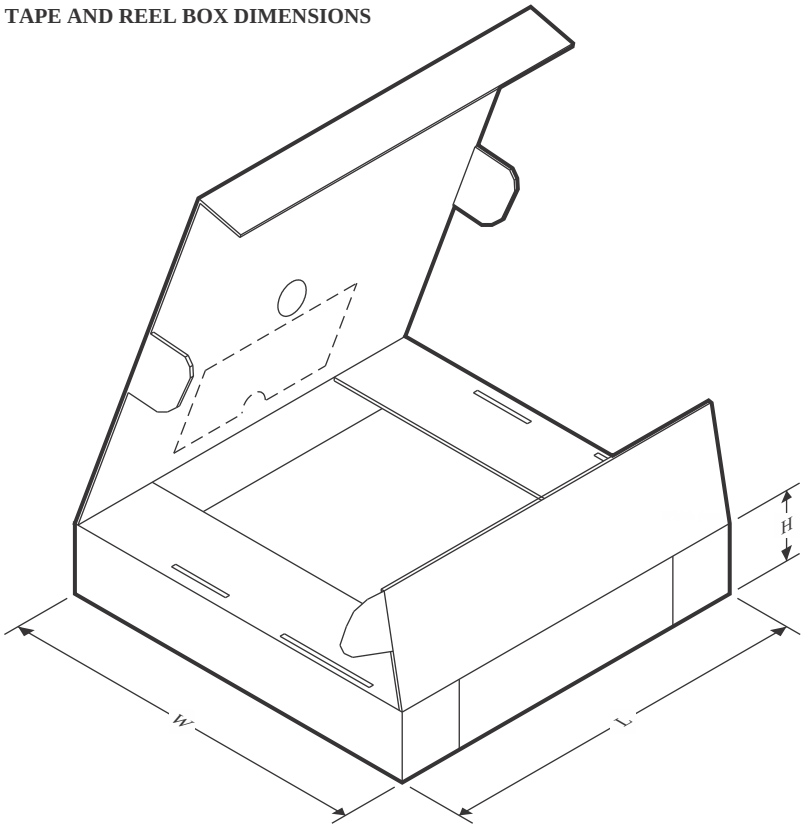
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISOM8710DFFR	SOIC	DFF	5	2000	330.0	12.4	8.0	3.8	2.7	12.0	12.0	Q1
ISOM8711DFFR	SOIC	DFF	5	2000	330.0	12.4	8.0	3.8	2.7	12.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

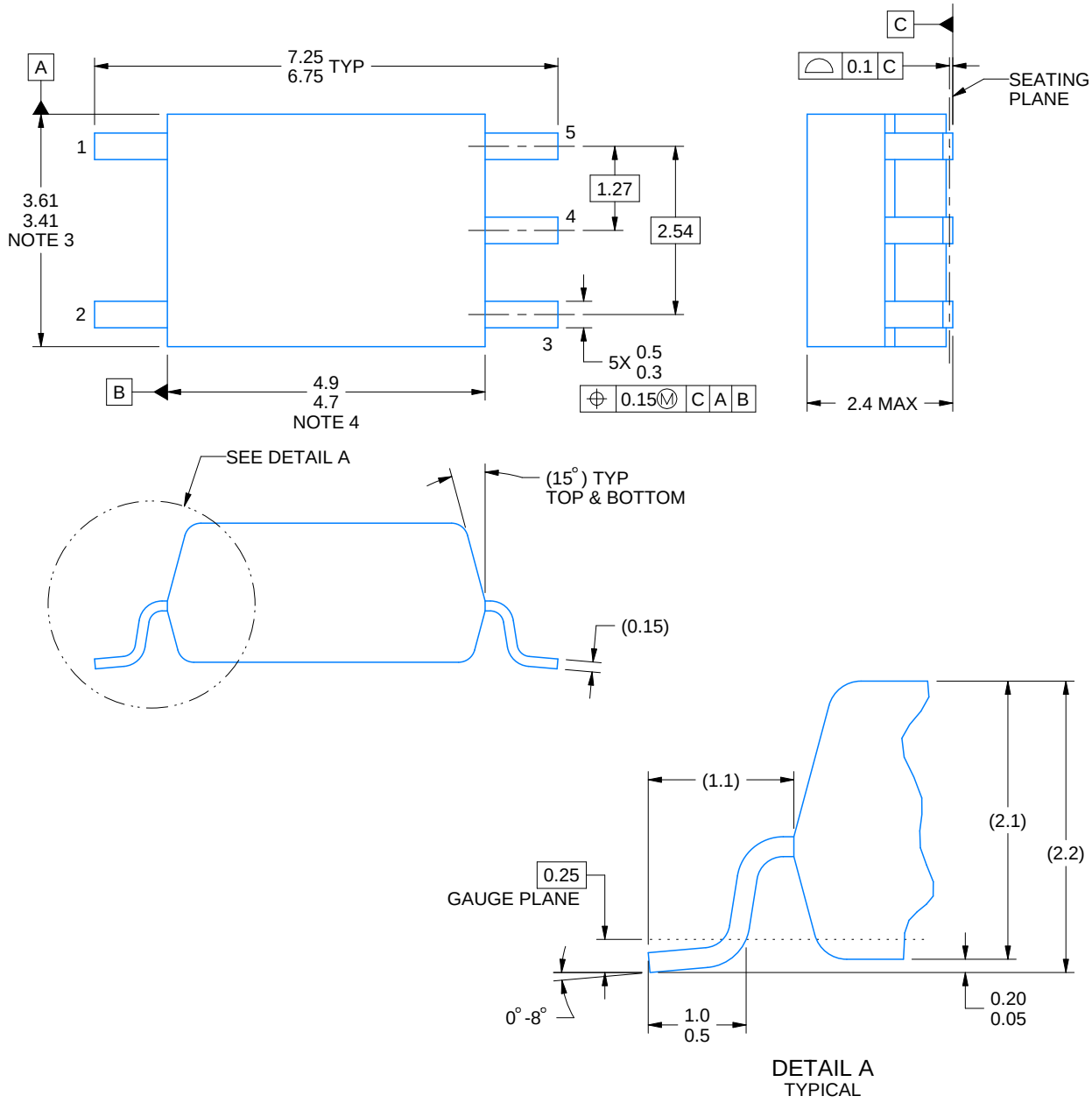
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISOM8710DFFR	SOIC	DFF	5	2000	353.0	353.0	32.0
ISOM8711DFFR	SOIC	DFF	5	2000	353.0	353.0	32.0

PACKAGE OUTLINE

DFF0005A

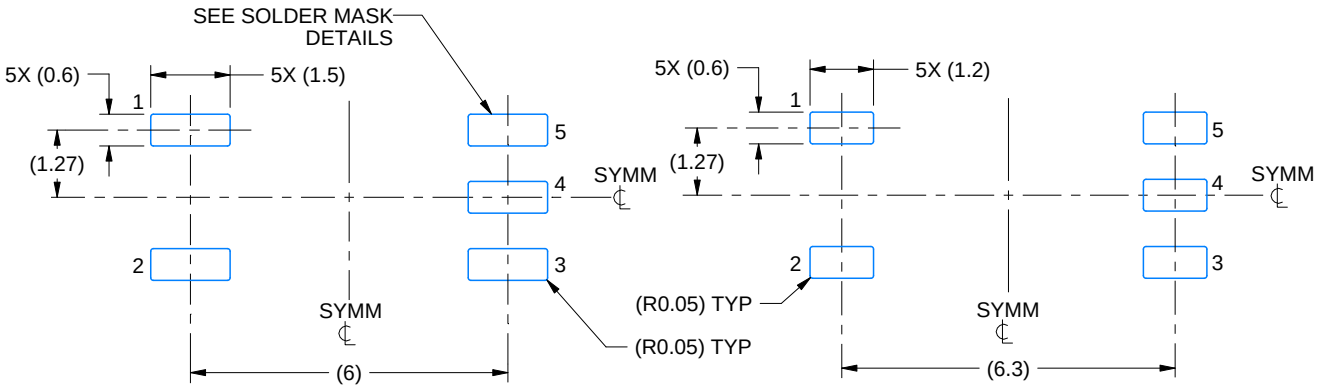
SOIC - 2.4 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

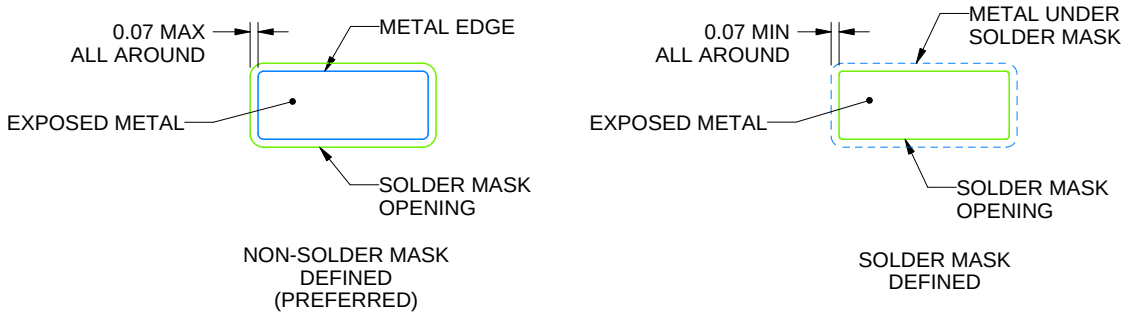


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 mm per side.
4. This dimension does not include interlead flash.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 7X



SOLDER MASK DETAILS

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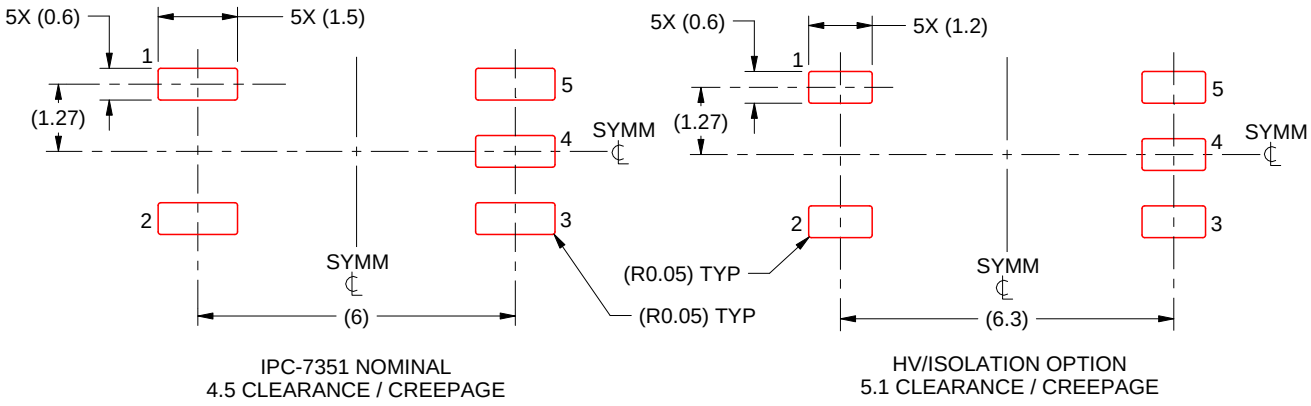
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
4.5 CLEARANCE / CREEPAGE

HV/ISOLATION OPTION
5.1 CLEARANCE / CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 7X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025