ISOW308x Robust-EMC, Isolated RS-485/RS-422 Transceiver With Integrated DC-DC Converter

ADVANCE INFORMATION

1 Features

- Data rates
  - ISOW3080 and ISOW3080P : 500kbps
  - ISOW3086 and ISOW3086P : 12Mbps
- Integrated best in class emissions DC-DC converter
  - Meets CISPR 32 Class B with margin on a two-layer PCB
- High efficiency output power
  - Typical efficiency: 41.5%
  - V_{ISOOUT} accuracy: ±10%
- Independent power supply for RS-485 and DC-DC
  - Logic supply (V_{DDL}): 2.25V to 5.5V
  - Power converter supply (V_{DD}): 3V to 5.5V
- RS485 compatibility on ISOW3080 and ISOW3086 with 3.3V VISOOUT.
- PROFIBUS compatibility on ISOW3080P and ISOW3086P with 5V VISOOUT.
- High-performance with integrated protection
  - Open, short, and idle bus failsafe
  - 1/8 unit load: up to 256 nodes on bus
  - Glitch-free power up and power down
- Reinforced and Basic isolation options
- High ESD bus protection
  - HBM: ±16kV
  - IEC 61000-4-2 contact discharge: ±8kV
- Operating temperature range: -55°C to 125°C
- Current limit and thermal shutdown
- 16-pin wide SOIC package
- Safety Related Certifications:
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL 1577 component recognition program
  - IEC 62368-1, IEC 61010-1, IEC 60601-1 and GB 4943.1-2011 certifications

2 Applications

- Factory automation
- Building automation
- Industrial transport
- Solar inverters, protection relay
- Motor drives

3 Description

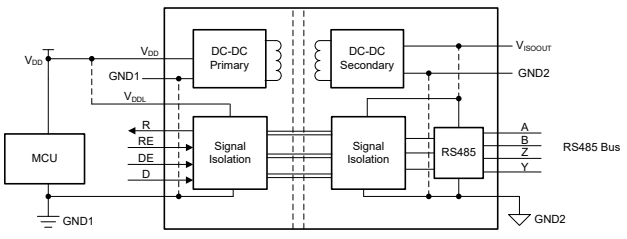
The ISOW308x devices are isolated RS-485/RS-422 transceivers with a built-in isolated DC-DC converter, that eliminates the need for a separate isolated power supply in space constrained isolated designs. The low-emissions, isolated DC-DC converter meets CISPR 32 radiated emissions Class B standard on a simple two-layer PCB.

Two options of data rates are provided: ISOW3080 is optimized for maximum 500kbps and ISOW3086 is designed for maximum 12Mbps data rate. These devices do not require any external components other than supply decoupling capacitors to realize an isolated RS-485 port, best for long distance communications. Isolation breaks the ground loop between the communicating nodes, allowing for a much larger common mode voltage range. Both signal and power paths are $5kV_{RMS}$ isolated per UL1577 and are qualified for reinforced and basic isolation per VDE, TUV and CQC. The bus pins of these devices can endure up to 16kV of HBM stress.

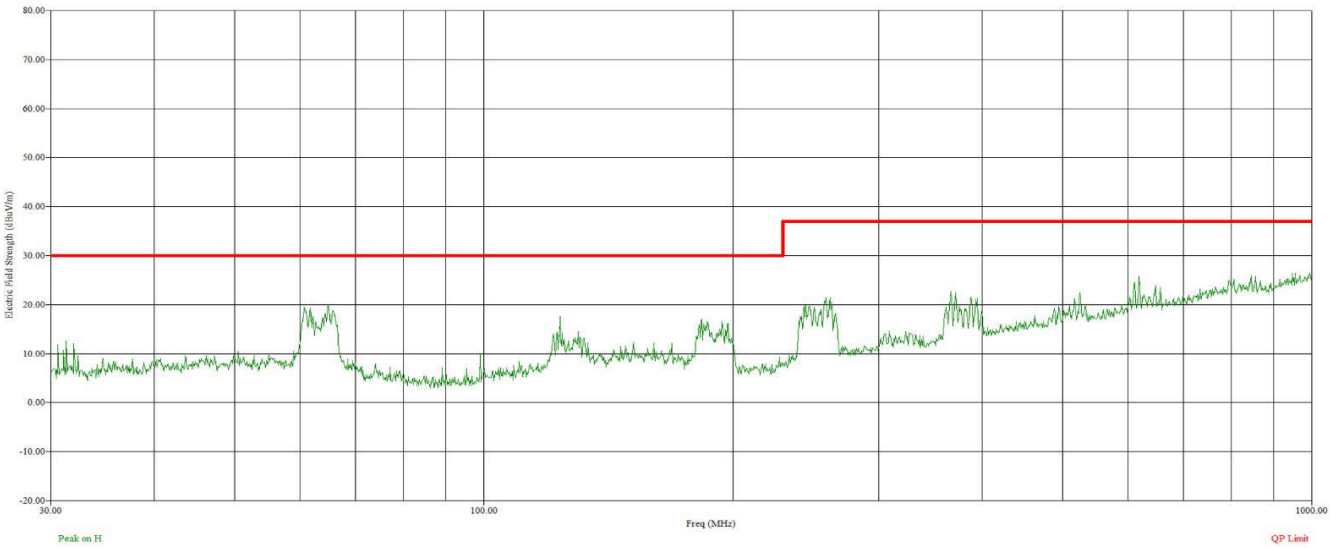
The ISOW308x can operate from a single supply voltage of 3V to 5.5V by connecting V_{DDL} and V_{DD} together on PCB. If lower logic levels are required, 2.25V to 5.5V logic supply (V_{DDL}) can be separated and independent from the power converter supply (V_{DD}) of 3V to 5.5V. These devices support a wide operating ambient temperature range from –55°C to +125°C and are available in 16-pin DWE (SOIC-16 footprint compatible package) offering a minimum of 8mm creepage and clearance.

Table 3-1. Package Information

PART NUMBER	PACKAGE	PACKAGE SIZE	BODY SIZE
ISOW3080 ISOW3086	DWE (SOIC, 16)	10.30mm × 10.30mm	10.30mm × 7.50mm
ISOW3080P ISOW3086P			



Simplified Schematic



ISOW308x CISPR-32 Class B Radiated Emission With 54Ω load

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4 Device Comparison Table

PART NUMBER	COMMUNICATION PROTOCOL	DATA RATE	VISOOUT	PACKAGE	BODY SIZE (NOM)	PACKAGE SIZE
ISOW3080	RS485	500kbps	3.3V	DWE (SOIC, 16)	10.30mm × 7.50mm	10.30mm × 10.30mm
ISOW3080P	Profibus	500kbps	5V	DWE (SOIC, 16)		
ISOW3086	RS485	12Mbps	3.3V	DWE (SOIC, 16)		
ISOW3086P	Profibus	12Mbps	5V	DWE (SOIC, 16)		

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5 Pin Configuration and Functions

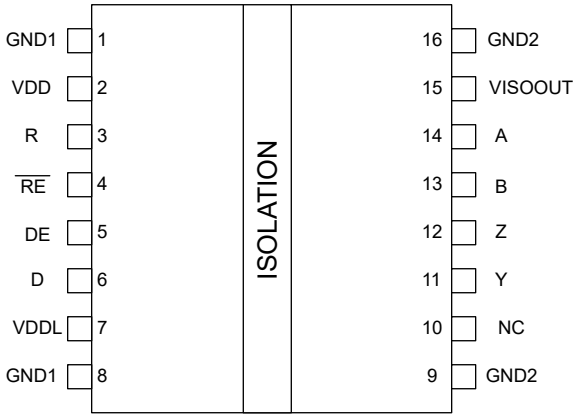

Figure 5-1. ISOW308x 16-pin DWE Top View

Table 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
V_{DDL}	7	--	Side 1 logic supply
D	6	I	Data input
DE	5	I	Driver enable. If pin is floating, driver is disabled (internal pull-down resistor)
R	3	O	Received data output
$\overline{RE}$	4	I	Receiver enable. If pin is floating, receiver buffer is disabled (internal pull-up resistor)
GND1	8	--	Ground connections for V_{DDL} and V_{DD}.
V_{DD}	2	--	Side 1 DC-DC converter power supply
GND2	16	--	Ground connection for V_{ISOOUT}.
V_{ISOOUT}	15	--	Isolated power converter output voltage.
Y	11	O	RS-485 driver non-inverting output
Z	12	O	RS-485 driver inverting output
B	13	I	RS-485 receiver inverting input
A	14	I	RS-485 receiver non-inverting input

(1) I = Input; O = Output

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{DD}	Power converter supply voltage	–0.5	6	V
V_{ISOOUT}	Isolated supply voltage, Power converter output (ISOW3080 and ISOW3086)	–0.5	6	V
V_{ISOOUT}	Isolated supply voltage, Power converter output (ISOW3080P and ISOW3086P)	–0.5	6	V
V_{DDL}	Logic supply voltage	–0.5	6	V
V_{BUS}	Voltage on bus pins (A, B, Y, Z with respect to GND2)	–12	15	V
V_{LOGIC_IO}	Logic I/O voltage level (D, DE, $\overline{RE}$, R)	–0.5	6	V
I_O	Output current on R	–15	15	mA
T_J	Junction temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground pin (GND1 or GND2). All voltage values except differential I/O bus voltages are peak voltage values.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except bus pins	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Bus pins with respect to GND2	±16000	V
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101(2)		±1500	V
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	Bus pins and GND1(across barrier)	±6500	V
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	Bus pins and GND2(same side)	±8000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD controlprocess.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD controlprocess.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{DDL}	Logic supply voltage	2.5-V, 3.3-V, and 5-V operation	2.25		5.5	V
V_{DD}	Power converter supply voltage	Power converter supply voltage (ISOW3080 and ISOW3086)	3		5.5	V
V_{DD}	Power converter supply voltage	Power converter supply voltage (ISOW3080P and ISOW3086P)	4.5		5.5	V
$V_{DD(UVLO+)}$	Positive threshold when power converter supply is rising			2.65	2.86	V
$V_{DD(UVLO-)}$	Positive threshold when power converter supply is falling		2.44	2.56		V
$V_{HYS1(UVLO)}$	Power converter supply voltage hysteresis		78			mV
$V_{DDL(UVLO+)}$	Rising threshold of logic supply voltage			1.95	2.24	V
$V_{DDL(UVLO-)}$	Falling threshold of logic supply voltage		1.6	1.78		V
$V_{HYS2(UVLO)}$	Logic supply voltage hysteresis		100			mV
V_{BUS}	Input voltage at any bus terminal (separately with respect to GND2 or common mode)		–7		12	V
V_{IH}	High-level input voltage (D, DE and $\overline{RE}$ inputs)		0.7 × V_{DDL}		V_{DDL}	V
V_{IL}	Low-level input voltage (D, DE and $\overline{RE}$ inputs)		0		0.3 × V_{DDL}	V
V_{ID}	Differential input voltage (receiver terminals A with respect to B)		–12		12	V
$I_{O(DRV)}$	Output current, driver (Y, Z)		–60		60	mA
I_O	Output current, R	V_{DDL} = 4.5 to 5.5 V	–4		4	mA
		V_{DDL} = 3 to 3.6 V	-2		2	mA
		V_{DDL} = 2.25 to 2.75 V	-1		1	mA
R_L	Differential load resistance on bus		54			Ω
$1/t_{UI}$	Signaling rate	ISOW3080 and ISOW3080P			500	kbps
$1/t_{UI}$	Signaling rate	ISOW3086 and ISOW3086P			12	Mbps
t_{pwrup}	Power up time after applying input supply(Isolated output supply reaches 90% of setpoint and data transmission can start after this)			2.2		ms
T_A	Ambient operating temperature, no extra current available on V_{ISOOUT} (ISOW3080 and ISOW3086); V_{DD} = 3V to 3.3V		–55		125	°C
T_A	Ambient operating temperature, 20 mA extra current available on V_{ISOOUT} (1) (ISOW3080 and ISOW3086); V_{DD} = 4.5V to 5.5V		–55		105	°C
T_A	Ambient operating temperature, no extra current available on V_{ISOOUT} (ISOW3080P and ISOW3086P); V_{DD} = 4.5V to 5.5V		–55		105	°C
T_A	Ambient operating temperature, 20 mA extra current available on V_{ISOOUT} (1) (ISOW3080P and ISOW3086P); V_{DD} = 4.5V to 5.5V		–55		85	°C

(1) Extra current is only available at VDD=5 V ± 10% mode

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6.4 Thermal Information

THERMAL METRIC(1)		ISOW308x DWE 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	20.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	34.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

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6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides) (ISOW3086)	V_{DD} = 3.6V, V_{DDL} = 5.5V, T_J = 150°C, Y-Z load = 54Ω||50pF, Y shorted to A, Z shorted to B(loopback), Load on R = 15pF, Input a 6MHz 50% duty cycle square wave to D pin with V_{DE} = V_{DDL}, V_{RE} = GND1, ISOW3086			624	mW
P_{D1}	Maximum power dissipation (side-1) (ISOW3086)				339	mW
P_{D2}	Maximum power dissipation by (side-2) (ISOW3086)				285	mW
P_D	Maximum power dissipation (both sides) (ISOW3086P)	V_{DD}= V_{DDL}= 5.5V, T_J=150°C, Y-Z load= 54Ω|| 50pF, Y shorted to A, Z shorted to B(loopback), Load on R=15pF, Input a 6MHz 50% duty cycle square wave to D pin with V_{DE}=V_{DDL}, V_{RE}=GND1, ISOW3086P			1420	mW
P_{D1}	Maximum power dissipation (side-1) (ISOW3086P)				710	mW
P_{D2}	Maximum power dissipation by (side-2) (ISOW3086P)				710	mW
P_D	Maximum power dissipation (both sides) (ISOW3080)	V_{DD} = 3.6V, V_{DDL} = 5.5V, T_J = 150°C, Y-Z load = 54Ω||50pF, Y shorted to A, Z shorted to B(loopback), Load on R = 15pF, Input a 250kHz 50% duty cycle square wave to D pin with V_{DE} = V_{DDL}, V_{RE} = GND1, ISOW3080			624	mW
P_{D1}	Maximum power dissipation (side-1) (ISOW3080)				339	mW
P_{D2}	Maximum power dissipation by (side-2) (ISOW3080)				285	mW
P_D	Maximum power dissipation (both sides) (ISOW3080P)	V_{DD}= V_{DDL} = 5.5V, T_J=150°C, Y-Z load= 54Ω|| 50pF, Y shorted to A, Z shorted to B(loopback), Load on R=15pF, Input a 250kHz 50% duty cycle square wave to D pin with V_{DE}=V_{DDL}, V_{RE}=GND1, ISOW3086P			1420	mW
P_{D1}	Maximum power dissipation (side-1) (ISOW3080P)				710	mW
P_{D2}	Maximum power dissipation by (side-2) (ISOW3080P)				710	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	> 8	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	> 8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance – capacitive signal isolation)	> 17	µm
		Minimum internal gap (internal clearance- transformer power isolation)	> 100	
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V_{RMS}	I-IV	
		Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN VDE V 0884-11:2017-01(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1500	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage (sine wave) Time dependent dielectric breakdown (TDDB) test	1061	V_{RMS}
		DC voltage	1500	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production)	7071	V_{PK}
V_{IMP}	Maximum impulse voltage ISOW308x	Tested in air, 1.2/50-µs waveform per IEC 62368-1	8000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage ISOW308x(3)	$V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	10400	V_{PK}
q_{pd}	Apparent charge(4)	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; ISOW308x: $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s, t_m = 10 s	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; ISOW308x: $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.4 sin (2πft), f = 1 MHz	3.5	pF
R_{IO}	Isolation resistance, input to output(5)	V_{IO} = 500 V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	Ω
		V_{IO} = 500 V at T_S = 150°C	> 10^{9}	Ω
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$ = 5000 V_{RMS}, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$ = 6000 V_{RMS}, t = 1 s (100% production)	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
(2) ISOW308x is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-terminal device

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6.7 Safety-Related Certifications

VDE	UL	TUV	CQC
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Plan to certify according to UL 1577 Component Recognition Program	Plan to certify according to GB4943.1	Plan to certify according to EN 61010-1 and EN 62368-1
Certificate planned	Certificate planned	Certificate planned	Certificate planned

6.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current(1)	$R_{\theta JA}$ = 65.5°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			345	mA
		$R_{\theta JA}$ = 65.5°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C			525	
P_S	Safety input, output, or total power(1)	$R_{\theta JA}$ = 65.5°C/W, T_J = 150°C, T_A = 25°C			1900	mW
T_S	Safety temperature(1)				150	°C

(1) The maximum safety temperature,T_S, has the same value as the maximum junction temperature,T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

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6.9 Electrical Characteristics

Over recommended operating conditions, typical values are at V_{DD} = V_{DDL} = 3.3 V and T_A =25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device						
V_{ISOOUT}	Isolated output supply voltage	ISOW308x, DE=GND1, D, $\overline{RE}$ floating	3	3.3	3.6	V
	Isolated output supply voltage	ISOW308xP, DE=GND1, D, $\overline{RE}$ floating	4.5	5	5.5	V
V_{OH}	Output high voltage on R pin	V_{DDL} = 5 V ± 10%, I_{OH} = –4 mA, IN=V_{ISOIN}	V_{DDL} – 0.4			V
		V_{DDL} = 3.3 V ± 10% , I_{OH} = –2 mA, IN=V_{ISOIN}	V_{DDL} – 0.3			V
		V_{DDL} = 2.5 V ± 10% , I_{OH} = –1 mA, IN=V_{ISOIN}	V_{DDL} – 0.2			V
V_{OL}	Output low voltage on R pin	V_{DDL} = 5 V ± 10%, I_{OL} = 4 mA, IN=GND2			0.4	V
		V_{DDL} = 3.3 V ± 10% , I_{OL} = 2 mA, IN=GND2			0.3	V
		V_{DDL} = 2.5 V ± 10%, I_{OL} = 1 mA, IN=GND2			0.2	V
Driver						
$\|V_{OD}\|$	Differential output voltage magnitude	ISOW308x : Unloaded bus, V_{DD} = 3 V to 3.6 V or ISOW308xP :Unloaded bus, V_{DD} = 4.5 V to 5.5 V	1.5		V_{ISOOUT}	V
		ISOW308x, R_L = 60 Ω, –7 V ≤ V_{TEST} ≤ 12 V (see Figure 7-1), V_{DD} = 3 V to 3.6 V	1.5		V_{ISOOUT}	
		ISOW308x, R_L = 100 Ω (see Figure 7-2) (RS-422 load), V_{DD} = 3 V to 3.6 V	2		V_{ISOOUT}	
		ISOW308x, R_L = 54 Ω (see Figure 7-2) (RS-485 load), V_{DD} = 3 V to 3.6 V	1.5		V_{ISOOUT}	
$\|V_{OD}\|$	Differential output voltage magnitude	ISOW308xP, R_L = 54 Ω, V_{DD} = 4.5 V to 5.5 V, see Figure 7-2	2.1		V_{ISOOUT}	V
$\|V_{OD}\|$	Differential output voltage magnitude	ISOW308xP, R_L = 100 Ω (see Figure 7-2) (RS-422 load), V_{DD} = 4.5 V to 5.5 V	2.1		V_{ISOOUT}	V
$\|V_{OD}\|$	Differential output voltage magnitude	ISOW308xP. R_L = 60 Ω, –7 V ≤ V_{TEST} ≤ 12 V (see Figure 7-1), VDD = 4.5 V to 5.5V	2.1		V_{ISOOUT}	V
$\Delta\|V_{OD}\|$	Change in differential output voltage between the two states	R_L = 54 Ω or 100 Ω (see Figure 7-2)	–200		200	mV
V_{OC}	Common-mode output voltage	R_L = 54 Ω or 100 Ω (see Figure 7-2)	1	0.5 × V_{ISOOUT}	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between the two states	R_L = 54 Ω or 100 Ω (see Figure 7-2)	–200		200	mV
$V_{OC(PP)}$	Peak-to-peak common mode output voltage	ISOW308x, R_L = 54 Ω or 100 Ω see Figure 7-2		400		mV
I_{OS}	Short-circuit output current	V_{DE} = V_{DDL}, V_D=V_{DDL} or GND1, –7 V ≤ Y or Z ≤ 12 V, or Y shorted to Z, see Figure 7-10		150		mA
I_I	Input current for D, DE	V_D, V_{DE} at 0 V or V_{DDL}	–25		25	µA
Receiver						
I_{I1}	Bus input current	V_{DE} = 0 V, V_{ISOIN} = 0 V or 3.3 V or 5V, ISOW3080/ISOW3080P or ISOW3086/ ISOW3086P, V_A or V_B = –7 V to 12 V, other input at 0 V	–100		125	µA
V_{TH+}	Positive-going input-threshold voltage	–7 V ≤ V_{CM} ≤ 12 V	See(1)	–78	–20	mV
$V_{TH–}$	Negative-going input-threshold voltage	–7 V ≤ V_{CM} ≤ 12 V	–200	–141	See(1)	mV
V_{hys}	Input hysteresis (V_{TH+} – $V_{TH–}$)	–7 V ≤ V_{CM} ≤ 12 V		49		mV

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Over recommended operating conditions, typical values are at V_{DD} = V_{DDL} = 3.3 V and T_A =25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Output high voltage on R pin	V_{DDL} = 5 V ± 10%, I_{OH} = –4 mA, V_{ID} ≥ 200 mV	V_{DDL} – 0.4			V
		V_{DDL} = 3.3 V ± 10%, I_{OH} = –2 mA, V_{ID} ≥ 200 mV	V_{DDL} – 0.3			
		V_{DDL} = 2.5 V ± 10% , I_{OH} = –1 mA, V_{ID} ≥ 200 mV	V_{DDL} – 0.2			
V_{OL}	Output low voltage on R pin	V_{DDL} = 5 V ± 10%, I_{OL} = 4 mA, V_{ID} ≤ –200 mV			0.4	V
		V_{DDL} = 3.3 V ± 10%, I_{OL} = 2 mA, V_{ID} ≤ –200 mV			0.3	
		V_{DDL} = 2.5 V ± 10% , I_{OL} = 1 mA, V_{ID} ≤ –200 mV			0.2	
I_{OZ}	Output high-impedance current on R pin	V_R = 0 V or V_{DDL}, $V_{\overline{RE}}$ = V_{DDL}	–1.5		1.5	µA
$I_{I(RE)}$	Input current on $\overline{RE}$ pin	$V_{\overline{RE}}$ at 0 V or V_{DDL}	–25		25	µA

(1) The V_{TH+} voltage is specified to be greater than the $V_{TH–}$ voltage by at least the V_{hys} voltage under any specific conditions.

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6.10 Supply Current Characteristics at V_{ISOOUT} = 3.3 V (ISOW308x)

over recommended operating conditions, V_{DD} = V_{DDL} = 3 to 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power converter supply current: Driver enabled, receiver disabled						
I_{DD}	Power converter supply current	V_{DE} = V_{DDL}, $V_{\overline{RE}}$ = V_{DDL}, bus load = 120 Ω, V_D= V_{DDL}, V_{DD} = 5 V ± 10%, A and B floating		51	68.5	mA
		V_{DE} = V_{DDL}, $V_{\overline{RE}}$ = V_{DDL}, bus load = 120 Ω, V_D= V_{DDL}, V_{DD} = 3.3 V ± 10%, A and B floating		67	103.5	mA
I_{DD}	Power converter supply current, ISOW3080	V_{DE} = V_{DDL}, $V_{\overline{RE}}$ = V_{DDL}, bus load = 120 Ω || 50 pF, D = 500-kbps square wave 50% duty, V_{DD} = 5 V ± 10%		55	82.5	mA
		V_{DE} = V_{DDL}, $V_{\overline{RE}}$ = V_{DDL}, bus load = 100 Ω || 50 pF, D = 500-kbps square wave 50% duty, V_{DD} = 5 V ± 10%		60	88	mA
		V_{DE} = V_{DDL}, $V_{\overline{RE}}$ = V_{DDL}, bus load = 54 Ω || 50 pF, D = 500-kbps square wave 50% duty, V_{DD} = 5 V ± 10%		80	114.5	mA
		V_{DE} = V_{DDL}, $V_{\overline{RE}}$ = V_{DDL}, bus load = 120 Ω || 50 pF, D = 500-kbps square wave 50% duty, V_{DD} = 3.3 V ± 10%		72	124	mA
		V_{DE} = V_{DDL}, $V_{\overline{RE}}$ = V_{DDL}, bus load = 100 Ω || 50 pF, D = 500-kbps square wave 50% duty, V_{DD} = 3.3 V ± 10%		79	133	mA
		V_{DE} = V_{DDL}, $V_{\overline{RE}}$ = V_{DDL}, bus load = 54 Ω || 50 pF, D = 500-kbps square wave 50% duty, V_{DD} = 3.3 V ± 10%		107	173	mA
I_{DD}	Power converter supply current, ISOW3086	V_{DE} = V_{DDL}, $V_{\overline{RE}}$ = V_{DDL} = V_{DDL}, bus load = 120 Ω || 50 pF, D = 12-Mbps square wave 50% duty, V_{DD} = 5 V ± 10%		60	86	mA
		V_{DE} = V_{DDL}, $V_{\overline{RE}}$ = V_{DDL}, bus load = 100 Ω || 50 pF, D = 12-Mbps square wave 50% duty, V_{DD} = 5 V ± 10%		65	92.5	mA
		V_{DE} = V_{DDL}, $V_{\overline{RE}}$ = V_{DDL}, bus load = 54 Ω || 50 pF, D = 12-Mbps square wave 50% duty, V_{DD} = 5 V ± 10%		87	120	mA
		V_{DE} = V_{DDL}, $V_{\overline{RE}}$ = V_{DDL}, bus load = 120 Ω || 50 pF, D = 12-Mbps square wave 50% duty, V_{DD} = 3.3 V ± 10%		80	130	mA
		V_{DE} = V_{DDL}, $V_{\overline{RE}}$ = V_{DDL}, bus load = 100 Ω || 50 pF, D = 12-Mbps square wave 50% duty, V_{DD} = 3.3 V ± 10%		87	140	mA
		V_{DE} = V_{DDL}, $V_{\overline{RE}}$ = V_{DDL}, bus load = 54 Ω || 50 pF, D = 12-Mbps square wave 50% duty, V_{DD} = 3.3 V ± 10%		116	182	mA
Power converter supply current: Driver disabled, receiver enabled						
I_{DD}	Power converter supply current, ISOW3080	V_{DE} = V_{GND1}, $V_{\overline{RE}}$ = V_{GND1}, Y and Z bus loaded and unloaded, A-B = square wave 500-kbps 50% duty V_D= V_{GND1}, V_{DD} = 5 V ± 10%, C_L on R = 15 pF		12	19	mA
		V_{DE} = V_{GND1}, $V_{\overline{RE}}$ = V_{GND1}, Y and Z bus loaded and unloaded, A-B = square wave 500-kbps 50% duty V_D= V_{GND1}, V_{DD} = 3.3 V ± 10%, C_L on R = 15 pF		15	27.5	
I_{DD}	Power converter supply current, ISOW3086	V_{DE} = V_{GND1}, $V_{\overline{RE}}$ = V_{GND1}, Y and Z bus loaded and unloaded, A-B = square wave 12-Mbps 50% duty V_D= V_{GND1}, V_{DD} = 5 V ± 10%, C_L on R = 15 pF		13	21.5	mA
		V_{DE} = V_{GND1}, $V_{\overline{RE}}$ = V_{GND1}, Y and Z bus loaded and unloaded, A-B = square wave 12-Mbps 50% duty V_D= V_{GND1}, V_{DD} = 3.3 V ± 10%, C_L on R = 15 pF		17	31.5	
Power converter supply current: Driver enabled, receiver enabled						
I_{DD}	Power converter supply current, ISOW3080	V_{DE} = V_{DDL}, $V_{\overline{RE}}$ = V_{GND1}, Y and Z bus load = 120 Ω || 50 pF, loopback(1), D = 500-kbps 50% duty, V_{DD} = 5 V ± 10%, C_L on R = 15 pF		56	84.5	mA
		V_{DE} = V_{DDL}, $V_{\overline{RE}}$ = V_{GND1}, Y and Z bus load = 120 Ω || 50 pF, loopback(1), D = 500-kbps 50% duty, V_{DD} = 3.3 V ± 10%, C_L on R = 15 pF		76	127.5	

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over recommended operating conditions, V_{DD} = V_{DDL} = 3 to 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Power converter supply current, ISOW3086	V_{DE} = V_{DDL}, $V_{\overline{RE}}$ = V_{GND1}, Y and Z bus load = 120 Ω || 50 pF, loopback(1), D = 12-Mbps 50% duty, V_{DD} = 5 V ± 10%, C_L on R = 15 pF		63	90.5	mA
		V_{DE} = V_{DDL}, $V_{\overline{RE}}$ = V_{GND1}, Y and Z bus load = 120 Ω || 50 pF, loopback(1), D = 12-Mbps 50% duty, V_{DD} = 3.3 V ± 10%, C_L on R = 15 pF		84	137	
Logic supply current: Driver disabled, receiver disabled						
I_{DDL}	Logic supply current	V_{DE} = V_{GND1}, $V_{\overline{RE}}$ = V_{DDL} , V_D = V_{DDL}, V_{DDL}= 3.3 V ± 10%		3.3	4.6	mA
Logic supply current: Driver enabled, Receiver enabled, static						
I_{DDL}	Logic supply current	V_{DE} = V_{DDL}, $V_{\overline{RE}}$ = V_{GND1}, V_D = V_{DDL}, loopback(1), V_{DDL}= 3.3 V ± 10%		5.3	6.6	mA
Logic supply current: Driver enabled, receiver enabled, dynamic						
I_{DDL}	Logic supply current, ISOW3080	V_{DE} = V_{DDL}, $V_{\overline{RE}}$ = V_{GND1}, D = 500-kbps 50% duty square wave, loopback(1), V_{DDL} = 3.3 V ± 10%		6.1	7.6	mA
I_{DDL}	Logic supply current, ISOW3086	V_{DE} = V_{DDL}, $V_{\overline{RE}}$ = V_{GND1} , D = 12-Mbps 50% duty square wave, loopback(1), V_{DDL} = 3.3 V ± 10%		6.2	8	mA

(1) The output of the driver is connected to the input of a receiver in a loopback mode.

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6.11 Supply Current Characteristics at V_{ISOOUT} = 5 V (ISOW308xP)

over recommended operating conditions, V_{DD} = V_{DDL} = 4.5V to 5.5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power converter supply current: Driver enabled, receiver disabled						
I_{DD}	Power converter supply current	V_{DE} = V_{DDL}, $V_{\overline{RE}}$ = V_{DDL}, bus load = 120 Ω, V_D= V_{DDL}, V_{DD} = 5 V ± 10%, A and B floating		93	137	mA
I_{DD}	Power converter supply current, ISOW3080P	V_{DE} = V_{DDL}, $V_{\overline{RE}}$ = V_{DDL}, bus load = 120 Ω || 50 pF, D = 500-kbps square wave 50% duty, V_{DD} = 5 V ± 10%		113	188	mA
		V_{DE} = V_{DDL}, $V_{\overline{RE}}$ = V_{DDL}, bus load = 100 Ω || 50 pF, D = 500-kbps square wave 50% duty, V_{DD} = 5 V ± 10%		124	201	mA
		V_{DE} = V_{DDL}, $V_{\overline{RE}}$ = V_{DDL}, bus load = 54 Ω || 50 pF, D = 500-kbps square wave 50% duty, V_{DD} = 5 V ± 10%		167	257	mA
I_{DD}	Power converter supply current, ISOW3086P	V_{DE} = V_{DDL}, $V_{\overline{RE}}$ = V_{DDL} = V_{DDL}, bus load = 120 Ω || 50 pF, D = 12-Mbps square wave 50% duty, V_{DD} = 5 V ± 10%		110	169	mA
		V_{DE} = V_{DDL}, $V_{\overline{RE}}$ = V_{DDL}, bus load = 100 Ω || 50 pF, D = 12-Mbps square wave 50% duty, V_{DD} = 5 V ± 10%		121	185	mA
		V_{DE} = V_{DDL}, $V_{\overline{RE}}$ = V_{DDL}, bus load = 54 Ω || 50 pF, D = 12-Mbps square wave 50% duty, V_{DD} = 5 V ± 10%		168	250	mA
Power converter supply current: Driver disabled, receiver enabled						
I_{DD}	Power converter supply current, ISOW3080P	V_{DE} = V_{GND1}, $V_{\overline{RE}}$ = V_{GND1}, Y and Z bus loaded and unloaded, A-B = square wave 500-kbps 50% duty V_D= V_{GND1}, V_{DD} = 5 V ± 10%, C_L on R = 15 pF		14	26	mA
I_{DD}	Power converter supply current, ISOW3086P	V_{DE} = V_{GND1}, $V_{\overline{RE}}$ = V_{GND1}, Y and Z bus loaded and unloaded, A-B = square wave 12-Mbps 50% duty V_D= V_{GND1}, V_{DD} = 5 V ± 10%, C_L on R = 15 pF		18	31.5	mA
Power converter supply current: Driver enabled, receiver enabled						
I_{DD}	Power converter supply current, ISOW3080P	V_{DE} = V_{DDL}, $V_{\overline{RE}}$ = V_{GND1}, Y and Z bus load = 120 Ω || 50 pF, loopback(1), D = 500-kbps 50% duty, V_{DD} = 5 V ± 10%, C_L on R = 15 pF		115	191	mA
I_{DD}	Power converter supply current, ISOW3086P	V_{DE} = V_{DDL}, $V_{\overline{RE}}$ = V_{GND1}, Y and Z bus load = 120 Ω || 50 pF, loopback(1), D = 12-Mbps 50% duty, V_{DD} = 5 V ± 10%, C_L on R = 15 pF		115	178	mA
Logic supply current: Driver disabled, receiver disabled						
I_{DDL}	Logic supply current	V_{DE} = V_{GND1}, $V_{\overline{RE}}$ = V_{DDL} , V_D = V_{DDL}, V_{DDL}= 3.3 V ± 10%		3.1	4.6	mA
Logic supply current: Driver enabled, Receiver enabled, static						
I_{DDL}	Logic supply current	V_{DE} = V_{DDL}, $V_{\overline{RE}}$ = V_{GND1}, V_D = V_{DDL}, loopback(1), V_{DDL}= 3.3 V ± 10%		4.9	6.6	mA
Logic supply current: Driver enabled, receiver enabled, dynamic						
I_{DDL}	Logic supply current, ISOW3080P	V_{DE} = V_{DDL}, $V_{\overline{RE}}$ = V_{GND1}, D = 500-kbps 50% duty square wave, loopback(1), V_{DDL} = 3.3 V ± 10%		5.8	7.6	mA
I_{DDL}	Logic supply current, ISOW3086P	V_{DE} = V_{DDL}, $V_{\overline{RE}}$ = V_{GND1} , D = 12-Mbps 50% duty square wave, loopback(1), V_{DDL} = 3.3 V ± 10%		6.2	8	mA

(1) The output of the driver is connected to the input of a receiver in a loopback mode.

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6.12 Switching Characteristics at V_{ISOOUT} = 3.3 V (ISOW308x)

Min / Max specifications are over recommended operating conditions, typical values are at V_{DD} = V_{DDL} = 3.3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver: 500-kbps device (ISOW3080)						
t_r, t_f	Differential output rise time and fall time	R_L = 54 Ω, C_L = 50 pF, see Figure 7-3	190	270	600	ns
t_{PHL}, t_{PLH}	Propagation delay	R_L = 54 Ω, C_L = 50 pF, see Figure 7-3		400	610	ns
PWD	Pulse width distortion(1), $\lvert t_{PHL} - t_{PLH} \rvert$	R_L = 54 Ω, C_L = 50 pF, see Figure 7-3		6.5	40	ns
t_{PHZ}, t_{PLZ}	Disable time	See Figure 7-5 and Figure 7-6		57	200	ns
t_{PZH}, t_{PZL}	Enable time	See Figure 7-5 and Figure 7-6		220	600	ns
Receiver: 500-kbps device (ISOW3080)						
t_r, t_f	Output rise time and fall time	C_L = 15 pF, see Figure 7-7			5.6	ns
t_{PHL}, t_{PLH}	Propagation delay	C_L = 15 pF, see Figure 7-7		80	175	ns
PWD	Pulse width distortion(1), $\lvert t_{PHL} - t_{PLH} \rvert$	C_L = 15 pF, see Figure 7-7		1.5	15	ns
t_{PHZ}, t_{PLZ}	Disable time	See Figure 7-8 and Figure 7-9		8	30	ns
t_{PZH}, t_{PZL}	Enable time	See Figure 7-8 and Figure 7-9		6	30	ns
Driver: 12-Mbps device (ISOW3086)						
t_r, t_f	Differential output rise time and fall time	R_L = 54 Ω, C_L = 50 pF, see Figure 7-3	6	15	25	ns
t_{PHL}, t_{PLH}	Propagation delay	R_L = 54 Ω, C_L = 50 pF, see Figure 7-3		51	125	ns
PWD	Pulse width distortion(1), $\lvert t_{PHL} - t_{PLH} \rvert$	R_L = 54 Ω, C_L = 50 pF, see Figure 7-3		2	12	ns
t_{PHZ}, t_{PLZ}	Disable time	See Figure 7-5 and Figure 7-6		31	125	ns
t_{PZH}, t_{PZL}	Enable time	See Figure 7-5 and Figure 7-6		34	110	ns
Receiver: 12-Mbps device (ISOW3086)						
t_r, t_f	Output rise time and fall time	C_L = 15 pF, see Figure 7-7			6	ns
t_{PHL}, t_{PLH}	Propagation delay	C_L = 15 pF, see Figure 7-7		80	160	ns
PWD	Pulse width distortion(1), $\lvert t_{PHL} - t_{PLH} \rvert$	C_L = 15 pF, see Figure 7-7		2	10	ns
t_{PHZ}, t_{PLZ}	Disable time	See Figure 7-8 and Figure 7-9		8	30	ns
t_{PZH}, t_{PZL}	Enable time	See Figure 7-8 and Figure 7-9		6	30	ns

(1) Also known as pulse skew.

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6.13 Switching Characteristics at V_{ISOOUT} = 5 V (ISOW308xP)

Min / Max specifications are over recommended operating conditions, typical values are at V_{DD} = V_{DDL} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver: 500-kbps device (ISOW3080P)						
t_r, t_f	Differential output rise time and fall time	R_L = 54 Ω, C_L = 50 pF, see Figure 7-3	200	300	600	ns
t_{PHL}, t_{PLH}	Propagation delay	R_L = 54 Ω, C_L = 50 pF, see Figure 7-3		350	610	ns
PWD	Pulse width distortion(1), $\lvert t_{PHL} - t_{PLH} \rvert$	R_L = 54 Ω, C_L = 50 pF, see Figure 7-3		4.5	40	ns
t_{PHZ}, t_{PLZ}	Disable time	See Figure 7-5 and Figure 7-6		54	200	ns
t_{PZH}, t_{PZL}	Enable time	See Figure 7-5 and Figure 7-6		160	600	ns
Receiver: 500-kbps device (ISOW3080P)						
t_r, t_f	Output rise time and fall time	C_L = 15 pF, see Figure 7-7			6	ns
t_{PHL}, t_{PLH}	Propagation delay	C_L = 15 pF, see Figure 7-7		80	175	ns
PWD	Pulse width distortion(1), $\lvert t_{PHL} - t_{PLH} \rvert$	C_L = 15 pF, see Figure 7-7		2.5	20	ns
t_{PHZ}, t_{PLZ}	Disable time	See Figure 7-8 and Figure 7-9		8	30	ns
t_{PZH}, t_{PZL}	Enable time	See Figure 7-8 and Figure 7-9		6	30	ns
Driver: 12-Mbps device (ISOW3086P)						
t_r, t_f	Differential output rise time and fall time	R_L = 54 Ω, C_L = 50 pF, see Figure 7-3	4	8.5	18	ns
t_{PHL}, t_{PLH}	Propagation delay	R_L = 54 Ω, C_L = 50 pF, see Figure 7-3		37	125	ns
PWD	Pulse width distortion(1), $\lvert t_{PHL} - t_{PLH} \rvert$	R_L = 54 Ω, C_L = 50 pF, see Figure 7-3		1.5	10	ns
t_{PHZ}, t_{PLZ}	Disable time	See Figure 7-5 and Figure 7-6		26	125	ns
t_{PZH}, t_{PZL}	Enable time	See Figure 7-5 and Figure 7-6		33	150	ns
Receiver: 12-Mbps device (ISOW3086P)						
t_r, t_f	Output rise time and fall time	C_L = 15 pF, see Figure 7-7			6	ns
t_{PHL}, t_{PLH}	Propagation delay	C_L = 15 pF, see Figure 7-7		80	160	ns
PWD	Pulse width distortion(1), $\lvert t_{PHL} - t_{PLH} \rvert$	C_L = 15 pF, see Figure 7-7		2.5	10	ns
t_{PHZ}, t_{PLZ}	Disable time	See Figure 7-8 and Figure 7-9		8	30	ns
t_{PZH}, t_{PZL}	Enable time	See Figure 7-8 and Figure 7-9		6	30	ns

(1) Also known as pulse skew.

ADVANCE INFORMATION

7 Parameter Measurement Information

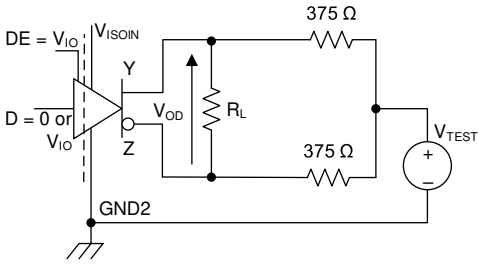
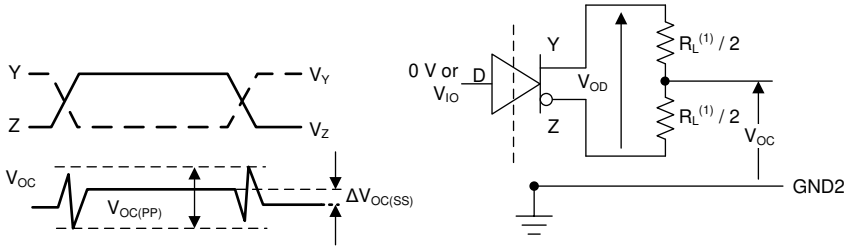
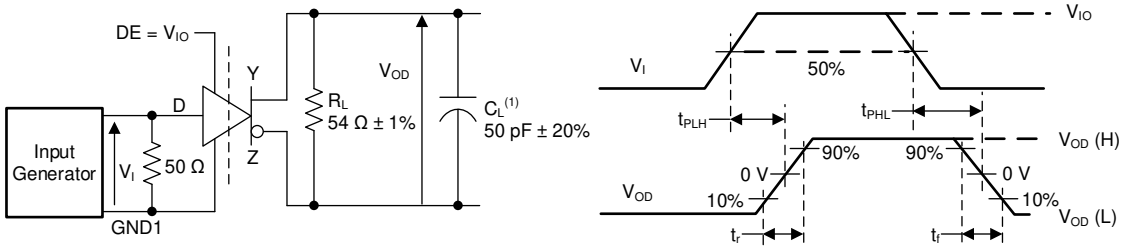


Figure 7-1. Driver Voltages



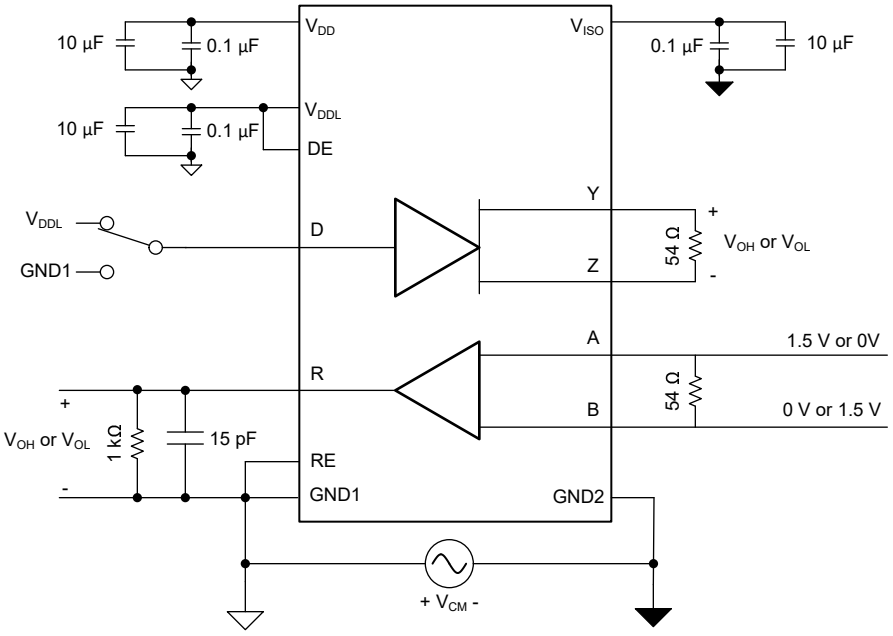
A. R_L = 100Ω for RS-422, R_L = 54Ω for RS-485

Figure 7-2. Driver Voltages



A. C_L includes fixture and instrumentation capacitance

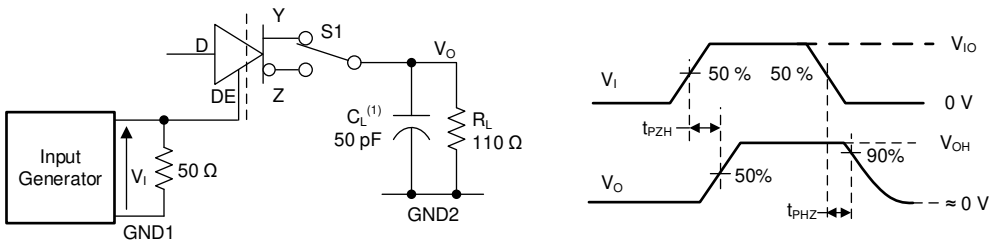
Figure 7-3. Driver Switching Specifications



A. Includes probe and fixture capacitance

B. Pass-fail criteria: Device is tested in both half-duplex and full-duplex conditions. Both the signal path and power path must be in specification compliant region during the application of CMTI pulse. This means no bit flips on R, and both V_{ISOOUT} and Driver V_{OD} must be within specifications mentioned in electrical characteristics table.

Figure 7-4. Common Mode Transient Immunity (CMTI)—Full Duplex



A. C_L includes fixture and instrumentation capacitance

Figure 7-5. Driver Enable and Disable Times

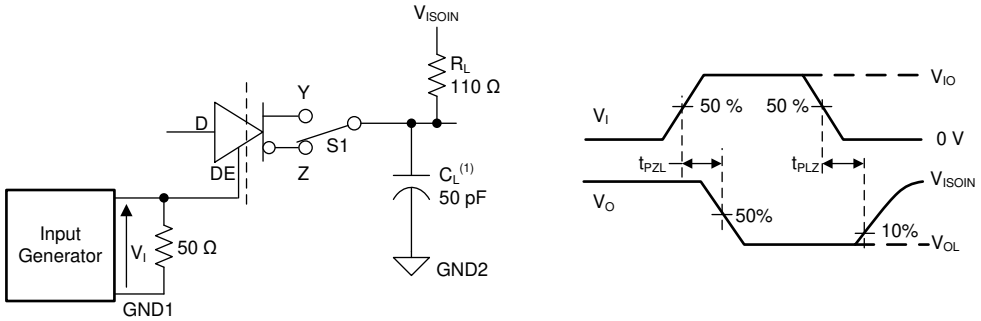
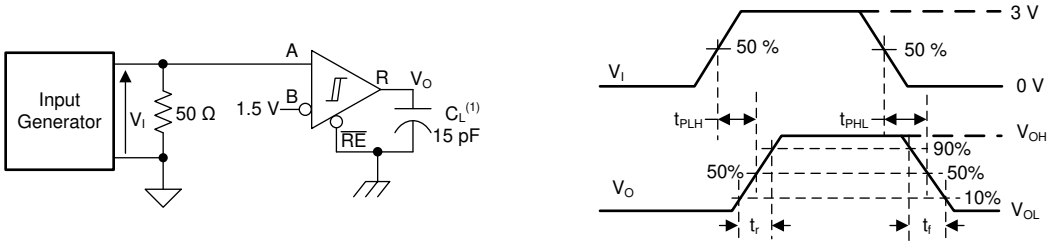


Figure 7-6. Driver Enable and Disable Times

ADVANCE INFORMATION



A. C_L includes fixture and instrumentation capacitance

Figure 7-7. Receiver Switching Specifications

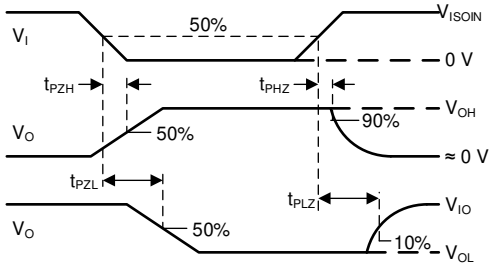


Figure 7-8. Receiver Enable and Disable Times

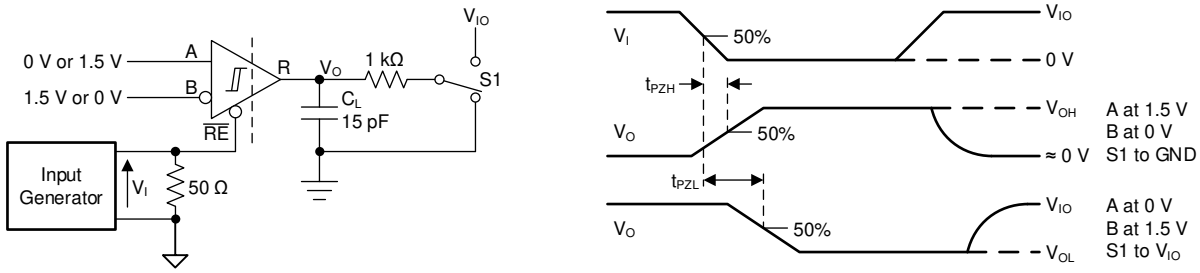
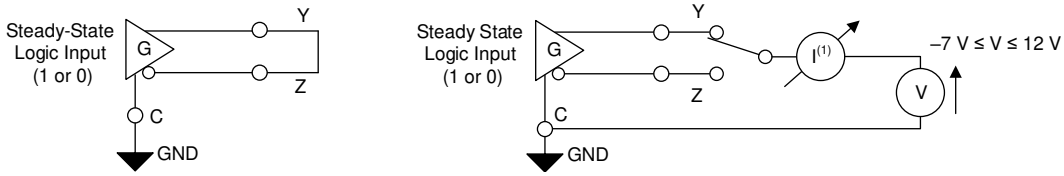


Figure 7-9. Receiver Enable and Disable Times



A. The driver must not sustain any damage with this configuration

Figure 7-10. Short-Circuit Current Limiting

ADVANCE INFORMATION

8 Detailed Description

8.1 Overview

The ISOW308x family of devices has signal isolation channels, power isolation with integrated transformer and RS-485 transceiver all integrated in one package. ISOW3080 supports maximum signaling rate up to 500kbps, while ISOW3086 is designed for 12Mbps maximum data rate. Figure 10-1 shows functional block diagram of ISOW308x family of devices.

8.2 Power Isolation

The integrated isolated DC-DC converter uses advanced circuit and on-chip layout techniques to reduce radiated emissions and achieve up to 43.5% typical efficiency. The integrated transformer uses thin film polymer as the insulation barrier. Output voltage of power converter can be either 3.3V or 5V based on the chosen orderable part number. The output voltage, V_{ISOOUT}, is monitored and feedback information is conveyed to the primary side. The duty cycle of the primary switching stage is adjusted accordingly. The fast feedback control loop of the power converter provides low overshoots and undershoots during load transients. Undervoltage lockout (UVLO) with hysteresis is integrated on the V_{DDL}, V_{DD} and V_{ISOOUT} supplies which verifies robust fails-safe system performance under noisy conditions. An integrated soft-start mechanism provides controlled inrush current and avoids any overshoot on the output during power up.

8.3 Signal Isolation

The integrated signal isolation channels employ an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon-dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one state and sends no signal to represent the other state. The receiver demodulates the signal after signal conditioning and produces the output through a buffer stage. The signal-isolation channels incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions from the high frequency carrier and IO buffer switching. Figure 8-2 shows a functional block diagram of a typical signal isolation channel.

To keep any noise coupling from power converter away from signal path, power supplies on side1 for power converter (V_{DD}) and signal path(V_{DDL}) are kept separate. Power converter output (V_{ISOOUT}) is internally connected to power supply of RS-485 transceiver die.

8.4 RS-485

In a typical RS-485 network, multiple nodes can be connected on the bus and the distance of communicating nodes can be as far as 4000 to 5000 feet. While communicating at such large distances, usual common mode of non-isolated RS-485 transceiver is not sufficient. ISOW308x has integrated isolation barrier with up to 1500Vpk working voltage rating. Isolation breaks the ground loop between the communicating nodes and allows for data transfer in the presence of large ground potential differences. These devices have a higher typical differential output voltage (V_{OD}) than traditional transceivers for better noise immunity. For ISOW3080P / ISOW3086P - V_{ISOOUT} = 5V and a minimum differential output voltage of 2.1V, which meets the requirements for PROFIBUS applications.

The ISOW308x family of devices is designed for applications that have limited board space and require more integration. Only external bypass capacitors are needed to fully realize an isolated RS-485 port. These family of devices are also built for very-high voltage applications, where power transformers for discrete isolated supply meeting the required isolation specifications are bulky and expensive. Though the device family is full-duplex, the device can also be used for half-duplex applications by connecting driver output (Y , Z) to receiver input (A , B) on PCB - this helps to reduce cabling costs. For more details, refer to Application Information.

ADVANCE INFORMATION

8.5 Functional Block Diagram

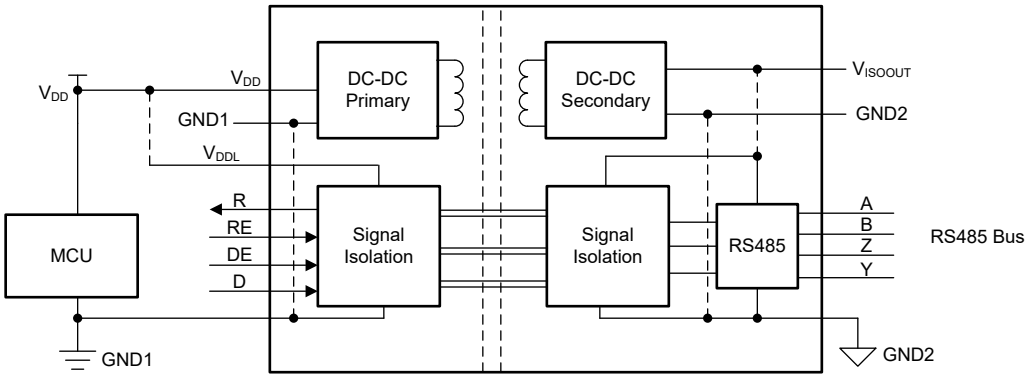


Figure 8-1. Block Diagram

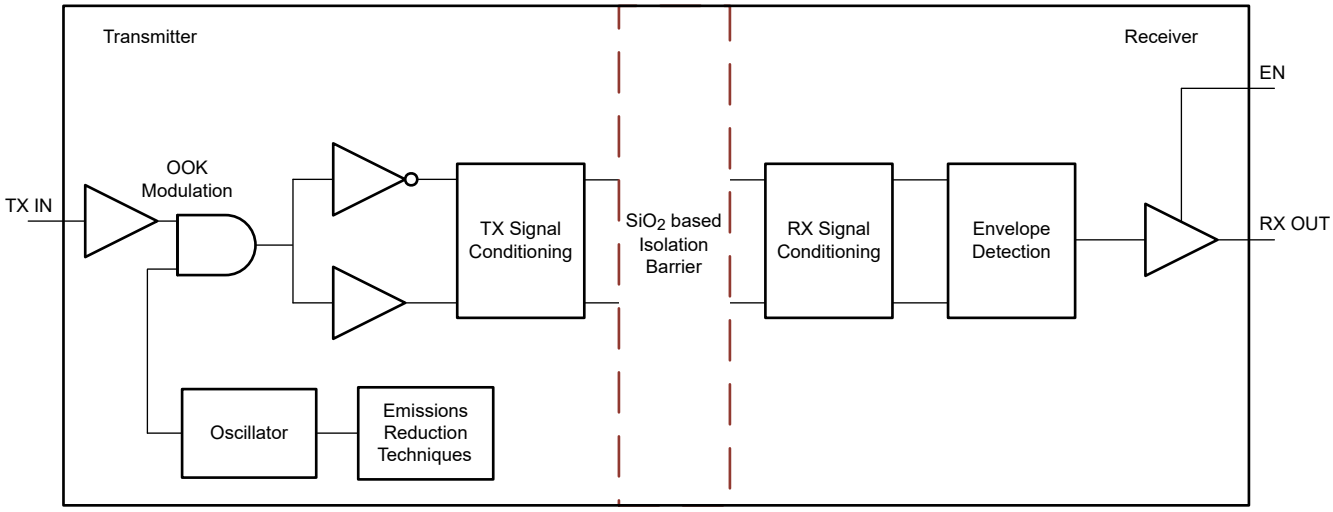


Figure 8-2. Signal Isolation Channel

ADVANCE INFORMATION

8.6 Feature Description

8.6.1 Power-Up and Power-Down Behavior

The ISOW308x family of has built-in under-voltage lockout (UVLO) on all supplies (V_{DD}, V_{DDL} and V_{ISOOUT}) with positive-going and negative-going thresholds and hysteresis. Both the power converter supply (V_{DD}) and Logic supply (V_{DDL}) need to be present for the device to work. If either of them is below the UVLO, both the signal path and the power converter are disabled.

Assuming V_{DDL} is above UVLO+, when the V_{DD} voltage crosses the positive-going UVLO threshold during power-up, the DC-DC converter initializes and the power converter duty cycle is increased in a controlled manner. This soft-start scheme limits primary peak currents drawn from the V_{DD} supply and charges the V_{ISOOUT} output in a controlled manner, avoiding overshoots. RS-485 driver output is in high impedance state in this duration. When the UVLO positive-going threshold is crossed on the secondary side V_{ISOOUT} pin, the feedback channel starts providing feedback to the primary controller. The regulation loop takes over and RS-485 drive output, Received data output R takes the respective state defined by the inputs to the device, such as the Driver enable (DE), Driver data to be transmitted D and Receiver enable $\overline{RE}$. Designers must consider a sufficient time margin (typically 2.5ms with 10µF load capacitance) to allow this power up sequence before any usable system functionality.

When either of V_{DD} or V_{DDL} is lost, the primary side DC-DC controller turns off when the UVLO lower threshold is reached. The V_{ISOOUT} capacitor then discharges depending on the isolation channels and RS-485 load.

8.6.2 Protection Features

The ISOW308x family of devices have multiple protection features to create a robust system level design.

- These devices are protected against output overload and short circuit. In cases of overload or short on power converter output V_{ISOOUT}, maximum duty cycle of power converter is limited. In cases of driver bus short circuit due to the external power supply cable shorting to the bus cable, or due to bus contention, short circuit current protection on RS-485 chip restricts the bus current to ±250mA maximum.
- Thermal protection is also integrated to help prevent the device from getting damaged under such scenarios. An increase in the die temperature is monitored and the device is disabled when the die temperature becomes 165℃ (typical), thus disabling the short condition. The device is re-enabled when the junction temperature becomes 155℃ (typical). If an overload or output short-circuit condition prevails, this protection cycle is repeated. Take care in the system design to prevent repeated or prolonged exposure to bus shorts as this exposes the device to high junction temperatures for extreme amounts of time affecting device reliability.

8.6.3 Failsafe Receiver

The differential receiver of the ISOW308x has failsafe protection from invalid bus states caused by:

- Open bus conditions such as a broken cable or a disconnected connector
- Shorted bus conditions such as insulation breakdown of a cable that shorts the twisted-pair
- Idle bus conditions that occur when no driver on the bus is actively driving.

The differential input of the RS-485 receiver is 0 in any of these conditions for a terminated transmission line. The receiver outputs a failsafe logic-high state on R pin so that the output of the receiver is determinate. The receiver thresholds are offset in the receiver design so that the indeterminate range does not include a 0V differential. See Receiver functional table for more details.

8.6.4 Glitch-Free Power Up and Power Down

Communication on the bus that already exist between a controller node and target node in an RS-485 network must not be disturbed when a new node is swapped in or out of the network. Glitches do not occur on the bus when the device is:

- Hot plugged into the network in an unpowered state
- Hot plugged into the network in a powered state and disabled state
- Powered up or powered down in a disabled state when already connected to the bus

ADVANCE INFORMATION

The ISOW308x devices meet above criteria and do not cause any false data toggling on the bus when powered up or powered down in a disabled state with supply ramp rates ≥ 50µs.

8.7 Device Functional Modes

Table 8-1 lists the supply configuration for these devices:

Table 8-1. Supply Configuration Function Table

INPUTS		OUTPUT
V_{DD} (1)	V_{DDL}	V_{ISOOUT} Section 6.3
< $V_{DD(UVLO+)}$	>$V_{DDL(UVLO+)}$	OFF
>$V_{DD(UVLO+)}$	<$V_{DDL(UVLO+)}$	ON

(1) V_{DD}= 3.3V for Profibus devices (ISOW3080P and ISOW3086P) is an invalid operation and is not supported

Table 8-2 shows the driver functional modes:

Table 8-2. Driver Functional Table

INPUTS				OUTPUTS	
V_{DD} (1)	V_{DDL}	D	DE	Y, A	Z, B
PU	PU	H	H	H	L
		L	H	L	H
		X	L	Hi-Z	Hi-Z
		X	Open	Hi-Z	Hi-Z
		Open	H	H	L
PD	PU	X	X	Hi-Z	Hi-Z
PU	PD(2)	X	X	Invalid Operation	

(1) PU=Powered up, PD=Powered down; H=high level; L=Low level; X=Irrelevant; Hi-Z=High impedance state
(2) A strongly driven input signal on D, DE or RE can weakly power the floating V_{DDL} through an internal protection diode and cause an undetermined output.

When the driver enable pin, DE, is logic high, the differential outputs, Y and Z, follow the logic states at data input, D. A logic high at the D input causes the Y output to go high and the Z output to go low. Therefore the differential output voltage defined by Equation 1 is positive.

$$V_{OD} = V_Y - V_Z \quad (1)$$

A logic low at the D input causes the Z output to go high and the Y output to go low. Therefore the differential output voltage defined by Equation 1 is negative. A logic low at the DE input causes both outputs to go to the high-impedance (Hi-Z) state. The logic state at the D pin is irrelevant when the DE input is logic low. The DE pin has an internal pulldown resistor to ground. The driver is disabled (bus outputs are in the Hi-Z) by default when the DE pin is left open. The D pin has an internal pullup resistor. The Y output goes high and the Z output goes low when the D pin is left open while the driver enabled.

Table 8-3 shows the receiver functional modes:

ADVANCE INFORMATION

Table 8-3. Receiver Functional Table

INPUTS				OUTPUT
V_{DD} (1)	V_{DDL}	Differential Input $V_{ID} = V_A - V_B$	$\overline{RE}$	R
PU	PU	$V_{ID} > V_{IT+}$	L	H
		$V_{IT-} < V_{ID} < V_{IT+}$	L	Indeterminate
		$V_{ID} < V_{IT-}$	L	L
		X	H	Hi-Z
		X	Open	Hi-Z
		Open, Short, Idle	L	H
PD	PU	X	X	Hi-Z
PU	PD(2)	X	X	Invalid Operation

(1) PU=Powered up, PD=Powered down; H=high level; L=Low level; X=Irrelevant; Hi-Z=High impedance state
(2) A strongly driven input signal on D, DE or $\overline{RE}$ can weakly power the floating V_{DDL} through an internal protection diode and cause an undetermined output.

The receiver is enabled when the receiver enable pin, $\overline{RE}$, is logic low. The receiver output, R, goes high when the differential input voltage defined by Equation 2 is greater than the positive input threshold, V_{TH+}.

$$V_{ID} = V_A - V_B \quad (2)$$

The receiver output, R, goes low when the differential input voltage defined by Equation 2 is less than the negative input threshold, V_{TH-} . If the V_{ID} voltage is between the V_{TH+} and V_{TH-} thresholds, the output is indeterminate. The receiver output is in the Hi-Z state and the magnitude and polarity of V_{ID} are irrelevant when the $\overline{RE}$ pin is logic high or left open. The internal biasing of the receiver inputs causes the output to go to a failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

ADVANCE INFORMATION

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISOW308x devices are designed for bidirectional data transfer on multipoint RS-485 networks. An RS-485 bus has multiple transceivers that connect in parallel to a bus cable. Both cable ends are terminated with a termination resistor, R_T, to remove line reflections. The value of R_T matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, lets higher data rates be used over a longer cable length.

Full-duplex implementation requires two signal pairs (four wires). Full-duplex implementation lets each node to transmit data on one pair while simultaneously receiving data on the other pair.

Driver outputs Y and Z are shorted to A and B respectively. This reduces overall cabling requirements. Also DE/RE are shorted to each other, and at a time, any node acts as either a driver or a receiver. Split termination in this configuration helps to boost network immunity in noisy environments by providing common-mode noise filtering and also reduces radiated emissions by providing low impedance path to earth to the bus common mode excursions.

9.2 Typical Application

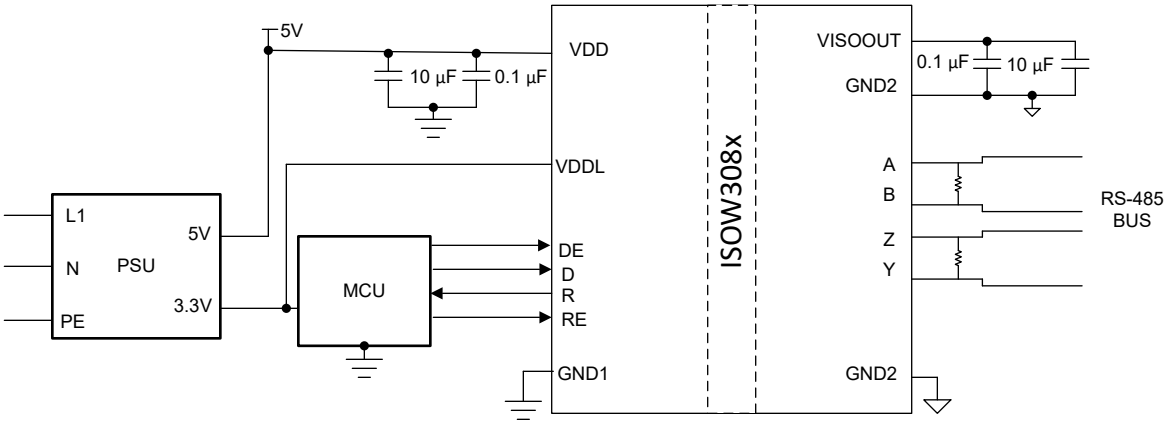


Figure 9-1. Application circuit for ISOW308x

9.2.1 Design Requirements

Unlike an optocoupler-based design, which requires several external components to improve performance, provide bias, or limit current, the ISOW308x only require external bypass capacitors to operate as shown in above application diagram. Because of high peak currents flowing through V_{DD} and V_{ISOOUT} supplies, bulk capacitance of minimum 10µF is recommended on both pins. Higher values of bulk capacitors (nearly100uF) attenuates noise and ripple further, enhancing performance. Better to select bulk capacitors of DC bias rating greater than 25V to prevent capacitor derating.

9.2.2 Detailed Design Procedure

The RS-485 bus is a robust electrical interface designed for long-distance communications. The RS-485 interface can be used in a wide range of applications with varying requirements of distance of communication, data rate, and number of nodes.

ADVANCE INFORMATION

9.2.2.1 *Data Rate, Bus Length and Bus Loading*

The RS-485 standard has typical curves similar to those shown in Figure 9-2. These curves show the inverse relationship between signaling rate and cable length. If the data rate of the payload between two nodes is lower, the cable length between the nodes can be longer. Use below Figure as a guideline for cable selection, data rate, cable length and subsequent jitter budgeting.

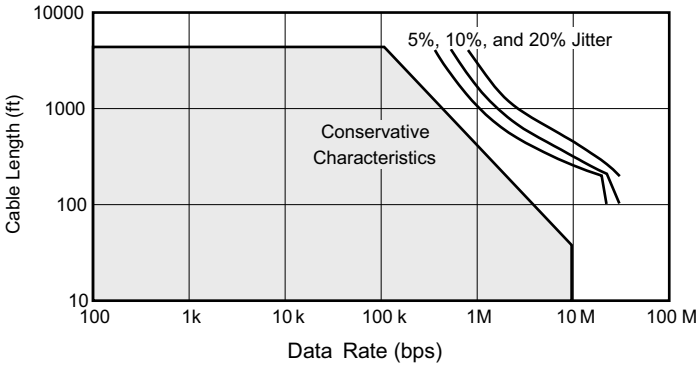


Figure 9-2. Cable length vs Data rate characteristics

The current supplied by the driver must supply into a load because the output of the driver depends on this current. Add transceivers to the bus to increase the total bus loading. The RS-485 standard specifies a hypothetical term of a unit load (UL) to estimate the maximum number of possible bus loads. The UL represents a load impedance of approximately 12kΩ. Standard-compliant drivers must be able to drive 32 of these ULs. The ISOW308x devices has 1/8 UL impedance transceiver and can connect up to 256 nodes to the bus.

9.2.2.2 *Stub Length*

In an RS-485 network, the distance between the transceiver inputs and the cable trunk is known as the stub. The stub must be as short as possible when a node is connected to the bus. Stubs are a non-terminated piece of bus line that can introduce reflections of varying phase as the length of the stub increases. The electrical length, or round-trip delay, of a stub must be less than one-tenth of the rise time of the driver as a general guideline. Therefore, the maximum physical stub length (L(STUB)) is calculated as shown in Equation 3.

$$L(STUB) \leq 0.1 \times tr \times v \times c \quad (3)$$

where:

- tr is the 10/90 rise time of the driver.
- c is the speed of light (3 × 108m/s).
- v is the signal velocity of the cable or trace as a factor of c.

ADVANCE INFORMATION

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Digital Isolator Design Guide*
- Texas Instruments, *Isolation Glossary*

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

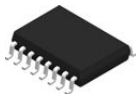
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 5, 2026 to March 4, 2026 (from Revision * (February 2026) to Revision A (March 2026))	Page
• Updated spacing in the *Safety Limiting Values* table notes	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

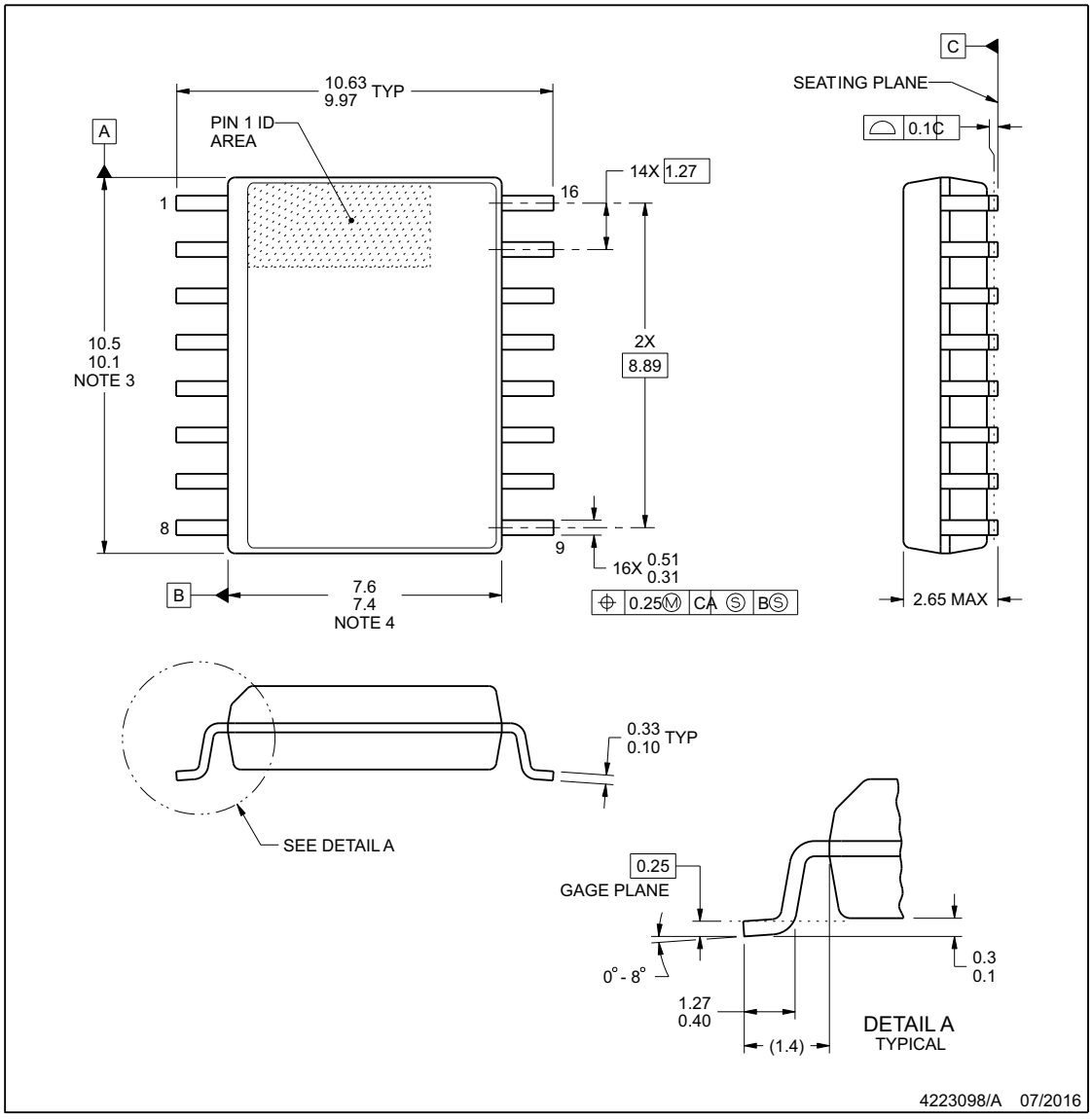


PACKAGE OUTLINE

DWE0016A

SOIC - 2.65 mm max height

SOIC



NOTES:

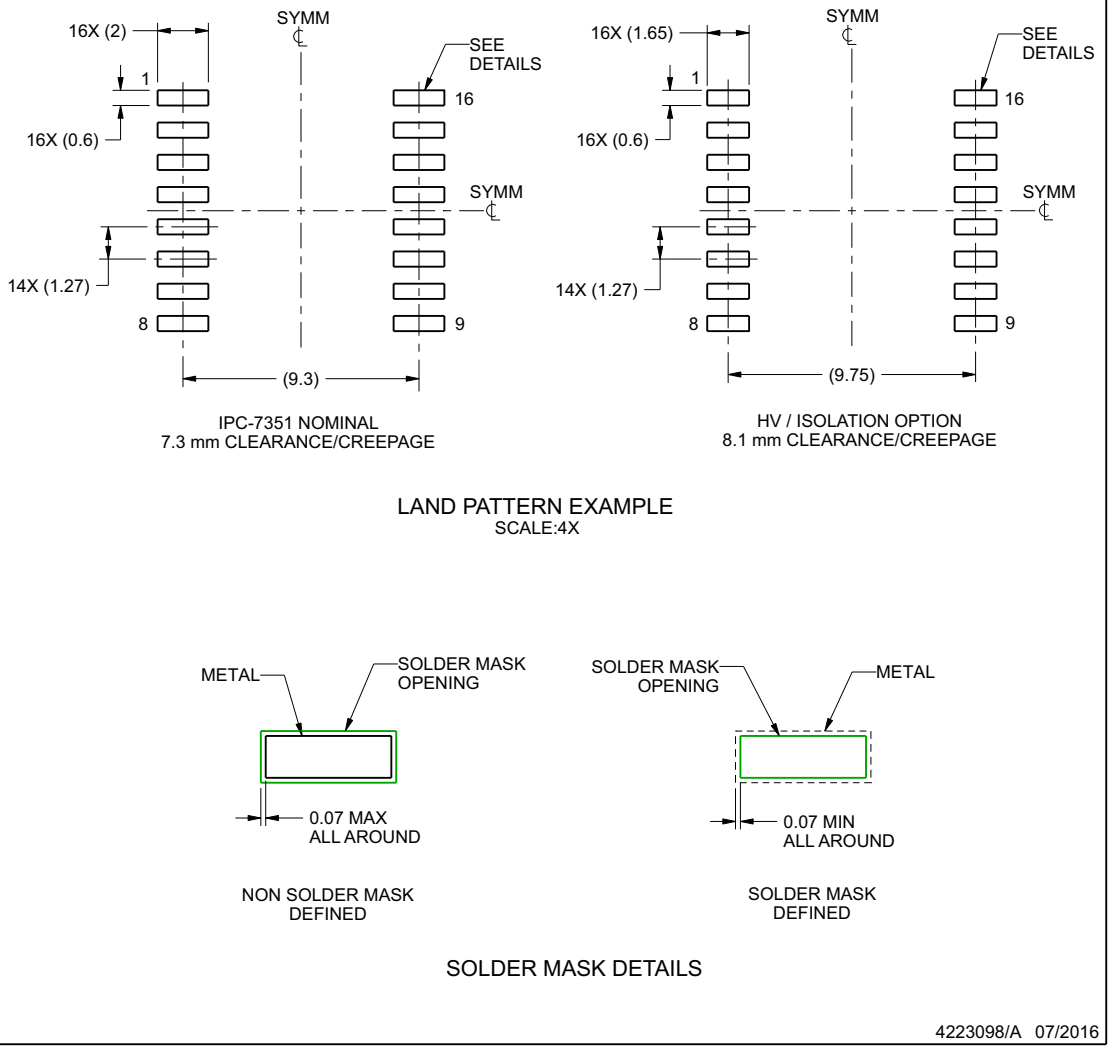
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

DWE0016A — SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

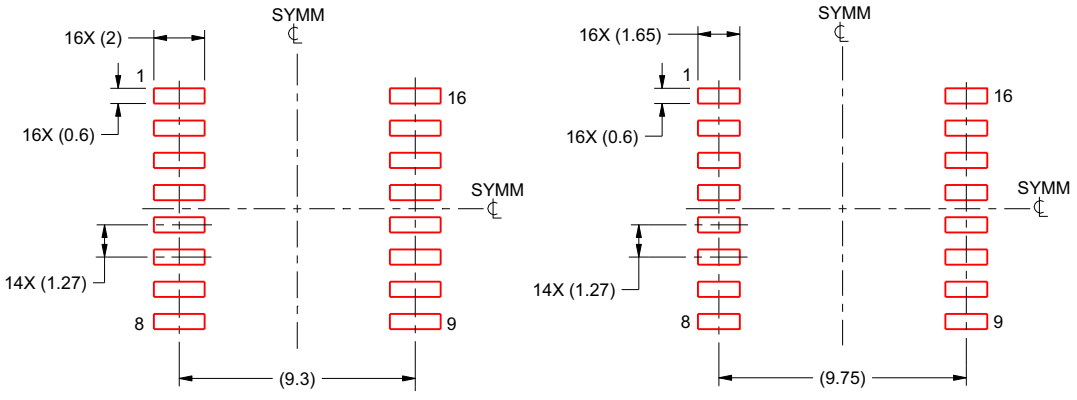
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DWE0016A

SOIC - 2.65 mm max height

SOIC



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4223098/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/Ball material (4)	MSL rating/Peak reflow (5)	Op temp (°C)	Part marking (6)
XISOW3080DWER	Pre-Production		SOIC (DWE) | 16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	XISOW3080
XISOW3086DWER	Pre-Production		SOIC (DWE) | 16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	XISOW3086
XISOW3080PDWER	Pre-Production		SOIC (DWE) | 16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	XISOW3080P
XISOW3086PDWER	Pre-Production		SOIC (DWE) | 16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	XISOW3086P

(1) **Status:** For more details on status, see our product life cycle.
(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

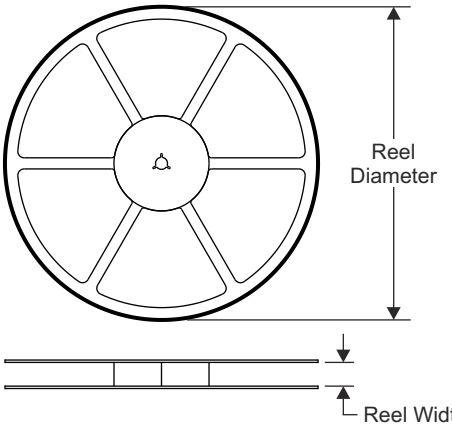
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

ADVANCE INFORMATION

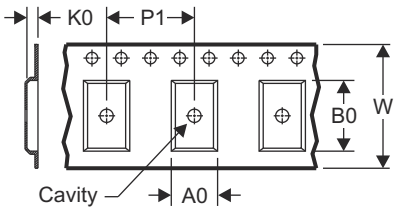
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

12.1 Tape and Reel Information

REEL DIMENSIONS

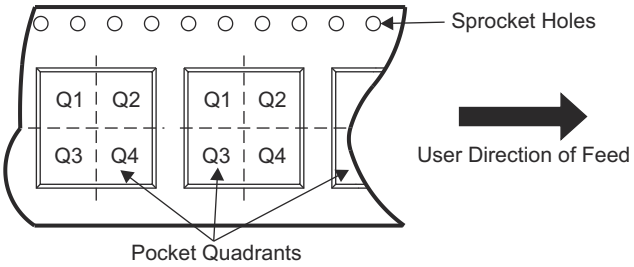


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

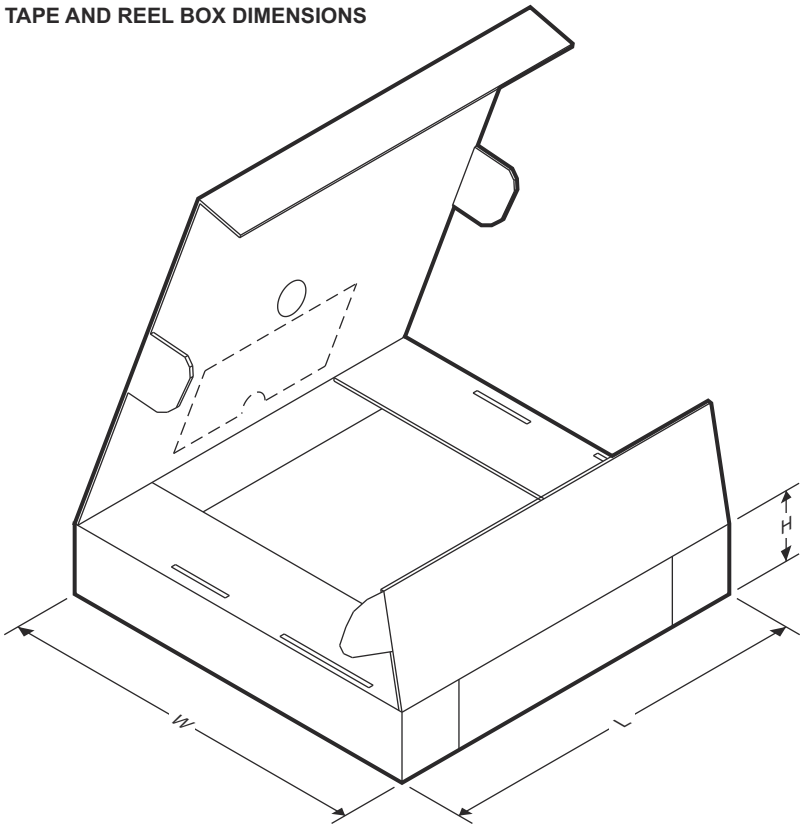
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
XISOW3080DWER	SOIC	DWE	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
XISOW3086DWER	SOIC	DWE	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
XISOW3080PDWER	SOIC	DWE	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
XISOW3086PDWER	SOIC	DWE	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
XISOW3080DWER	Active	Preproduction	SOIC (DWE) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-55 to 125	
XISOW3080PDWER	Active	Preproduction	SOIC (DWE) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-55 to 125	
XISOW3086DWER	Active	Preproduction	SOIC (DWE) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-55 to 125	
XISOW3086PDWER	Active	Preproduction	SOIC (DWE) | 16	2000 | LARGE T&R	-	Call TI	Call TI	-55 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

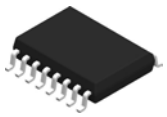
(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

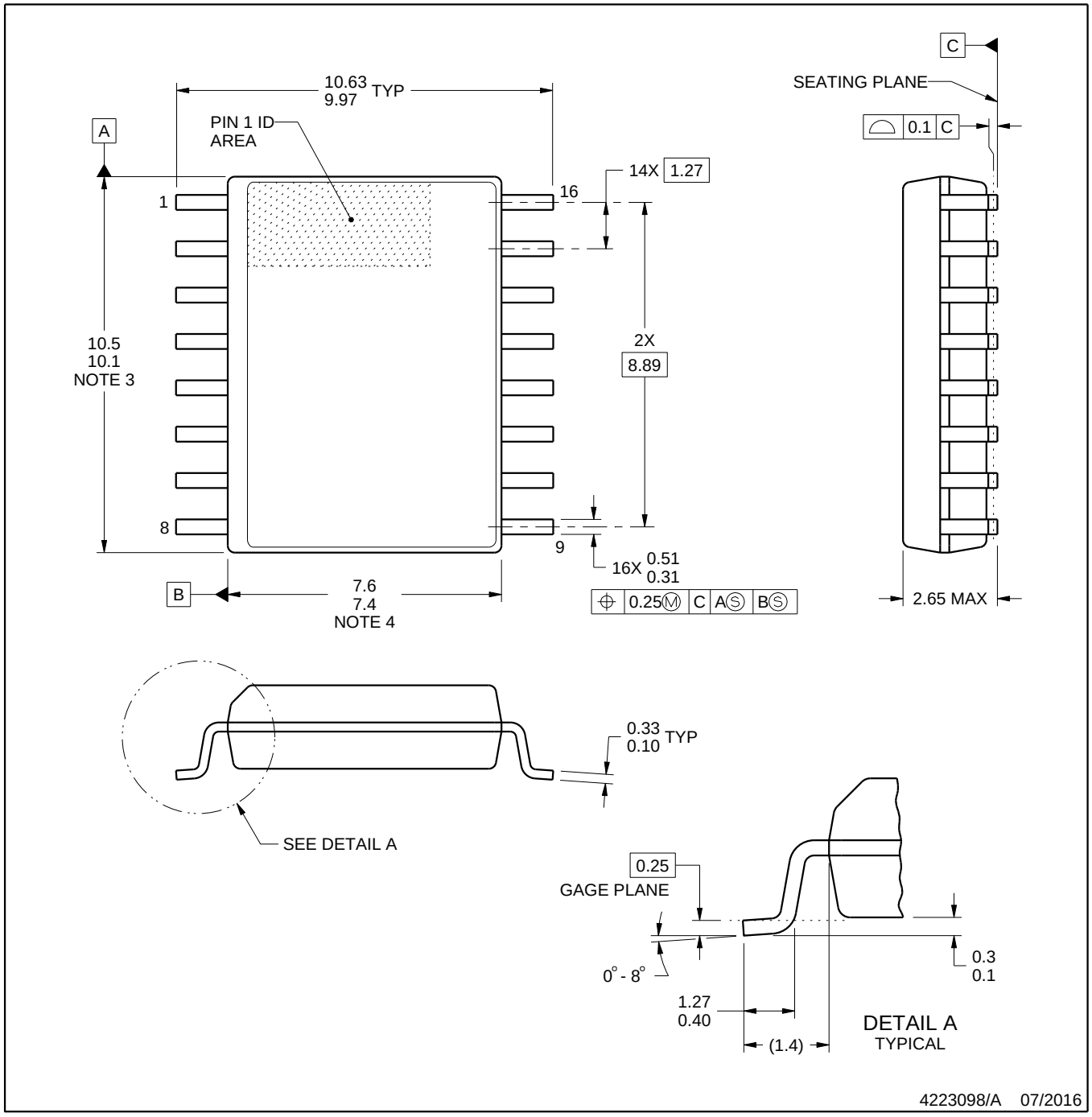


PACKAGE OUTLINE

DWE0016A

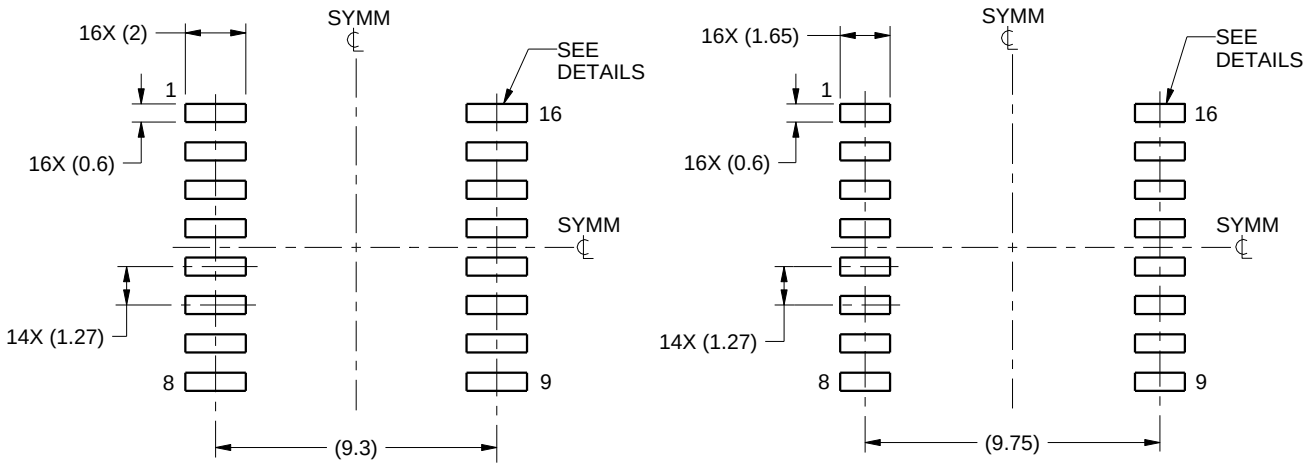
SOIC - 2.65 mm max height

SOIC



NOTES:

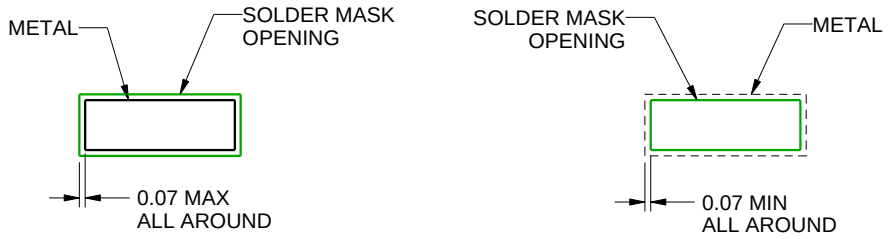
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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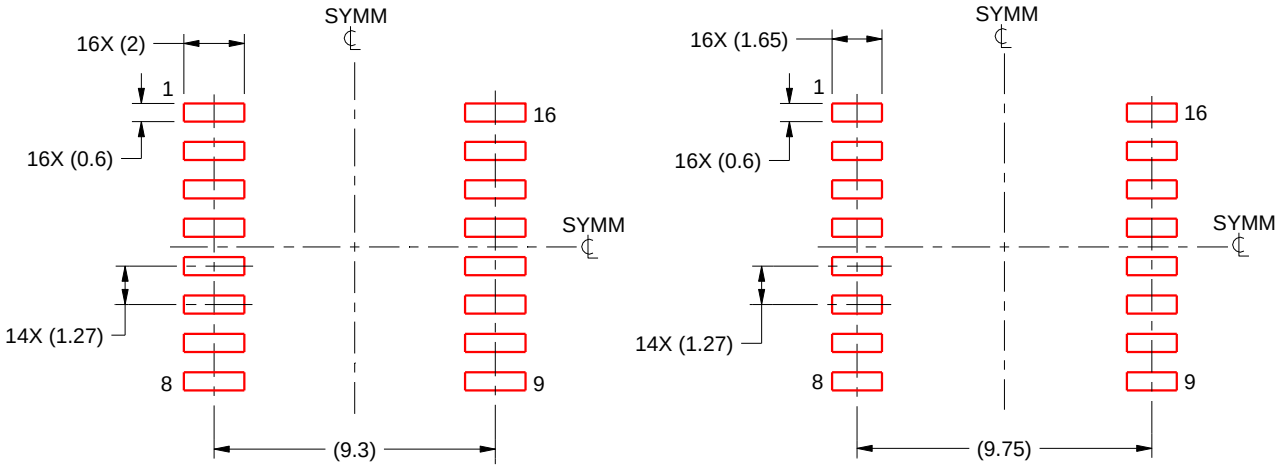
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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